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(54) Title: METHOD FOR PROVIDING HIGH ETCH RATE

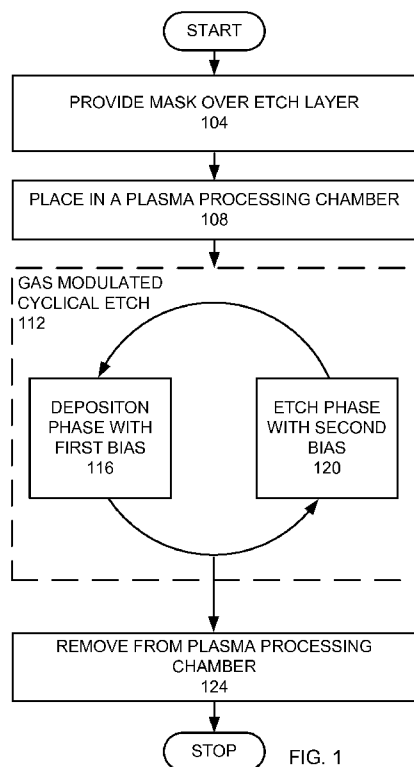


FIG. 1

(57) Abstract: A method for etching features into an etch layer in a plasma processing chamber, comprising a plurality of cycles is provided. Each cycle comprises a deposition phase and an etching phase. The deposition phase comprises providing a flow of deposition gas, forming a plasma from the deposition gas in the plasma processing chamber, providing a first bias during the deposition phase to provide an anisotropic deposition, and stopping the flow of the deposition gas into the plasma processing chamber. The etching phase, comprises providing a flow of an etch gas, forming a plasma from the etch gas in the plasma processing chamber, providing a second bias during the etch phase, wherein the first bias is greater than the second bias, and stopping the flow of the etch gas into the plasma processing chamber.



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— *without international search report and to be republished upon receipt of that report (Rule 48.2(g))*

METHOD FOR PROVIDING HIGH ETCH RATE

BACKGROUND OF THE INVENTION

Field of the Invention

- 5 **[0001]** The invention relates to a method of obtaining a structure on a semiconductor wafer by etching an etch layer.

Description of the related art

- [0002]** In forming semiconductor devices on a substrate, an etch layer is etched. The etch layer may be part of the substrate or a layer above the substrate. The etching
10 may occur in a plasma processing chamber.

SUMMARY OF THE INVENTION

- [0003]** To achieve the foregoing and in accordance with the purpose of the present invention, a method for etching features into an etch layer in a plasma processing chamber comprising a plurality of cycles is provided. Each cycle comprises a
15 deposition phase and an etching phase. The deposition phase comprises providing a flow of deposition gas, forming a plasma from the deposition gas in the plasma processing chamber, providing a first bias during the deposition phase to provide an anisotropic deposition, and stopping the flow of the deposition gas into the plasma processing chamber. The etching phase, comprises providing a flow of an etch gas,
20 forming a plasma from the etch gas in the plasma processing chamber, providing a second bias during the etch phase, wherein the first bias is greater than the second bias, and stopping the flow of the etch gas into the plasma processing chamber.

- [0004]** In another manifestation of the invention, a method for providing a gas modulated semiconductor process in a plasma processing chamber comprising a
25 plurality of cycles wherein each cycle comprises a first phase and a second phase is provided. The first phase comprises providing a flow of first phase gas, forming a plasma from the first phase gas in the plasma processing chamber, and stopping the flow of the first phase gas into the plasma processing chamber. The second phase comprises providing a flow of second phase gas, forming a plasma from the second
30 phase gas in the plasma processing chamber, and stopping the flow of the second phase gas into the plasma processing chamber. A parameter is ramped in either the

first phase or the second phase in a first direction over at least three cycles and then ramped in a second direction opposite the first direction over at least three cycles.

[0005] These and other features of the present invention will be described in more details below in the detailed description of the invention and in conjunction with the following figures.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] The present invention is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings and in which like reference numerals refer to similar elements and in which:

10 [0007] FIG. 1 is a flow chart of an embodiment of the invention.

[0008] FIGS. 2A-D are schematic views of the formation of a feature using the inventive process.

[0009] FIG. 3 is a schematic view of a plasma processing chamber that may be used in an embodiment of the invention.

15 [0010] FIG. 4 is a schematic view of a computer system that may be used in practicing the invention.

[0011] FIG. 5 is a more detailed flow chart of the deposition phase.

[0012] FIG. 6 is a more detailed flow chart of the etch phase.

[0013] FIG. 7 illustrates the pressure ramping during the etching phase.

20 [0014] FIG. 8 illustrates pressure oscillation during a plurality of cycles.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0015] The present invention will now be described in detail with reference to a few preferred embodiments thereof as illustrated in the accompanying drawings. In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be apparent, however, to one skilled in the art, that the present invention may be practiced without some or all of these specific details. In other instances, well known process steps and/or structures have not been described in detail in order to not unnecessarily obscure the present invention.

30 [0016] FIG. 1 is a high level flow chart of an embodiment of the invention. In this embodiment, a patterned mask is formed over an etch layer on a substrate (step 104). The etch layer may be part of the substrate, such as a silicon layer of a silicon wafer or

may be a layer over the substrate, such as a dielectric or conductive layer. The substrate is placed in a plasma processing chamber (step 108). The etch layer is subjected to a gas modulated cyclical etch (step 112). The gas modulated cyclical etch comprises a plurality of cycles, where each cycle comprises a deposition phase with a first bias (step 116) and an etch phase with a second bias lower than the first bias (step 120). The wafer is then removed from the plasma processing chamber (step 124).

Example

[0017] In a preferred embodiment of the invention, the features to be etched are through semiconductor wafer vias (TSVs). In this embodiment, the mask is a photoresist mask patterned on a silicon wafer (step 104). FIG. 2A is a schematic cross-sectional view of a silicon wafer 208, over which a patterned organic mask 204 has been formed. One or more intermediate patterning layers, such as an antireflective coating (ARC) may be disposed between the silicon wafer (substrate) 208 and the patterned organic mask 204 to improve the mask patterning process.

[0018] The substrate is placed in a processing tool (step 108). FIG. 3 schematically illustrates an example of a plasma processing system 300 which may be used to perform the process of etching a silicon wafer in accordance with one embodiment of the present invention. The plasma processing system 300 includes a plasma reactor 302 having a plasma processing chamber 304 therein. A plasma power supply 306, tuned by a match network 308, supplies power to a TCP coil 310 located near a power window 312 to create a plasma 314 in the plasma processing chamber 304. The TCP coil (upper power source) 310 may be configured to produce a uniform diffusion profile within processing chamber 304. For example, the TCP coil 310 may be configured to generate a toroidal power distribution in the plasma 314. The power window 312 is provided to separate the TCP coil 310 from the plasma chamber 304 while allowing energy to pass from the TCP coil 310 to the plasma chamber 304. A wafer bias voltage power supply 316 tuned by a match network 318 provides power to an electrode 320 to set the bias voltage on a wafer 322 which is supported by the electrode 320. A controller 324 sets points for the plasma power supply 306 and the wafer bias voltage supply 316.

[0019] The plasma power supply 306 and the wafer bias voltage power supply 316 may be configured to operate at specific radio frequencies such as, for example, 13.56

MHz, 27 MHz, 2 MHz, 400 kHz, or combinations thereof. Plasma power supply 306 and wafer bias power supply 316 may be appropriately sized to supply a range of powers in order to achieve desired process performance. For example, in one embodiment of the present invention, the plasma power supply 306 may supply the power in a range of 300 to 10000 Watts, and the wafer bias voltage power supply 316 may supply a bias voltage of in a range of 10 to 1000 V. In addition, the TCP coil 310 and/or the electrode 320 may be comprised of two or more sub-coils or sub-electrodes, which may be powered by a single power supply or powered by multiple power supplies.

10 **[0020]** As shown in FIG. 3, the plasma processing system 300 further includes a gas source/gas supply mechanism 330. The gas source includes a deposition phase gas source 332, an etching phase gas source 334, and optionally, an additional gas source 336. The gas sources 332, 334, and 336 are in fluid connection with processing chamber 304 through a gas inlet, such as a shower head 340. The gas inlet
15 may be located in any advantageous location in chamber 304, and may take any form for injecting gas. Preferably, however, the gas inlet may be configured to produce a “tunable” gas injection profile, which allows independent adjustment of the respective flow of the gases to multiple zones in the process chamber 304. The process gases and byproducts are removed from the chamber 304 via a pressure control valve 342
20 and a pump 344, which also serve to maintain a particular pressure within the plasma processing chamber 304. The gas source/gas supply mechanism 330 is controlled by the controller 324. A 2300 Syndion by Lam Research Corp. may be used to practice an embodiment of the invention. To this device, an optical window 352 is added. An optical spectrometer 356 is positioned to measure light from the plasma that
25 passes through the optical window 352. Output from the optical spectrometer 356 is provided to the controller 324.

[0021] FIG. 4 is a high level block diagram showing a computer system 400, which is suitable for implementing a controller 324 used in embodiments of the present invention. The computer system may have many physical forms ranging from
30 an integrated circuit, a printed circuit board, and a small handheld device up to a huge super computer. The computer system 400 includes one or more processors 402, and further can include an electronic display device 404 (for displaying graphics, text, and

other data), a main memory 406 (e.g., random access memory (RAM)), storage device 408 (e.g., hard disk drive), removable storage device 410 (e.g., optical disk drive), user interface devices 412 (e.g., keyboards, touch screens, keypads, mice or other pointing devices, etc.), and a communication interface 414 (e.g., wireless network interface). The communication interface 414 allows software and data to be transferred between the computer system 400 and external devices via a link. The system may also include a communications infrastructure 416 (e.g., a communications bus, cross-over bar, or network) to which the aforementioned devices/modules are connected.

10 **[0022]** Information transferred via communications interface 414 may be in the form of signals such as electronic, electromagnetic, optical, or other signals capable of being received by communications interface 414, via a communication link that carries signals and may be implemented using wire or cable, fiber optics, a phone line, a cellular phone link, a radio frequency link, and/or other communication channels.

15 With such a communications interface, it is contemplated that the one or more processors 402 might receive information from a network, or might output information to the network in the course of performing the above-described method steps. Furthermore, method embodiments of the present invention may execute solely upon the processors or may execute over a network such as the Internet in conjunction with remote processors that shares a portion of the processing.

20 **[0023]** The term “non-transient computer readable medium” is used generally to refer to media such as main memory, secondary memory, removable storage, and storage devices, such as hard disks, flash memory, disk drive memory, CD-ROM and other forms of persistent memory and shall not be construed to cover transitory subject matter, such as carrier waves or signals. Examples of computer code include machine code, such as produced by a compiler, and files containing higher level code that are executed by a computer using an interpreter. Computer readable media may also be computer code transmitted by a computer data signal embodied in a carrier wave and representing a sequence of instructions that are executable by a processor.

25 **[0024]** The etch layer is subjected to a gas modulated cyclical etch (step 112). The gas modulated cyclical etch comprises a plurality of cycles, where each cycle comprises a deposition phase with a first bias (step 116) and an etch phase with a

second bias less than the first bias (step 120). FIG. 5 is a more detailed flow chart of the deposition phase. A deposition gas is flowed into the plasma processing chamber 304 (step 504). The deposition gas is formed into a plasma (step 508). A first bias is provided (step 512). The flow of the deposition gas is stopped (step 516). FIG. 2B is a cross-sectional view of the silicon wafer 208 and mask 204 after a deposition layer 212 has been formed during the deposition phase (step 116). The high bias during deposition is used to remove deposition at the bottom of the features.

[0025] An example of a deposition recipe provides a flow of 100 sccm C_4F_8 to the plasma pressure chamber. A pressure of 100 mTorr, a bias of 500 volts, and 2000 Watts of RF are provided.

[0026] FIG. 6 is a more detailed flow chart of the etch phase (step 120). An etch gas is flowed into the plasma processing chamber 304 (step 604). The pressure during the etch phase is ramped with respect to the previous cycle (step 608). The etch gas is formed into a plasma (step 612). A second bias which is less than the first bias is provided (step 616). The flow of the etch gas is stopped (step 620). FIG. 2C is a cross-sectional view of the silicon wafer 208 and mask 204 after an etch phase (step 120), which forms part of the etch feature 216.

[0027] An example of an etch recipe provides a flow of 150 sccm SF_6 to the plasma process chamber. When the presence of SF_6 is detected in the plasma processing chamber, a pressure of 120 mTorr a bias of 200 volts, and 2300 Watts of RF power are provided to the plasma processing chamber.

[0028] FIG. 2D is a cross-sectional view of the silicon wafer 208 and mask 204 after over 100 cycles of the deposition phase and the etch phase, where the etch feature 216 is almost completely etched.

[0029] In an embodiment where the silicon wafer is the etch layer, the silicon wafer may be etched completely through to form through silicon vias. In an embodiment where the etch layer is a dielectric layer, the plasma processing chamber may provide capacitive coupling instead of inductive coupling. In another embodiment, the etch layer may be a conductive layer.

[0030] Without being bound by theory, in the prior art using a single etch step before gas modulation, a high bias was used for the etch process. The high bias provided a directional anisotropic etch. Otherwise, an isotropic etch would cause the

etch features to be rounded on the sides (bowed) instead of having a straight profile. The high bias etch was carried to the gas modulation process using a plurality of cycles of deposition and etches to provide an etch. The high biased etch was used to provide a directional etch which in addition to etching would clear polymer at the
5 bottom of the etch features.

[0031] The invention unexpectedly found that using a directional anisotropic deposition phase in a gas modulation process allows for the use of a non-directional isotropic etch phase providing an improved etch. The high bias deposition has been found to provide deposition on the tops and sidewalls of the etch features, but not at
10 the bottoms of the etch features. It has been found that the high bias during the deposition may be used to sputter away deposition on the bottoms of the etch features. Because the deposition selectively deposited on the tops and sidewalls of the etch features, without deposition on the bottoms of the etch features, a subsequent non-directional anisotropic etch will etch the bottoms of the etch features as the sidewalls
15 and top depositions protect the sidewalls and tops of the etch features. The anisotropic non-directional etch phase etches faster than a directional etch phase and causes less damage to the sidewalls than a directional etch phase, which subjects sidewalls to ion bombardment. Etchant ion bombardment of sidewalls from a high bias directional etch phase causes defects in the forms of striation, bowing, roughness,
20 and the formation of silicon shards. Therefore not only does the bias applied by the invention increase the etch rate, the bias of the invention improves feature shape, reducing sidewall damage, such as striation, bowing, roughness, and the formation of silicon shards.

[0032] Preferably, the bias is provided at a frequency between 100 kHz and 1
25 MHz. More preferably, the bias is provided at a frequency between 300 kHz to 500 kHz. Most preferably, the bias is provided at a frequency of about 400 kHz. Preferably, the first bias during the deposition phase is from 300 to 1000 volts. More preferably, the first bias during the deposition phase is 400 to 800 volts. Most preferably, the first bias during the deposition phase is 500 to 700 volts. Preferably,
30 the second bias during the etch phase is between 0 to 300 volts. More preferably, the second bias during the etch phase is between 0 to 250 volts. Most preferably, the second bias during the etch phase is less than 150 volts. Such voltage ranges were

found to provide the highest etch rates with the least sidewall damage and best profiles.

[0033] FIG. 7 is a graph of a pressure ramp during the etching phase over 100 cycles, used in this embodiment of the invention. In this embodiment, pressure during the etching phase is first ramped up over about 70 cycles from about 300 mtorr to about 600 mtorr and then ramped down over about 30 cycles from about 600 mtorr to about 300 mtorr. FIG. 8 is a more detailed graph of pressure 804, showing both the deposition phase pressure 808 and etching phase pressure 812 over 5 cycles, that would be an example of a process that provides part of the etching phase pressure ramp shown in FIG. 7. In this example, the deposition phase pressure 808 is lower than the etching phase pressure 812. In this example, the deposition phase pressure decreases, as shown in that the deposition phase pressure from T₃ to T₄ is lower than the deposition phase pressure from T₁ to T₂. In contrast in this example, the etching phase pressure increases, as shown in that the etching phase pressure from T₄ to T₅ is higher than the etching phase pressure from T₂ to T₃. Although the pressure from phase to phase oscillates from cycle to cycle, in FIG. 8, the etching phase pressure increases and the deposition phase pressure decreases. It has been found that initially in etching a via, it is desirable to start at a low etching pressure to help reduce undercutting. As the via depth increases, pressure is increased to increase the etch rate. After the vias reach certain depth, it has been found that it is desirable to decrease etch pressure to improve critical etch profile and maintain etch rate. As a result, it has been found that providing an etch that first ramps up pressure and then ramps down pressure increases the overall etch rate.

[0034] In another embodiment, the invention provides a semiconductor process that comprises a plurality of cycles comprising at least a first phase and a second phase. The first phase flows a first phase gas, which is formed into a plasma. The flow of the first phase gas is then stopped. The second phase flows a second phase gas, which is formed into a plasma. The flow of the second phase gas is then stopped. In either the first phase or second phase a parameter is ramped in a first direction from cycle to cycle and over at least three cycles. The parameter is then ramped in a second direction from cycle to cycle over at least three cycles, where the first direction is opposite the second direction. More preferably, the parameter is ramped in the first

direction for more than ten cycles and then ramped in the second direction more than ten cycles. Most preferably, the parameter is ramped in the first direction for more than 20 cycles and then ramped in the second direction more than 20 cycles.

Increasing the number of cycles over which the ramping takes place provides an
5 increased etch rate and improved feature shape. The parameter may be any plasma processing parameter such as bias RF power, ionization RF power, pressure, phase time, and gas flows. As shown in FIG. 8, one phase may ramp a parameter in one direction while another phase ramps the same parameter in the opposite direction. Preferably, the parameters are ramped independently. Other parameters may be
10 independently ramped. The ramp shape can be linear or non-linear.

[0035] While this invention has been described in terms of several preferred embodiments, there are alterations, permutations, and substitute equivalents, which fall within the scope of this invention. It should also be noted that there are many alternative ways of implementing the methods and apparatuses of the present
15 invention. It is therefore intended that the following appended claims be interpreted as including all such alterations, permutations, and substitute equivalents as fall within the true spirit and scope of the present invention.

CLAIMS

What is claimed is:

1. A method for etching features into an etch layer in a plasma processing chamber, comprising a plurality of cycles, wherein each cycle comprises:
 - 5 a deposition phase, comprising:
 - providing a flow of deposition gas;
 - forming a plasma from the deposition gas in the plasma processing chamber;
 - providing a first bias during the deposition phase to provide an
 - 10 anisotropic deposition; and
 - stopping the flow of the deposition gas into the plasma processing chamber; and
 - an etching phase, comprising:
 - providing a flow of an etch gas;
 - 15 forming a plasma from the etch gas in the plasma processing chamber;
 - providing a second bias during the etch phase, wherein the first bias is greater than the second bias; and
 - stopping the flow of the etch gas into the plasma processing
 - 20 chamber.
 2. The method, as recited in claim 1, wherein the bias during deposition phase is between 300 to 1000 volts and wherein the bias during the etch phase is between 0 to 300 volts.
 3. The method, as recited in claim 1, wherein the bias during deposition phase is
 - 25 between 400 to 800 volts and wherein the bias during the etch phase is between 0 to 200 volts.
 4. The method, as recited in claim 3, wherein the etch layer is a silicon based etch layer.
 5. The method, as recited in claim 4, wherein the etch features are through silicon
 - 30 vias.
 6. The method, as recited in claim 5, further comprising ramping a parameter in either the deposition phase or the etch phase in a first direction over at least three

cycles and ramping the parameter is a second direction opposite the first direction over at least three cycles.

7. The method, as recited in claim 6, wherein the parameter is pressure during the etching phase wherein the first direction is ramping up the pressure and the second
5 direction is ramping down the pressure.

8. The method, as recited in claim 6, wherein the wherein the ramping in the first direction is for at least 10 cycles and wherein the ramping in the second direction is for at least 10 cycles.

9. The method, as recited in claim 6, wherein the wherein the ramping in the first
10 direction is for at least 20 cycles and wherein the ramping in the second direction is for at least 20 cycles.

10. The method, as recited in claim 5, wherein the plurality of cycles is over 100 cycles.

11. The method, as recited in claim 3, wherein the plurality of cycles is over 100
15 cycles.

12. A method for providing a gas modulated semiconductor process in a plasma processing chamber, comprising a plurality of cycles, wherein each cycle comprises:

a first phase, comprising:

providing a flow of first phase gas;
20 forming a plasma from the first phase gas in the plasma processing chamber; and
stopping the flow of the first phase gas into the plasma processing chamber;

a second phase, comprising:

25 providing a flow of second phase gas;
forming a plasma from the second phase gas in the plasma processing chamber; and
stopping the flow of the second phase gas into the plasma processing chamber; and

30 ramping a parameter in either the first phase or the second phase in a first direction over at least three cycles and ramping the parameter is a second direction opposite the first direction over at least three cycles.

13. The method, as recited in claim 12, wherein the wherein the ramping in the first direction is for at least 10 cycles and wherein the ramping in the second direction is for at least 10 cycles.
14. The method, as recited in claim 13, wherein the parameter is ramped in the first phase, and further comprising ramping the parameter in an opposite direction during the second phase.
15. The method, as recited in claim 12, wherein the wherein the ramping in the first direction is for at least 20 cycles and wherein the ramping in the second direction is for at least 20 cycles.
16. The method, as recited in claim 15, wherein the plurality of cycles is over 100 cycles.
17. The method, as recited in claim 12, wherein the ramping of the parameter in the first phase is independent of ramping of the first parameter in the second phase.
18. The method, as recited in claim 12, wherein the parameter is pressure during the second phase, wherein the second phase is an etching phase and wherein the first direction is ramping up the pressure and the second direction is ramping down the pressure.
19. The method, as recited in any of claims 12-13, wherein the parameter is ramped in the first phase, and further comprising ramping the parameter in an opposite direction during the second phase.
20. The method, as recited in any of claims 12-13 and 19, wherein the wherein the ramping in the first direction is for at least 20 cycles and wherein the ramping in the second direction is for at least 20 cycles.
21. The method, as recited in any of claims 12-13 and 19-20, wherein the plurality of cycles is over 100 cycles.
22. The method, as recited in any of claims 12-13 and 19-21, wherein the ramping of the parameter in the first phase is independent of ramping of the first parameter in the second phase.
23. The method, as recited in any of claims 12-13 and 19-22, wherein the parameter is pressure during the second phase, wherein the second phase is an etching phase and wherein the first direction is ramping up the pressure and the second direction is ramping down the pressure.

24. The method, as recited in any of claims 1-3, wherein the etch layer is a silicon based etch layer.
25. The method, as recited in any of claims 1-3 and 24, wherein the etch features are through silicon vias.
- 5 26. The method, as recited in any of claims 1-3 and 24-25, further comprising ramping a parameter in either the deposition phase or the etch phase in a first direction over at least three cycles and ramping the parameter in a second direction opposite the first direction over at least three cycles.
27. The method, as recited in claim 26, wherein the parameter is pressure during
10 the etching phase wherein the first direction is ramping up the pressure and the second direction is ramping down the pressure.
28. The method, as recited in any of claims 26 and 27, wherein the wherein the ramping in the first direction is for at least 10 cycles and wherein the ramping in the second direction is for at least 10 cycles.
- 15 29. The method, as recited in any of claims 26 and 27, wherein the wherein the ramping in the first direction is for at least 20 cycles and wherein the ramping in the second direction is for at least 20 cycles.
30. The method, as recited in any of claims 1-3 and 24-29, wherein the plurality of cycles is over 100 cycles.

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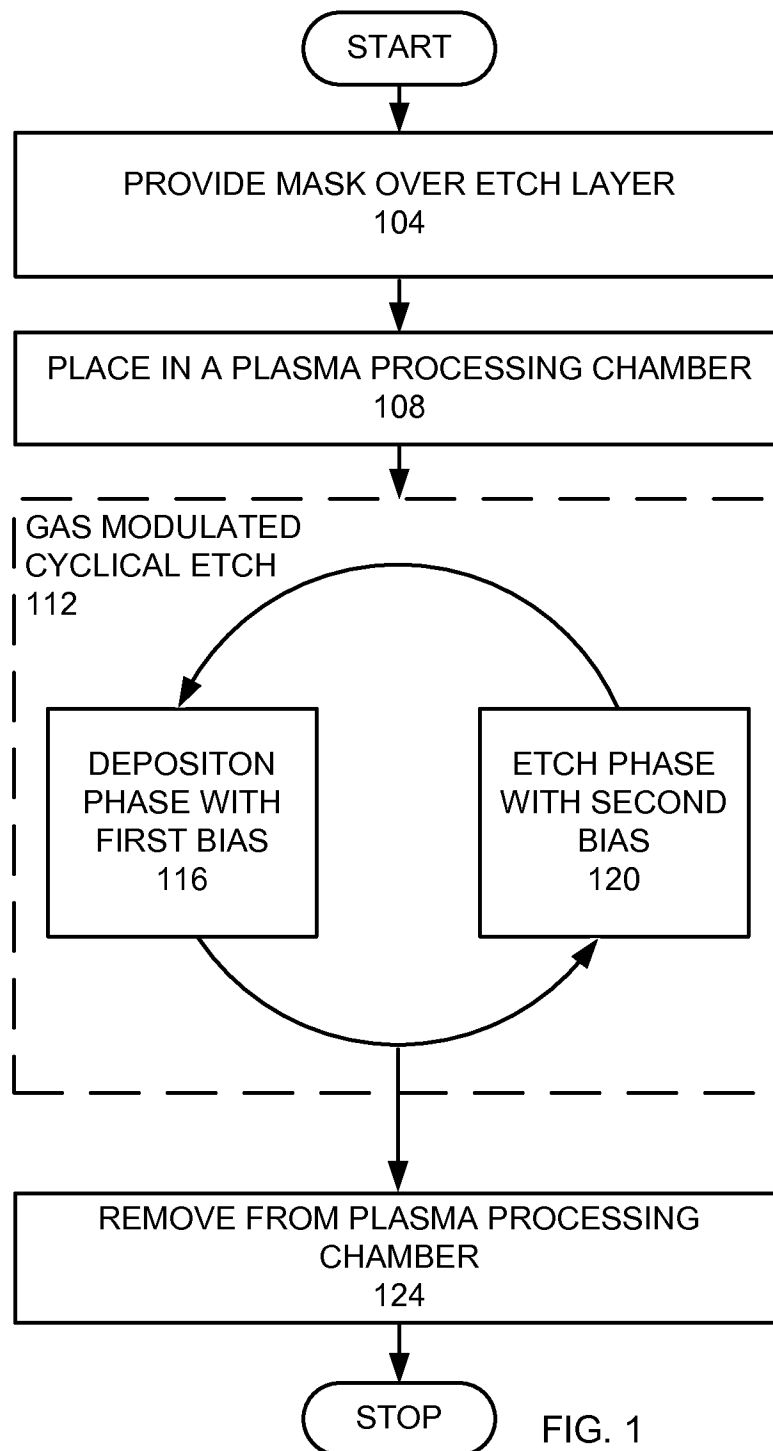


FIG. 1

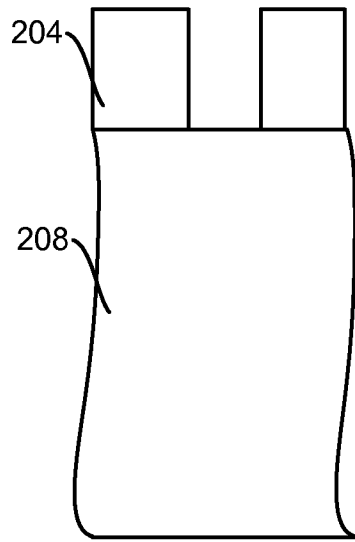


FIG. 2A

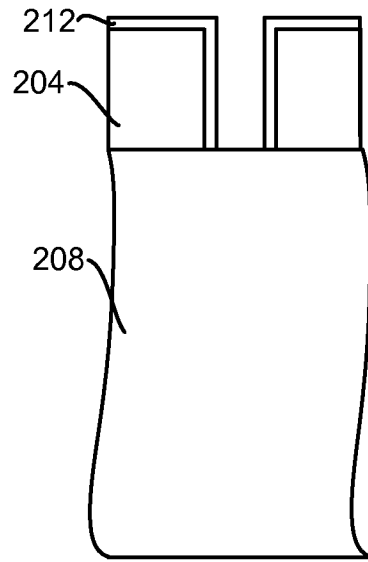


FIG. 2B

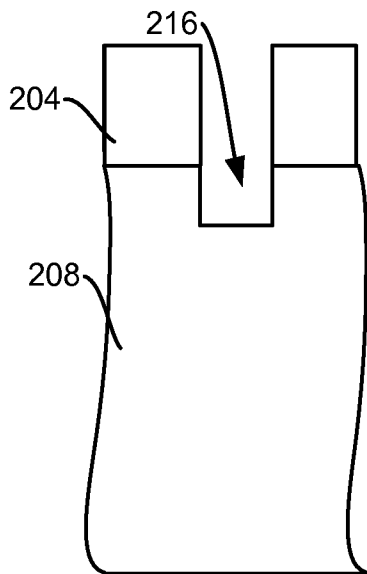


FIG. 2C

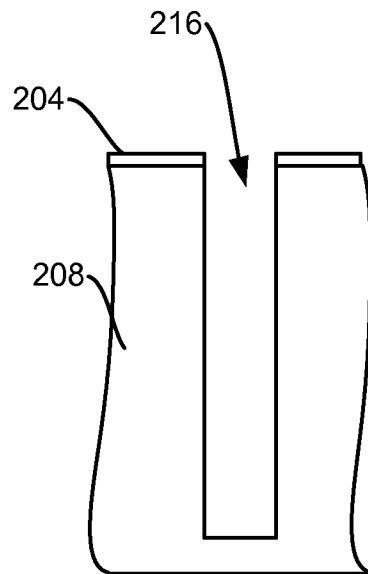


FIG. 2D

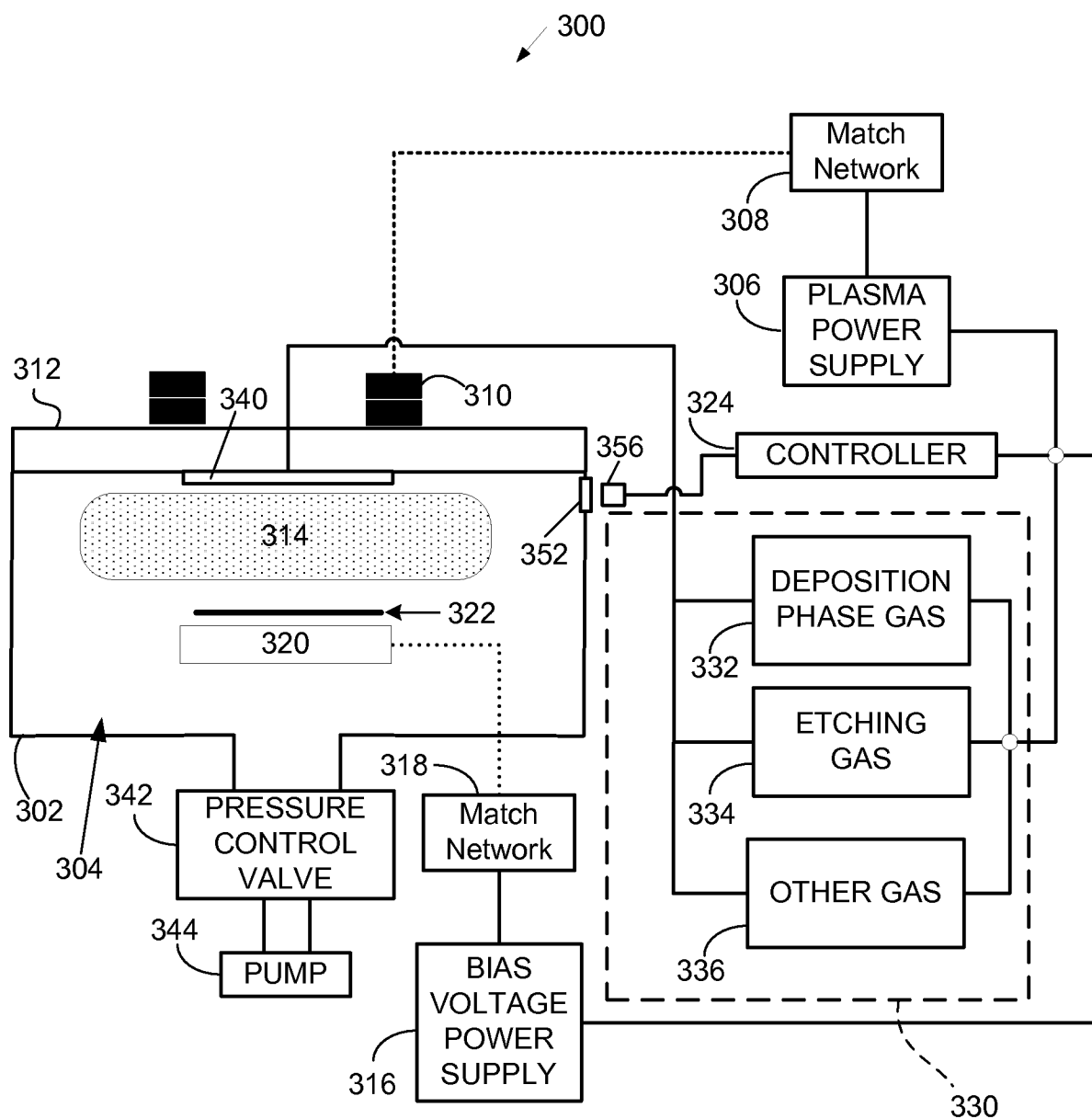


FIG. 3

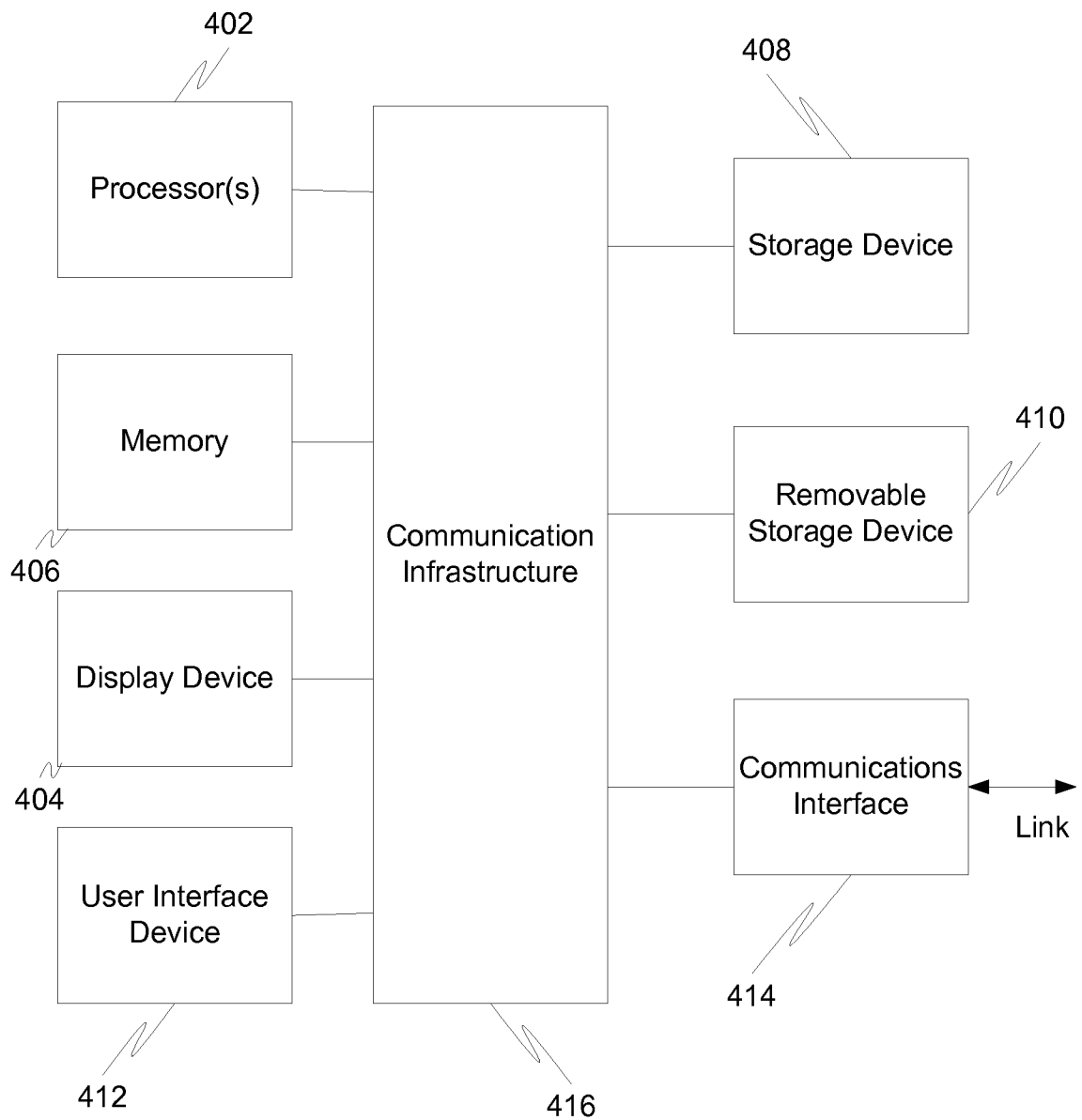
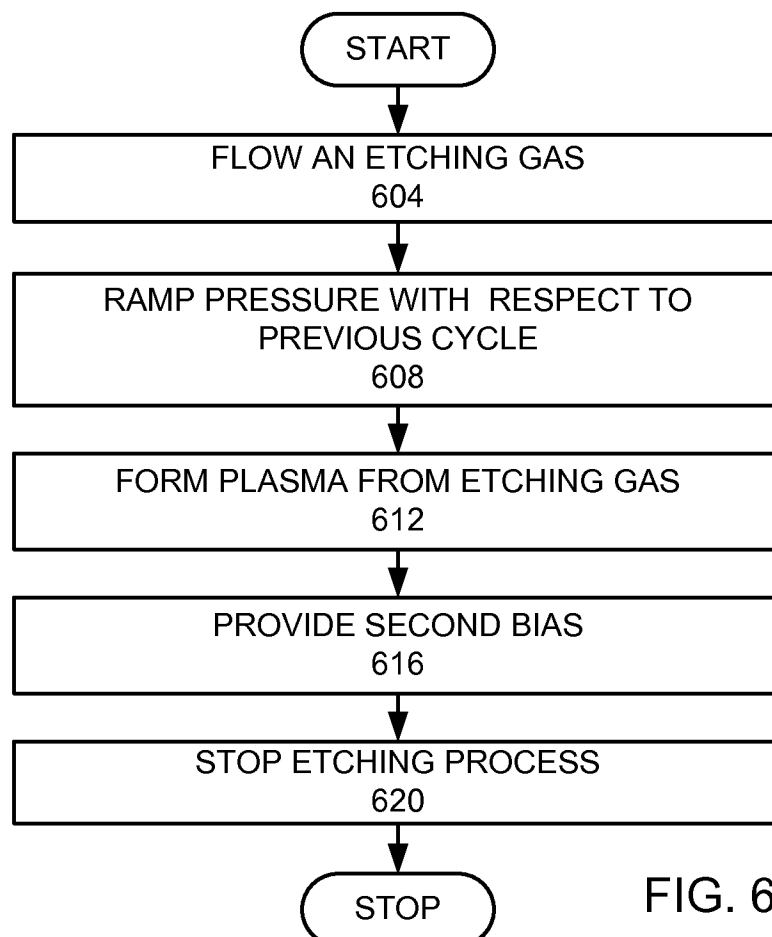
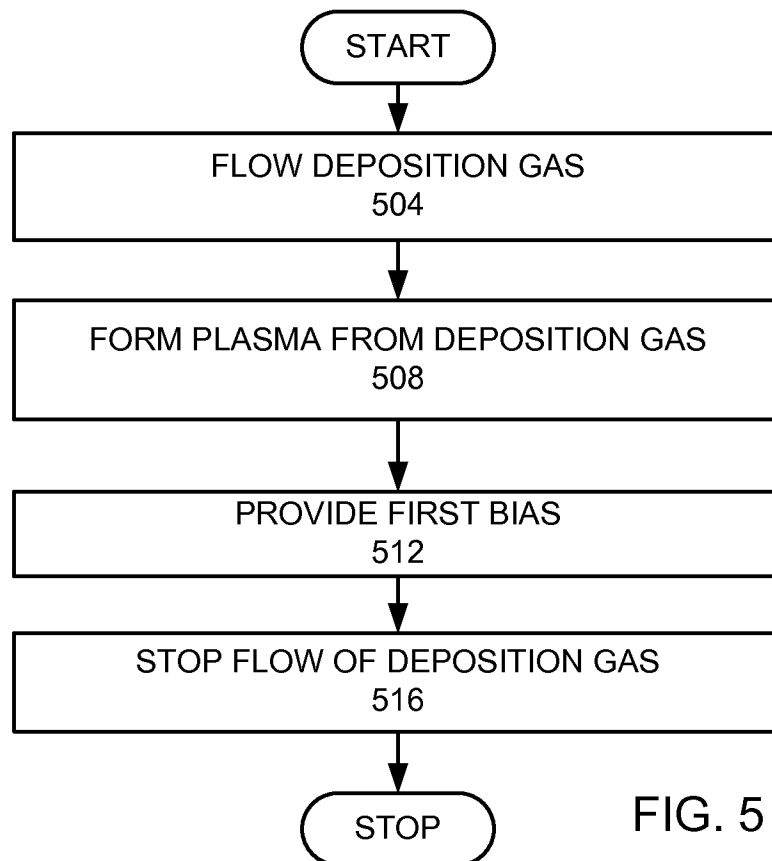


FIG. 4

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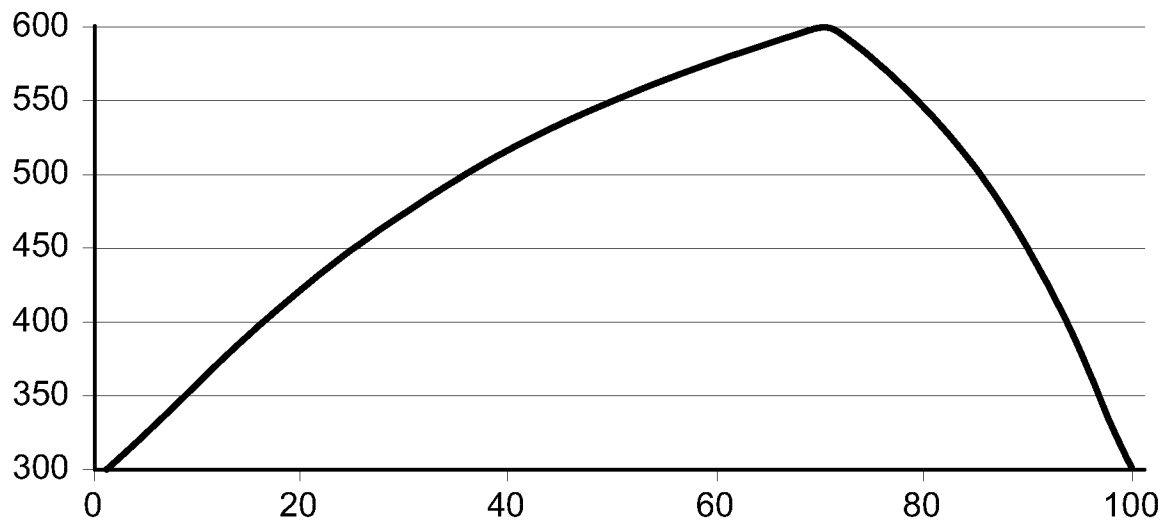


FIG. 7

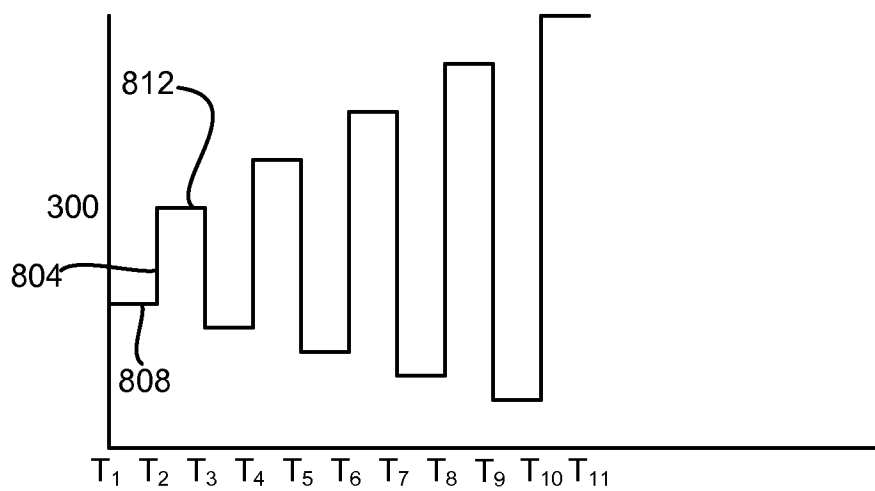


FIG. 8