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(54) **Title**: MONOLITHICALLY INTEGRATED ACTIVE SNUBBER

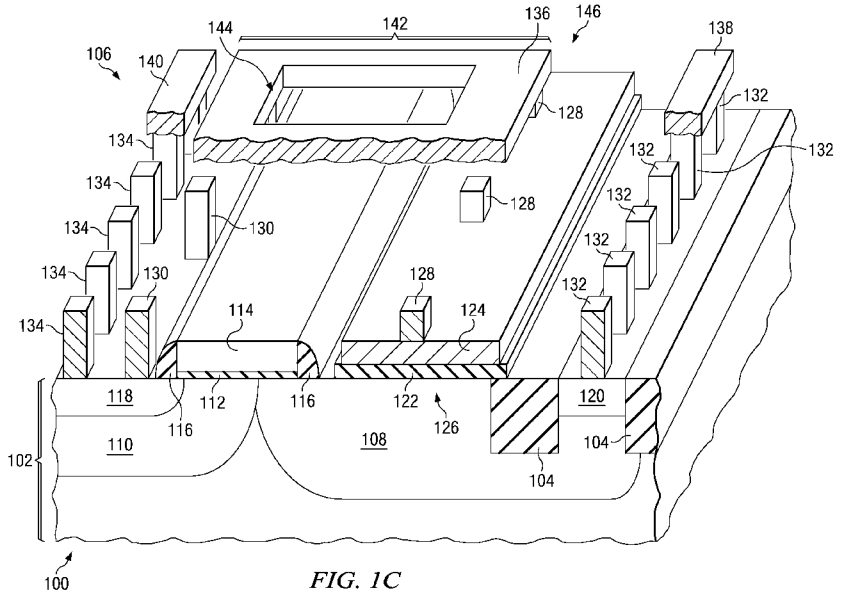

FIG. 1C

(57) **Abstract**: A semiconductor device (100) containing an extended drain MOS transistor (106) with an integrated snubber formed by forming a drain drift region (108) of the MOS transistor, forming a snubber capacitor including a capacitor dielectric layer (122) and capacitor plate (124) over the extended drain (108), and forming a snubber resistor (136) over a gate (114) of the MOS transistor so that the resistor is connected in series between the capacitor plate and a source (118) of the MOS transistor.

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MONOLITHICALLY INTEGRATED ACTIVE SNUBBER

[0001] This relates to semiconductor devices including extended drain metal oxide semiconductor (MOS) transistors.

BACKGROUND

[0002] A semiconductor device may be part of or contain a circuit which produces undesired voltage excursions, such as a buck converter circuit which receives an input DC voltage and generates an output DC voltage that is lower than the input voltage. The semiconductor device may include an extended drain metal oxide semiconductor (MOS) transistor, which, during operation of the circuit, switching of the MOS transistor between the on state and the off state may cause undesirable voltage oscillations, commonly referred to as ringing, at the drain node. It may be desirable to add a snubber to the semiconductor device which damps the ringing. Integrating a snubber in the semiconductor device with desired performance and without significantly increasing fabrication cost and complexity of the semiconductor device may be problematic.

SUMMARY

[0003] A semiconductor device containing an extended drain metal oxide semiconductor (MOS) transistor may be formed with an integrated snubber by a process of forming a drain drift region in an extended drain of the MOS transistor, and forming a snubber capacitor including a capacitor dielectric layer and capacitor plate over the extended drain. A snubber resistor is formed over a gate of the MOS transistor and connected in series between the capacitor plate and a source of the MOS transistor. The snubber resistor and snubber capacitor form the integrated snubber for the MOS transistor. The resistor may be formed concurrently with other elements of the semiconductor device.

BRIEF DESCRIPTION OF DRAWINGS

[0004] FIGS. 1A - 1C are perspective cross sections illustrating stages in the fabrication of a semiconductor device including an extended drain MOS transistor with a snubber according to an example embodiment.

[0005] FIGS. 2A- 2C are perspective cross sections illustrating stages in the fabrication of a semiconductor device including an extended drain MOS transistor with a snubber according to a modified embodiment.

[0006] FIGS. 3A- 3C are perspective cross sections illustrating stages in the fabrication of a semiconductor device including an extended drain MOS transistor with a snubber according to another modified embodiment.

[0007] FIGS. 4A and 4B are perspective cross sections illustrating stages in the fabrication of a semiconductor device including an extended drain MOS transistor with a snubber according to another modified embodiment.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0008] A semiconductor device containing an extended drain metal oxide semiconductor (MOS) transistor may be formed with an integrated snubber integrated into the MOS transistor. The semiconductor device may be formed by a process including steps of forming a drain drift region in an extended drain of the MOS transistor A snubber capacitor is formed over the drain drift region by forming a capacitor dielectric layer and capacitor plate over the extended drain. A snubber resistor is formed over a gate of the MOS transistor and connected in series between the capacitor plate and a source of the MOS transistor. The snubber resistor and snubber capacitor form the integrated snubber for the MOS transistor. The resistor may be formed concurrently with other elements of the semiconductor device. The resistor may be formed concurrently with the capacitor plate.

[0009] The semiconductor device may be a discrete power device which includes the extended drain MOS transistor with the integrated snubber. Alternatively, the semiconductor device may be an integrated circuit which includes other circuits, such as sense circuits and/or control circuits, in addition to the extended drain MOS transistor with the integrated snubber.

[0010] To avoid repetition, the formation of n-channel extended drain MOS transistors is described. However, it will be appreciated that, with appropriate changes in polarities of dopants and conductivity types, the same description applies also to the formation of p-channel extended drain MOS transistors.

[0011] FIGS. 1A - 1C illustrate stages in the fabrication of a semiconductor device including an extended drain MOS transistor with a snubber according to an example embodiment.

[0012] Referring to FIG. 1A, the semiconductor device 100 is formed in and on a semiconductor substrate 102 which may be a single crystal silicon wafer, a silicon-on-insulator (SOI) wafer, a hybrid orientation technology (HOT) wafer with regions of different crystal orientations, or other material appropriate for fabrication of the semiconductor device 100. Semiconductor material at a top surface of the substrate 102 is p-type. Field oxide 104 may be formed at the top surface of the substrate 102. The field oxide 104 may include silicon dioxide between 250 and 600 nanometers thick, and may be formed by shallow trench isolation (STI) or local oxidation of silicon (LOCOS) processes. In STI processes, silicon dioxide may be deposited by high density plasma (HDP) or high aspect ratio process (HARP).

[0013] The semiconductor device 100 contains the extended drain MOS transistor 106. The MOS transistor 106 has an n-type drain drift region 108 extending to the top surface of the substrate 102. The drain drift region 108 may be formed, for example, by ion implanting a first set of n-type dopants, such as phosphorus and arsenic, and possibly antimony, at doses from $1 \cdot 10^{11}$ to $1 \cdot 10^{13}$ atoms/cm^2, into an area exposed by a drift region implant mask, such as a photoresist pattern.. A subsequent anneal process activates at least a portion of the first set of n-type dopants to form the drain drift region 108. The drain drift region 108 may extend to a depth between 350 to 1000 nanometers in the substrate 102. The drain drift region 108 may be formed concurrently with other components of the semiconductor device 100 such as n-type wells for p-channel MOS transistors, not shown.

[0014] The MOS transistor 106 further includes a p-type body region 110 in the substrate 102 abutting the drain drift region 108. The body region 110 may be formed, for example, by ion implanting a set of p-type dopants, such as boron and possibly gallium and/or indium, at doses from $1 \cdot 10^{11}$ to $1 \cdot 10^{14}$ atoms/cm^2, into an area exposed by a body region implant mask, such as a photoresist pattern.. A subsequent anneal process activates at least a portion of the p-type dopants to form the body region 110. The body region 110 may extend to a depth between 300 to 1000 nanometers in the substrate 102. The body region 110 may be formed concurrently with other components of the semiconductor device 100 such as

p-type wells for n-channel MOS transistors, not shown. The anneal process to activate the p-type dopants may be performed concurrently with the anneal process to activate the first set of n-type dopants in the drain drift region 108.

[0015] A gate dielectric layer 112 of the MOS transistor 106 is formed over the substrate 102 overlapping a portion of the body region 110 and a portion of the drain drift region 108. The gate dielectric layer 112 may be one or more layers of silicon dioxide, silicon oxy-nitride, aluminum oxide, aluminum oxy-nitride, hafnium oxide, hafnium silicate, hafnium silicon oxy-nitride, zirconium oxide, zirconium silicate, zirconium silicon oxy-nitride, a combination of the aforementioned materials, or other insulating material. The gate dielectric layer 112 may include nitrogen as a result of exposure to a nitrogen containing plasma or a nitrogen containing ambient gas at temperatures between 50 C and 800 C. The gate dielectric layer 112 may be formed by any of a variety of gate dielectric formation processes, for example thermal oxidation, plasma nitridation of an oxide layer, and/or dielectric material deposition by atomic layer deposition (ALD). The gate dielectric layer 112 may be, for example, between 10 and 80 nanometers thick.

[0016] A gate 114 of the MOS transistor 106 is formed on the gate dielectric layer 112, overlapping a portion of the body region 110 and a portion of the drain drift region 108. The gate 114 may include, for example, one or more layers of polycrystalline silicon, commonly referred to as polysilicon, metal silicide such as tungsten silicide, titanium silicide, cobalt silicide and/or nickel silicide, and/or metal such as aluminum, tungsten and/or titanium nitride.

[0017] Optional gate sidewalls 116 may be formed on lateral surfaces of the gate 114, for example by deposition of one or more conformal layers of silicon nitride and/or silicon dioxide on a top and lateral surfaces of the gate 114 and the top surface of the substrate 102, followed by removal of the conformal layer material from the top surface of the gate 114 and the top surface of the substrate 102 by anisotropic etching methods such as reactive ion etching (RIE), leaving the conformal layer material on the lateral surfaces of the gate 114 so as to form the gate sidewalls 116.

[0018] The MOS transistor 106 also includes an n-type source region 118 and possibly an optional n-type drain contact region 120. The source region 118 is formed in the substrate 102 adjacent to the gate 114 opposite from the drain drift region 108. The drain

contact region 120 is formed in the substrate 102 contacting the drain drift region 108 opposite from the gate 114. The source region 118 and the drain contact region 120 may be formed, for example, by ion implanting a second set of n-type dopants, such as phosphorus and arsenic, and possibly antimony, at a total dose between $3 \cdot 10^{14}$ and $1 \cdot 10^{16}$ atoms/cm^2 into an area exposed by a source/drain implant mask, such as a photoresist pattern. A subsequent source/drain anneal process activates a portion of the second set of n-type dopants to form the source region 118 and the drain contact region 120. The source region 118 and the drain contact region 120 may extend from the top surface of the substrate 102 to a depth between 100 and 500 nanometers. The source region 118 and the drain contact region 120 may be formed concurrently with other components of the semiconductor device 100 such as source/drain regions for other n-channel MOS transistors, not shown. A layer or metal silicide, not shown, such as titanium silicide, cobalt silicide or nickel silicide, may be formed on the source region 118 and the drain contact region 120.

[0019] An element of the field oxide 104 may be disposed in the drain drift region 108 so as to laterally separate the drain contact region 120 from a remaining portion of the drain contact region 120; the drain contact region 120 extends under the field oxide 104.

[0020] Referring to FIG. 1B, a snubber capacitor dielectric layer 122 is formed over the drain drift region 108 adjacent to the gate 114. The snubber capacitor dielectric layer 122 may optionally overlap the field oxide element 104 disposed in the drain drift region 108 if present. The snubber capacitor dielectric layer 122 may include, for example, one or more layers of silicon dioxide, silicon oxy-nitride, aluminum oxide, aluminum oxy-nitride, hafnium oxide, hafnium silicate, hafnium silicon oxy-nitride, zirconium oxide, zirconium silicate, zirconium silicon oxy-nitride, a combination of the aforementioned materials, or other insulating material. The snubber capacitor dielectric layer 122 may be, for example, between 10 and 200 nanometers thick. The snubber capacitor dielectric layer 122 may be formed by any of a variety of gate dielectric formation processes, for example thermal oxidation, plasma nitridation of an oxide layer, and/or dielectric material deposition by ALD.

[0021] A snubber capacitor plate 124 is formed over the snubber capacitor dielectric layer 122 so as to be electrically isolated from the drain drift region 108. The snubber capacitor plate 124 may be formed of any electrically conductive material, such as one or more layers of polysilicon, tungsten, aluminum, titanium, tantalum, titanium tungsten, metal

silicide, titanium nitride, tantalum nitride, and/or tungsten nitride. The snubber capacitor plate 124 may be, for example between 1 and 10 microns wide in a direction perpendicular to a lateral boundary of the gate 114. The snubber capacitor plate 124 may be formed concurrently with other components in the semiconductor device 100 such as decoupling capacitor plates, not shown. The snubber capacitor plate 124, the snubber capacitor dielectric layer 122 and the drain drift region 108 form a snubber capacitor 126.

[0022] A pre-metal dielectric (PMD) layer is formed over an existing top surface of the semiconductor device 100. The PMD layer may be, for example, a dielectric layer stack including a PMD liner, a PMD main layer, and an optional PMD cap layer. The PMD liner may be silicon nitride or silicon dioxide, 10 to 100 nanometers thick, deposited by plasma enhanced chemical vapor deposition (PECVD) on the existing top surface of the semiconductor device 100. The PMD main layer may be a layer of silicon dioxide formed by a HARP process followed by a layer of silicon dioxide, phospho-silicate glass (PSG) or boro-phospho-silicate glass (BPSG), 100 to 1000 nanometers thick, deposited by a PECVD process on a top surface of the PMD liner, and sometimes leveled by a chemical-mechanical polish (CMP) process. The optional PMD cap layer may be 10 to 100 nanometers of a hard material such as silicon nitride, silicon carbide nitride or silicon carbide, formed on a top surface of the PMD main layer. The PMD layer is not shown in FIG. 1C to more clearly illustrate the other elements of the MOS transistor 106.

[0023] Referring to FIG. 1C, one or more snubber capacitor contacts 128 are formed through the PMD layer so as to make electrical contact with the snubber capacitor plate 124. One or more snubber source contacts 130 are formed in the PMD layer so as to make electrical contact with the source region 118. The snubber capacitor contacts 128 and snubber source contacts 130 may be formed concurrently.

[0024] One or more transistor drain contacts 132 are formed through the PMD layer so as to make electrical contact with the drain drift region 108, through the drain contact region 120 if present. One or more transistor source contacts 134 are formed through the PMD layer so as to make electrical contact with the source region 118. The transistor drain contacts 132 and the transistor source contacts 134 may be formed concurrently, and may be formed concurrently with the snubber capacitor contacts 128 and the snubber source contacts 130.

[0025] The transistor drain contacts 132, the transistor source contacts 134, the snubber capacitor contacts 128 and the snubber source contacts 130 may be formed, for example, by defining contact areas on a top surface of the PMD with a contact photoresist pattern, not shown, etching contact holes in the contact areas by removing PMD layer material using etching methods such as RIE to expose the snubber capacitor plate 124, the source region 118 and the drain contact region 120, and filling the contact holes with a contact liner, such as titanium and titanium nitride, and a contact fill metal, such as tungsten, followed by removal of the contact fill metal and contact liner from the top surface of the PMD layer using etching and/or CMP methods.

[0026] A snubber resistor link 136 is formed over the PMD layer so as to make electrical contact with the snubber capacitor contacts 128 and the snubber source contacts 130. A drain interconnect 138 is formed over the PMD layer so as to make electrical contact with the transistor drain contacts 132 and a source interconnect 140 is formed over the PMD layer so as to make electrical contact with the transistor source contacts 134. In the instant embodiment, the drain interconnect 138, the source interconnect 140 and the snubber resistor link 136 are formed concurrently, and may be formed concurrently with other interconnects, not shown, in the semiconductor device 100.

[0027] The drain interconnect 138, the source interconnect 140 and the snubber resistor link 136 may be formed using an aluminum metallization process, which includes forming a layer of barrier metal such as titanium tungsten or titanium nitride between 5 and 15 nanometers thick on the PMD layer, forming a layer of aluminum interconnect metal such as an alloy of 96 percent aluminum, 2 percent silicon and 2 percent copper between 100 and 1500 nanometers thick on the layer of barrier metal, and forming a layer of cap metal such as titanium tungsten or titanium nitride between 5 and 15 nanometers thick on the layer of aluminum interconnect metal. A metallization etch mask such as a photoresist pattern is formed over the layer of cap metal so as to expose the layer of cap metal in areas to remove unwanted metal. A metallization etch process is performed, such as an RIE step including fluorine to remove the cap metal in the exposed area, a subsequent RIE step including chlorine to etch the aluminum interconnect metal with fluorine to passivate lateral surfaces of the etched aluminum interconnect metal, followed by another RIE step including fluorine to etch the barrier metal, so as to leave an interconnect element.

[0028] Alternatively, the drain interconnect 138, the source interconnect 140 and the snubber resistor link 136 may be formed using a copper damascene interconnect process, which includes forming an interlevel dielectric (ILD) layer such as silicon dioxide or a low-k dielectric over the PMD layer, and etching trenches in the ILD layer, commonly between 100 and 250 nanometers deep, in areas defined for the copper damascene interconnects. The trenches expose top surfaces of the drain interconnect 138, the source interconnect 140 and the snubber resistor link 136. A layer of liner metal such as tantalum nitride is formed on a bottom and sides of the trenches, commonly by physical vapor deposition, atomic layer deposition or chemical vapor deposition. A seed layer of copper is formed on the liner metal, commonly by sputtering. The trenches are subsequently filled with copper, commonly by electroplating. Copper and liner metal are removed from a top surface of the ILD layer by CMP and etch processes, leaving the copper damascene interconnects in the ILD layer.

[0029] In the instant embodiment, the snubber capacitor contacts 128, the snubber resistor link 136 and the snubber source contacts 130 form a snubber resistor 142 which is connected in series between the snubber capacitor plate 124 and the source region 118. One or more resistor apertures 144 may be formed in the snubber resistor link 136 to increase an electrical resistance of the snubber resistor 142. A total quantity of the snubber capacitor contacts 128 and/or a total quantity of the snubber source contacts 130 may be selected to provide a desired value of the electrical resistance of the snubber resistor 142. The electrical resistance of the snubber resistor 142 may be, for example, between 0.5 ohms and 20 ohms. The snubber resistor 142 and the snubber capacitor 126 form an integrated snubber 146.

[0030] FIGS. 2A - 2C illustrate stages in the fabrication of a semiconductor device including an extended drain MOS transistor with a snubber according to a modified example embodiment.

[0031] Referring to FIG. 2A, the semiconductor device 200 is formed in and on a semiconductor substrate 202 as described in reference to FIG. 1A. Field oxide, not shown, may optionally be formed at the top surface of the substrate 202, as described in reference to FIG. 1A. The MOS transistor 204 has an n-type drain drift region 206, as described in reference to FIG. 1A, extending to the top surface of the substrate 202. The MOS transistor 204 further includes a p-type body region 208 in the substrate 202 abutting the drain drift region 206, as described in reference to FIG. 1A. A gate dielectric layer 210, gate 212 and

optional gate sidewalls 214 of the MOS transistor 204 are formed over the substrate 202 overlapping a portion of the body region 208 and a portion of the drain drift region 206, as described in reference to FIG. 1A. The MOS transistor 204 also includes an n-type source region 216 and possibly an optional n-type drain contact region 218, as described in reference to FIG. 1A.

[0032] A snubber capacitor dielectric layer 220 is formed over an existing top surface of the semiconductor device 200. The snubber capacitor dielectric layer 220 may be formed of materials described in reference to FIG. 1B. In the instant embodiment, the snubber capacitor dielectric layer 220 extends above the drain drift region 206 and over the gate 212 and source region 216.

[0033] Referring to FIG. 2B, a snubber resistor/capacitor layer 222 is formed on the snubber capacitor dielectric layer 220, extending above the drain drift region 206 and over the gate 212 and source region 216. The snubber resistor/capacitor layer 222 is patterned so as to be electrically isolated from other components, not shown, in the semiconductor device 200. The snubber resistor/capacitor layer 222 may include one or more layers of electrically conductive material such as polysilicon, metal silicide such as tungsten silicide, titanium silicide, cobalt silicide or nickel silicide, metal such as aluminum, tungsten, titanium, tantalum, or metal alloy such as titanium tungsten, titanium nitride, tantalum nitride, nickel chromium, silicon chromium or thin film resistor material such as cermet, a ceramic-metal material.

[0034] A portion of the snubber resistor/capacitor layer 222 over the drain drift region 206 forms a snubber capacitor plate 224. The snubber capacitor plate 224, the snubber capacitor dielectric layer 220 and the drain drift region 206 form a snubber capacitor 226.

[0035] A portion of the snubber resistor/capacitor layer 222 over the gate 212 and source region 216 forms a snubber resistor 228. A thickness of the snubber resistor/capacitor layer 222 may be selected so as to provide a desired value of electrical resistance of the snubber resistor 228. One or more resistor apertures 230 may be formed in the snubber resistor/capacitor layer 222 so as to increase the electrical resistance of the snubber resistor 228. The electrical resistance of the snubber resistor 228 may be, for example, between 0.5 and 20 ohms.

[0036] A PMD layer, not shown, is formed over an existing top surface of the semiconductor device 200, as described in reference to FIG. 1C. The PMD layer is not shown in FIG. 2C to more clearly illustrate the other elements of the MOS transistor 204.

[0037] Referring to FIG. 2C, one or more transistor drain contacts 232 are formed through the PMD layer so as to make electrical contact with the drain drift region 206, through the drain contact region 218 if present. One or more transistor source contacts 234 are formed through the PMD layer so as to make electrical contact with the source region 216 and the snubber resistor 228. The transistor drain contacts 232 and the transistor source contacts 234 may be formed as described in reference to FIG. 1C.

[0038] The snubber resistor 228 and the snubber capacitor 226 form an integrated snubber 236.

[0039] FIGS. 3A - 3C illustrate stages in the fabrication of a semiconductor device including an extended drain MOS transistor with a snubber according to another modified example embodiment.

[0040] Referring to FIG. 3A, the semiconductor device 300 is formed in an on a thin semiconductor substrate 302. The substrate 302 may be single crystal silicon or a semiconductor allow such as silicon germanium. In the instant embodiment, the substrate 302 is between 5 and 100 microns thick. The MOS transistor 304 includes an n-type drain drift region 306 which extends from a top surface of the substrate 302 to, or proximate to, a bottom surface of the substrate 302. The MOS transistor 304 may optionally include an n-type drain contact region 308 at the bottom surface of the substrate 302 and contacting the drain drift region 306. The drain contact region 308 may be formed by ion implanting the bottom surface of the substrate 302 with n-type dopants and subsequently performing an anneal process to activate at least a portion of the implanted dopants. The MOS transistor 304 further includes a drain contact metal layer 310 on, and making electrical connection with, the bottom surface of the substrate 302.

[0041] The MOS transistor 304 includes a p-type body region 312 in the substrate 302 abutting the drain drift region 306, at the top surface of the substrate 302. A gate dielectric layer 314 and gate 316 of the MOS transistor 304 are formed over the substrate 302 overlapping a portion of the body region 312 and a portion of the drain drift region 306 at the top surface of the substrate 302. The MOS transistor 304 also includes an n-type source

region 318 formed in the substrate 302 adjacent to the gate 316 opposite from the drain drift region 306, and isolated from the drain drift region 306 by the body region 312.

[0042] Referring to FIG. 3B, a snubber capacitor dielectric layer 320 is formed over an existing top surface of the semiconductor device 300. The snubber capacitor dielectric layer 320 may be formed of materials described in reference to FIG. 1B. In the instant embodiment, the snubber capacitor dielectric layer 320 extends above the drain drift region 306 and over the gate 316 and source region 318.

[0043] A source trench 322 is formed in the substrate 302 through the source region 318 and into the body region 312, adjacent to, but laterally separated from, the gate 316.

[0044] Referring to FIG. 3C, a snubber resistor/capacitor layer 324 is formed on the snubber capacitor dielectric layer 320, extending above the drain drift region 306 and over the gate 316 and source region 318, and into the source trench 322 so as to make electrical contact with the source region 318 and the body region 312. The snubber resistor/capacitor layer 324 is patterned so as to be electrically isolated from other components, not shown, in the semiconductor device 300. The snubber resistor/capacitor layer 324 may be formed of the materials described in reference to FIG. 2C.

[0045] A portion of the snubber resistor/capacitor layer 324 over the drain drift region 306 forms a snubber capacitor plate 326. The snubber capacitor plate 326, the snubber capacitor dielectric layer 320 and the drain drift region 306 form a snubber capacitor 328.

[0046] A portion of the snubber resistor/capacitor layer 324 over the gate 316 forms a snubber resistor 330. A thickness of the snubber resistor/capacitor layer 324 may be selected so as to provide a desired value of electrical resistance of the snubber resistor 330. One or more resistor apertures 332 may be formed in the snubber resistor/capacitor layer 324 so as to increase the electrical resistance of the snubber resistor 330. The electrical resistance of the snubber resistor 330 may be, for example, between 0.5 and 20 ohms. The snubber resistor 330 and the snubber capacitor 328 form an integrated snubber 334.

[0047] FIGS. 4A and 4B illustrate stages in the fabrication of a semiconductor device including an extended drain MOS transistor with a snubber according to another modified example embodiment.

[0048] Referring to FIG. 4A, the semiconductor device 400 is formed in and on a semiconductor substrate 402 as described in reference to FIG. 1A. Field oxide 404 may be formed at the top surface of the substrate 402, as described in reference to FIG. 1A, for example to laterally isolate the MOS transistor 406 from other components, not shown, in the semiconductor device 400. The MOS transistor 406 has an n-type drain drift region 408, as described in reference to FIG. 1A, extending to the top surface of the substrate 402. The MOS transistor 406 further includes a p-type body region 410 in the substrate 402 abutting the drain drift region 408, as described in reference to FIG. 1A. A gate dielectric layer 412, gate 414 and optional gate sidewalls 416 of the MOS transistor 406 are formed over the substrate 402 overlapping a portion of the body region 410 and a portion of the drain drift region 408, as described in reference to FIG. 1A. The MOS transistor 406 also includes an n-type source region 418 and possibly an optional n-type drain contact region 420, as described in reference to FIG. 1A. The drain contact region 420 may be laterally isolated by an additional element of field oxide 404, as depicted in FIG. 4A.

[0049] A snubber capacitor dielectric layer 422 is formed over the drain drift region 408 adjacent to the gate 414, as described in reference to FIG. 1B. The snubber capacitor dielectric layer 422 may optionally overlap the field oxide element 404 disposed in the drain drift region 408 if present. A snubber capacitor plate 424 is formed over the snubber capacitor dielectric layer 422 so as to be electrically isolated from the drain drift region 408, as described in reference to FIG. 1B. The snubber capacitor plate 424, the snubber capacitor dielectric layer 422 and the drain drift region 408 form a snubber capacitor 426.

[0050] A PMD layer, not shown, is formed over an existing top surface of the semiconductor device 400, as described in reference to FIG. 1C. The PMD layer is not shown in FIG. 4B to more clearly illustrate the other elements of the MOS transistor 406. One or more snubber capacitor contacts 428, for example continuous snubber capacitor contacts 428 as depicted in FIG. 4A, are formed through the PMD layer so as to make electrical contact with the snubber capacitor plate 424, as described in reference to FIG. 1C. One or more transistor drain contacts 430, for example continuous transistor drain contacts 430, are formed through the PMD layer so as to make electrical contact with the drain drift region 408, through the drain contact region 420 if present. One or more transistor source contacts 432, for example continuous transistor source contacts 432, are formed through the

PMD layer so as to make electrical contact with the source region 418. The transistor drain contacts 430, the transistor source contacts 432 and the snubber capacitor contacts 428 may be formed as described in reference to FIG. 1C, using contact trenches for continuous contacts.

[0051] A snubber resistor 434 is formed over the PMD layer so as to make electrical contact with the snubber capacitor contacts 428 and the transistor source contacts 432. The snubber resistor 434 is patterned so as be electrically isolated from other components, not shown, in the semiconductor device 400. A portion of the snubber resistor 434 is removed in FIG. 4A to illustrate the transistor source contacts 432. The snubber resistor 434 may include one or more layers of electrically conductive material, such as such as polysilicon, metal silicide such as tungsten silicide, titanium silicide, cobalt silicide or nickel silicide, metal such as aluminum, tungsten, titanium, tantalum, or metal alloy such as titanium tungsten, titanium nitride, tantalum nitride, nickel chromium, silicon chromium or thin film resistor material such as cermet. One or more resistor apertures 436 may be formed in the snubber resistor 434 so as to increase the electrical resistance of the snubber resistor 434. The electrical resistance of the snubber resistor 434 may be, for example, between 0.5 and 20 ohms. The snubber resistor 434 and the snubber capacitor 426 form an integrated snubber 438.

[0052] Referring to FIG. 4B, a drain interconnect 440 is formed on the PMD layer so as to make electrical contact with the transistor drain contacts 430. A source interconnect 442 is formed on the snubber resistor 434 so as to make electrical contact with the transistor source contacts 432 through the snubber resistor 434. The drain interconnect 440 and the source interconnect 442 may be formed by an aluminum metallization process or a copper damascene metallization process, as described in reference to FIG. 1C.

[0053] Those skilled in the art to which the invention relates will appreciate that further modifications may be made to the described example implementations, and also that many other embodiments are possible, within the scope of the claimed invention.

CLAIMS

What is claimed is:

1. A semiconductor device, comprising:

a semiconductor substrate;

an extended drain metal oxide semiconductor (MOS) transistor, including:

a drain drift region disposed in said substrate, said drain drift region having a first conductivity type;

a body region disposed in said substrate such that said body region abuts said drain drift region at a top surface of said substrate, said body region having a second conductivity type opposite from said first conductivity type;

a gate disposed over said substrate, said gate overlapping a portion of said drain drift region and a portion of said body region; and

a source region disposed in said substrate adjacent to said gate and opposite from said drain drift region, said source region having said first conductivity type; and

an integrated snubber, comprising:

a snubber capacitor, said snubber capacitor including said drain drift region, a snubber dielectric layer disposed over said drain drift region, and a snubber capacitor plate disposed over said dielectric layer; and

a snubber resistor disposed over said gate, said snubber resistor being electrically coupled to said source region and electrically coupled to said snubber capacitor plate.

2. The device of claim 1, wherein:

said snubber dielectric layer is between 10 and 200 nanometers thick; and

said snubber resistor includes:

at least one snubber capacitor contact disposed in a pre-metal dielectric (PMD) layer, said snubber capacitor contact being disposed on, and electrically connected to, said snubber capacitor plate;

at least one snubber source contact disposed in said PMD layer, said snubber source contact being disposed on, and electrically connected to said source region; and

a snubber resistor link disposed on said PMD layer, said snubber resistor link making electrical contact to said snubber capacitor contact and to said snubber source contact.

3. The device of claim 1, wherin said snubber resistor includes at least one resistor aperture disposed through said snubber resistor.

4. The device of claim 1,wherein:

said snubber capacitor dielectric layer is between 10 and 200 nanometers thick;

said snubber capacitor dielectric layer is further disposed over said gate;

said snubber capacitor plate is a portion of a snubber resistor/capacitor layer disposed over said drain drift region, said snubber resistor/capacitor layer being disposed on said snubber capacitor dielectric layer, so that said snubber resistor/capacitor layer extends above said drain drift region, over said gate and over said source region;

said snubber resistor is a portion of said snubber resistor/capacitor layer disposed over said gate and said source region; and

said snubber resistor/capacitor layer is electrically coupled to said source region through at least one transistor source contact.

5. The device of claim 4, wherein said snubber resistor/capacitor layer includes at least one resistor aperture disposed through said snubber resistor/capacitor layer.

6. The device of claim 1, in which:

said drain drift region extends from said top surface of said substrate to a depth of approximately 5 and 100 microns of said substrate;

said MOS transistor includes a drain contact region disposed at said bottom surface of said substrate, said drain contact region contacting said drain drift region, such that said drain contact region has said first conductivity type;

said snubber capacitor dielectric layer is between 10 and 200 nanometers thick;

said snubber capacitor dielectric layer is further disposed over said gate;

said substrate includes a source trench disposed through said source region and into said body region adjacent to, but laterally separated from, said gate;

said snubber capacitor plate is a portion of a snubber resistor/capacitor layer disposed over said drain drift region, said snubber resistor/capacitor layer being disposed on said snubber capacitor dielectric layer, so that said snubber resistor/capacitor layer extends above said drain drift region, over said gate, over said source region and in said source trench so as to make electrical contact with said source region and said body region; and

said snubber resistor is a portion of said snubber resistor/capacitor layer disposed over said gate and said source region.

7. The device of claim 6, in which said snubber resistor/capacitor layer includes at least one resistor aperture disposed through said snubber resistor/capacitor layer.

8. The device of claim 1, wherein:

said snubber capacitor dielectric layer is between 10 and 200 nanometers thick;

said snubber resistor is disposed over a pre-metal dielectric (PMD) layer;

said snubber resistor includes at least one layer of material selected from the group consisting of polysilicon, tungsten silicide, titanium silicide, cobalt silicide, nickel silicide, aluminum, tungsten, titanium, tantalum, titanium tungsten, titanium nitride, tantalum nitride, nickel chromium, silicon chromium, and cermet;

said snubber resistor is electrically connected to said snubber capacitor plate through at least one snubber capacitor contact, said snubber capacitor contact being disposed in said PMD layer on said snubber capacitor plate;

said snubber resistor is electrically connected to said source region through at least one transistor source contact, said transistor source contact being disposed in said PMD layer on said snubber capacitor plate; and

said semiconductor device includes source interconnect disposed on said snubber resistor so as to make electrical contact with said transistor source contacts through said snubber resistor.

9. The device of claim 8, wherein said snubber resistor includes at least one resistor aperture disposed through said snubber resistor.

10. A method of forming a semiconductor device, comprising steps:

providing a semiconductor substrate;

forming an extended drain metal oxide semiconductor (MOS) transistor, by a process including steps:

forming a drain drift region in said substrate, said drain drift region having a first conductivity type;

forming a body region in said substrate, so that said body region abuts said drain drift region at a top surface of said substrate, said body region having a second conductivity type opposite from said first conductivity type;

forming a gate over said substrate, so that said gate overlaps a portion of said drain drift region and a portion of said body region; and

forming a source region in said substrate adjacent to said gate and opposite from said drain drift region, said source region having said first conductivity type; and

forming an integrated snubber, by a process including steps:

forming a snubber capacitor, by a process including steps:

forming a snubber dielectric layer over said drain drift region ; and

forming a snubber capacitor plate over said snubber dielectric layer; and

forming a snubber resistor over said gate, said snubber resistor being electrically coupled to said source region and electrically coupled to said snubber capacitor plate.

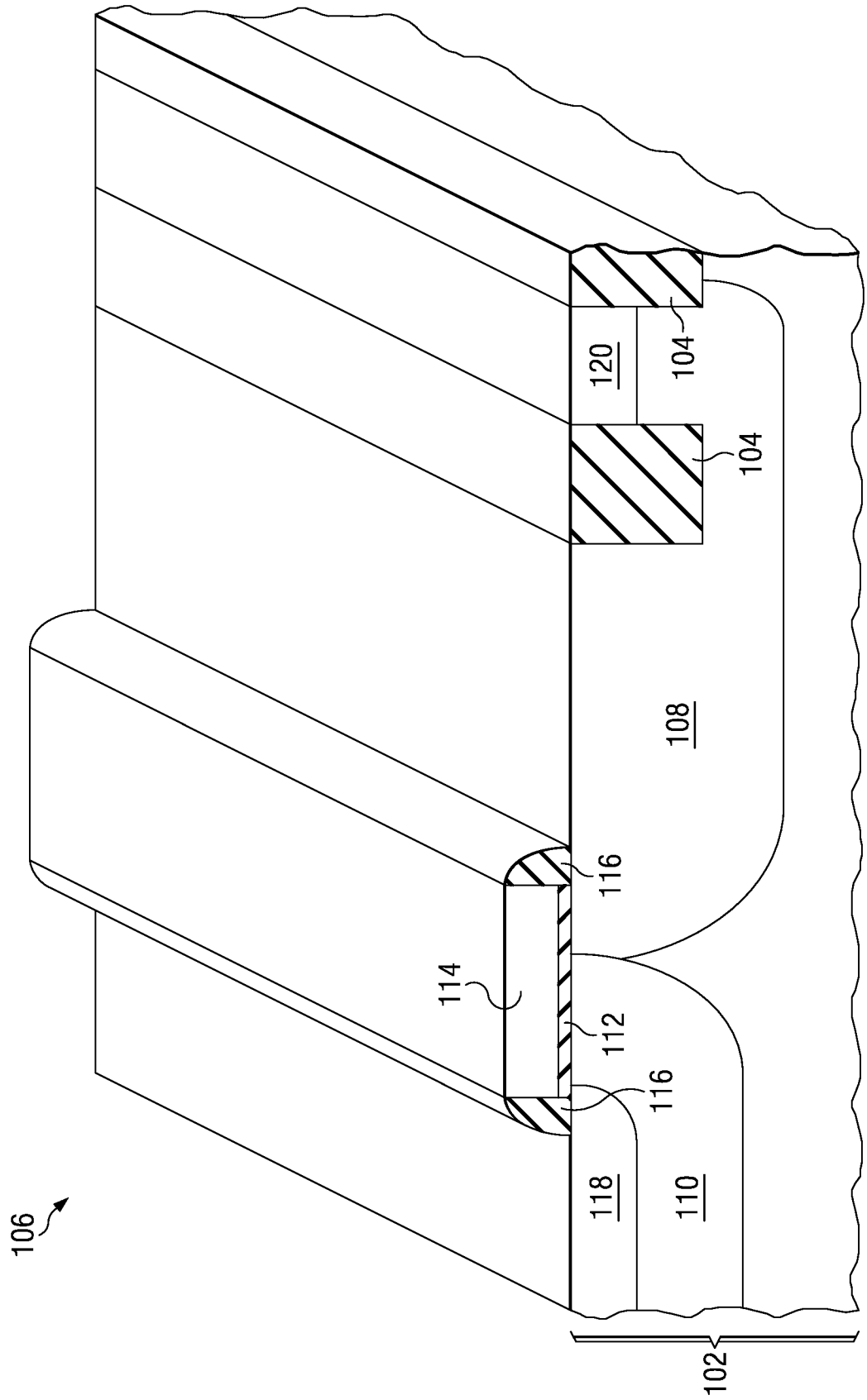

FIG. 1A

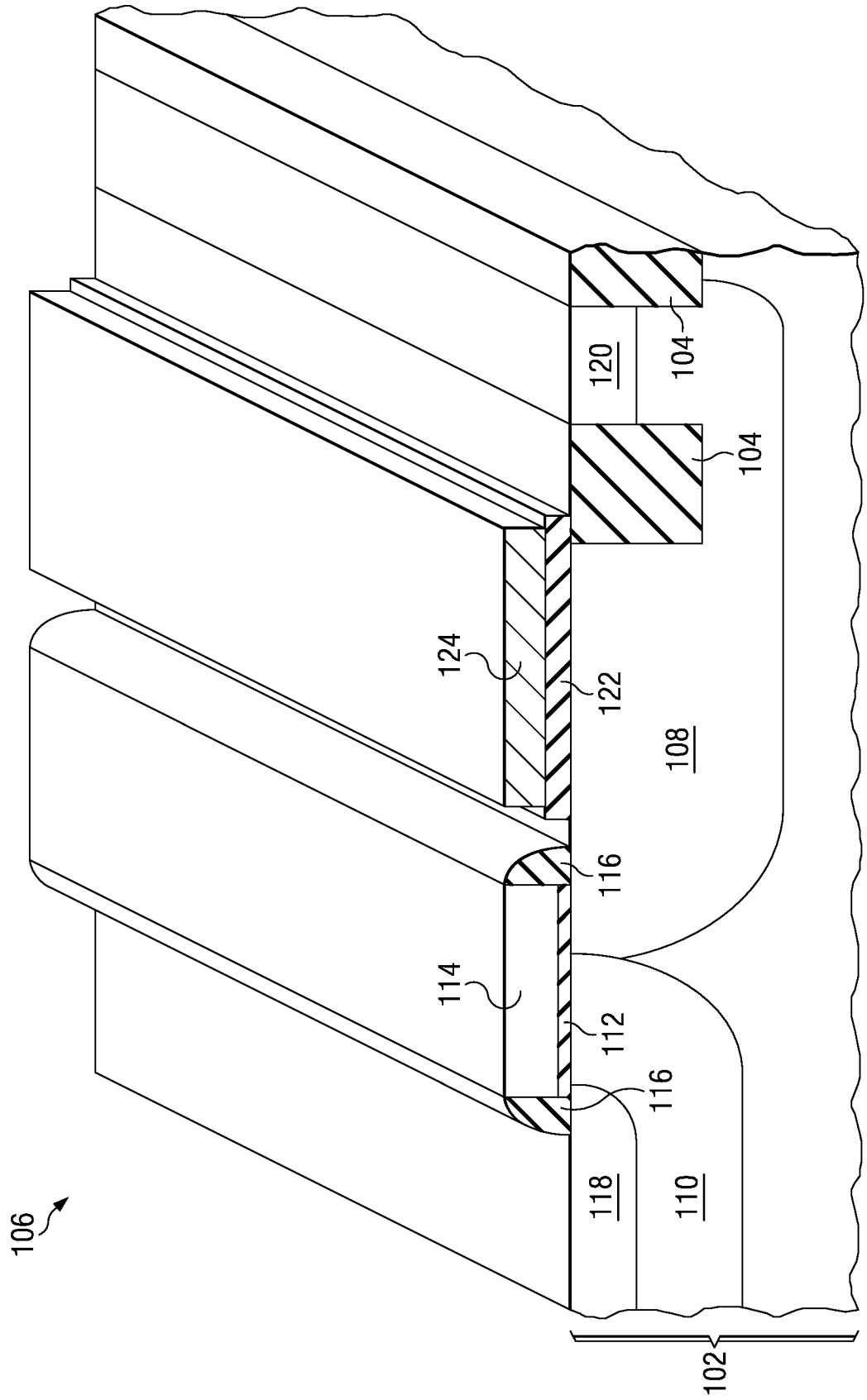

FIG. 1B

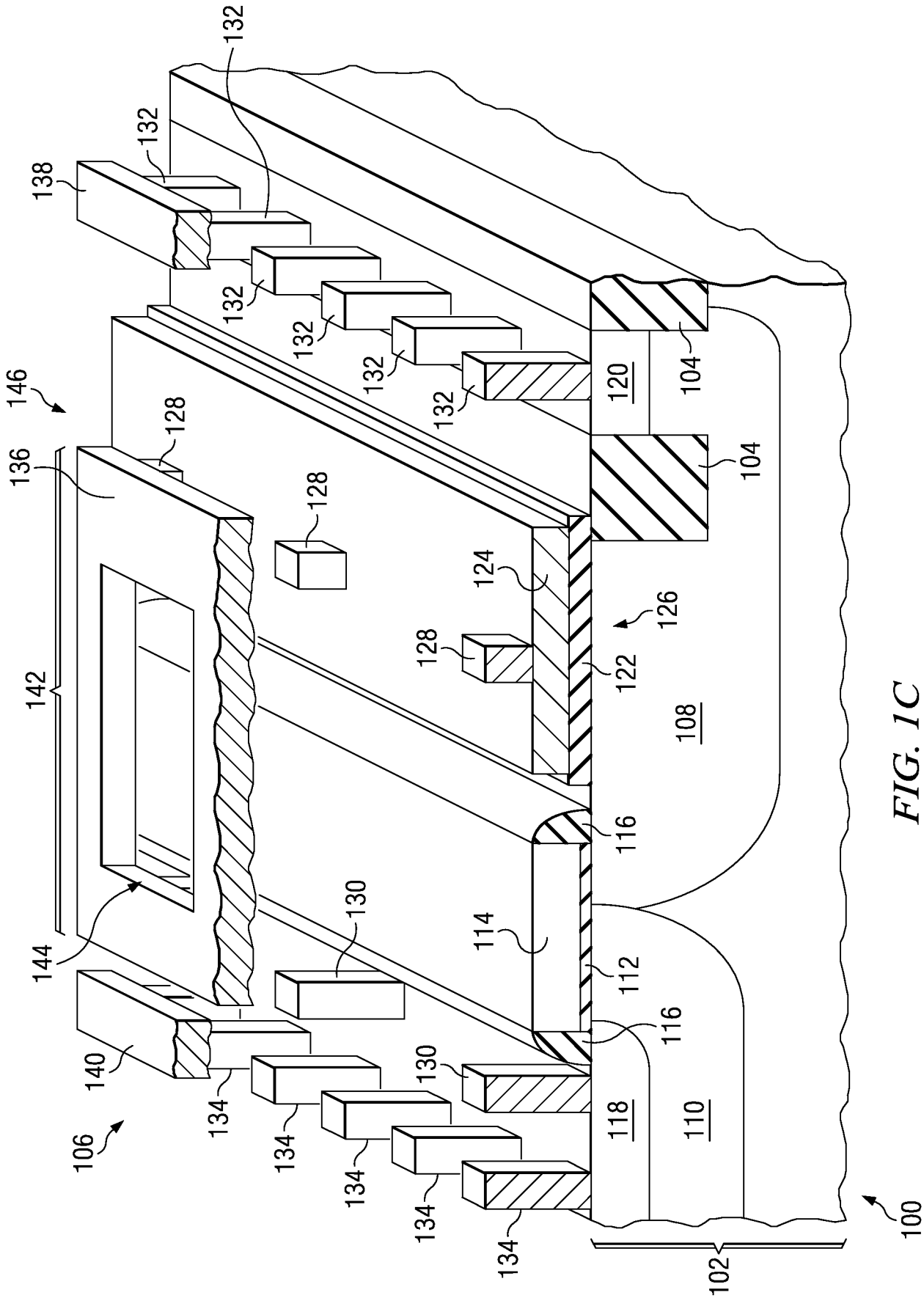
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FIG. 1C

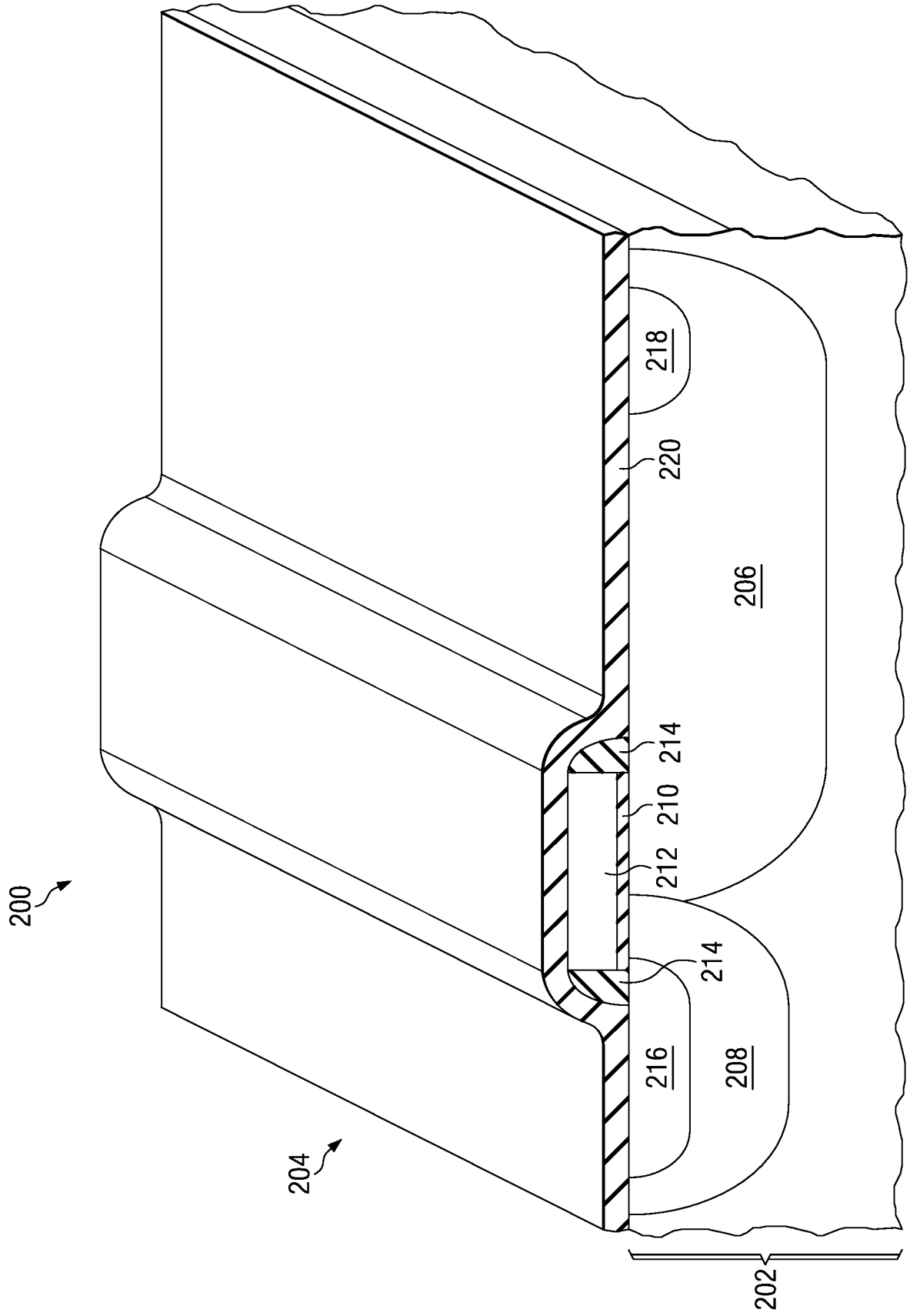

FIG. 2A

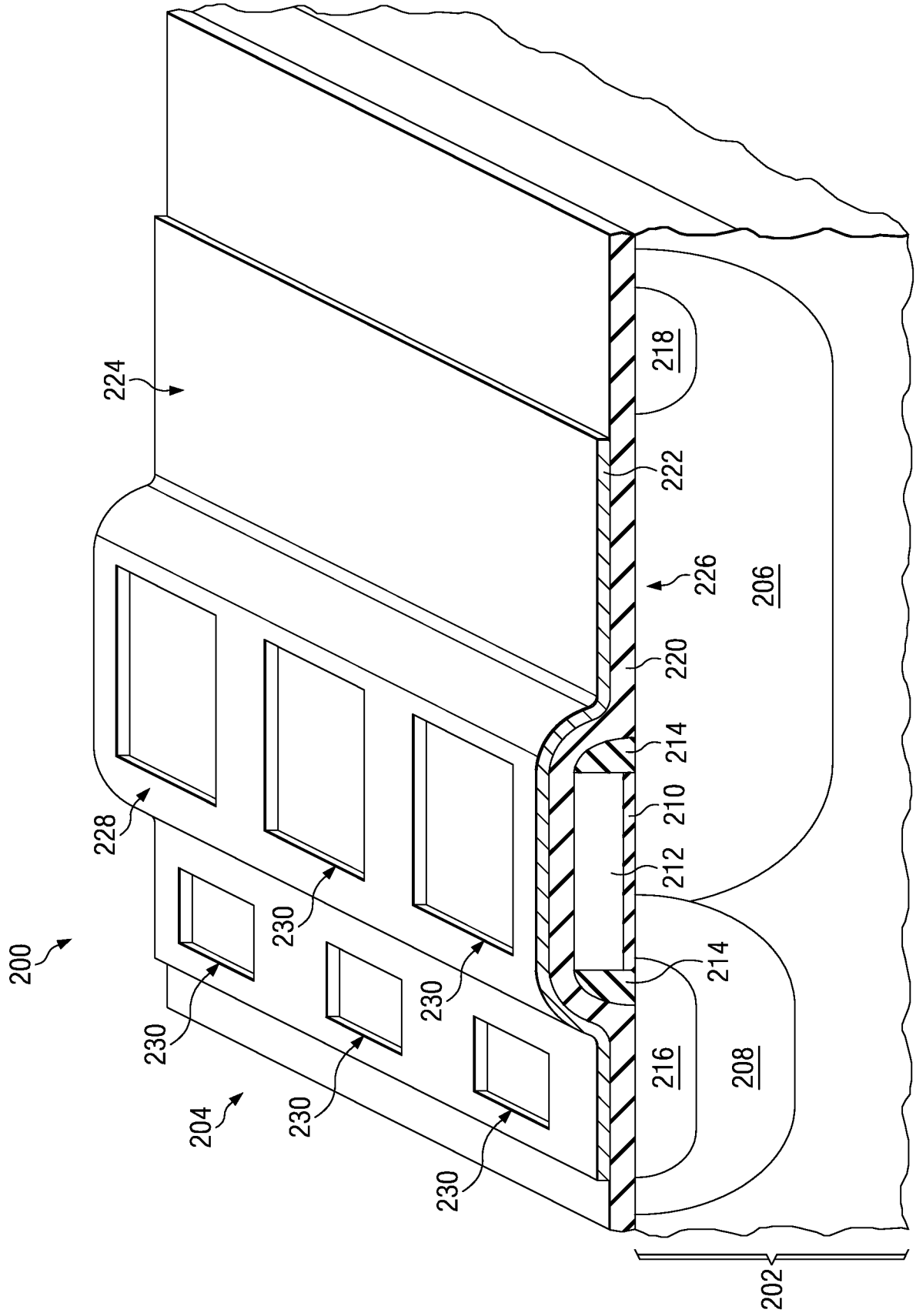

FIG. 2B

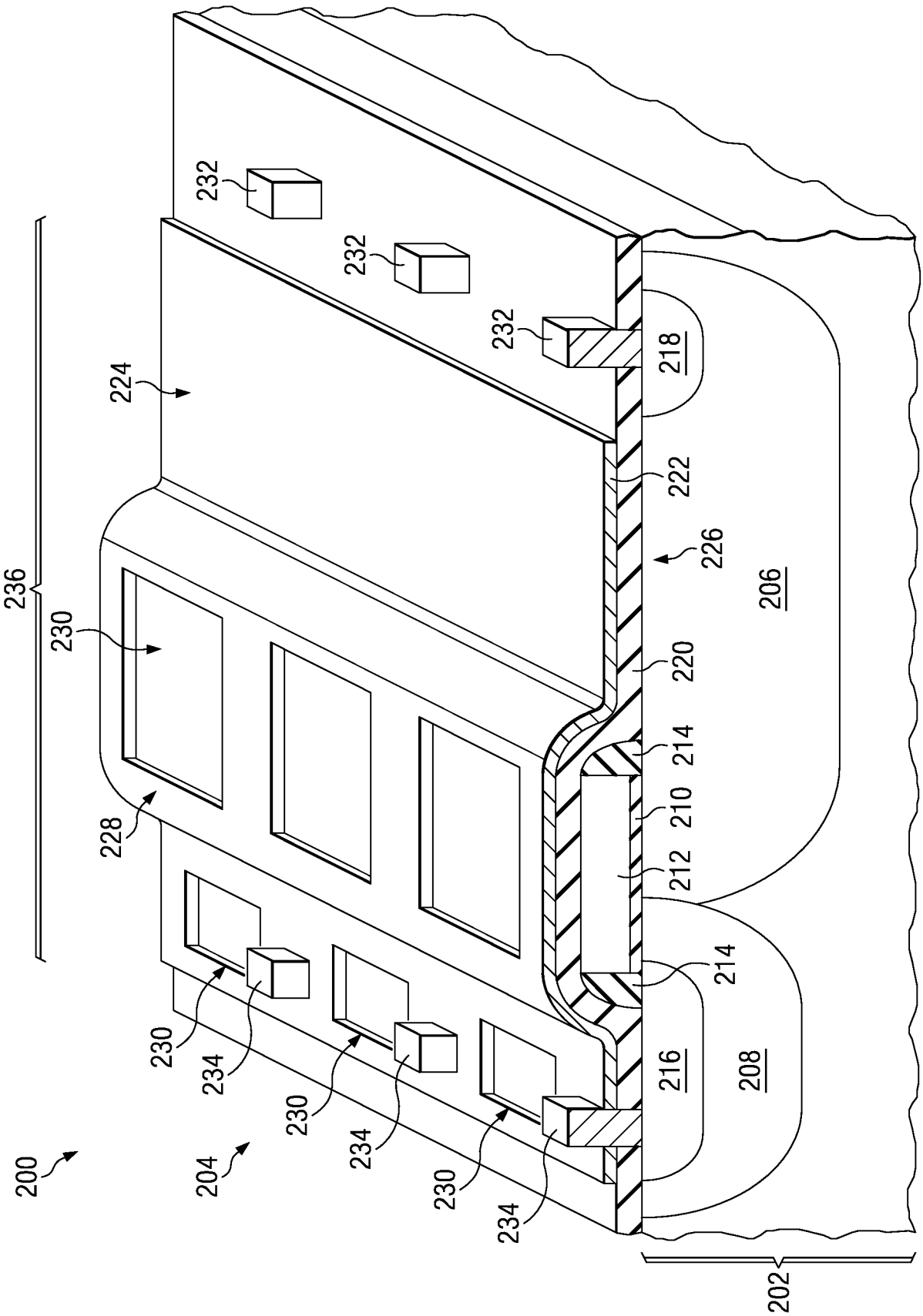
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FIG. 2C

FIG. 3A

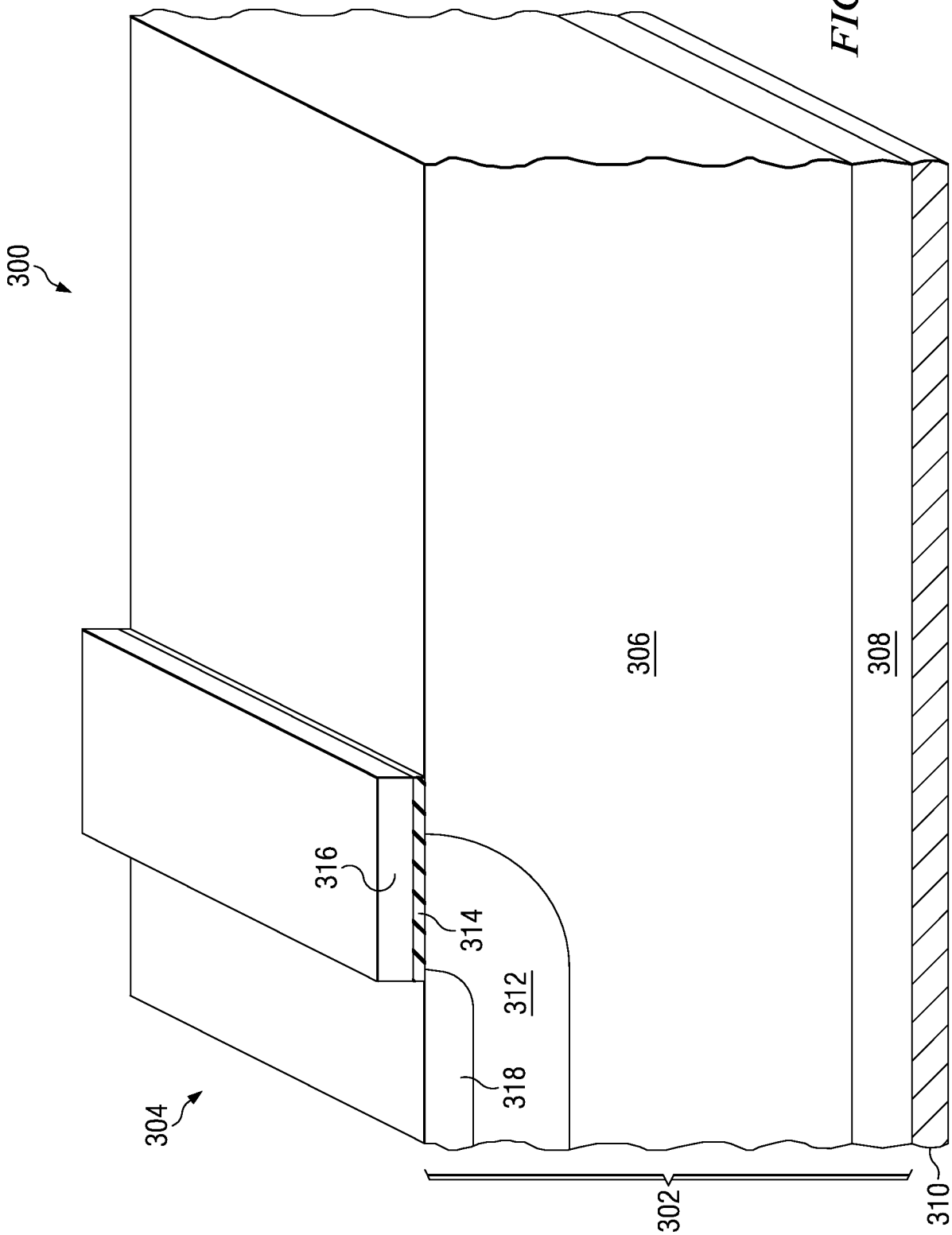
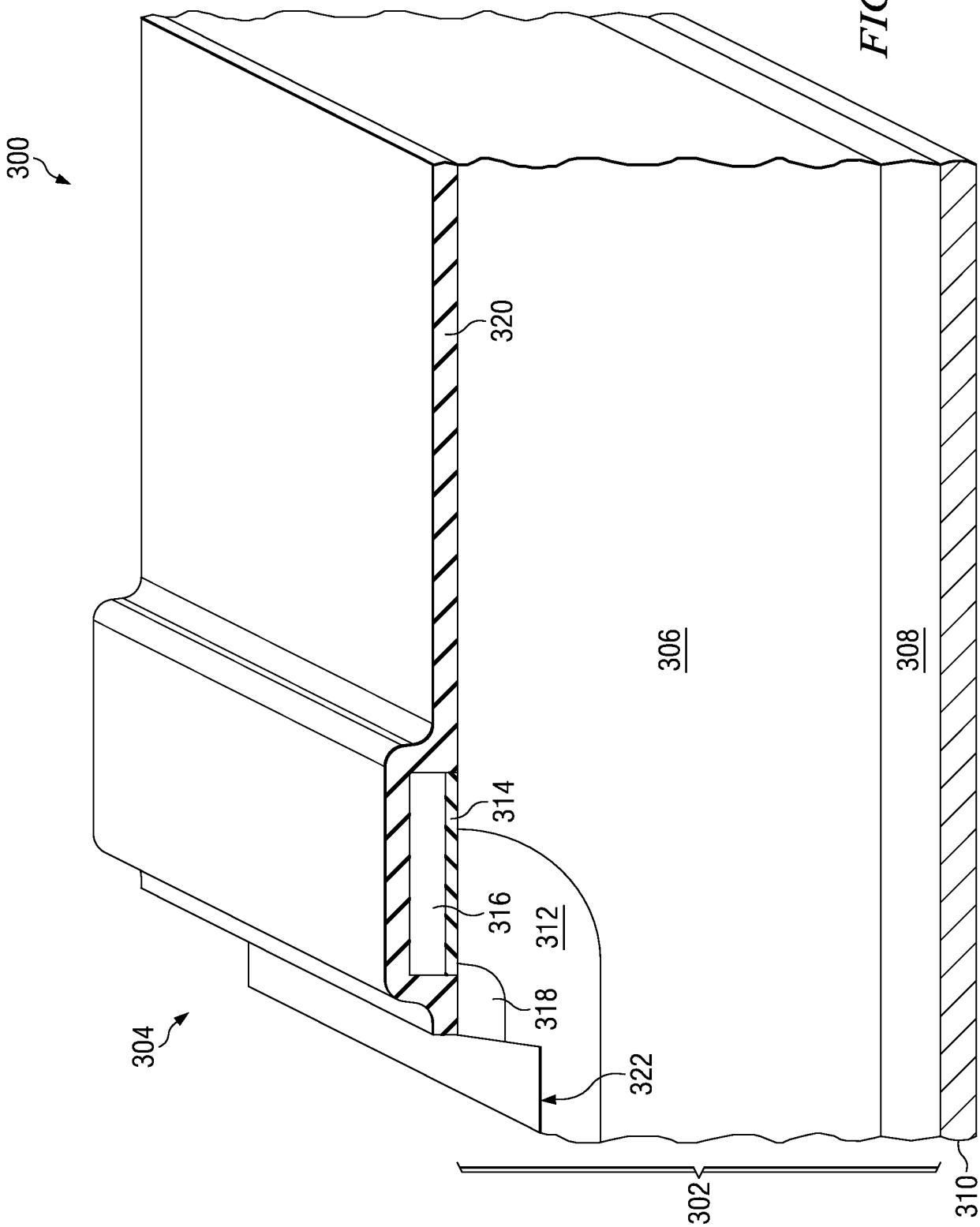


FIG. 3B



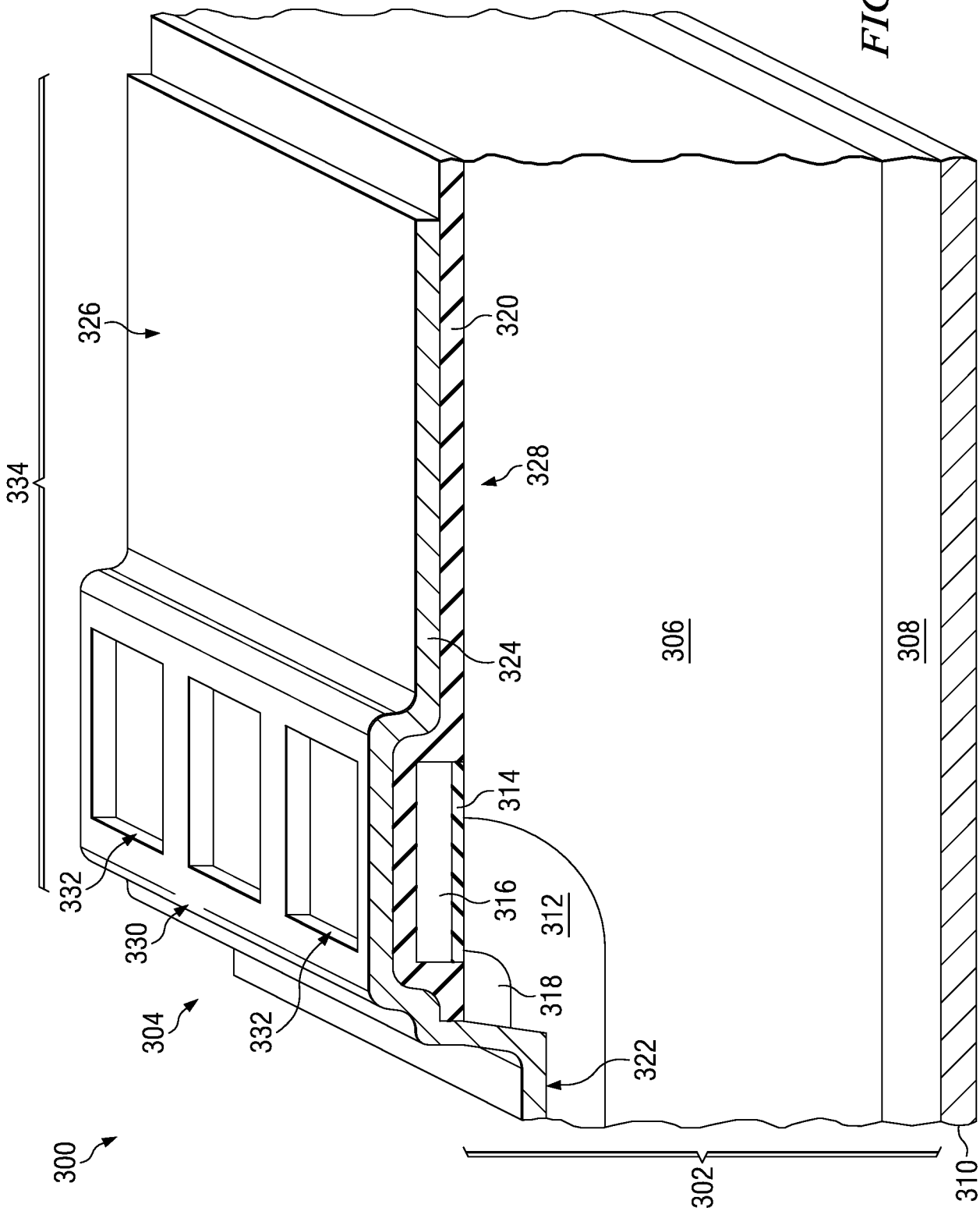

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FIG. 3C

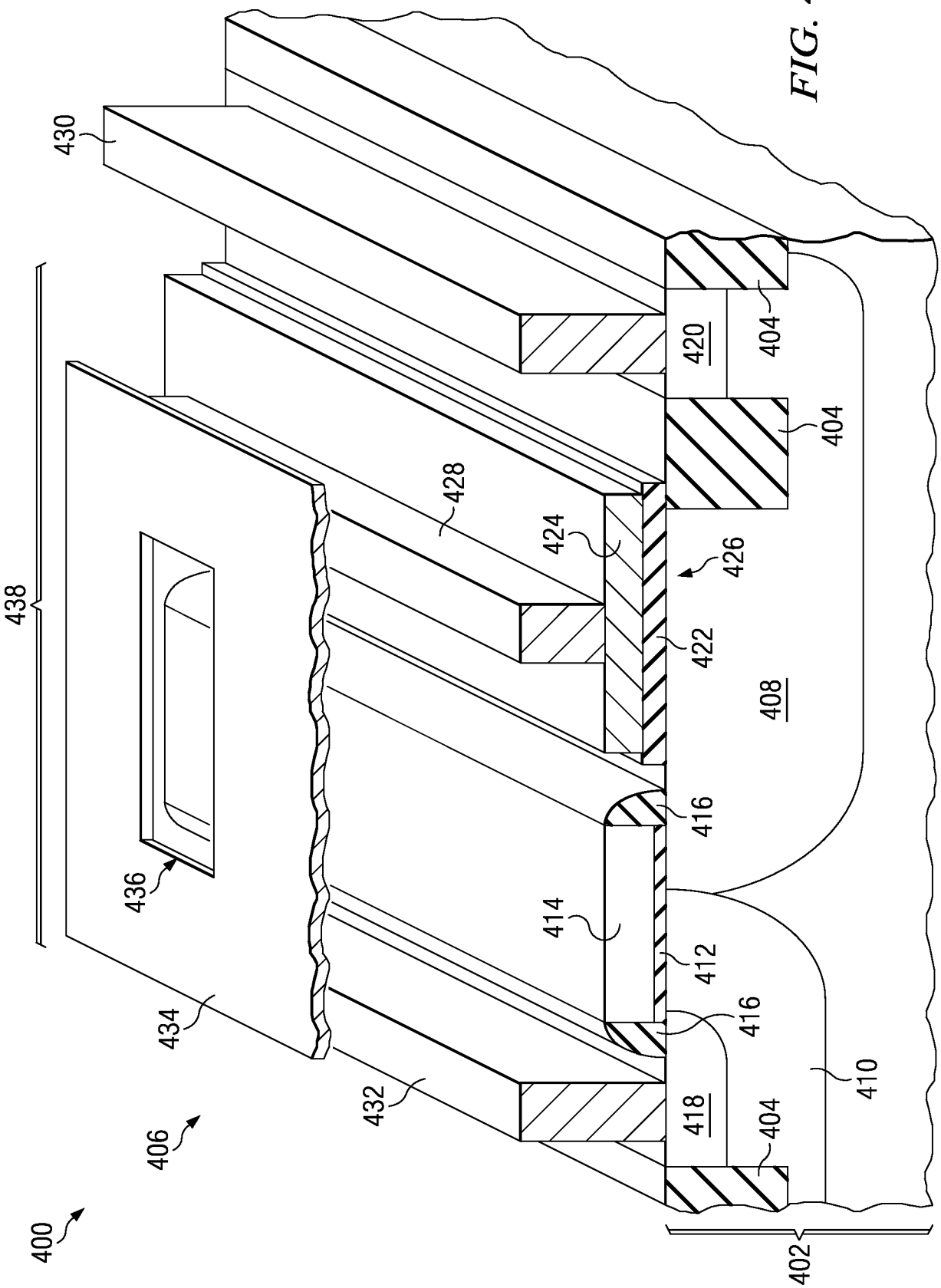
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FIG. 4A

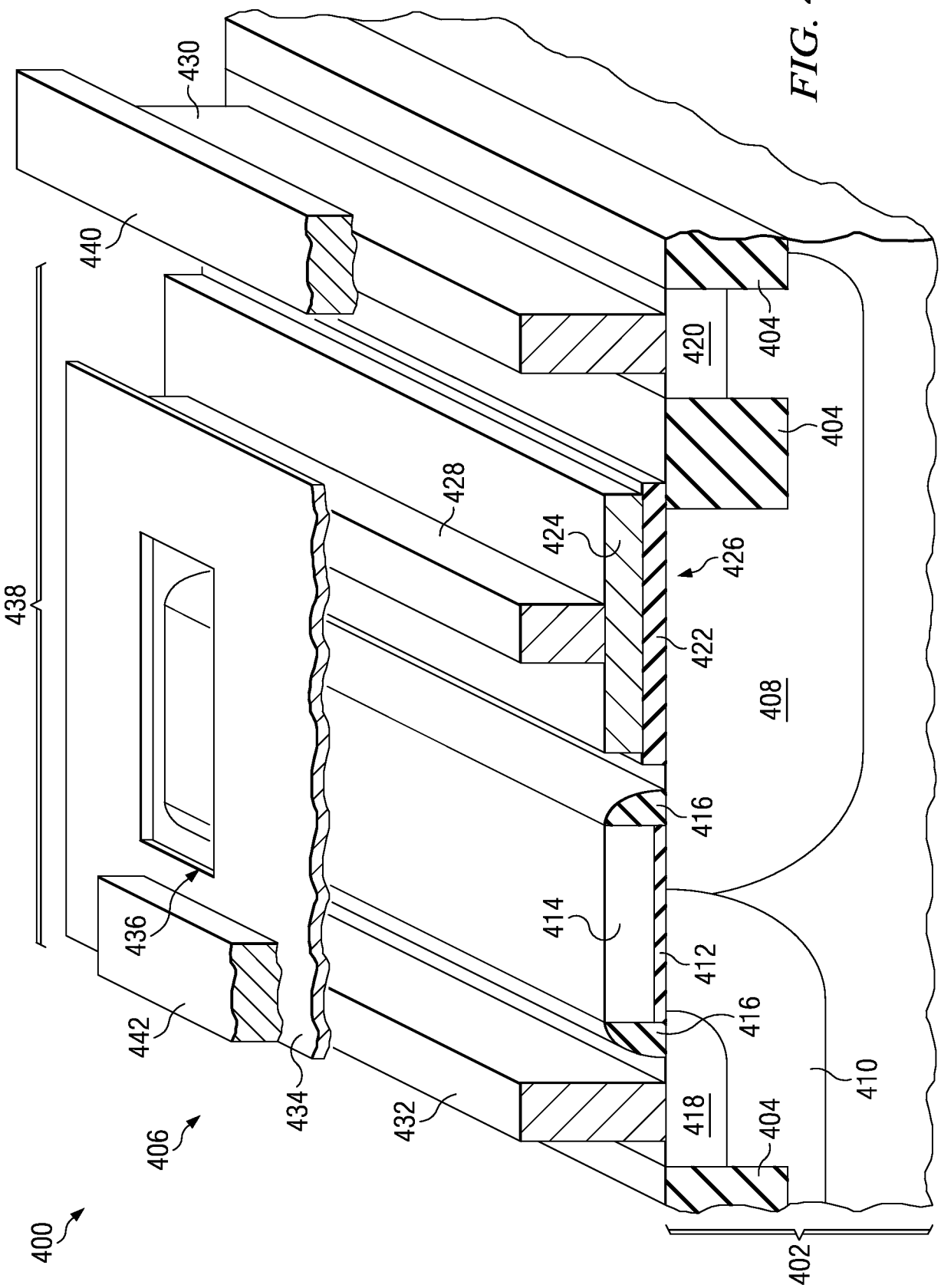
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FIG. 4B