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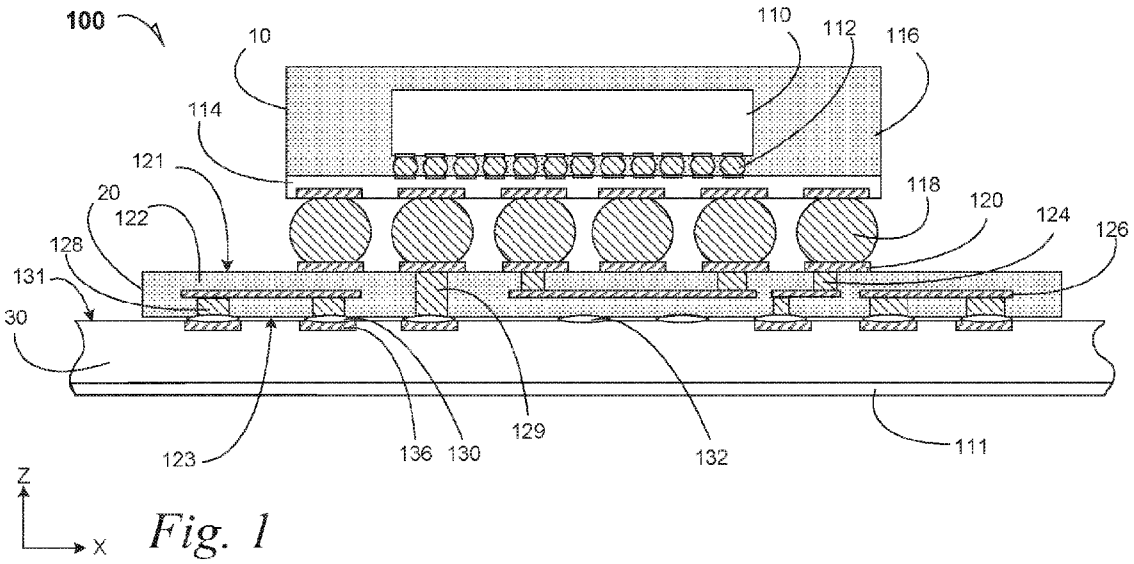


Fig. 1

(57) Abstract: A printed wiring-board island relieves added complexity to a printed circuit board. The printed wiring-board island creates an island form factor in the printed circuit board. Coupling of a semiconductive device package to the printed wiring-board island includes a ball-grid array. The ball-grid array can at least partially penetrate the printed wiring-board island.

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PRINTED WIRING-BOARD ISLANDS FOR CONNECTING CHIP PACKAGES AND METHODS OF ASSEMBLING SAME

FIELD

This disclosure relates to printed wiring-board islands that are mated to printed circuit boards for connecting chip packages.

BACKGROUND

Printed circuit boards have routing densities that can require multiple layers for mounting semiconductive device packaging. Routing densities sometimes require increased printed circuit-board complexity.

BRIEF DESCRIPTION OF THE DRAWINGS

Disclosed embodiments are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings where like reference numerals may refer to similar elements, in which:

Figure 1 is a cross-section elevation of a printed wiring-board island in an apparatus according to an embodiment;

Figure 2 is a cross-section elevation of a printed wiring-board island in an apparatus according to an embodiment;

Figure 3 is a cross-section elevation of a printed wiring-board island in an apparatus according to an embodiment;

Figure 4 illustrates a top plan cut away and a cross-section elevation of a portion of a printed wiring-board island according to an embodiment;

Figure 5 illustrates a top plan cut away and a cross-section elevation of a portion of a printed wiring-board island according to an embodiment;

Figure 6 is a cross-section elevation of a portion of a printed wiring-board island in an apparatus according to an embodiment;

Figure 7 is perspective elevation of a computing system according to an embodiment

Figure 8 is a process flow diagram for assembly of a printed wiring-board island according to several embodiments; and

Figure 9 is included to show an example of a higher-level device application for the disclosed embodiments.

DETAILED DESCRIPTION

Increased routing density requirements for a given motherboard is accommodated by locating a printed wiring-board island onto a subsection of a larger motherboard or other printed circuit board.

Routing density of a printed wiring-board island can match that of a printed circuit board, but the need is ameliorated, to engineer and manufacture entire additional layers for the printed circuit board. Routing density of the printed wiring-board island on the die side may be different than that of the printed circuit board, and the printed wiring-board island translates from one routing density to the other between the die side and the board side.

Figure 1 is a cross-section elevation of a printed wiring-board island 20 in an apparatus 100 according to an embodiment. A semiconductive device package 10 includes a semiconductive device 110 that is micro bumped 112 onto a redistribution substrate 114. The semiconductive device 110 is encapsulated in a molding compound 116 according to an embodiment.

A printed circuit board 30 such as a motherboard 30 has a given wiring density that may be determined by a set of design rules and wiring layers (not illustrated), but assembly of the semiconductive device package 10 requires different routing density than what is contained the printed circuit board 30 in an embodiment. In an embodiment, the routing density is the same for the printed wiring-board island 20 and the printed circuit board 30, but the need is ameliorated to fabricate an entire additional layer in the printed circuit board 30. Hereinafter, the printed circuit board 30, or also referred to as the motherboard 30, may be referred to as a printed circuit board (PCB) 30.

In an embodiment, a printed wiring-board island 20 is presented against the PCB 30. The printed wiring-board island 20 electrically couples the semiconductive device package 10 to the PCB 30 through a land-side ball-grid array 118 (one instance enumerated) that mates to a series of ball pads 120 (one instance enumerated). In an embodiment, the package 10 includes an integrated passive device (IPD) that communicates through the land-side ball-grid array 118. In an embodiment, the package 10 includes both a semiconductive device such as the illustrated semiconductive device 110, as well as a IPD (not pictured) that is either side-by-side along the X-direction of the illustrated cross section, or side-by-side with the semiconductive device 110 in the Y-direction, which is either into or out of the plane of the drawing illustrated in Figure 1.

In an embodiment, the printed wiring-board island (PWB island) 20 includes an organic section 122 with a die side 121 and a board side 123. The organic section 122 may be several

layers that accommodate lateral traces and vertical vias. In an embodiment, one or more integrated passive devices (IPDs) (not pictured) are mounted on the die side 121 of the PWB island 20 side-by-side with the package 10 along the X-direction of the illustrated cross section. Within the organic section 122 is found in this embodiment, a one-layer trace redistribution complexity illustrated by a die-coupling via 124 (one instance indicated), a trace level 126 and a board-coupling via 128. In an embodiment, the PWB island 20 illustrated also includes a through-board via 129 that communicates from the die side 121 to the board side 123 of the PWB island 20.

In an embodiment, the PWB island 20 includes the structural function of translating between a die-side routing density to a board-side routing density. For example, the semiconductive device package 10 has a routing density that the PWB island 20 is configured to meet, and the PWB island 20 includes a routing density on the board side 123 that is configured to meet the routing density of the PCB 30. In an embodiment, the die-side routing density is different from the board-side routing density. In an embodiment, the die-side routing density is the same as the board-side routing density, but because the PWB island 20 is used, an entire additional at least one layer is not required to add to the PCB 30.

In any event, the PWB island 20 provides sufficient complexity to mate the semiconductive device package 10 to the PCB 30, without requiring an additional entire new layer or layers, to be designed and added to the PCB 30. Consequently, local complexity of a PWB island embodiment relieves additional design and fabrication burdens required to couple a given semiconductive device package to a given PCB.

As illustrated, the PCB 30 is depicted only as a portion of a complete printed circuit board, and it is illustrated only where the PWB island 20 needs to be located, and not to the entire package-side surface 131 of the PCB 30.

In an embodiment, attachment and electrical communication between the PWB island 20 and the PCB 30 is accomplished by solder-paste printing (SPP) onto the PWB island 20 at locations for board-coupling vias 128 as well as for through-board vias 129. For example, a printed solder paste 130 has been printed onto the PWB island 20 on the board side 123, and the PWB island 20 is thermally bonded to the PCB 30 at PCB bond pads 136 (one instance enumerated). In another example embodiment, the printed solder paste 130 has been printed onto the PCB 30 and the PWB island 20 is thermally bonded to the PCB 30 at the several PCB bond pads 136.

Further attachment mechanisms are used in an embodiment, such as a thermo-coupling, non-conductive paste (TCnCP) 132 that is located at a useful position to complement and

supplement bonding qualities of the printed solder-paste 130. In an embodiment, the TCnCP 132 is identical to the printed solder paste 130, but because it has been placed in a useful location without completing any electrical couplings, it may be referred to as a dummy printed solder paste 132. In an embodiment, the TCnCP 132 is similar in bonding quality to the printed solder paste 130, but it does not exhibit electrical conductivity. In any event, because the TCnCP 132 has been placed in a useful location without any electrically conductive qualities, it may be referred to as a dummy printed solder paste 132.

In an embodiment, the PWB island 20 has a single trace layer 126 (as illustrated) to address accommodating the wiring density of the semiconductive device package 10 to the different- or less-complex wiring of the PCB 30. In an embodiment, the PWB island 20 has a two trace layers. In an embodiment, the PWB island 20 has a three trace layers. In an embodiment, the PWB island 20 has a four trace layers.

As illustrated, the PWB island 20 creates an island form factor upon the PCB 30. One aspect of the PWB island 20 form factor is a die side 121 surface in a difference Z-direction plane than the package-side surface 131 of the PCB 30. Additionally, at least one dimension in the X-Y plane for the PWB island 20 is smaller than that of the PBC 30.

Figure 2 is a cross-section elevation of a printed wiring-board island 20 in an apparatus 200 according to an embodiment. A semiconductive device package 10 includes a semiconductive device 110 that is micro bumped 112 onto a redistribution substrate 114. The semiconductive device 110 is encapsulated in a molding compound 116 according to an embodiment. In an embodiment, the PWB island 20 is the same PWB island 20 depicted in Figure 1, but the cross-section elevation view is taken from a different location orthogonal to the plane of the Figure 1 drawing.

A printed circuit board 30 such as a motherboard 30 has a given set of wiring density that may be determined by useful design rules and wiring layers (not illustrated), but assembly of the semiconductive device package 10 requires more wiring density than is contained the printed wiring board 30. Hereinafter, the printed circuit board 30, or also referred to as the motherboard 30, may be referred to as a printed circuit board (PCB) 30.

In an embodiment, a printed wiring-board island 20 is presented against the PCB 30. The PWB island 20 electrically couples the semiconductive device package 10 to the PCB 30 through a land-side ball-grid array 118 (one instance enumerated) that mates to a series of ball pads 120 (one instance enumerated).

In an embodiment, the PWB island 20 includes an organic section 122 with a die side 121 and a board side 123. The organic section 122 may be several layers that accommodate lateral

traces and vertical vias. Within the organic section 122 is found in this embodiment, a one-layer trace redistribution complexity illustrated by a trace level 126 and a board-coupling via 128. The PWB island 20 also fans out over a section of the PCB 30 to accommodate the routing density of the PCB 30.

In any event, the PWB island 20 provides sufficient complexity to mate the semiconductive device package 10 to the PCB 30, without requiring an additional entire new layer or layers, to be designed and added to the PCB 30. Consequently, local complexity of a PWB island embodiment relieves additional design and fabrication burdens required to couple a given semiconductive device package to a given PCB.

As illustrated, the PCB 30 is depicted only as a portion of a complete printed circuit board, and is illustrated only where the PWB island 20 needs to be located, and not to the entire package-side surface 131 of the PCB 30.

In an embodiment, attachment and electrical communication between the PWB island 20 and the PCB 30 is accomplished by solder-paste printing onto locations for board-coupling vias 128. For example, a printed solder-paste 130 has been printed onto the PWB island 20 on the board side 123, and the PWB island 20 is thermally bonded to the PCB 30. In another example, the printed solder paste 130 has been printed onto the PCB 30 at a PCB bond pad 136 (one instance enumerated) and the PWB island 20 is thermally bonded to the PCB 30.

Further attachment mechanisms are used in an embodiment, such as a TCnCP 132 that is located at a useful position to complement and supplement bonding qualities of the printed solder-paste 130. In an embodiment, the TCnCP 132 is identical to the printed solder paste 130, but because it has been placed in a useful location without completing any electrical couplings, it may be referred to as a dummy printed solder paste 132. In an embodiment, the TCnCP 132 is similar in bonding quality to the printed solder paste 130, but it does not exhibit electrical conductivity. In any event, because the TCnCP 132 has been placed in a useful location without any electrically conductive qualities, it may be referred to as a dummy printed solder paste 132.

In an embodiment, the PWB island 20 has a single trace layer to address accommodating the wiring complexity of the semiconductive device package 10 to the less-complex wiring of the PCB 30. In an embodiment, the PWB island 20 has a two trace layers. In an embodiment, the PWB island 20 has a three trace layers. In an embodiment, the PWB island 20 has a four trace layers.

Figure 3 is a cross-section elevation of a printed wiring-board island 23 in an apparatus 300 according to an embodiment. In some embodiments, applications of a given PWB island 23

is useful to maintain a lower Z-profile by allowing the land-side ball-grid array 318 to penetrate at least partially through the PWB island 23.

A semiconductive device package 10 includes a semiconductive device 110 that is micro bumped 112 onto a redistribution substrate 114. The semiconductive device 110 is encapsulated in a molding compound 116 according to an embodiment.

A printed circuit board 30 such as a motherboard 30 has a given wiring density that may be determined by a set of design rules and wiring layers (not illustrated), but assembly of the semiconductive device package 10 requires more wiring density than contained in the printed circuit board 30. Hereinafter, the printed circuit board 30, or also referred to as the motherboard 30, may be referred to as a printed circuit board (PCB) 30.

In an embodiment, the printed wiring-board island 23 is presented against the PCB 30. The PWB island 23 electrically couples the semiconductive device package 10 to the PCB 30 through the penetrating ball-grid array 318 (one instance enumerated) that mates to the redistribution substrate 114, passes at least partially through the PWB island 23, and bonds to the PCB bond pads 136.

In an embodiment, the PWB island 23 includes an organic section 122 with a die side 121 and a board side 123. The organic section 122 may be several layers that accommodate lateral traces and vertical vias. Within the organic section 122 is found in this embodiment, a one-layer trace redistribution complexity illustrated by a trace level 326 and a board-coupling via 128.

In any event, the PWB island 23 provides sufficient complexity to mate the semiconductive device package 10 to the PCB 30, without requiring additional new layer or layers, to be designed and added to the PCB 30. Consequently, local complexity of a PWB island embodiment relieves additional design and fabrication burdens required to couple a given semiconductive device package to a given PCB.

In the illustrated embodiment, the several penetrating balls of the penetrating ball-grid array 318 are connected to a bus trace 326, and the bus trace 326 also has an X-direction fan-out feature.

As illustrated, the PCB 30 is depicted only as a portion of a complete printed circuit board, and it is illustrated only where the PWB island 23 needs to be located, and not to the entire package-side surface 131 of the PCB 30.

In an embodiment, attachment and electrical communication between the PWB island 23 and the PCB 30 is accomplished by solder-paste printing onto locations for board-coupling vias 128. For example, a printed solder-paste 130 has been printed onto the PWB island 23 and the PWB island 23 is thermally bonded to the PCB 30. In another example, the printed solder paste

130 has been printed onto the PCB 30 and the PWB island 23 is thermally bonded to the PCB 30.

Further attachment mechanisms are used in an embodiment, such as printed solder paste 134 that mates the several PCB bond pads 136 to the penetrating ball-grid array 318. In an embodiment, only the printed solder paste 130 is used as the printed solder paste 134 is not necessary where the penetrating ball-grid array 318 reflows through the PWB island 23 and bonds onto the PCB bond pads 136.

In an embodiment, the PWB island 23 has a single trace layer (as illustrated) to address accommodating the wiring complexity of the semiconductive device package 10 to the less-complex wiring of the PCB 30. In an embodiment, the PWB island 23 has two trace layers. In an embodiment, the PWB island 23 has a three trace layers. In an embodiment, the PWB island 23 has a four trace layers.

In an embodiment although the several penetrating balls 318 may mate onto the PCB 30 and the package side 131, a given penetrating ball 319 mates onto a dummy bond pad 137 and the connection is solely structural and not electrical.

Figure 4 illustrates a top plan cut away (X-Y) and a cross-section elevation (X-Z) of a portion of a printed wiring-board island 24 according to an embodiment.

In the top plan cut away X-Y, a trace 426 that is part of the PWB island 24, similar to the PWB island 23 depicted in Figure 3, has been laid bare within the organic section 422. The top plan cut away X-Y is taken from the section line Y – Y from the cross-section elevation XZ.

A meshed bump pad 427 is embedded within the organic section 422, and the meshed bump pad 427 is part of the trace 426, and the meshed bump pad 427 allows for a penetrating solder such as the penetrating balls 318 such as depicted in Figure 3, to partially pass through the meshed bump pad 427 and bond with the PCB bond pad 136, also depicted in Figure 3.

In the cross-section elevation X-Z, this embodiment illustrates the meshed bump pad 427 as it is exposed with a bump corridor 430 that opens the die side 421 of the PWB island 24 within the organic section 422 of the PWB island 24. Additionally in this embodiment, a second trace level 428 is depicted above the first trace 426, such that the organic section 422 has two trace layers.

Figure 5 illustrates a top plan cut away (X-Y) and a cross-section elevation (X-Z) of a portion of a printed wiring-board island 25 according to an embodiment.

In the top plan cut away X-Y, a trace 526 that is part of the PWB island 25, similar to the PWB island 23 depicted in Figure 3, has been laid bare within the organic section 522. The top plan cut away X-Y is taken from the section line Y – Y from the cross-section elevation X-Z.

A bump pad 527 is part of the trace 526, and the bump pad 527 is complemented by a solder-paste printed bump 534 (see the cross-section elevation X-Z), that allows for a continuing electrical connection for the solder balls such as the solder balls 318 depicted in part in Figure 3, to pass through the PWB island 25 and electrically connect with the bond pad 527. Accordingly, the solder-paste printed bump 534, the bond pad 527 and the solder ball (see item 318 in Figure 3) complete a connection through the PWB island 25. As illustrated, the solder-paste printed bump 534 is in contact with the bump pad 527 at a board side 523 of the PWB island 25.

In the cross-section elevation X-Z, this embodiment illustrates the bump pad 527 as it is exposed with a bump corridor 530. The bump corridor 530 opens the die side 521 of the PWB island 25 within the organic section 522 of the PWB island 25.

The bump corridor 530 can also open the board side 523 of the PWB island 25. Additionally in this embodiment, a second trace level 528 is depicted above the first trace 526. Additionally in this embodiment, a third trace level 532 is depicted above the second trace level 528, such that the organic section 522 has three trace layers.

Figure 6 is a cross-section elevation of a portion of a printed wiring-board island 26 in an apparatus 600 according to an embodiment. A trace 626 is part of the PWB island 26, similar to the PWB island 23 depicted in Figure 3. The trace 626 is found within the organic section 622. A bump pad 627 is part of the trace 626, and the bump pad 627 is complemented by a solder-paste printed bump 634 that allows for a continuing electrical connection for the solder ball 618, to partially pass through the PWB island 26 and electrically connect with the bump pad 627. Accordingly, the solder-paste printed bump 634, the bump pad 627 and a penetrating solder ball 618 complete a connection through the PWB island 26.

Additionally in this embodiment, a second trace level 628 is depicted above the first trace 626. Additionally in this embodiment, a third trace level 632 is depicted above the second trace level 628. Additionally in this embodiment, a fourth trace level 638 is depicted above the third trace level 632, such that the organic section 622 has four trace layers.

It may now be understood that each embodiment illustrated in Figure 1 may include up to four trace levels as illustrated in Figure 6. It may now be understood that each embodiment illustrated in Figure 2 may include up to four trace levels as illustrated in Figure 6. It may now be understood that each embodiment illustrated in Figure 3 may include up to four trace levels as illustrated in Figure 6. It may now be understood that each embodiment illustrated in Figure 4 may include up to four trace levels as illustrated in Figure 6. It may now be understood that each embodiment illustrated in Figure 5 may include up to four trace levels as illustrated in Figure 6.

Figure 7 is perspective elevation of a computing system 700 according to an embodiment. A printed circuit board 30 carries several active devices and components (not pictured), and the PCB 30 is configured with a printed wiring-board island 20 similar to the PWB island 20 depicted in Figure 1 for example. The PCB 30 includes an entire upper surface that is a package-side surface 731.

The semiconductive device 110 is affixed in a molding compound 116, and the semiconductive device 110 is depicted in ghosted lines within the molding compound 116. In an embodiment, the semiconductive device 110 is mated to a PWB island 20 such as the PWB island 23 depicted in Figure 3.

As illustrated, the PWB island 20 creates an island form factor upon the PCB 30. One aspect of the PWB island 20 form factor is a die side 121 surface in a difference Z-direction plane than the package-side surface 731 of the PCB 30. Additionally, at least one dimension in the X-Y plane for the PWB island 20 is smaller than that of the PBC 30. In other words, the island form factor includes at least one edge of the PWB island 20, within the X-Y plane, not sharing an edge with the PCB 30 in an X-Z plane, nor in a Y-Z plane. As illustrated, no edge of the PWB island 20 shares an edge, neither in the X-Z plane nor the Y-Z plane with any edge of the PCB 30.

In several embodiments, selected ball sizes are used for a given useful application. Table 1 depicts selected ball sizes for application to through-PWB island embodiments.

Table – 1 Package Standoff during PWB Island Assembly

Ball size, *e.g.* item 118	Z-height after Ball apply	Z-height after PCB assembly
300 µm	210 µm	180 µm
250 µm	190 µm	150 µm
230 µm	170 µm	130 µm
220 µm	160 µm	120 µm
200 µm	140 µm	100 µm
180 µm	110 µm	80 µm

In an embodiment, a system in a package includes a PWB island 27 and several devices embedded in a package 70 that includes a molding compound 716. A core processor 710 (depicted in ghosted lines) is paired with a baseband processor 710''. A memory module 710''' is also affixed in the molding compound 716, and a combination memory-controller hub and platform-controller hub 710'''' is mated with the other devices. The several devices 710, 710'',

710''' and 710'''' communicate through the PWB island 27 to the PCB 30. As illustrated, the PWB island 27 creates an island form factor upon the PCB 30.

In an embodiment, at least one semiconductor device package is mounted on the PWB island 27. In an embodiment, several devices are assembled, side-by-side on the PWB island 27. For example, item 710 is a processor package, item 710'' is a baseband processor package including a baseband processor and an IPD, item 710''' is a memory-controller hub package, and item 710'''' is a platform-controller hub package. In an embodiment, any subset of the aforementioned packages is mounted on the PWB island 27, and the molding compound 716, if present, covers the several packages.

As illustrated, the PWB island 27 creates an island form factor upon the PCB 30. One aspect of the PWB island 27 form factor is a die side 721 surface in a difference Z-direction plane than the package-side surface 731 of the PCB 30. Additionally, at least one dimension in the X-Y plane for the PWB island 20 is smaller than that of the PBC 30. In other words, the island form factor includes at least one edge of the PWB island 27, within the X-Y plane, not sharing an edge with the PCB 30 in an X-Z plane, nor in a Y-Z plane. As illustrated, no edge of the PWB island 27 shares an edge, neither in the X-Z plane nor the Y-Z plane with any edge of the PCB 30.

Figure 8 is a process flow diagram 800 for assembly of a printed wiring-board island according to several embodiments.

At 810, the process includes solder-paste printing onto a printed circuit board.

At 820, the process alternatively includes solder-paste printing onto the printed wiring-board island.

At 830, the process alternatively includes printing a TCnCP onto one of the PCB and the PWB island for the utility of uniform adhesion and package-to-board leveling.

At 840, the process includes assembling the printed wiring-board island to the printed circuit board. The assembly process may include thermal reflow of the ball-grid array. In an embodiment, processing begins at 840.

At 842, the process alternatively includes assembling the ball-grid array by at least partially penetrating the PWB island.

At 850, the process includes assembling the PWB island-containing semiconductive device package to a computing system.

Figure 9 is included to show an example of a higher-level device application for the disclosed embodiments. The printed wiring-board island embodiments may be found in several parts of a computing system. In an embodiment, a printed wiring-board island computing

system 900 includes, but is not limited to, a desktop computer. In an embodiment, a printed wiring-board island system 900 includes, but is not limited to a laptop computer. In an embodiment, a printed wiring-board island system 900 includes, but is not limited to a netbook. In an embodiment, a printed wiring-board island system 900 includes, but is not limited to a tablet. In an embodiment, a printed wiring-board island system 900 includes, but is not limited to a notebook computer. In an embodiment, a printed wiring-board island system 900 includes, but is not limited to a personal digital assistant (PDA). In an embodiment, a printed wiring-board island system 900 includes, but is not limited to a server. In an embodiment, a printed wiring-board island computing system 900 includes, but is not limited to a workstation. In an embodiment, a printed wiring-board island system 900 includes, but is not limited to a cellular telephone. In an embodiment, a printed wiring-board island system 900 includes, but is not limited to a mobile computing device. In an embodiment, a printed wiring-board island system 900 includes, but is not limited to a smart phone. In an embodiment, a printed wiring-board island system 900 includes, but is not limited to an internet appliance. In an embodiment, the printed wiring-board island computing system is part of a wearable computing system. In an embodiment, the printed wiring-board island computing system is part of a drone. Other types of computing device may be configured with the printed wiring-board island computing system that includes non-planar interconnect embodiments.

In an embodiment, the processor 910 has one or more processing cores 912 and 912N, where 912N represents the Nth processor core inside processor 910 where N is a positive integer. In an embodiment, the electronic device system 900 using a printed wiring-board island computing system embodiment that includes multiple processors including 910 and 905, where the processor 905 has logic similar or identical to the logic of the processor 910. In an embodiment, the processing core 912 includes, but is not limited to, pre-fetch logic to fetch instructions, decode logic to decode the instructions, execution logic to execute instructions and the like. In an embodiment, the processor 910 has a cache memory 916 to cache at least one of instructions and data for the printed wiring-board island in the system 900. The cache memory 916 may be organized into a hierarchal structure including one or more levels of cache memory.

In an embodiment, the processor 910 includes a memory controller 914, which is operable to perform functions that enable the processor 910 to access and communicate with memory 930 that includes at least one of a volatile memory 932 and a non-volatile memory 934. In an embodiment, the processor 910 is coupled with memory 930 and chipset 920. The processor 910 may also be coupled to a wireless antenna 978 to communicate with any device configured to at least one of transmit and receive wireless signals. In an embodiment, the

wireless antenna interface 978 operates in accordance with, but is not limited to, the IEEE 802.11 standard and its related family, Home Plug AV (HPAV), Ultra Wide Band (UWB), Bluetooth, WiMax, or any form of wireless communication protocol.

In an embodiment, the volatile memory 932 includes, but is not limited to, Synchronous Dynamic Random Access Memory (SDRAM), Dynamic Random Access Memory (DRAM), RAMBUS Dynamic Random Access Memory (RDRAM), and/or any other type of random access memory device. The non-volatile memory 934 includes, but is not limited to, flash memory, phase change memory (PCM), read-only memory (ROM), electrically erasable programmable read-only memory (EEPROM), or any other type of non-volatile memory device.

The memory 930 stores information and instructions to be executed by the processor 910. In an embodiment, the memory 930 may also store temporary variables or other intermediate information while the processor 910 is executing instructions. In the illustrated embodiment, the chipset 920 connects with processor 910 via Point-to-Point (PtP or P-P) interfaces 917 and 922. Either of these PtP embodiments may be achieved using a printed wiring-board island computing system embodiment as set forth in this disclosure. The chipset 920 enables the processor 910 to connect to other elements in the printed wiring-board island embodiments in a system 900. In an embodiment, interfaces 917 and 922 operate in accordance with a PtP communication protocol such as the Intel® QuickPath Interconnect (QPI) or the like. In other embodiments, a different interconnect may be used.

In an embodiment, the chipset 920 is operable to communicate with the processor 910, 905N, the display device 940, and other devices 972, 976, 974, 960, 962, 964, 966, 977, etc. The chipset 920 may also be coupled to a wireless antenna 978 to communicate with any device configured to at least do one of transmit and receive wireless signals.

The chipset 920 connects to the display device 940 via the interface 926. The display 940 may be, for example, a liquid crystal display (LCD), a plasma display, cathode ray tube (CRT) display, or any other form of visual display device. In and embodiment, the processor 910 and the chipset 920 are merged into a printed wiring-board island apparatus in a system. Additionally, the chipset 920 connects to one or more buses 950 and 955 that interconnect various elements 974, 960, 962, 964, and 966. Buses 950 and 955 may be interconnected together via a bus bridge 972 such as at least one printed wiring-board island embodiment. In an embodiment, the chipset 920 couples with a non-volatile memory 960, a mass storage device(s) 962, a keyboard/mouse 964, and a network interface 966 by way of at least one of the interface 924 and 974, the smart TV 976, and the consumer electronics 977, *etc.*

In and embodiment, the mass storage device 962 includes, but is not limited to, a solid state drive, a hard disk drive, a universal serial bus flash memory drive, or any other form of computer data storage medium. In one embodiment, network interface 966 is implemented by any type of well-known network interface standard including, but not limited to, an Ethernet interface, a universal serial bus (USB) interface, a Peripheral Component Interconnect (PCI) Express interface, a wireless interface and/or any other suitable type of interface. In one embodiment, the wireless interface operates in accordance with, but is not limited to, the IEEE 802.11 standard and its related family, Home Plug AV (HPAV), Ultra Wide Band (UWB), Bluetooth, WiMax, or any form of wireless communication protocol.

While the modules shown in Figure 9 are depicted as separate blocks within the printed wiring-board island embodiment in a computing system 900, the functions performed by some of these blocks may be integrated within a single semiconductor circuit or may be implemented using two or more separate integrated circuits. For example, although cache memory 916 is depicted as a separate block within processor 910, cache memory 916 (or selected aspects of 916) can be incorporated into the processor core 912.

Where useful, the computing system 900 may have an outer shell. Referring to Figures 1, 2 and 3, the PCB 30 includes a shell structure 111 that provides both physical and electrical protection for the PWB island-containing semiconductive package 10.

To illustrate the printed wiring-board island embodiments and assembly methods disclosed herein, a non-limiting list of examples is provided herein:

Example 1 is a semiconductive device substrate, comprising: a printed wiring-board island including a die side and a board side, wherein the a semiconductive-package includes a routing density on the die-side and a printed circuit board routing density on the board-side; a printed circuit board onto which the printed wiring-board island is mounted, wherein the printed circuit board includes the printed circuit board routing density, wherein the printed wiring-board island board-side routing density matches the printed circuit board routing density, and wherein the printed wiring-board island creates an island form factor on the printed circuit board.

In Example 2, the subject matter of Example 1 optionally includes a reflowed solder-paste printed on one of the printed wiring-board island and the printed circuit board, wherein the reflowed solder paste bonds the printed wiring-board island to the printed circuit board.

In Example 3, the subject matter of any one or more of Examples 1–2 optionally include a reflowed solder-paste printed on one of the printed wiring-board island and the printed circuit board, wherein the reflowed solder paste bonds the printed wiring-board island to the printed

circuit board; and a thermo-coupling, non-conductive paste also bonding the printed wiring-board island and the printed circuit board.

In Example 4, the subject matter of any one or more of Examples 1–3 optionally include a semiconductive device package disposed on the printed wiring-board island and coupled to the printed wiring-board island on the die-side by a ball-grid array, wherein the ball-grid array reflects the semiconductive-package routing density.

In Example 5, the subject matter of any one or more of Examples 1–4 optionally include wherein the printed wiring-board island includes trace-layer structure selected from the group consisting of a single trace layer, two trace layers, three trace layers and four trace layers.

In Example 6, the subject matter of any one or more of Examples 1–5 optionally include at least one semiconductive device package disposed on the printed wiring-board island and coupled to the printed wiring-board island and to the printed circuit board by a ball-grid array, wherein the ball-grid array at least partially penetrates the printed wiring-board island, and wherein the ball-grid array partially reflects the semiconductive-package routing density.

In Example 7, the subject matter of Example 6 optionally includes a bump pad embedded within the printed wiring-board island at a trace level, wherein a ball from the ball-grid array contacts the bump pad.

In Example 8, the subject matter of Example 7 optionally includes a bump pad embedded within the printed wiring-board island at a trace level, wherein a ball from the ball-grid array contacts and passes through a mesh structure of the bump pad.

In Example 9, the subject matter of any one or more of Examples 6–8 optionally include wherein the printed wiring-board island includes trace-layer structure selected from the group consisting of a single trace layer, two trace layers, three trace layers and four trace layers.

In Example 10, the subject matter of any one or more of Examples 7–9 optionally include a solder-paste printed bump in contact with the bump pad at a board side of the printed wiring-board island.

In Example 11, the subject matter of any one or more of Examples 6–10 optionally include a bump pad embedded within the printed wiring-board island at a trace level, wherein the bump pad has a mesh form factor.

In Example 12, the subject matter of any one or more of Examples 1–11 optionally include a semiconductive device package disposed on the printed wiring-board island and coupled to the printed wiring-board island on the die-side by a ball-grid array, wherein the ball-grid array reflects the semiconductive-package routing density, wherein the semiconductive

device package includes a core processor, a baseband processor, a memory module and at least one of a memory-controller hub and a platform-controller hub.

In Example 13, the subject matter of Example 12 optionally includes a bump pad embedded within the printed wiring-board island at a trace level, wherein a ball from the ball-grid array contacts the bump pad.

In Example 14, the subject matter of any one or more of Examples 12–13 optionally include a bump pad embedded within the printed wiring-board island at a trace level, wherein a ball from the ball-grid array contacts and passes through a mesh structure of the bump pad.

In Example 15, the subject matter of any one or more of Examples 13–14 optionally include a reflowed solder-paste printed on one of the printed wiring-board island and the printed circuit board, wherein the reflowed solder paste bonds the printed wiring-board island to the printed circuit board; and a thermo-coupling, non-conductive paste also bonding the printed wiring-board island and the printed circuit board.

Example 16 is a method of assembling a semiconductive device substrate, comprising: assembling a printed wiring-board island to a printed circuit board, wherein the printed wiring board includes a die-side routing density and a board-side routing density; and assembling a semiconductive device package to the printed wiring-board island on the die side.

In Example 17, the subject matter of Example 16 optionally includes solder-paste printing onto the printed circuit board before assembling the printed wiring-board island to the printed circuit board.

In Example 18, the subject matter of Example 17 optionally includes printing a thermo-coupling non-conductive paste onto one of the printed wiring-board island and the printed circuit board.

In Example 19, the subject matter of any one or more of Examples 16–18 optionally include solder-paste printing onto the printed wiring-board island before assembling the printed wiring-board island to the printed circuit board.

In Example 20, the subject matter of Example 19 optionally includes printing a thermo-coupling non-conductive paste onto one of the printed wiring-board island and the printed circuit board.

Example 21 is a computing system, comprising: a printed wiring-board island including a semiconductive-package routing density on a die-side thereof and a printed circuit board routing density on a board-side thereof; a printed circuit board onto which the printed wiring-board is mounted, wherein the printed circuit board includes the printed circuit board routing density, and wherein the printed wiring-board island creates an island form factor on the printed circuit board;

a semiconductive device package disposed on the printed wiring-board island and coupled to the printed wiring-board island by a ball-grid array, wherein the ball-grid array reflects the semiconductive-package routing density; and an outer shell covering the semiconductive device package, the printed wiring-board island and the printed circuit board.

In Example 22, the subject matter of Example 21 optionally includes wherein the ball-grid array least partially penetrates the printed wiring-board island, and wherein the ball-grid array partially reflects the semiconductive-package routing density.

The above detailed description includes references to the accompanying drawings, which form a part of the detailed description. The drawings show, by way of illustration, specific embodiments in which the invention can be practiced. These embodiments are also referred to herein as "examples." Such examples can include elements in addition to those shown or described. However, the present inventors also contemplate examples in which only those elements shown or described are provided. Moreover, the present inventors also contemplate examples using any combination or permutation of those elements shown or described (or one or more aspects thereof), either with respect to a particular example (or one or more aspects thereof), or with respect to other examples (or one or more aspects thereof) shown or described herein.

In the event of inconsistent usages between this document and any documents so incorporated by reference, the usage in this document controls.

In this document, the terms "a" or "an" are used, as is common in patent documents, to include one or more than one, independent of any other instances or usages of "at least one" or "one or more." In this document, the term "or" is used to refer to a nonexclusive or, such that "A or B" includes "A but not B," "B but not A," and "A and B," unless otherwise indicated. In this document, the terms "including" and "in which" are used as the plain-English equivalents of the respective terms "comprising" and "wherein." Also, in the following claims, the terms "including" and "comprising" are open-ended, that is, a system, device, article, composition, formulation, or process that includes elements in addition to those listed after such a term in a claim are still deemed to fall within the scope of that claim. Moreover, in the following claims, the terms "first," "second," and "third," etc. are used merely as labels, and are not intended to impose numerical requirements on their objects.

Method examples described herein can be machine or computer-implemented at least in part. Some examples can include a computer-readable medium or machine-readable medium encoded with instructions operable to configure an electrical device to perform methods as described in the above examples. An implementation of such methods can include code, such as

microcode, assembly language code, a higher-level language code, or the like. Such code can include computer readable instructions for performing various methods. The code may form portions of computer program products. Further, in an example, the code can be tangibly stored on one or more volatile, non-transitory, or non-volatile tangible computer-readable media, such as during execution or at other times. Examples of these tangible computer-readable media can include, but are not limited to, hard disks, removable magnetic disks, removable optical disks (e.g., compact disks and digital video disks), magnetic cassettes, memory cards or sticks, random access memories (RAMs), read only memories (ROMs), and the like.

The above description is intended to be illustrative, and not restrictive. For example, the above-described examples (or one or more aspects thereof) may be used in combination with each other. Other embodiments can be used, such as by one of ordinary skill in the art upon reviewing the above description. The Abstract is provided to comply with 37 C.F.R. §1.72(b), to allow the reader to quickly ascertain the nature of the technical disclosure. It is submitted with the understanding that it will not be used to interpret or limit the scope or meaning of the claims. Also, in the above Detailed Description, various features may be grouped together to streamline the disclosure. This should not be interpreted as intending that an unclaimed disclosed feature is essential to any claim. Rather, inventive subject matter may lie in less than all features of a particular disclosed embodiment. Thus, the following claims are hereby incorporated into the Detailed Description as examples or embodiments, with each claim standing on its own as a separate embodiment, and it is contemplated that such embodiments can be combined with each other in various combinations or permutations. The scope of the disclosed embodiments should be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.

CLAIMS

1. A semiconductive device substrate, comprising:

a printed wiring-board island including a die side and a board side, wherein printed wiring-board island includes a die-side routing density on the die-side and a board-side routing density on the board-side;

a printed circuit board onto which the printed wiring-board island is mounted, wherein the printed circuit board includes a printed circuit board routing density, wherein the printed wiring-board island board-side routing density matches the printed circuit board routing density, and wherein the printed wiring-board island creates an island form factor on the printed circuit board.

2. The semiconductive device substrate of claim 1, further including a reflowed solder-paste printed on one of the printed wiring-board island and the printed circuit board, wherein the reflowed solder paste bonds the printed wiring-board island to the printed circuit board.

3. The semiconductive device substrate of claim 1, further including:

a reflowed solder-paste printed on one of the printed wiring-board island and the printed circuit board, wherein the reflowed solder paste bonds the printed wiring-board island to the printed circuit board; and

a thermo-coupling, non-conductive paste also bonding the printed wiring-board island and the printed circuit board.

4.The semiconductive device substrate of claim 1, further including a semiconductive device package disposed on the printed wiring-board island and coupled to the printed wiring-board island on the die-side by a ball-grid array, wherein the ball-grid array reflects the semiconductive-package routing density.

5.The semiconductive device substrate of claim 1, wherein the printed wiring-board island includes trace-layer structure selected from the group consisting of a single trace layer, two trace layers, three trace layers and four trace layers.

6.The semiconductive device substrate of claim 1, further including at least one semiconductive device package disposed on the printed wiring-board island and coupled to the printed

wiring-board island and to the printed circuit board by a ball-grid array, wherein the ball-grid array at least partially penetrates the printed wiring-board island, and wherein the ball-grid array partially reflects the semiconductive-package routing density.

7. The semiconductive device substrate of claim 6, further including a bump pad embedded within the printed wiring-board island at a trace level, wherein a ball from the ball-grid array contacts the bump pad.

8. The semiconductive device substrate of claim 7, further including a bump pad embedded within the printed wiring-board island at a trace level, wherein a ball from the ball-grid array contacts and passes through a mesh structure of the bump pad.

9. The semiconductive device substrate of claim 6, wherein the printed wiring-board island includes trace-layer structure selected from the group consisting of a single trace layer, two trace layers, three trace layers and four trace layers.

10. The semiconductive device substrate of claim 7, further including a solder-paste printed bump in contact with the bump pad at a board side of the printed wiring-board island.

11. The semiconductive device substrate of claim 6, further including a bump pad embedded within the printed wiring-board island at a trace level, wherein the bump pad has a mesh form factor.

12. The semiconductive device substrate of claim 1, further including a semiconductive device package disposed on the printed wiring-board island and coupled to the printed wiring-board island on the die-side by a ball-grid array, wherein the ball-grid array reflects the semiconductive-package routing density, wherein the semiconductive device package includes a core processor, a baseband processor, a memory module and at least one of a memory-controller hub and a platform-controller hub.

13. The semiconductive device substrate of claim 12, further including a bump pad embedded within the printed wiring-board island at a trace level, wherein a ball from the ball-grid array contacts the bump pad.

14. The semiconductive device substrate of claim 12, further including a bump pad embedded within the printed wiring-board island at a trace level, wherein a ball from the ball-grid array contacts and passes through a mesh structure of the bump pad.

15. The semiconductive device substrate of claim 13, further including:

a reflowed solder-paste printed on one of the printed wiring-board island and the printed circuit board, wherein the reflowed solder paste bonds the printed wiring-board island to the printed circuit board; and

a thermo-coupling, non-conductive paste also bonding the printed wiring-board island and the printed circuit board.

16. A method of assembling a semiconductive device substrate, comprising:

assembling a printed wiring-board island to a printed circuit board, wherein the printed wiring board includes a die-side routing density and a board-side routing density, wherein the die-side routing density is different than the board-side routing density; and

assembling a semiconductive device package to the printed wiring-board island on the die side.

17. The method of claim 16, further including solder-paste printing onto the printed circuit board before assembling the printed wiring-board island to the printed circuit board.

18. The method of claim 17, further including printing a thermo-coupling non-conductive paste onto one of the printed wiring-board island and the printed circuit board.

19. The method of claim 16, further including solder-paste printing onto the printed wiring-board island before assembling the printed wiring-board island to the printed circuit board.

20. The method of claim 19, further including printing a thermo-coupling non-conductive paste onto one of the printed wiring-board island and the printed circuit board.

21. A computing system, comprising:

a printed wiring-board island including a semiconductive-package routing density on a die-side thereof and a printed circuit board routing density on a board-side thereof;

a printed circuit board onto which the printed wiring-board is mounted, wherein the printed circuit board includes the printed circuit board routing density, and wherein the printed wiring-board island creates an island form factor on the printed circuit board;

a semiconductive device package disposed on the printed wiring-board island and coupled to the printed wiring-board island by a ball-grid array, wherein the ball-grid array reflects the semiconductive-package routing density; and

an outer shell covering the semiconductive device package, the printed wiring-board island and the printed circuit board.

22.The computing system of claim 21, wherein the ball-grid array least partially penetrates the printed wiring-board island, and wherein the ball-grid array partially reflects the semiconductive-package routing density.

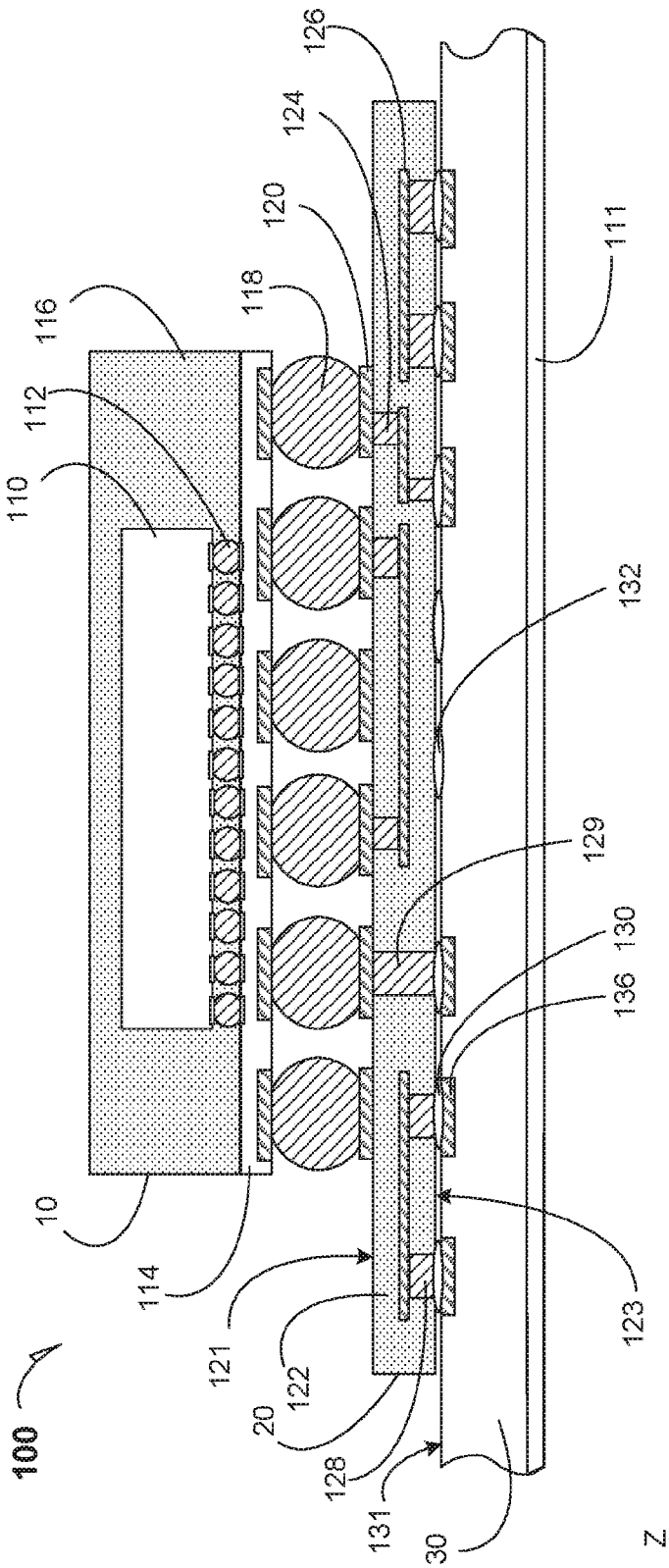

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Fig. 1

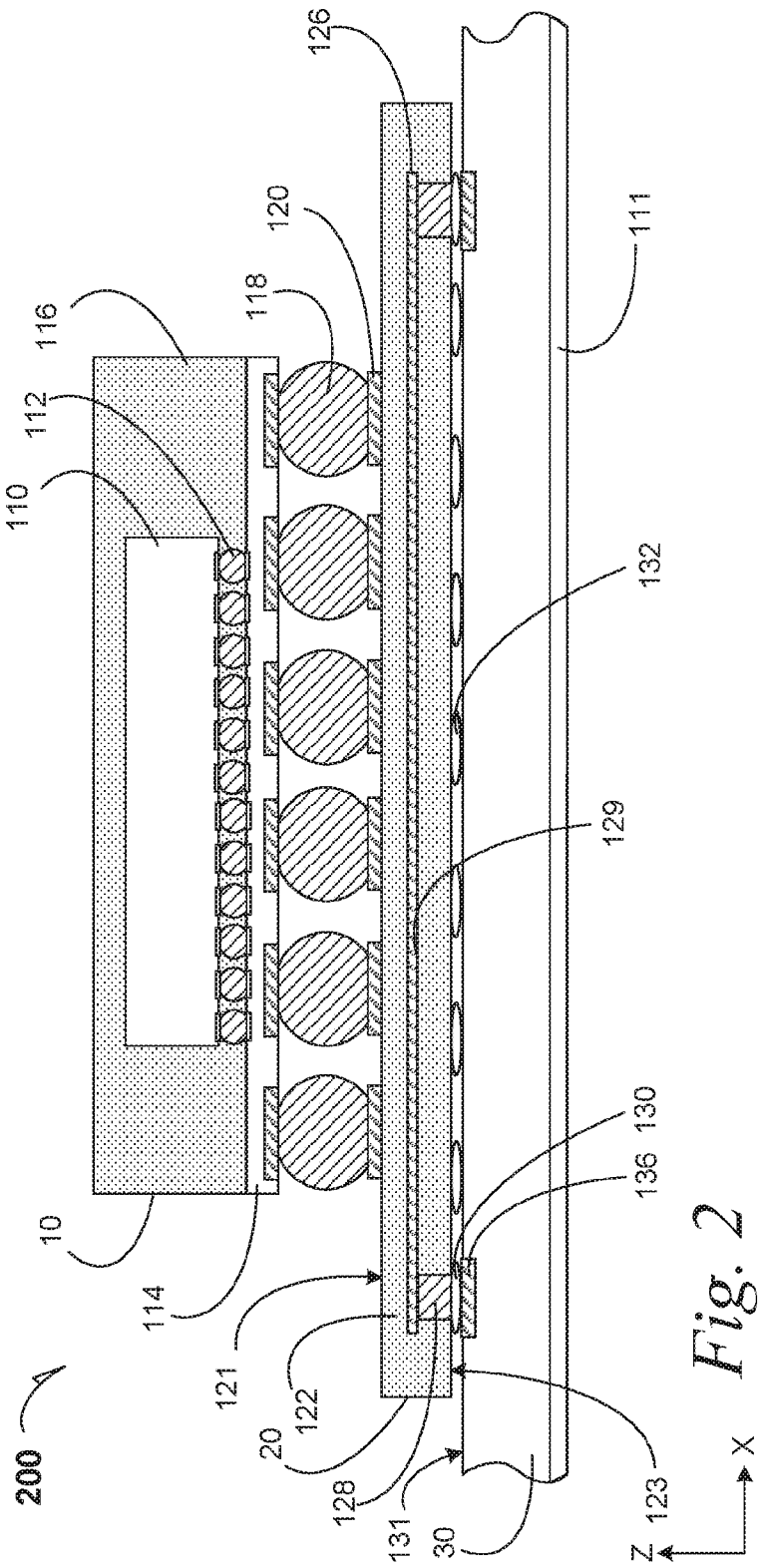

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Fig. 2

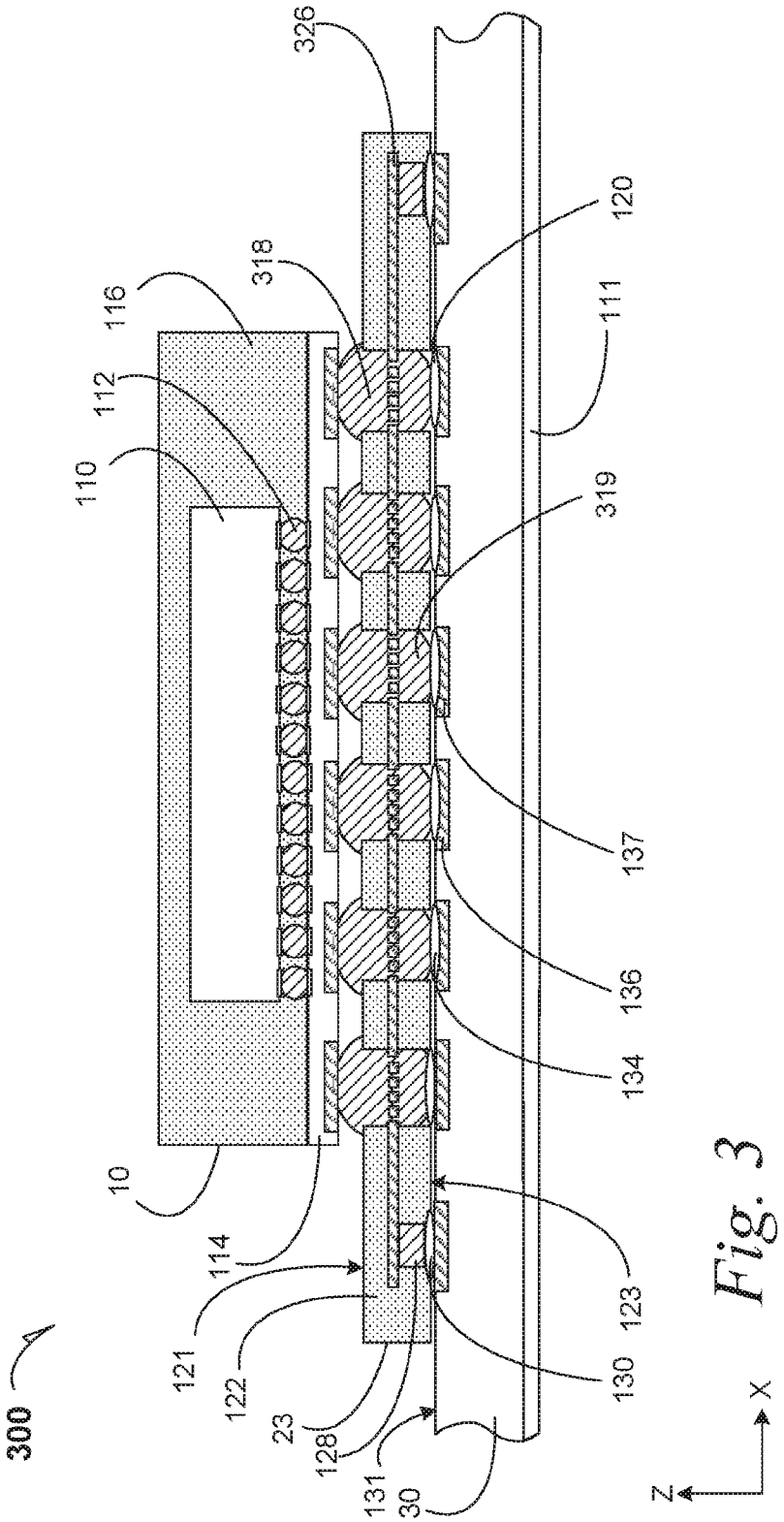

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Fig. 3

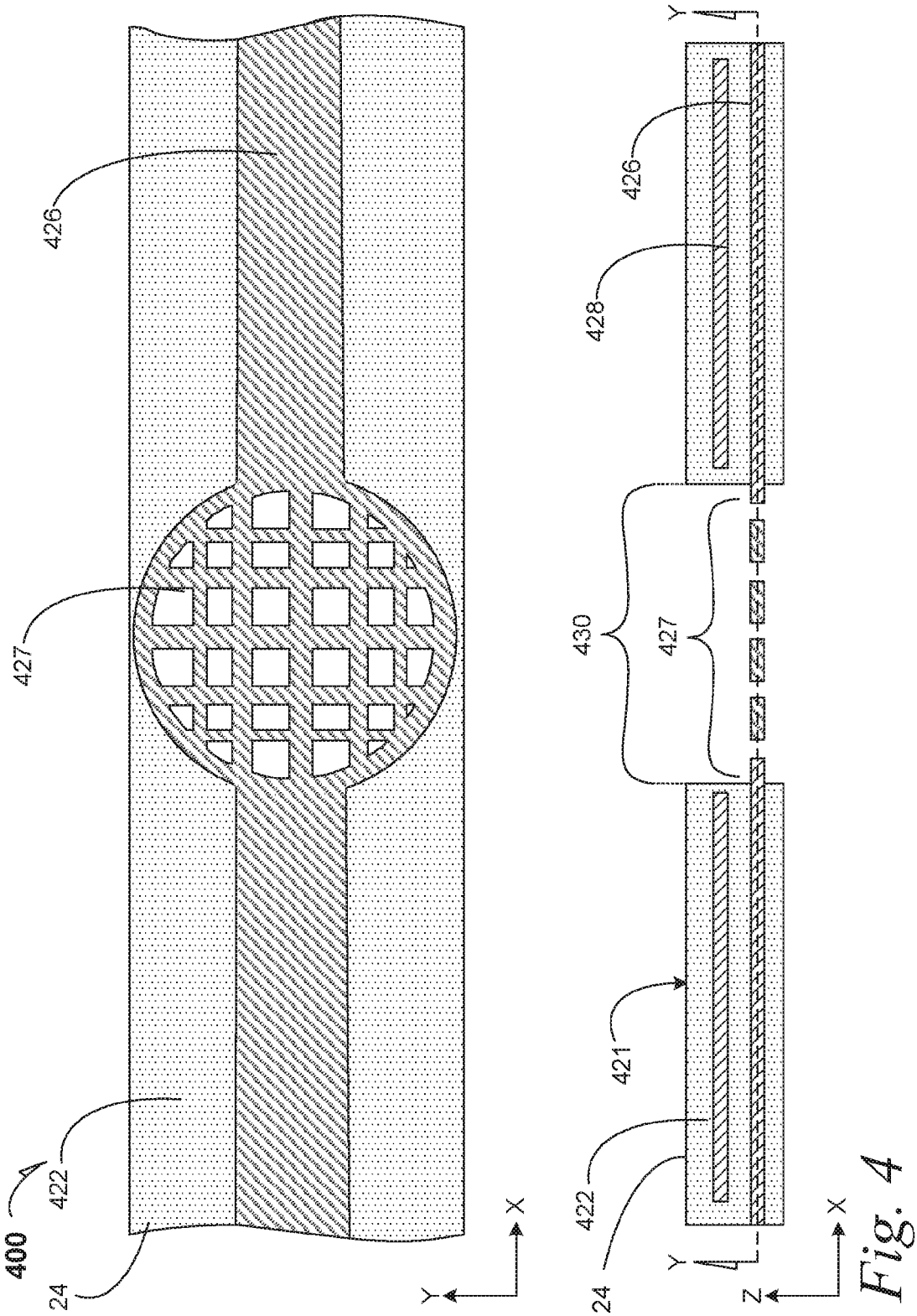


Fig. 4

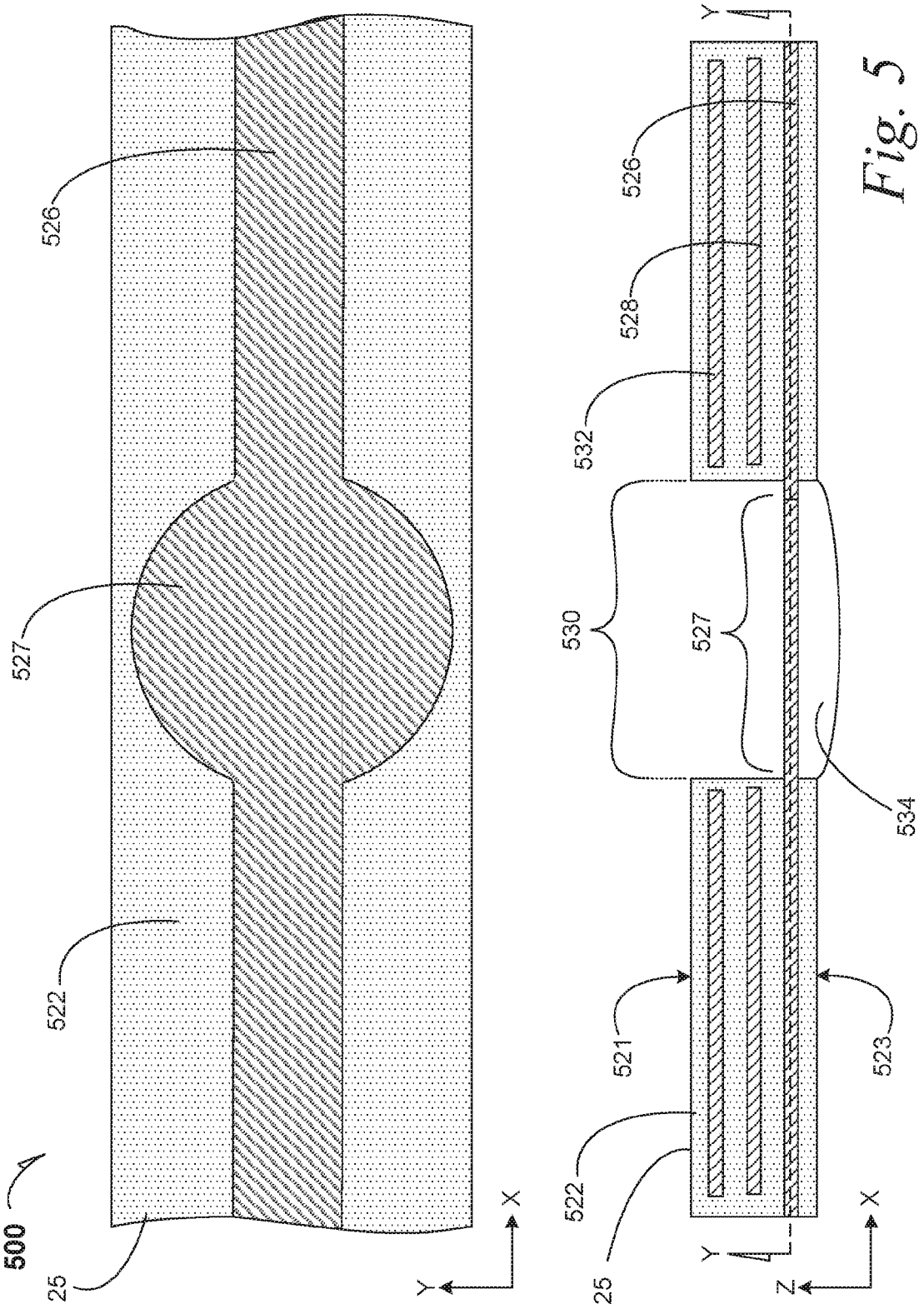


Fig. 5

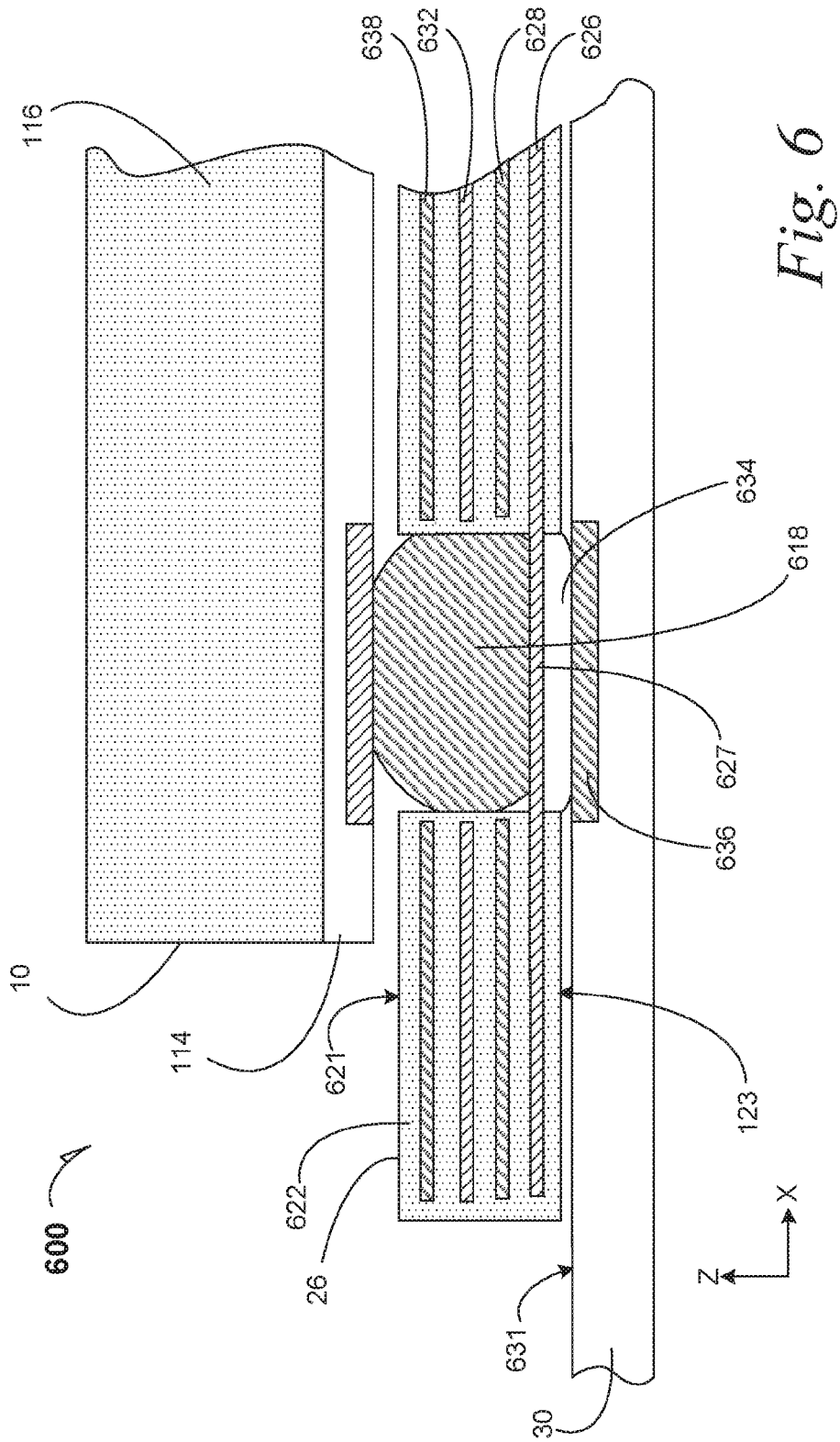

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Fig. 6

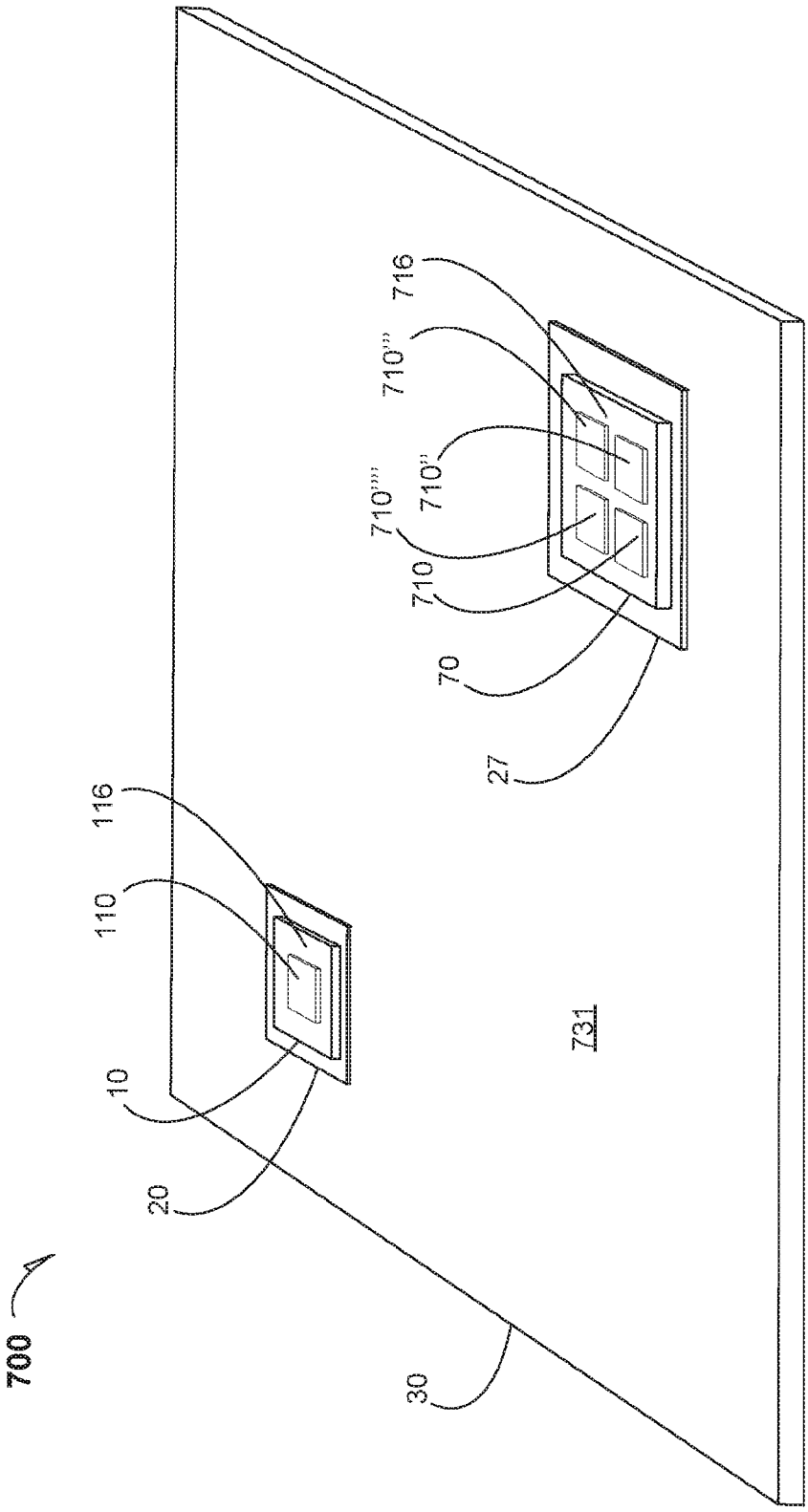


Fig. 7

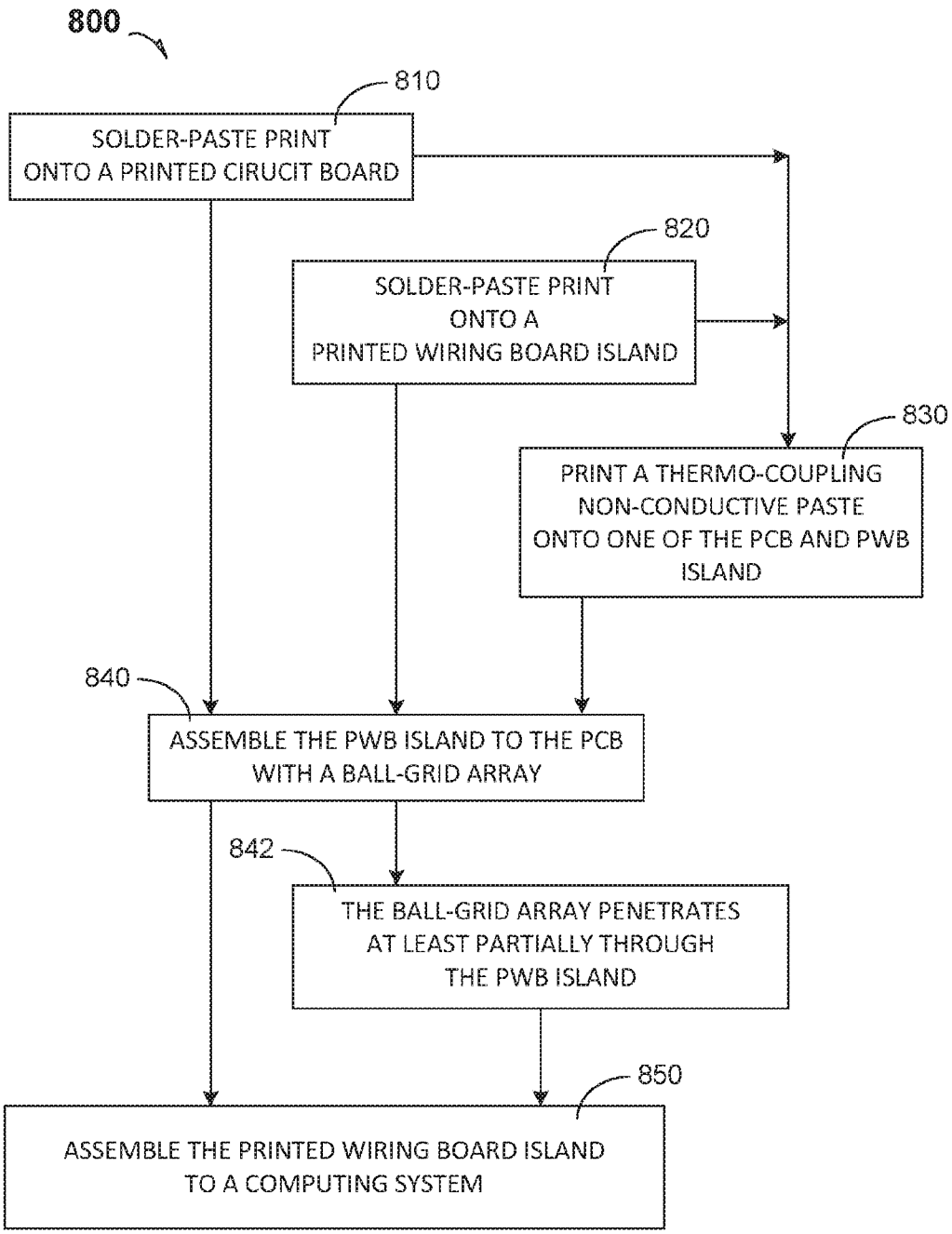

800
810
SOLDER-PASTE PRINT ONTO A PRINTED CIRUCIT BOARD
820
SOLDER-PASTE PRINT ONTO A PRINTED WIRING BOARD ISLAND
830
PRINT A THERMO-COUPLING NON-CONDUCTIVE PASTE ONTO ONE OF THE PCB AND PWB ISLAND
840
ASSEMBLE THE PWB ISLAND TO THE PCB WITH A BALL-GRID ARRAY
842
THE BALL-GRID ARRAY PENETRATES AT LEAST PARTIALLY THROUGH THE PWB ISLAND
850
ASSEMBLE THE PRINTED WIRING BOARD ISLAND TO A COMPUTING SYSTEM

Fig. 8

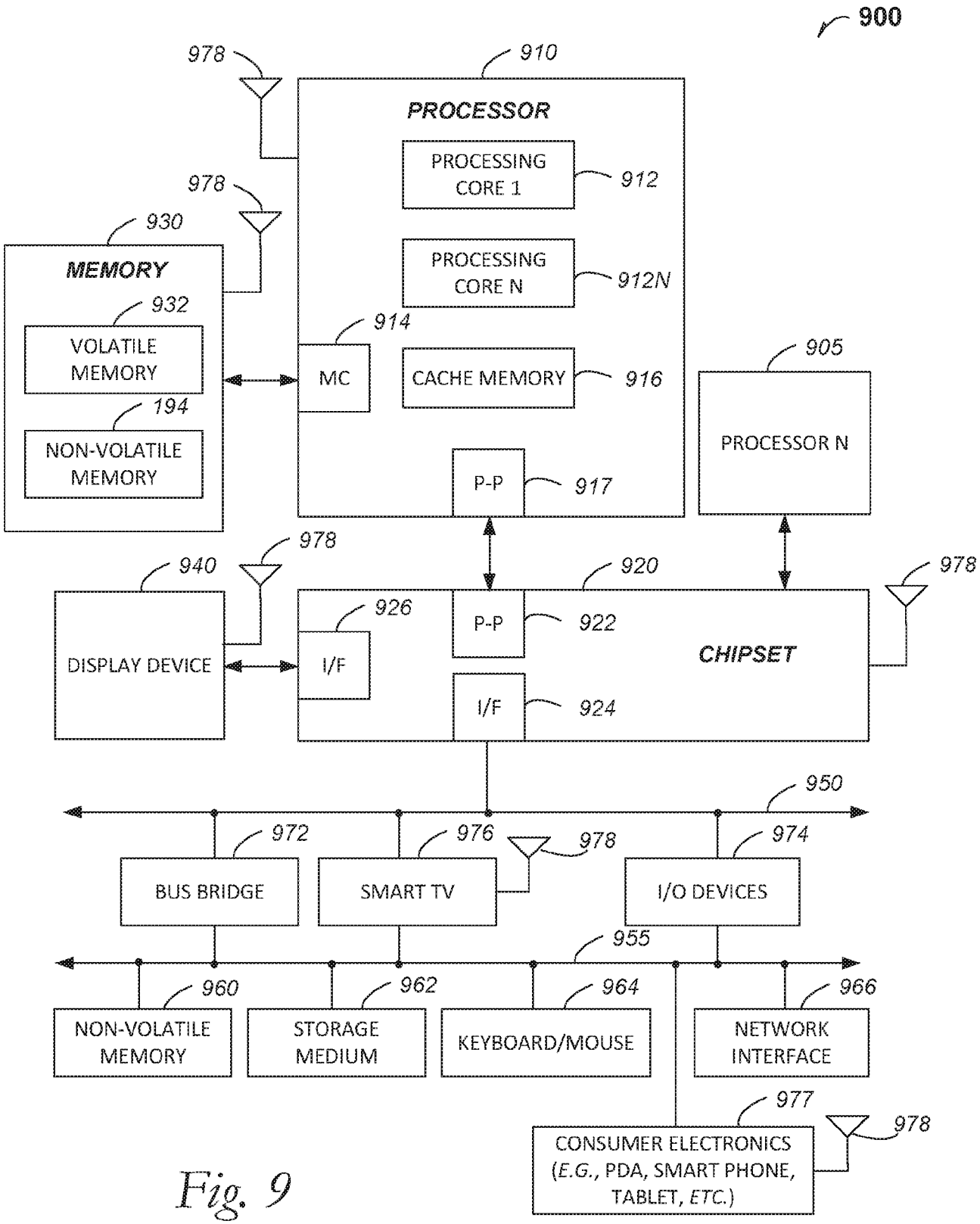

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PROCESSOR
PROCESSING CORE 1
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MEMORY
PROCESSING CORE N
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VOLATILE MEMORY
MC
CACHE MEMORY
916
905
194
NON-VOLATILE MEMORY
P-P
917
PROCESSOR N
978
940
920
978
926
P-P
922
DISPLAY DEVICE
I/F
CHIPSET
I/F
924
950
972
976
978
974
BUS BRIDGE
SMART TV
I/O DEVICES
955
960
962
964
966
NON-VOLATILE MEMORY
STORAGE MEDIUM
KEYBOARD/MOUSE
NETWORK INTERFACE
977
978
CONSUMER ELECTRONICS (E.G., PDA, SMART PHONE, TABLET, ETC.)

Fig. 9

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2017/054548

A. CLASSIFICATION OF SUBJECT MATTER

H01L 25/065(2006.01)i, H01L 25/07(2006.01)i, H01L 23/00(2006.01)i, H01L 23/498(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 25/065; H05K 1/18; H01L 23/52; H05K 3/30; H01L 21/50; H05K 3/34; H01L 23/48; H05K 3/00; H01L 25/07; H01L 23/00; H01L 23/498

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: printed wiring-board island, printed circuit board, routing density, package

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 2012-0279059 A1 (BRENT M. ROBERTS et al.) 08 November 2012 See paragraphs [0019]-[0043] and figures 1-6.	1-2,4-5,12,16-17,19,21 3,6-11,13-15,18,20,22
Y	US 2016-0095220 A1 (INTEL CORPORATION) 31 March 2016 See paragraphs [0021]-[0030] and figures 1-7.	3,15,18,20
Y	US 2008-0036050 A1 (PAUL T. LIN et al.) 14 February 2008 See paragraphs [0009], [0028]-[0035] and figures 1-9B.	6-11,13-15,22
A	US 2006-0138636 A1 (PIERRE BORMANN et al.) 29 June 2006 See paragraphs [0023]-[0040] and figures 1-2.	1-22
A	US 2012-0244728 A1 (JAMES RATHBURN) 27 September 2012 See paragraphs [0045]-[0060] and figures 1A-3B.	1-22

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 June 2018 (28.06.2018)	**28 June 2018 (28.06.2018)**

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea
Facsimile No. +82-42-481-8578

Authorized officer
CHOI, Sang Won
Telephone No. +82-42-481-8291

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2017/054548

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