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[Continued on next page]

(54) Title: FORMING A RECESS IN A MULTI-LAYERED DEVICE

Layer No.	Material Type	Thickness (MM)	Routing Type
L1	Conductive Plating (104)	0.02	Signal
L2	Conductive Plating (104)	0.045	Signal
L3	Conductive Plating (104)	0.075	Signal
L4	Conductive Plating (104)	0.015	GND
L5	Conductive Plating (104)	0.015	Signal
L6	Conductive Plating (104)	0.015	GND
L7	Conductive Plating (104)	0.015	Signal
L8	Conductive Plating (104)	0.015	PWR
L9	Conductive Plating (104)	0.015	Signal
L10	Conductive Plating (104)	0.015	Signal
L11	Conductive Plating (104)	0.015	GND
L12	Conductive Plating (104)	0.045	Signal
	Solder Mask (102)	0.02	

200B
FIG. 2B

(57) Abstract: A method related to removing layers in a multi-layered PCB is described. The method includes removing one or more layers of a multi-layered printed circuit board (PCB) layer via material removal techniques. The removal of the layers reduces the thickness of the multi-layered PCB in a section while the thickness in another section of the PCB is maintained. The method includes forming a recess in the section of the multi-layered PCB to provide additional spacing on the multi-layered PCB. The method further includes placing components in the recessed section of the multi-layered PCB.



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FORMING A RECESS IN A MULTI-LAYERED DEVICE

BACKGROUND

[0001] Design requirements, including size and thickness requirements for a printed circuit board (PCB), are a concern for system board designers. In some cases, such design requirements may limit real estate for placement of electrical components on the PCB of a device. For example, the PCB must be of a particular thickness to obtain proper signal routing or to fit into a pre-existing form factor, among other considerations. However, the thickness of a PCB that includes various mounted electrical components, such as memory modules, power sources, may conflict with height restrictions imposed by a device to fit the PCB in an enclosure of the device. In some cases, an electronic device may impose a maximum vertical height for a PCB with mounted components within an enclosure of the device. If the height of the PCB with mounted components exceeds the maximum vertical height imposed by the device, less important components and features may be removed from the PCB in order to provide spacing for required components. The removal of components may lead to problems related to circuit performance, increased design time, and time-consuming revisions.

BRIEF DESCRIPTION OF THE DRAWINGS

[0002] The advantages of the present techniques are better understood by referring to the following detailed description and the attached drawings, in which:

[0003] Fig. 1 is a cross-sectional view of an example of various layers of a printed circuit board (PCB) layer stack-up;

[0004] Fig. 2A is a cross-sectional view of an example of a multi-layered PCB as used in an electronic device;

[0005] Fig. 2B is a cross-sectional view of an example of the multi-layered PCB with three layers removed from a top portion of the PCB;

[0006] Fig. 2C is a cross-sectional view of an example of the multi-layered PCB with six layers removed from a top portion of the PCB;

[0007] Fig. 2D is a cross-sectional view of an example of the multi-layered PCB with three layers removed from a bottom portion of the PCB;

[0008] Fig. 2E is a cross-sectional view of an example of the multi-layered PCB with six layers removed from a bottom portion of the PCB;

[0009] Fig. 3 is a block method diagram of an example of a method for removing layers from a multi-layered PCB; and

[0010] Fig. 4 is a block method diagram of an example of a method for installing a number of components in a recessed section of a multi-layered PCB.

DETAILED DESCRIPTION OF SPECIFIC EXAMPLES

[0011] Examples disclosed herein are generally related to techniques for reducing the thickness of a printed circuit board (PCB) of an electronic device to optimize spacing for components and alleviate height restrictions imposed by the electronic device.

[0012] The tendency in modern electronic devices is toward a smaller, lighter electronic device with increased functionality. In particular, the miniaturization of an electronic device, such as a server, may provide enhanced portability and system capabilities, among other advantages. However, such enhancements may lead to an increase in the number of components electrically mounted on the PCB. For example, decreasing component size and pitch of memory modules may encourage board designers to increase the original number of memory modules located on an existing PCB space. While this increase may provide faster transmission of data signals and a reduction in data signal loss and crossing delays, additional PCB real estate may be needed to prevent component overcrowding and thermal management issues related to overheating, among other issues.

[0013] One solution to deal with the lack of PCB surface area is to embed electrical components within the PCB rather than on the surface of the PCB. However, embedded electrical components may pose long-term reliability problems. For instance, subsequent soldering processes, such as reflow on surface-mount devices, may affect the solder joints of the embedded components. Furthermore, embedded electrical components may be difficult to test and replace following a failure, and thus, may cause additional problems after the device PCB is manufactured. In some cases, typical solutions, including the embedding of components and custom-built solutions to design PCBs are less economical than

industry standard solutions since a designer may have to qualify a lower-profile custom component within the same footprint.

[0014] Fig. 1 is a cross-sectional view of an example of various layers of a printed circuit board (PCB) layer stack-up 100. The PCB 100 layer stack-up of Fig. 1 may be used in various electronic devices, for example, servers, desktop computers, and portable mobile devices, among others. Various types of materials may be used in the manufacturing of the PCB 100 layer stack-up where material determinations may be based on certain properties include electrical, temperature, and other related property specifications. In the present examples, the PCB 100 layer stack-up 100 may include four basic material layers, including a solder mask layer 102, a conductive plating layer 104, a core layer 106, and a pre-preg layer 108.

[0015] The solder mask layer 102 is a non-conductive layer and may be made of a polymer material, such as an epoxy, an acrylic, or a polyurethane, among others. The polymer material may provide a protective coating for electrical traces of the PCB layer stack-up 100. In some cases, the solder mask layer 102 may be applied to the PCB layer stack-up 100 to prevent solder material from bridging between the electrical traces of the stack-up 100, thereby preventing short circuits. The top and bottom layers of the PCB layer stack-up 100 may include the solder mask layer 102, as shown in Fig. 1.

[0016] The core layer 106 may be made of a panel of dielectric material used to build the inner layers of the PCB layer stack-up 100. The dielectric material of the core layer 106 may include a fiber-glass, reinforced epoxy, among other types of materials.

[0017] The conductive plating layer 104 is pre-plated onto a top surface and a bottom surface of the core layer 106. In this manner, a standard thickness of the core layer 106 may be formed by applying one ounce (oz.) of a conductive material over an area of about one square foot on the top and bottom surfaces of the core 106. The conductive plating layer 104 formed using one ounce (oz.) of a conductive material may be about 0.04 mm in thickness. However, the amount of conductive material used to form the conductive plating layer may vary to form layers of different thicknesses. For example, the amount of conductive material used may include 0.5 oz. (to form a layer of about 0.02 mm in thickness), 2 oz. (to form a layer of about 0.07 mm in thickness), or 3 oz. (to form a layer of about 0.11 mm in thickness), or

any other amount based on manufacturers specifications. In most cases, the conductive plating layer 104 is a copper plating layer.

[0018] The pre-preg layer 108 may be made of a fiberglass material that functions as an adhesive to bind the core layers 106 together and to maintain the adhesion between the core layers 106, for example, during fabrication. In one example, the pre-preg layer 108 is an uncured fiberglass-epoxy resin weave that acts both as insulation between the core layers 106 of the PCB layer stack-up 100 and as an adhesive agent. During the manufacturing process of the PCB layer stack-up 100, the conductive plating layers 104, the core layers 106, and the pre-preg layer 108 may be heat-pressed together. The heat-press treatment cures the pre-preg material and binds all of the various layers 102, 104, 106, and 108 in various configurations to form a multi-layered PCB, as will be later discussed.

[0019] It is to be understood that the illustration of Fig. 1 is not intended to indicate that the PCB layer stack-up 100 is to include or is limited to the number of layers shown. Further, it is not intended to indicate that the PCB layer stack-up 100 is to include or is limited to the type of material layers shown. Any number of layers or types of materials may be included within the PCB layer stack-up 100, depending on the details of the specific implementation.

[0020] Fig. 2A is a cross-sectional view of an example of a multi-layered printed circuit board (PCB) 200A as used in an electronic device. Like numbers are as described with respect to Fig. 1. The multi-layered PCB 200A includes the various material layers as shown in Fig. 1, including solder mask layers 102, conductive plating layers 104, core layers 106, and pre-preg layers 108. In particular, the PCB, as depicted in Fig. 2A, is a multi-layered PCB 200A that includes a configuration of 12 stacked layers.

[0021] In the present examples, the number of conductive plating layers 104, as represented by the column labeled "Layer Number (No.)" 202, may vary depending on factors such as functional requirements and complexity of the electronic device. In particular, such factors may include the number of signals that are routed on the multi-layered PCB 200A and the component density for electrical components located on the multi-layered PCB 200A.

[0022] Each individual conductive plating layer 104 of multi-layered PCB 200A is labeled with an "L" designation that represents the number of a particular conductive

plating layer 104. As shown in Fig. 2A, the stacked conductive plating layers are labeled with an increasing number designation, i.e., L1-L12, as the number of layers increases. In some examples, the conductive plating layers 104 may include several signal routing layers "Signal", several ground layers "GND", and several power layers "PWR". The conductive plating layers 104 may be routed in either a horizontal routing direction or a vertical routing direction.

[0023] The multi-layered PCB 200A, of the present examples, includes several layers of conductive layers 104 separated by dielectric materials similar to the configuration as shown in Fig. 1A. The column labeled as "Material Type" 204 identifies the type of material associated with each layer in the multi-layered PCB 200A. The column labeled as "Routing Type" 206 provides the type of signal carried by a layer. As shown, "power layer PWR" represents a power conduit, "Signal" represents a signal routing layer, and "GND" represents a ground layer.

[0024] The multi-layered PCB 200A of Fig. 2A may be considered as a full multi-layered PCB since no layers of the PCB 200A have been removed. In some examples, the total thickness of the multi-layered PCB 200A, with no layers removed, is based on the combined measured thickness of all of the layers 102, 104, 106, and 108. The thickness of each layer may vary depending on the functional requirements and the complexity of the electronic device in which the multi-layered PCB 200A is located. In some examples, the thickness of the layers may range from about 0.010 millimeters (mm) to about 0.09 mm, giving a total thickness for the PCB 200A of about 0.25 mm to about 3.2 mm.

[0025] Typical techniques may remove less important, i.e., non-required, electrical components to provide additional spacing on the multi-layered PCB 200A for required electrical components or other components deemed necessary to the functionality of the PCB 200A. However, the present examples may use material removal techniques to remove portions of the layers 102, 104, 106, 108 as needed, in an effort to maintain all components, whether required or non-required. The layers removed from the PCB 200A may be located in non-full section since a full multi-layered PCB is not required, for example, where required components are not mounted and all layers are not required for device functionality. Specifically, one or more layers in a particular section of the PCB 200A may be removed to form a recess or any type of opening. In some examples, the removal of the layers may

provide additional vertical spacing on the PCB 200A for vertical placement of components. The components of the present examples may include components soldered to PCB 200A, such tall inductors or standard connectors with a high vertical height, among other. In other examples, the components may not be physically connected to the PCB 200A, where the components may include customer owned equipment (COE) label recesses, mega-cell batteries, USB keep-out for larger devices, among others. As a result, electrical components that may have been removed in typical techniques may be placed in the recess and electrically connected to the PCB 200A.

[0026] The present examples may provide a multi-layered PCB that includes various sections including one or more thicker sections and one or more thinner sections of the multi-layered PCB. The one or more thicker sections of the multi-layered PCB do not include removal of any of the layers of the PCB. Instead, the thickness of the multi-layered PCB when originally manufactured may be maintained in the thicker sections so as to support signal routing and tolerance requirements, among other device requirements. The one or more thinner sections may include a reduction in the thickness of the multi-layered PCB, by removal of a portion of the layers, in order to provide space optimization and to substantially avoid height restrictions imposed by a device, as will be later described. For example, the thinner sections may accommodate electrical components of a particular size, such as taller components.

[0027] It is to be understood that the illustrations of Fig. 2A is not intended to indicate that the multi-layered PCB is to include all of the components shown in Fig. 2A in every case. Further, any number of additional components can be included within the multi-layered PCB, depending on the details of the specific implementation. For example, more or fewer layers may be present.

[0028] Fig. 2B is a cross-sectional view of an example of the multi-layered PCB 200B with three layers removed from a top portion of the PCB 200B. Like numbers are as described with respect to Fig. 2A. Further, the thickness of each layer is indicated in the column labeled "Thickness" 208, and is provided in units of "mm" (millimeters). The range of the thickness for each layer may vary based on functional requirements, as previously discussed.

[0029] As an example, a dual in-line memory module (DIMM) is a circuit board that holds a series of electrical components, e.g., memory integrated circuit (IC) chips, where the DIMM is designed to be mounted on the multi-layered PCB 200B. In some examples, the DIMM may be used as the multi-layered PCB 200B of a device. The example DIMM, as used in the present examples, has an overall thickness that includes the thickness of the DIMM and the thickness associated with the memory chips attached to the DIMM. The combined thickness of multi-layered PCB 200B, which includes the total of all layers, may be a particular thickness due to manufacturing requirements. Thus, the combined thickness of the multi-layered PCB 200B and the overall thickness of the DIMM, when the DIMM is mounted on the PCB 200B, may conflict with vertical height restrictions imposed by a device. Vertical height restrictions may be put in place to fit electrical components mounted on a PCB properly within an enclosure of the device.

[0030] For example, an electronic device may have a height restriction of about 1.20 mm for the mounting of a DIMM on the multi-layered PCB 200B, for example, to adequately fit within an enclosure of the electronic device. Thus, a DIMM with an overall thickness of 1.44 mm would not fit properly with the enclosure. However, examples described herein overcome the height restrictions and provide additional spacing by removing layers in particular sections, i.e., non-full sections, of the multi-layered PCB 200B while maintaining an existing thickness of the layers in other sections, e.g., full sections, of the PCB 200B.

[0031] As depicted in Fig. 2B, layers 1 through 3, i.e., L1-L3, of the multi-layered PCB 200B may be removed from a top portion to form a recess. The industry standard solution of removal one or more layers from a multi-layered PCB may provide additional vertical spacing for component placement. The removal of L1-L3 is depicted by slant lines, as shown in Fig. 2B. Various types of removal techniques may be used, including milling, drilling, or laser techniques, to remove the layers of the PCB 200B. The section of the multi-layered PCB 200B removed may not require a full multi-layered PCB. In particular, the layers L1-L3 are located in a section, i.e., a non-full section, of the PCB 200B not required to meet minimum system requirements for the electronic device since access to all layers of the PCB 200B is not needed. However, components required by the electronic device may be required, and thus, mounted in the full-section of the multi-layered PCB 200B since

access to all of the layers is required. As previously stated, a full-section of a multi-layered PCB includes all layers maintained, i.e., no layers removed, for optimal device performance, for example, in routing intensive areas or in order to route the necessary signal, ground, or power lines on the multi-layered PCB 200B.

[0032] As illustrated in Fig. 2B, removing L1-L3 from the top portion of the multi-layered PCB 200B, may provide an approximate 0.337 mm of additional vertical spacing. Following the example of the electronic device with the 1.20 mm height restriction, the removal provides a recess with a measurement of 0.337 mm within the multi-layered PCB 200B. The PCB 200B may now accommodate the DIMM with an overall thickness of 1.44 mm. In particular, 0.337 mm of the 1.44 mm thickness of the DIMM may be located within the recess of the multi-layered PCB 200B. As a result, a remaining thickness of 1.103 mm of the DIMM extends from the surface of the multi-layered PCB 200B and thus, meets the electronic device height restriction of 1.20 mm. Additionally, other full sections of the multi-layered PCB 200B may maintain the existing thickness of the PCB 200B were no material removal techniques were implemented.

[0033] It is to be understood that the illustration of Fig. 2B is not intended to indicate that the electronic device includes a multi-layered PCB 200B with three layers removed from the top portion of the PCB in every case. Any type of number of layers may be removed to provide space optimization and to avoid height restrictions as required by the electronic device.

[0034] Fig. 2C is a cross-sectional view of an example of the multi-layered PCB 200C with six layers removed from a top portion of the PCB 200C. Like numbers are as described with respect to Fig. 2A. As shown in Fig. 2C, layers L1 through L6 are removed from a top portion of the multi-layered PCB 200C. In particular, L1-L6 may be removed from a non-full section of the multi-layered PCB 200C. The removal of L1-L6 is depicted by slant lines, as shown in Fig. 2C. The removal of L1-L6 provides approximately 0.72 mm of additional vertical spacing to support additional components for placement on the multi-layered PCB 200C.

[0035] Following the example of the electronic device with the 1.20 mm height restriction for the placement of components, the removal provides a recess with a measurement of 0.72 mm within the multi-layered PCB 200C. The PCB 200C may now accommodate a DIMM with an overall thickness of 1.44 mm. In particular, 0.72

mm of the 1.44mm thickness of the DIMM may be located within the recess of the multi-layered PCB 200C. As a result, a remaining thickness of 0.72 mm of the DIMM extends from the surface of the multi-layered PCB 200C and meets the height restriction of 1.20 mm imposed by the electronic device. Additionally, other sections, i.e., full sections, of the multi-layered PCB 200C may maintain the existing thickness of the PCB 200C were material removal techniques are not used.

[0036] It is to be understood that the illustration of Fig. 2C is not intended to indicate that the electronic device includes a multi-layered PCB with six layers removed from the top portion of the PCB in every case. Any type of number of layers may be removed to provide space optimization and to avoid height restrictions as imposed by the electronic device.

[0037] Fig. 2D is a cross-sectional view of an example of the multi-layered PCB 200D with three layers removed from a bottom portion of the PCB 200D. Like numbers are as described with respect to Fig. 2A. As shown in Fig. 2D, layers L9 through L12, are removed from a section, e.g., a non-full section, of the multi-layered PCB 200D. The removal of L9-L12 is depicted by slant lines, as shown in Fig. 2D, where layers from the bottom portion of the multi-layered PCB 200D may be removed to provide additional vertical spacing on the PCB 200D. The removal of L9-L12 provides approximately 0.337 mm of additional vertical spacing to support additional components for placement on the bottom portion of the multi-layered PCB 200D.

[0038] Following the example of the electronic device with the 1.20 mm height restriction, the removal provides a recess with a measurement of 0.337 mm within the multi-layered PCB 200D. The bottom portion of the PCB 200D may now accommodate the DIMM with an overall thickness of 1.44 mm. In particular, 0.337 mm of the 1.44 mm thickness of the DIMM may be located within the recess of the multi-layered PCB 200D. As a result, a remaining thickness of 1.103 mm of the DIMM extends from the bottom portion of the multi-layered PCB 200D and meets the height restriction of 1.20 mm imposed by the electronic device

[0039] It is to be understood that the illustration of Fig. 2D is not intended to indicate that the electronic device includes a multi-layered PCB with three layers removed from the bottom portion of the PCB in every case. Any type of number of

layers may be removed to provide space optimization and to avoid vertical height restrictions as required by the electronic device.

[0040] Fig. 2E is a cross-sectional view of an example of the multi-layered PCB 200E with six layers removed from a bottom portion of the PCB 200E. Like numbers are as described with respect to Fig. 2E. As shown in Fig. 2E, layers L6 through L12 are removed from a section, i.e., a non-full section, of the multi-layered PCB 200E to provide additional spacing for additional electrical components. The removal of L6-L12 is depicted by slant lines, as shown in Fig. 2E. The removal of L6-L12 provides approximately 0.337 mm of additional vertical spacing to support additional components for placement on a bottom portion of the multi-layered PCB 200E.

[0041] Following the example of the electronic device with the 1.20 mm height restriction, the removal provides a recess with a measurement of 0.337 mm within the bottom portion of the multi-layered PCB 200E. The PCB 200E may now accommodate the DIMM with an overall thickness of 1.44 mm. In particular, 0.337 mm of the 1.44 mm thickness of the DIMM may be located within the recess of the multi-layered PCB 200E. As a result, a remaining thickness of 1.103 mm of the DIMM extends from a bottom surface of the PCB 200E and meets the height restriction of 1.20 mm imposed by the electronic device.

[0042] It is to be understood that the illustration of Fig. 2E is not intended to indicate that the electronic device includes a multi-layered PCB with six layers removed from the bottom portion of the PCB in every case. Any type of number of layers may be removed to provide space optimization and to avoid vertical height restrictions as required by the electronic device.

[0043] Fig. 3 is a block method diagram of an example of a method for removing layers from a multi-layered PCB. At block 302, techniques may be used to remove one or more layers of a multi-layered PCB. Various types of removal techniques may be used, including milling, drilling, and laser techniques, among others. The removal reduces the thickness of the PCB in a particular section, e.g., a non-full section, of the PCB to provide additional spacing for the mounting of various components. At block 304, due to the removal of the layers, a recess is formed in the section of the multi-layered PCB. The recess may provide additional vertical spacing on the multi-layered PCB. At block 306, the components may be placed in the recessed section of the multi-layered PCB. The components of the present

examples may include components soldered to the PCB 200A such as tall inductors or standard connectors with a high vertical height, among others. In other examples, the components may not be physically connected to the, where the components may include customer owned equipment (COE) label recesses, mega-cell batteries, USB keep-out for larger devices, among others.

[0044] It is to be understood that the process flow diagram of Fig. 3 is not intended to indicate that the method 300 is to include all of the blocks shown in Fig. 3 in every case. Further, any number of additional blocks can be included within the method 300, depending on the details of the specific implementation. In addition, it is to be understood that the process flow diagram of Fig. 3 is not intended to indicate that the method 300 is only to proceed in the order indicated by the blocks shown in Fig. 3 in every case.

[0045] Fig. 4 is a block method 400 diagram of an example of a method for installing a number of components in a recessed section of a multi-layered PCB. At block 402, a combined thickness of a plurality of components is determined. In some cases, an electronic device may provide a height restriction for the mounting of components, for example, to fit inside a housing or enclosure of the device. As a result, it may be difficult to mount electrical components on the multi-layered PCB when the combined thickness of the plurality of components exceeds the thickness of the multi-layered PCB. Accordingly, at block 404, it is determined whether the thickness of the plurality of components exceeds a height restriction for mounting the plurality of components on the multi-layered PCB.

[0046] If the thickness of the plurality of components exceeds the height restriction, at block 406, a section of the multi-layered PCB is removed, where the section may include a non-full section. The removal reduces the thickness of the multi-layered PCB in the non-full section where access to all of the layers of the PCB may not be required for device functionality. Various types of removal techniques may be used including milling, drilling, or laser cutting, among other removal techniques. At block 408, a recess may be formed in the non-full section of the multi-layered PCB using a removal technique. At block 410, the plurality of components may be placed in the recess in an effort to overcome any height restrictions and limitations imposed by the electronic device.

[0047] It is to be understood that the process flow diagram of Fig. 4 is not intended to indicate that the method 400 is to include all of the blocks shown in Fig. 4 in every case. Further, any number of additional blocks can be included within the method 400, depending on the details of the specific implementation. In addition, it is to be understood that the process flow diagram of Fig. 4 is not intended to indicate that the method 400 is only to proceed in the order indicated by the blocks shown in Fig. 4 in every case.

[0048] The placement of certain components on a multi-layered PCB may be considered more important to the overall function of the PCB. These components may include components required for device functionality, power management, and electrical noise management, among other considerations. The section of the multi-layered PCB where such required components are located may be considered a full section. Specifically, the thickness of the multi-layered PCB in the full section has not been reduced since the layers of the PCB have been maintained and not subjected to removal. Accordingly, the full multi-layered PCB may support device requirements including signal routing, input/output connections, power circuits, and ground lines, among others. However, other sections of the multi-layered PCB may not include all of the layers of the PCB where the layers are removed. Accordingly, the thickness of the multi-layered PCB in the other sections, e.g., non-full sections, may be reduced by removing a portion of the layers of the PCB to create a recess to mount components not required for device functionality.

[0049] While the present techniques may be susceptible to various modifications and alternative forms, the examples discussed above have been shown only by way of example. However, it should again be understood that the techniques are not intended to be limited to the particular examples disclosed herein. Indeed, the present techniques include all alternatives, modifications, and equivalents falling within the true spirit and scope of the appended claims.

CLAIMS

What is claimed is:

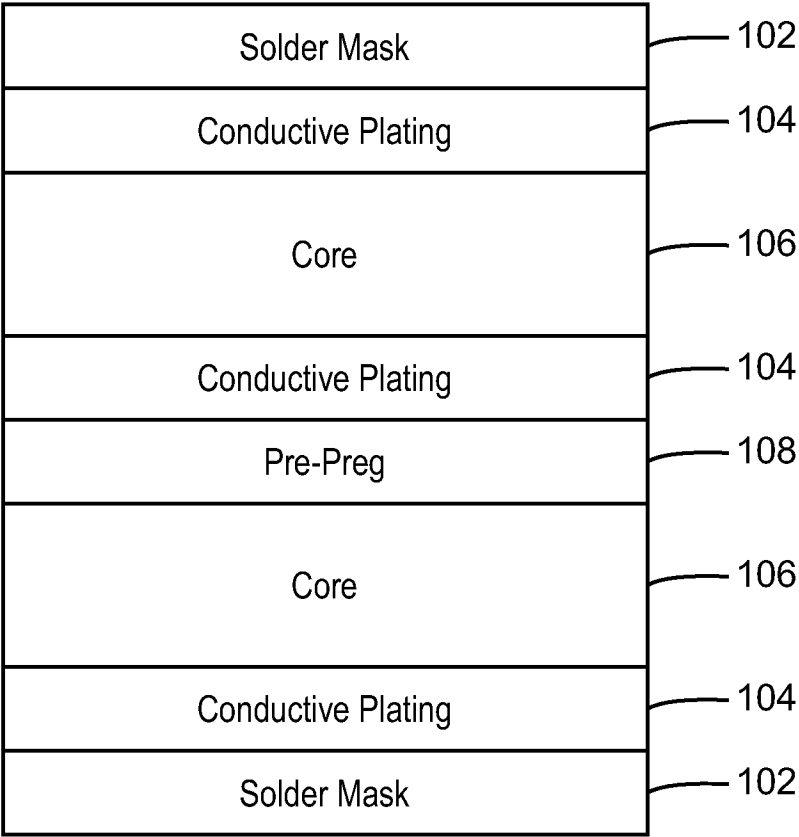
1. A method, comprising:
removing one or more layers of a multi-layered printed circuit board (PCB) via a material removal technique, wherein the removal reduces a thickness of the multi-layered PCB in a section, and wherein a thickness in another section of the PCB is maintained;
forming a recess in the section of the multi-layered PCB to provide additional spacing on the multi-layered PCB; and
placing components in the recessed section of the multi-layered PCB.
2. The method of claim 1, comprising maintaining signal integrity of the multi-layered PCB after removing the section, wherein the multi-layered PCB comprises signal layers, ground lines, and power layers stacked in layers.
3. The method of claim 1, wherein the removing comprises milling, drilling, laser cutting, or other material removal techniques.
4. The method of claim 1, wherein the another section of the multi-layered PCB comprises a full multi-layered PCB, wherein all layers of the multi-layered PCB are maintained.
5. The method of claim 1, disposing the multi-layered PCB within an enclosure of a device, wherein the device imposes height restrictions on the components.
6. The method of claim 1, comprising maintaining mechanical tolerance and electrical performance of the multi-layered PCB after removal of the section of the multi-layered PCB.
7. A device, comprising:
a plurality of layers, wherein the plurality of layers are stacked;
a section of the plurality of layers;

a recess in the section of the plurality of layers, wherein the recess is formed via a material removal technique, wherein a plurality of components are located in the recess, and wherein the plurality of components comprise a first thickness; and another section of the plurality of layers.

8. The device of claim 7, wherein the first thickness of the plurality of components is greater than a height restriction imposed by the device.
9. The device of claim 7, wherein the another section maintains the stack of the plurality of layers.
10. The device of claim 7, wherein the recess in the section of the plurality of layers is located in a top portion of the plurality of layers, a bottom portion of the plurality of layers, or both.
11. A method, comprising:
 - measuring a thickness of a plurality of components;
 - determining that the thickness of the plurality of components exceeds a height restriction for mounting the plurality of components on a multi-layered PCB;
 - removing a section of the multi-layered PCB via a material removal technique, and wherein the removal reduces the thickness of the multi-layered PCB in the section;
 - forming a recess in the section of the multi-layered PCB; and
 - mounting the plurality of components in the recess.
12. The method of claim 11, wherein the section of the multi-layered PCB that is removed comprises a non-full section of the multi-layered PCB and wherein the material removal technique comprises milling, drilling, laser cutting, or other material removal techniques.

13. The method of claim 11, wherein the placing of the plurality of components comprises vertical placement, horizontal placement, or both.
14. The method of claim 11, wherein dimensions for the section removed from the multi-layered PCB is based on a combined thickness of the plurality of components.
15. The method of claim 11, comprising maintaining a mechanical tolerance and electrical performance of the multi-layered PCB after the removal of the section of the multi-layered PCB.

1/8



100
FIG. 1

2/8

202 204 206

Layer No.	Material Type	Routing Type
	Solder Mask (102)	
L1	Conductive Plating (104)	Signal
	core (106)	
L2	Conductive Plating (104)	GND
	pre-preg (108)	
L3	Conductive Plating (104)	Signal
	core (106)	
L4	Conductive Plating (104)	Signal
	pre-preg (108)	
L5	Conductive Plating (104)	GND
	core (106)	
L6	Conductive Plating (104)	Signal
	pre-preg (108)	
L7	Conductive Plating (104)	Signal
	core (106)	
L8	Conductive Plating (104)	PWR
	pre-preg (108)	
L9	Conductive Plating (104)	Signal
	core (106)	
L10	Conductive Plating (104)	Signal
	pre-preg (108)	
L11	Conductive Plating (104)	GND
	core (106)	
L12	Conductive Plating (104)	Signal
	Solder Mask (102)	

200A
FIG. 2A

3/8

202 204 208 206

Layer No.	Material Type	Thickness (MM)	Routing Type
L1	Solder Mask (102)	0.02	
	Conductive Plating (104)	0.045	Signal
	core (106)	0.075	
L2	Conductive Plating (104)	0.015	GND
	pre-preg (108)	0.085	
	Conductive Plating (104)	0.015	Signal
L3	core (106)	0.165	
	Conductive Plating (104)	0.015	Signal
	pre-preg (108)	0.085	
L4	Conductive Plating (104)	0.015	GND
	core (106)	0.085	
	Conductive Plating (104)	0.015	Signal
L5	pre-preg (108)	0.17	
	Conductive Plating (104)	0.015	Signal
	core (106)	0.085	
L6	Conductive Plating (104)	0.015	PWR
	pre-preg (108)	0.085	
	Conductive Plating (104)	0.015	Signal
L7	core (106)	0.0165	
	Conductive Plating (104)	0.015	Signal
	pre-preg (108)	0.085	
L8	Conductive Plating (104)	0.015	GND
	core (106)	0.015	
	Conductive Plating (104)	0.045	Signal
L9	Solder Mask (102)	0.02	

Total = 0.337 mm

200B
FIG. 2B

4/8

Layer No.	Material Type	Thickness (MM)	Routing Type
	Solder Mask (102)	0.02	
L1	Conductive Plating (104)	0.045	Signal
	core (106)	0.075	
L2	Conductive Plating (104)	0.015	GND
	pre-preg (108)	0.085	
L3	Conductive Plating (104)	0.015	Signal
	core (106)	0.165	
L4	Conductive Plating (104)	0.015	Signal
	pre-preg (108)	0.085	
L5	Conductive Plating (104)	0.015	GND
	core (106)	0.085	
L6	Conductive Plating (104)	0.015	Signal
	pre-preg (108)	0.17	
L7	Conductive Plating (104)	0.015	Signal
	core (106)	0.085	
L8	Conductive Plating (104)	0.015	PWR
	pre-preg (108)	0.085	
L9	Conductive Plating (104)	0.015	Signal
	core (106)	0.0165	
L10	Conductive Plating (104)	0.015	Signal
	pre-preg (108)	0.085	
L11	Conductive Plating (104)	0.015	GND
	core (106)	0.015	
L12	Conductive Plating (104)	0.045	Signal
	Solder Mask (102)	0.02	

Total = 0.72 mm

200C
FIG. 2C

5/8

202 204 208 206

Layer No.	Material Type	Thickness (MM)	Routing Type
	Solder Mask (102)	0.02	
L1	Conductive Plating (104)	0.045	Signal
	core (106)	0.075	
L2	Conductive Plating (104)	0.015	GND
	pre-preg (108)	0.085	
L3	Conductive Plating (104)	0.015	Signal
	core (106)	0.165	
L4	Conductive Plating (104)	0.015	Signal
	pre-preg (108)	0.085	
L5	Conductive Plating (104)	0.015	GND
	core (106)	0.085	
L6	Conductive Plating (104)	0.015	Signal
	pre-preg (108)	0.17	
L7	Conductive Plating (104)	0.015	Signal
	core (106)	0.085	
L8	Conductive Plating (104)	0.015	PWR
	pre-preg (108)	0.085	
L9	Conductive Plating (104)	0.015	Signal
	core (106)	0.0165	
L10	Conductive Plating (104)	0.015	Signal
	pre-preg (108)	0.085	
L11	Conductive Plating (104)	0.015	GND
	core (106)	0.015	
L12	Conductive Plating (104)	0.045	Signal
	Solder Mask (102)	0.02	

Total = 0.337 mm

200D
FIG. 2D

6/8

Layer No.	Material Type	Thickness (MM)	Routing Type
	Solder Mask (102)	0.02	
L1	Conductive Plating (104)	0.045	Signal
	core (106)	0.075	
L2	Conductive Plating (104)	0.015	GND
	pre-preg (108)	0.085	
L3	Conductive Plating (104)	0.015	Signal
	core (106)	0.165	
L4	Conductive Plating (104)	0.015	Signal
	pre-preg (108)	0.085	
L5	Conductive Plating (104)	0.015	GND
	core (106)	0.085	
L6	Conductive Plating (104)	0.015	Signal
	pre-preg (108)	0.17	
L7	Conductive Plating (104)	0.015	Signal
	core (106)	0.085	
L8	Conductive Plating (104)	0.015	PWR
	pre-preg (108)	0.085	
L9	Conductive Plating (104)	0.015	Signal
	core (106)	0.0165	
L10	Conductive Plating (104)	0.015	Signal
	pre-preg (108)	0.085	
L11	Conductive Plating (104)	0.015	GND
	core (106)	0.015	
L12	Conductive Plating (104)	0.045	Signal
	Solder Mask (102)	0.02	

Total = 0.72 mm

200E

FIG. 2E

7/8

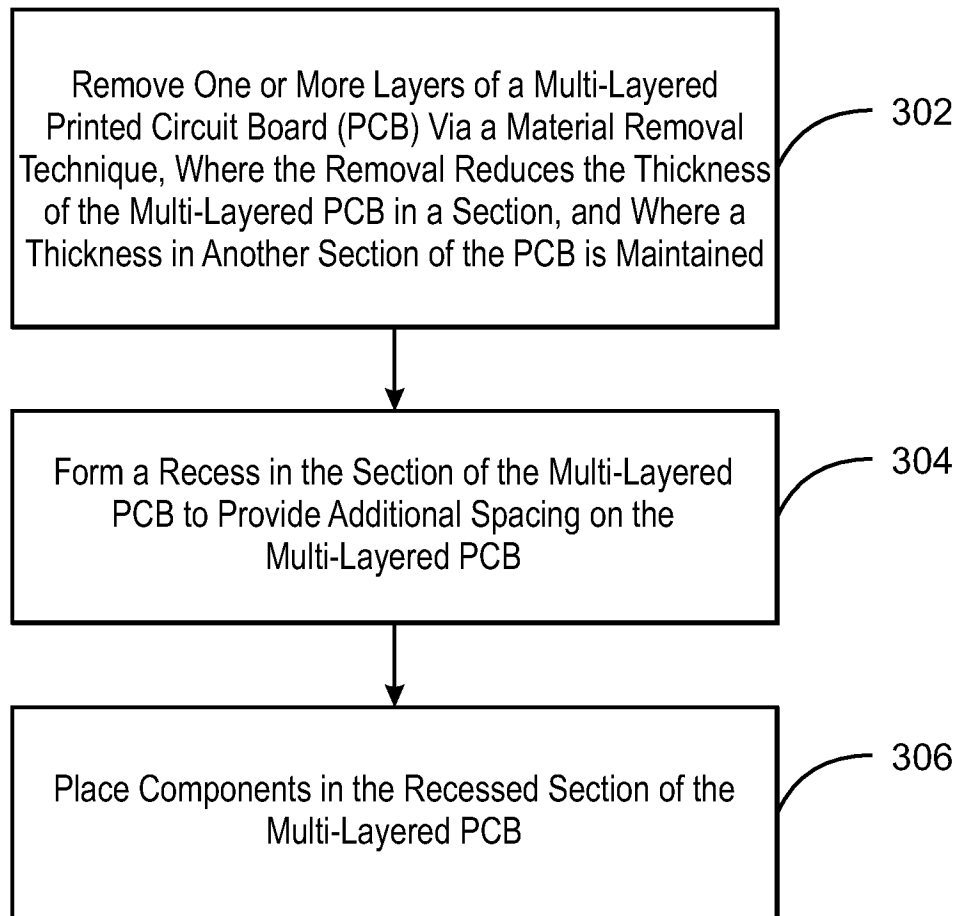
300

FIG. 3

8/8

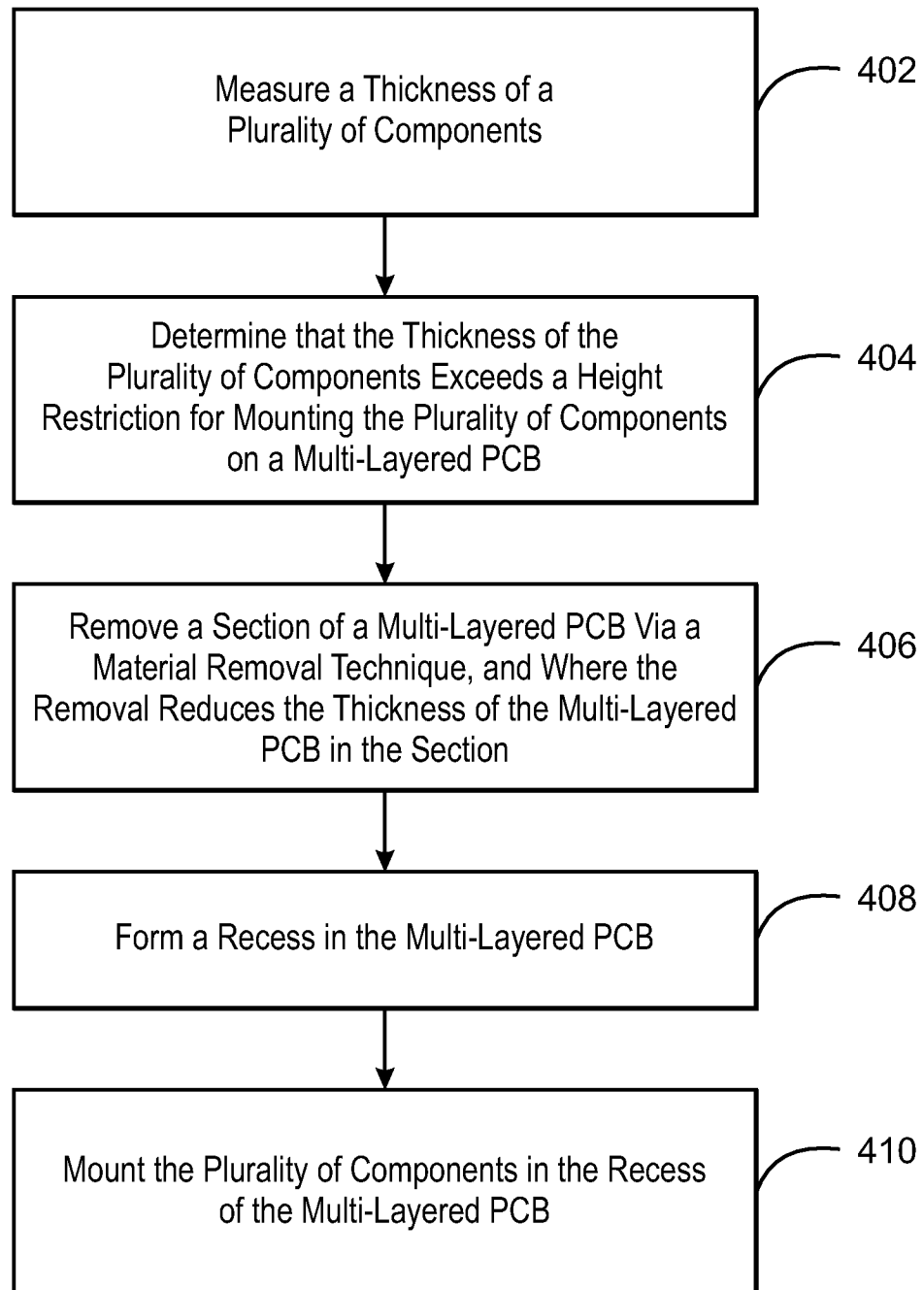
400

FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/011434**A. CLASSIFICATION OF SUBJECT MATTER****H05K 3/46(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H05K 3/46; H05K 3/34; B23P 19/04; H05K 3/10; H05K 1/14; H05K 3/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & keywords: multi-layered printed circuit board, recess, material removal technique, a section of PCB, another section of PCB, thickness

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2014-0055961 A1 (SHAYAN MALEK et al.) 27 February 2014 See paragraphs [0009], [0030]-[0032], [0044]-[0053], [0066], claim 14, and figures 2-3.	1,3-5,7,9-14
Y		2,6,8,15
Y	JP 2005-093783 A (SHINKO SEISAKUSHO K.K.) 07 April 2005 See abstract, paragraphs [0002]-[0013], claims 1-7, and figures 7-8.	2,6,8,15
A	US 2008-0205008 A1 (MING SUN et al.) 28 August 2008 See paragraph [0034], claims 1, 12, and figures 1-3J.	1-15
A	JP 2007-088288 A (SUMITOMO ELECTRIC IND. LTD.) 05 April 2007 See abstract, claims 1-9, and figures 4-5.	1-15
A	US 2012-0308718 A1 (RYOICHI WATANABE) 06 December 2012 See claim 1, and figures 1, 9-13.	1-15



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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Date of the actual completion of the international search

15 October 2015 (15.10.2015)

Date of mailing of the international search report

16 October 2015 (16.10.2015)

Name and mailing address of the ISA/KR

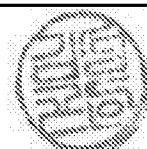
International Application Division
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2015/011434

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