A semiconductor structure with partially etched gate and method of fabricating the same. A semiconductor structure with a single-sided or dual-sided partially etched gate comprises a gate dielectric layer, a gate conductive layer and a cap layer sequentially stacked on a substrate to form a gate structure, and a lining layer disposed on sidewalls of the gate structure, wherein the lining layer is partially etched to expose the adjacent gate structure. In addition, an inter-layer dielectric layer covers the gate structure and a contact is formed in the inter-layer dielectric layer, exposing the substrate and a portion of the gate structure therein, wherein the lining layer of the exposed portion of the gate structure is partially removed.
FIG. 3

FIG. 4
FIG. 5

FIG. 6
FIG. 11

FIG. 12
FIELD OF THE INVENTION

The present invention relates to a semiconductor device and the fabricating method thereof. More particularly, it relates to a semiconductor structure with partially etched gate and method of fabricating the same.

BACKGROUND OF THE INVENTION

In general, the gate structure of a metal oxide semiconductor field effect transistor (MOSFET) device is composed of a metal layer and an oxide layer stacked on a semiconductor substrate. Typically, the metal layer is substituted with a polysilicon layer to act as a gate conductive layer of the gate structure because of poor adhesion between metal and the oxide layer. However, the resistance of polysilicon materials is higher than that of the metal such that the polysilicon layer is usually doped with impurities to lower the resistance thereof. After doping with impurities, the conductivity of the polysilicon layer is reduced but not low enough to act as a conductive layer. A possible solution is to form a metal silicide layer such as tungsten silicide (WSi) layer thereon for improving gate conductivity. In addition, a cap layer is further disposed over the metal silicide layer of the gate structure, and a lining layer and spacers are respectively disposed beside the gate structure to insulate conductive materials thereof. Preferably, the cap layer and the spacer material can be silicon nitride to provide better insulation.

A field after formation of the gate structure of individual MOSFET device, which acts as a wordline (WL), a thick insulating layer (typically borophosphatesilicate glass (BPSG)) is formed over the wordline. Then an opening is etched through the insulating layer to the substrate between two adjacent wordlines by conventional photolithography and etching. Conductive material is then filled in the opening to form a contact node that connects the follow-up devices such as a bitline. The described process is the so-called “self-aligned contact” (SAC) opening process and is frequently used in semiconductor fabrication procedure.

Moreover, a method of forming the semiconductor structure with single-sided partially etched gate comprises the steps of providing a semiconductor substrate with at least two adjacent gate structures thereon, wherein each gate structure is composed of a gate dielectric layer, a gate conductive layer, a cap layer, sequentially stacked on the substrate, and a lining layer covered on sidewalls thereof. Then a protective layer and a masking layer are sequentially formed over the gate structures and an opening is formed in the masking layer and the protective layer. The protective layer in the opening is etched to partially expose the lining layer covering one sidewall of the two adjacent gate structures. Next, after the exposed lining layers are removed, the masking layer and the protective layer are then removed. Next, a spacer is formed overlying sidewalks of each gate structure to form a plurality of single-sided partially etched gate structures. In addition, an inter-layer dielectric layer is formed over the gate structures and a bitline contact is formed in the inter-layer dielectric layer to expose the substrate and portions of the adjacent gate structures therein. Moreover, after removal of the exposed portions of the gate structures adjacent to the exposed lining layers can also be partially removed.

A semiconductor structure with a dual-sided partially etched gate in accordance with another embodiment of
the invention comprises a gate dielectric layer, a gate conductive layer and a cap layer, sequentially stacked on a substrate to form a gate structure, and a lining layer disposed on sidewalls of the gate structure, wherein the lining layer disposed on two sidewalls of the gate structure is partially etched to expose the adjacent gate structure. In addition, an inter-layer dielectric layer covers the gate structure and a contact is formed in the inter-layer dielectric layer to expose the substrate and a portion of the gate structure therein, wherein the lining layer of the exposed portion of the gate structure is partially removed.

[0015] Moreover, a method of forming the semiconductor structure with dual-sided partially etched gate comprises the steps of providing a semiconductor substrate with at least two adjacent gate structures thereon, wherein each gate structure is composed of a gate dielectric layer, a gate conductive layer, a cap layer, sequentially stacked on the substrate, and a lining layer covered on sidewalls thereof. A protective layer is then formed over the gate structures and portions of the protective layer are etched to partially expose the lining layer covering two sidewalls of the gate structures. After the exposed lining layers and the protective layer are removed, a spacer is formed overlying sidewalls of the gate structures to form a plurality of gate structures with dual-sided partially etched gate conductive layer. In addition, an inter-layer dielectric layer is formed, covering the gate structure, and a bitline contact is formed in the inter-layer dielectric layer to expose the substrate and portions of the gate structures therein, wherein the lining layers of the exposed gate structures are partially removed.

[0016] The semiconductor structure with single-sided or dual-sided partially etched gates in accordance with the present invention can prevent the so-called “CB to WL short”, “CB open” or “CB to CB short” and pitches between two adjacent gate structures can be enlarged to provide a larger window for the opening formation of the self-aligned contact (SAC) process to meet the demand for line/pitch shrinkage of gate structures.

[0017] Moreover, the semiconductor structure with partially etched gates in accordance with the present invention will not affect regions receiving ion implantation such as source/drain implantation and channel length of the partially etched gate structure remains the same and will not be affected by the structure thereof. The method of the present invention can be slightly modified from the in-line processes and quickly and easily applied to the fabrication process.

[0018] A detailed description is given in the following embodiments with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] The present invention can be more fully understood by reading the subsequent detailed description and examples with references made to the accompanying drawings, wherein:

[0020] FIGS. 1-7 are cross sections of a fabrication process for forming a SAC opening with a single-sided etched gate structure in accordance with one embodiment of the invention;

[0021] FIGS. 8-16 are cross sections of a fabrication process for forming a SAC opening with a dual-sided etched gate structure in accordance with another embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0022] The method of fabricating a semiconductor structure with partially etched gate in accordance with one embodiment of the invention is shown through FIG. 1 to FIG. 7 and an application thereof in the self-aligned contact (SAC) process is also illustrated.

[0023] In FIG. 1, a semiconductor substrate, for example a silicon substrate 10, with two adjacent gate structures G thereon is provided. Each of the gate structures G includes a gate dielectric layer 12, a polysilicon layer 14, a metal silicide layer 16, and a cap layer 18, sequentially stacked on the silicon substrate 10. A lining layer 20 is formed on the silicon substrate 10, and sidewalls of the gate dielectric layer 12, the polysilicon layer 14 and the metal silicide layer 16. Materials of the gate dielectric layer 12, the polysilicon layer 14, the metal silicide layer 16, the cap layer 18, and the lining layer 20 are preferably silicon dioxide, impurity doped polysilicon, tungsten silicide, silicon nitride and rapid thermal oxide (RTO). The polysilicon layer 14 and the metal silicide layer 16 comprise a gate conductive layer of the gate structures G.

[0024] In FIG. 2, a protective layer 22 and a first masking layer 24 are sequentially formed over the gate structures G. The protective layer 22 can be, for example, an anti-reflection coating (ARC) layer and materials of the first masking layer 24 can be, for example, photosresist (PR) materials. Next, photolithography (not shown) is performed to form an opening OP at a proper position in the first masking layer 24 and exposes the protective layer 22 thereunder. Here the position of the opening OP corresponds to a position of a follow-up bitline contact structure such as a bitline contact node or a bitline contact hole and the photolithography for forming the opening OP can be achieved using a bitline contact node reticle or a bit-line contact reticle.

[0025] In FIG. 3, the exposed protective layer 22 in the opening OP is then etched to leave portions remained on the lining layer 20 in the opening OP. Thus, the lining layer 20 disposed on one sidewall of each gate structure G is partially exposed.

[0026] In FIG. 4, an etching step (not shown), for example wet etching using diluted hydrofluoric acid (DHF) or buffer of etching (BOE) etchant containing hydrofluoric acid (HF) and ammonium fluoride (NH₄F), is performed to remove portions of the lining layer 20 exposed by the protective layer 22 in the opening OP. Thus, the gate structure G having a single-sided etched lining layer is formed. In addition, another etching step can optionally be proceeded with RCA1 etchant containing ammonium hydroxide (NH₄OH) and hydrogen peroxide (H₂O₂) to remove portions of the gate conductive layer of the gate structure G, for example the metal silicide layer 16 adjacent to the previously exposed lining layer 20 after the removal thereof. Thus, after removal of the first masking layer 24 and the residue protective layer 22, the gate structure G with single-sided partially etched gate conductive layer is formed.

[0027] At this point, those skilled in the art can adjust the height of the remaining protective layer 22 by controlling the described etching of the protective layer 22 within the opening OP to further expose the polysilicon layer 14 of the
gate conductive layer after removal of the exposed lining layer 20. Thus, exposure of the gate conductive layer can be adjusted and is not restricted to exposure of the previously formed metal silicide layer 16.

[0028] In FIG. 5, a spacer 26 is formed on sidewalls of each gate structure G through conventional deposition and etching-back of insulating materials such as silicon nitride. Each spacer 26 covers the lining layer 20 on sidewalls of the gate structure G and fills in the space created by the previously removed gate conductive layer, such as the metal silicide layer 16. Next, a plurality of doping regions 28 are formed in the silicon substrate 10 on both sides of each gate structure G through the known source/drain ion implantation (not shown) and act as source or drain regions for each gate structure G. Thus, MOSFET devices with single-sided partially etched gate structures G used as a wordline are formed.

[0029] In FIG. 6, a follow-up application of the so-called self-aligned contact (SAC) process relates to the described MOSFET device with single-sided partially etched gate structure G is shown. An inter-layer dielectric (ILD) layer 30, for example a borophosphosilicate glass (BPSG) layer, and a second masking layer 32, for example a photoresist (PR) layer, are sequentially formed over the substrate 10, covering the MOSFET devices thereon. Next, another opening OP is formed through the second masking layer 32 and the ILD layer 30 using conventional photolithography and etching (both not shown). During the formation of the opening OP, portions of the cap layer 18 and the spacer 26 are inevitably removed. Since portions of the gate structure G are partially removed in the previous process, the gate conductive layer in the gate structure G can still be insulated by the spacer 26 and the cap layer 18 in the opening OP and process window thereby extends.

[0030] In FIG. 7, after removal of the second masking layer 32, a bitline contact 34 for connections of follow-up devices such as metal lines (not shown) is formed in the opening OP by depositing and leveling conducting materials. Thus, a so-called self-aligned (SAC) contact is formed.

[0031] Moreover, the photolithography step for forming the described opening OP and OP in first masking layer 24 and second masking layer 32, respectively, is not restricted to conventional photolithography. Nanoimprint lithography (NIL) is also applicable.

[0032] Thus, a semiconductor structures with a partially etched gate in accordance with one embodiment of the present invention is respectively illustrated in FIG. 5 and FIG. 7.

[0033] In FIG. 5, a semiconductor structure with a single-sided partially etched gate comprises a semiconductor substrate (referring to the silicon substrate 10) with a gate structures G formed thereon, wherein the gate structure G is composed of a gate dielectric layer 12, a gate conductive layer (referring to the composite layer of the polysilicon layer 14 and the metal silicide layer 16) and a cap layer 18 stacked on the substrate. A lining layer 20 is disposed on sidewalls of the gate structure G, wherein the lining layer 20 disposed on one sidewall of the gate structure G is partially etched to expose the adjacent gate structure G. Optionally, the exposed gate structure, such as a metal silicide layer 16, can also be partially etched. In addition, a spacer 26 covers sidewalls of the gate structure G and the lining layer 20.

[0034] Thus in FIG. 7, a semiconductor structure with partially etched gate shown in FIG. 5 is provided with a follow-up application further comprises an inter-layer dielectric layer 30 covering the gate structure G. A contact (referring to the bitline contact 34) is formed in the inter-layer dielectric layer 30, exposing the substrate 10 and a portion of the gate structures G therein, wherein the lining layer 20 of the exposed portion of the gate structure G is partially removed.

[0035] A method of fabricating a semiconductor structure with a partially etched gate in accordance with another embodiment of the invention is shown in FIG. 8 through FIG. 16 and an application thereof in the self-aligned contact (SAC) process is also illustrated.

[0036] In FIG. 8, a semiconductor substrate, for example a silicon substrate 10, with two adjacent gate structures G thereon is provided. Each of the gate structures G comprises a gate dielectric layer 12, a polysilicon layer 14, a metal silicide layer 16, and a cap layer 18, sequentially stacked on the silicon substrate 10. A lining layer 20 is formed on the silicon substrate 10, and sidewalls of the polysilicon layer 14 and the metal silicide layer 16. Materials of the gate dielectric layer 12, the polysilicon layer 14, the metal silicide layer 16, the cap layer 18 and the lining layer 20 are preferably silicon dioxide, impurity doped polysilicon, tungsten silicide, silicon nitride, and rapid thermal oxide (RTO). The polysilicon layer 14 and the metal silicide layer 16 comprise a gate conductive layer of the gate structures G.

[0037] In FIG. 9, a protective layer 22 and a first masking layer are sequentially formed over the gate structures G. The protective layer 22 can be, for example, an anti-reflection coating (ARC) layer and materials of the first masking layer can be, for example, photoresist (PR) materials. Next, photolithography (not shown) is performed to pattern the first masking layer and leaves first masking patterns 24 respectively disposed on the position relative to each gate structure G therebelow.

[0038] In FIG. 10, the protective layer 22 exposed by the first masking patterns 24 is then etched to leave portions remained on the lining layer 20. Thus, the lining layer 20 disposed on both sidewalls of each gate structure G is partially exposed.

[0039] Moreover, the processes shown in FIG. 9 and FIG. 10 can be optionally substituted by the processes shown in FIG. 11 and FIG. 12. In FIG. 11, a protective layer 22 is formed over these gate structures G. The protective layer 22 can be, for example, an anti-reflection coating (ARC) layer or a photoresist (PR) layer.

[0040] In FIG. 12, an etching-back process (not shown) is performed to etch the protective layer 22 to leave portions remained on the lining layer 20. Thus, the lining layer 20 disposed on both sidewalls of each gate structure G is partially exposed.

[0041] In FIG. 13, an etching step (not shown), for example wet etching using diluted hydrofluoric acid (DHF) of buffer etching (BOE) etchant containing hydrofluoric acid (HF) and ammonium fluoride (NH₄F), is performed to remove portions of the lining layer 20 exposed by the protective layer 22. Thus, the gate structure G having a dual-sided etched lining layer is formed. In addition, another etching step can optionally be proceeded with RCA1 etchant.
containing ammonium hydroxide (NH₄OH) and hydrogen peroxide (H₂O₂) to remove portions of the gate conductive layer of the gate structure G, for example the metal silicide layer 16 adjacent to the previously exposed lining layer 20 after the removal thereof. Thus, after removal of the first masking layer 24 and/or the residue protective layer 22, the gate structure G with dual-sided partially etched gate conductive layer is formed.

[0042] At this point, those skilled in the art can adjust height of the remaining protective layer 22 by controlling the described etching of the protective layer 22 within the opening OP to further expose the polysilicon layer 14 of the gate conductive layer after the removal of the exposed lining layer 20. Thus, exposure of the gate conductive layer can be adjusted and is not restricted to exposure of the previously formed metal silicide layer 16.

[0043] In FIG. 14, a spacer 26 is formed on sidewalls of each gate structure G through conventional deposition and etching-back of insulating materials such as silicon nitride. Each spacer 26 covers the lining layer 20 on sidewalls of the gate structure G and fills in space created by the previously removed gate conductive layer such as the metal silicide layer 16. Next, a plurality of doping regions 28 are formed in the silicon substrate 10 on both sides of each gate structure G through the known source/drain ion implantation (not shown) and as source or drain regions for each gate structure G. Thus, MOSFET devices with dual-sided partially etched gate structure G used as a wordline are formed.

[0044] In FIG. 15, a follow-up application of the so-called self-aligned contact (SAC) process relating to the described MOSFET device with dual-sided partially etched gate structure G is shown. An inter-layer dielectric (ILD) layer 30, for example borophosphatesilicate glass (BPSG) layer, and a second masking layer 32, for example photosresist (PR) layer, are sequentially formed over the substrate 10, covering the MOSFET devices thereon. Next, an opening OP is formed through the second masking layer 32 and the ILD layer 30 using conventional photolithography and etching (both not shown). During the formation of the opening OP, portions of the cap layer 18 and the spacer 26 are inevitably removed. Since portions of the gate structure G are partially removed in the previous process, the gate conductive layer in the gate structure G can still be insulated by the spacer 26 and the cap layer 18 in the opening OP and process window thereof extends.

[0045] In FIG. 16, after removal of the second masking layer 32, a bitline contact 34 for connections of follow-up devices such as metal lines (not shown) is formed in the opening OP by depositing and leveling of conductive materials. Thus, a so-called self-aligned (SAC) contact is formed.

[0046] Moreover, the photolithography for forming the described opening OP in second masking layer 32 is not restricted to the conventional photolithography. Nanoimprint lithography (NIL) can also be applied.

[0047] Thus, a semiconductor structure with a partially etched gate in accordance with another embodiment of the present invention can be respectively illustrated in FIG. 14 and FIG. 16.

[0048] In FIG. 14, a semiconductor structure with a dual-sided partially etched gate comprises a semiconductor substrate (referring to the silicon substrate 10) with a gate structures G formed thereon, wherein the gate structure G is composed of a gate dielectric layer 12, a gate conductive layer (referring to the composite layer of the polysilicon layer 14 and the metal silicide layer 16) and a cap layer 18 stacked on the substrate. A lining layer 20 is disposed on sidewalls of the gate structure G, wherein the lining layer 20 disposed on both sidewalls of the gate structure G is partially etched to expose the adjacent gate structure G. Optionally, the exposed gate structure, such as a metal silicide layer 16, can also be partially etched. In addition, a spacer 26 covers sidewalls of the gate structure G and the lining layer 20.

[0049] Thus in FIG. 16, a semiconductor structure with a partially etched gate shown in FIG. 14 is provided in a follow-up application further comprising an inter-layer dielectric layer 30 covering the gate structure G. A contact (referring to the bitline contact 34) is formed in the inter-layer dielectric layer 30, exposing the substrate 10 and a portion of the gate structures G therein, wherein the lining layer 20 and the exposed portion of the gate structure G is partially removed.

[0050] The semiconductor structure with single-sided or dual-sided partially etched gates is shown in FIG. 6 and FIG. 15 respectively. During formation of the openings OP of the self-aligned contact (SAC) process, the conductive portions within the partially etched gate structure G can still be protected by the adjacent spacers 26 and will not be revealed. Thus, shorts between the bitline contacts (referring to the bitline contact 34) and the wordlines (referring to the gate structures G) can be avoided.

[0051] In addition, removal of portions of the gate conductive layer in a gate structure can be controlled by the described fabricating methods of the present invention to maintain the sheet resistance of a gate. Moreover, removal of the lining layer adjacent to materials of the gate conductive layer such as a metal silicide layer therein can enlarge the pitch (referring to the distance X shown in FIG. 6 and FIG. 15) between two adjacent gate structures G against the trend of line/pitch shrinking of gate structures. Thus, a larger window for the SAC process can be provided and the so-called “CB open” or “CB to CB short” caused by connections of two bitlines through a poorly formed ILD layer can be prevented. Channel length of the gate structure with partially etched gate can remain the same and will not be affected by the partially etched structure thereof.

[0052] Applications of the SAC process based on the gate conductive layer with a single or dual-sided partially etched gate conductive layer avoids the conventional problems such as CB to WL short, CB open, or CB to CB short. The fabrication method can be slightly modified from in-line processes and can be easily and quickly adopted to the fabrication process.

[0053] While the invention has been described by way of example and in terms of the preferred embodiments, it is to be understood that the invention is not limited to the disclosed embodiments. To the contrary, it is intended to cover various modifications and similar arrangements (as would be apparent to those skilled in the art). Therefore, the scope of the appended claims should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements.
What is claimed is:

1. A method of fabricating a semiconductor structure with partially etched gate, comprising the steps of:
   - providing a semiconductor substrate with at least two adjacent gate structures thereon, wherein each gate structure is composed of a gate dielectric layer, a gate conductive layer, a cap layer, sequentially stacked on the substrate, and a lining layer covered on sidewalls thereof;
   - sequentially forming a protective layer and a masking layer over the gate structures;
   - forming an opening in the masking layer and etching the protective layer thereunder to partially expose the lining layer covering one sidewall of the two adjacent gate structures;
   - removing the exposed lining layers;
   - removing the masking layer and the protective layer; and
   - forming a spacer overlying sidewalls of each gate structure to form a plurality of single-side partially etched gate structures.

2. The method as claimed in claim 1, further comprising, after removing the exposed lining layers, the step of partially removing the gate conductive layer adjacent to the exposed lining layer.

3. The method as claimed in claim 1, further comprising the steps of:
   - forming an inter-layer dielectric layer over the gate structures; and
   - performing photolithography and etching to form a bitline contact in the inter-layer dielectric layer and exposing the substrate and portions of the adjacent gate structures therein.

4. The method as claimed in claim 1, wherein the gate conductive layer is composed of a polysilicon layer and a metal silicide layer.

5. The method as claimed in claim 4, wherein material of the metal silicide layer is tungsten silicide.

6. The method as claimed in claim 1, wherein the protective layer is an anti-reflection coating (ARC) layer.

7. The method as claimed in claim 1, wherein material of the masking layer is photoresist (PR).

8. The method as claimed in claim 1, wherein materials of the cap layer and the spacer are silicon nitride.

9. The method as claimed in claim 1, wherein the lining layer is a rapid thermal oxide (RTO) layer.

10. The method as claimed in claim 4, wherein the gate structure adjacent to the exposed lining layer is the metal silicide layer.

11. The method as claimed in claim 3, wherein the opening is substantially relative to a position of the bitline contact.

12. The method as claimed in claim 3, wherein the method for forming the opening and the bitline contact is nanoimprint lithography (NIL) or photolithography.

13. The method as claimed in claim 1, wherein the reticle for forming the opening is bitline contact node reticle or bitline contact reticle.

14. The method as claimed in claim 1, wherein removal of the exposed lining layer is achieved using diluted hydrofluoric acid (DHF) or buffer of etching (BOE) etchant.

15. The method as claimed in claim 2, wherein partial removal of the gate conductive layer is achieved using of RCA1 etchant.

16. A method of fabricating a semiconductor structure with partially etched gate, comprising the steps of:
   - providing a semiconductor substrate with at least two adjacent gate structures thereon, wherein each gate structure is composed of a gate dielectric layer, a gate conductive layer, a cap layer, sequentially stacked on the substrate, and a lining layer covered on sidewalls thereof;
   - forming a protective layer over the gate structures;
   - etching portions of the protective layer to partially expose the lining layer covering two sidewalls of each gate structure;
   - removing the exposed lining layers;
   - removing the protective layer; and
   - forming a spacer overlying sidewalls of each gate structures to form a plurality of dual-sided partially etched gate structure.

17. The method as claimed in claim 16, further comprising, before removing the partially exposed lining layers, the steps of:
   - forming a masking layer over the protective layer; and
   - forming a plurality of masking patterns in the masking layer, respectively covering the protective layer over the gate structures.

18. The method as claimed in claim 16, further comprising, after removing the exposed lining layers, the step of partially removing the gate conductive layer adjacent to the exposed lining layers.

19. The method as claimed in claim 16, further comprising the steps of:
   - forming an inter-layer dielectric (ILD) layer over the gate structures; and
   - performing photolithography and etching to form a bitline contact in the inter-layer dielectric layer and exposing the substrate and portions of the adjacent gate structures therein.

20. The method as claimed in claim 16, wherein the gate conductive layer is composed of a polysilicon layer and a metal silicide layer.

21. The method as claimed in claim 16, wherein materials of the protective layer are an anti-reflection coating (ARC) and photoresist (PR).

22. The method as claimed in claim 16, wherein the protective layer is an anti-reflection coating (ARC) layer and the masking layer is a photoresist (PR) layer.

23. The method as claimed in claim 16, wherein materials of the cap layer and the spacer are silicon nitride.

24. The method as claimed in claim 19, wherein the gate structure adjacent to the exposed lining layer is the metal silicide layer.

25. The method as claimed in claim 16, wherein removal of the exposed lining layer is achieved using diluted hydrofluoric acid (DHF) or buffer of etching (BOE) etchant.

26. The method as claimed in claim 18, wherein partially removing the gate conductive layer is achieved using RCA1 solution containing ammonium hydroxide (NH$_4$OH) and hydrogen peroxide (H$_2$O$_2$).