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(54) **QUASI SELF-ALIGNED SOURCE/DRAIN FINFET PROCESS**

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(57) **ABSTRACT**

A method of forming a semiconductor structure including a plurality of finFFET devices in which crossing masks are employed in providing a rectangular patterns to define relatively thin Fins along with a chemical oxide removal (COR) process is provided. The present method further includes a step of merging adjacent Fins by the use of a selective silicon-containing material. The present invention also relates to the resultant semiconductor structure that is formed utilizing the method of the present invention.

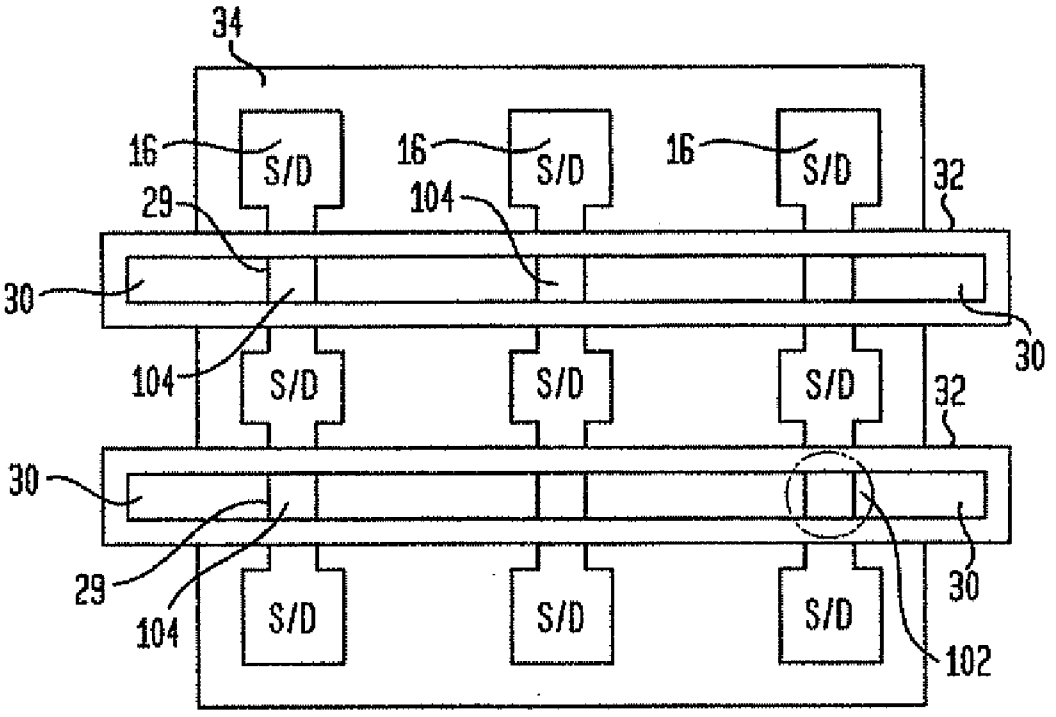

FIG. 1A

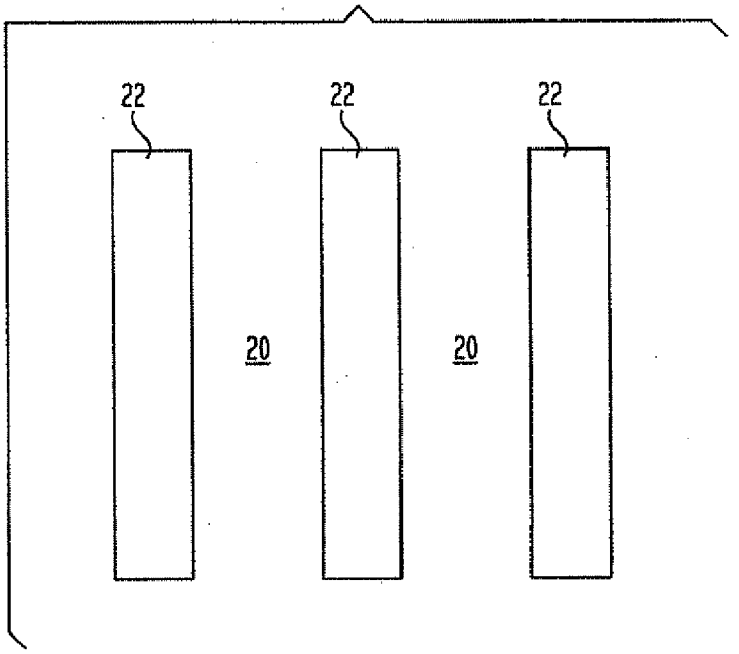

FIG. 1B

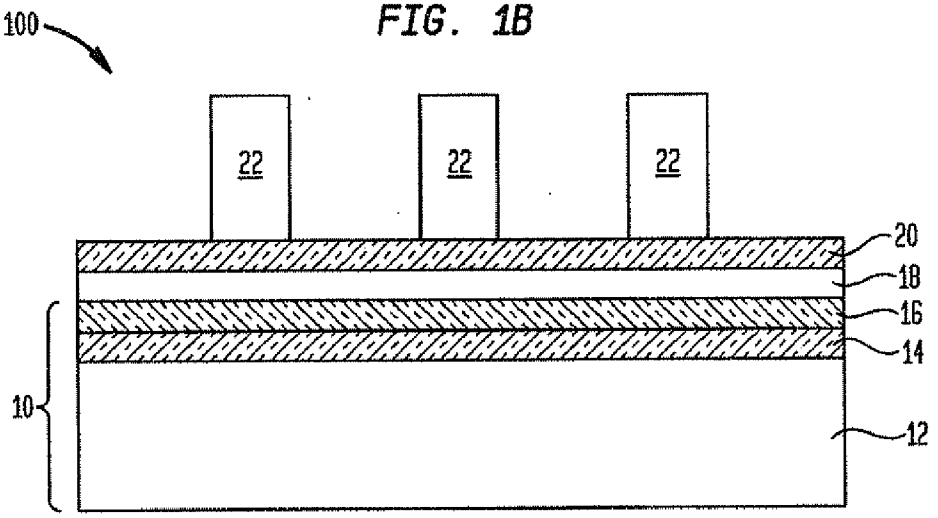

FIG. 2

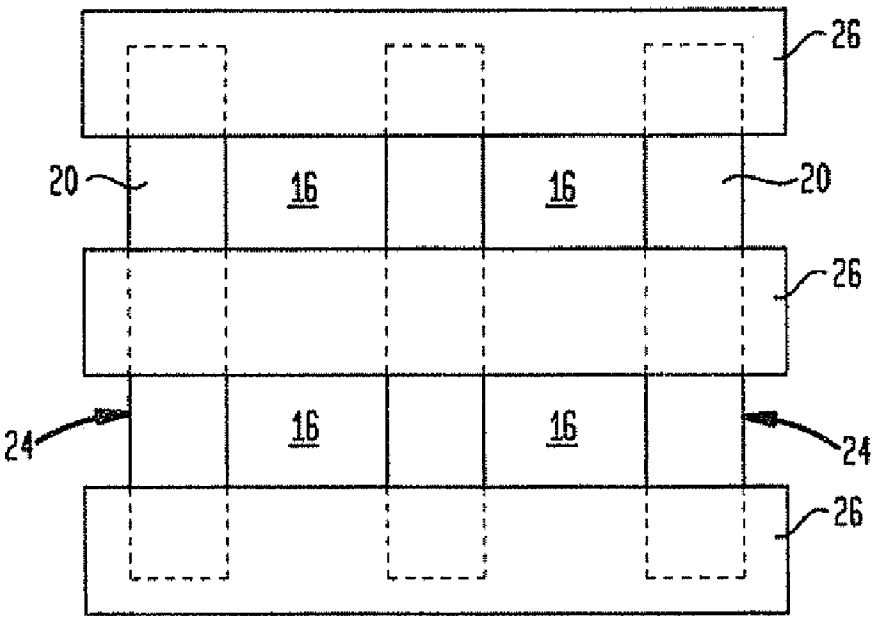
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FIG. 3

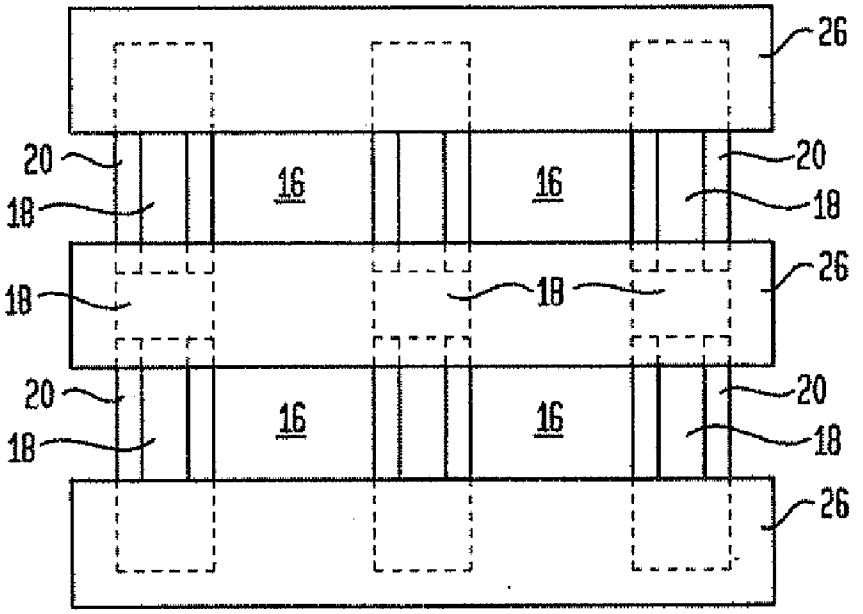
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FIG. 4

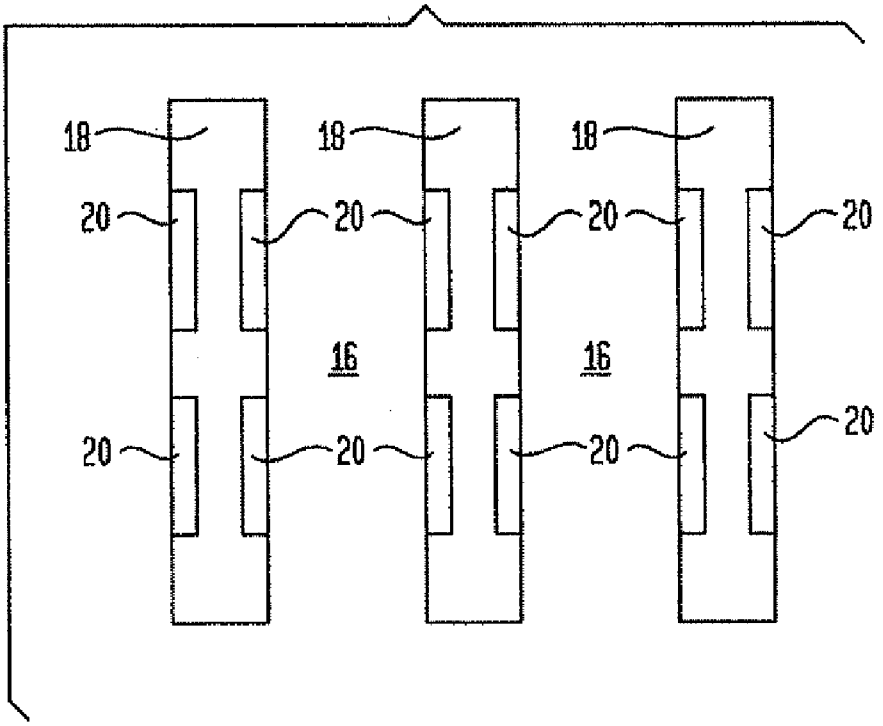


FIG. 5

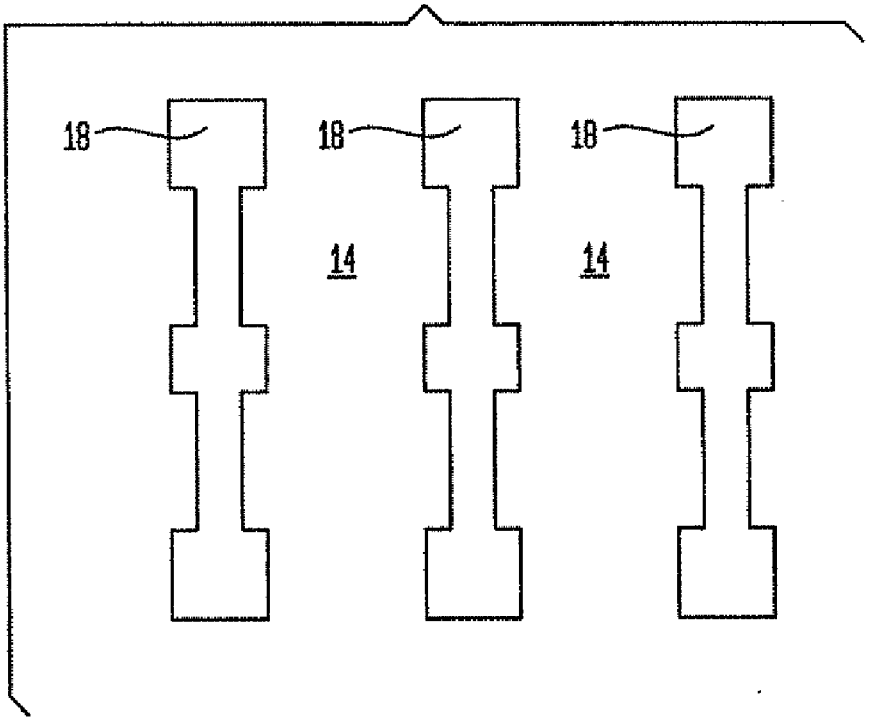


FIG. 6

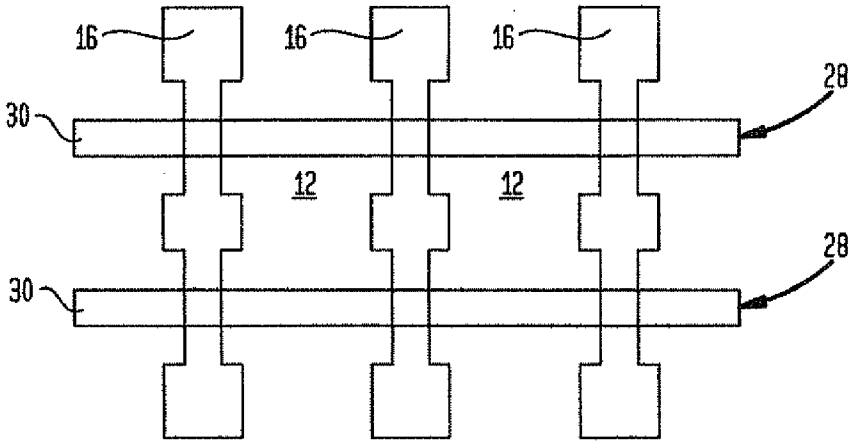


FIG. 7

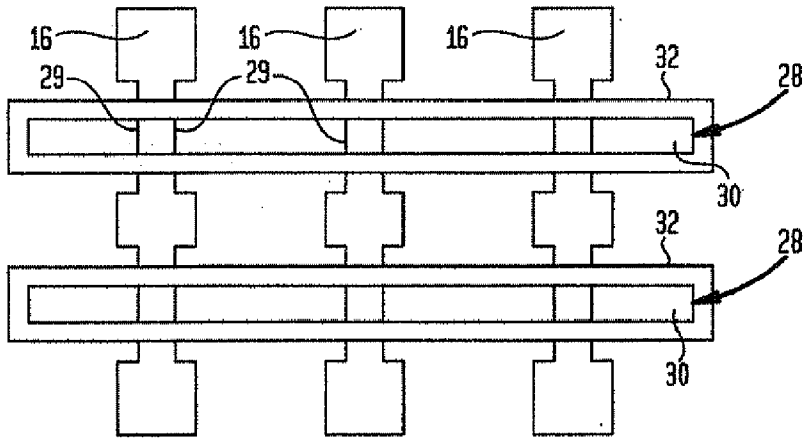
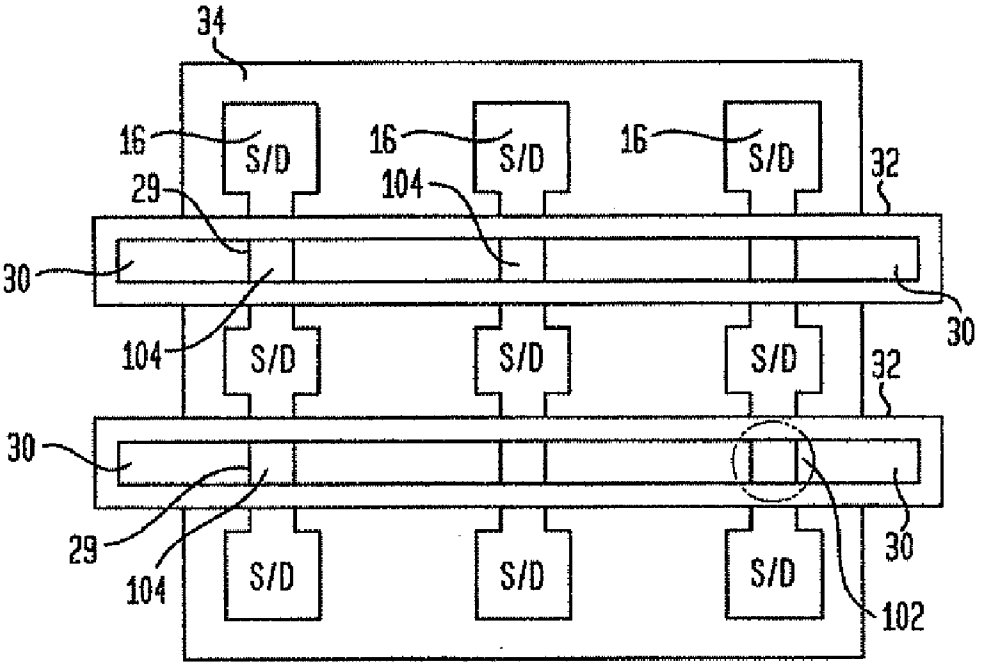


FIG. 8


34
16
S/D
16
S/D
16
S/D
32
29
104
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30
104
S/D
S/D
S/D
32
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29
104
S/D
S/D
S/D
30
102

QUASI SELF-ALIGNED SOURCE/DRAIN FINFET PROCESS

RELATED APPLICATION

[0001] This application is a divisional application of U.S. patent application Ser. No. 11/164,215, filed Nov. 15, 2005.

DESCRIPTION

[0002] 1. Field of the Invention

[0003] The present invention relates to semiconductor device processing, and more particularly to a method of forming a semiconductor structure that includes at least multiple FinFET devices in which a single mask is used in defining the Fins, which avoids rounding of the corners where the Fins join the source/drain regions. The term "Fin" is used throughout this application to denote an elevated portion of a semiconducting layer of a semiconductor substrate that includes at least the device channel in which the width thereof is less than its height. The present invention is also related to the semiconductor structure including the multiple FinFET devices that is fabricated using the inventive method.

[0004] 2. Background of the Invention

[0005] The dimensions of semiconductor field effect transistors (FETs) have been steadily shrinking over the last thirty 30 years or so, as scaling to smaller dimensions leads to continuing device performance improvements. Planar FET devices have a conducting gate electrode positioned above a semiconducting channel, and electrically isolated from the channel by a thin layer of gate oxide. Current through the channel is controlled by applying voltage to the conducting gate.

[0006] For a given device length, the amount of current drive for an FET is defined by the device width (w). Current drive scales proportionally to device width, with wider devices carrying more current than narrower devices. Different parts of integrated circuits (ICs) require the FETs to drive different amounts of current, i.e., with different device widths, which is particularly easy to accommodate in planar FET devices by merely changing the device gate width (via lithography).

[0007] With conventional planar FET scaling reaching fundamental limits, the semiconductor industry is looking at more unconventional geometries that will facilitate continued device performance improvements. One such class of devices is a FinFET.

[0008] A FinFET is a double gate FET in which the device channel is within a semiconducting "Fin" having a width w and height h, where typically w<h. The gate dielectric and gate are positioned around the Fin such that charge flows down the channel on the two sides of the Fin and optionally along the top surface.

[0009] FinFET devices typically include a fully depleted body in the Fin that provides several advantages over a conventional FET. These advantages include, for example, nearly ideal turn off in the sub-threshold regime, giving lower off-currents and/or allowing lower threshold voltages, no loss to drain currents from body effects, no 'floating' body effects (often associated with some silicon-on-insulator (SOI) FETs), higher current density, lower voltage operation, and reduced short channel degradation of threshold voltage and off current. Furthermore, FinFETs are more easily scaled to smaller physical dimensions and lower operating voltages than conventional FETs and SOI FETs.

[0010] Definition of both the semiconducting Fins and the source/drain regions by a single mask has been extremely difficult in the prior art due to rounding of the corners where the Fins join the wide source/drain areas. As a result, there is neither room for alignment of the gate to the active semiconducting material, nor room for extension implants into the sidewalls of the Fins.

[0011] A mask to separately pattern source and drain regions of silicon to link the Fins provides a solution for the rounding problem, but adds an extra overlay for added mask to the Fins, leaving little room for extension implants between the source and drain linking regions and the gate electrode, unless the registration of the various masks is nearly perfect.

[0012] In view of the above, there is a need for providing a method that can define both the Fins and the source/drain regions by a single mask that avoids the rounding problem mentioned above as well as the need for using additional overlays.

SUMMARY OF THE INVENTION

[0013] The present invention provides a method that overcomes the above mentioned problems using simple rectangular shapes to define the Fins which avoid rounding and yet joins the Fins by a deposition of a selective silicon-containing material post gate etch. More specifically, the present invention provides a method of forming a semiconductor structure including a plurality of FinFET devices in which crossing masks are employed in providing linear patterns to define relatively thin Fins along with a chemical oxide removal (COR) process. The present method further includes a step of merging adjacent Fins by the use of a selective silicon-containing material.

[0014] In general terms, the present invention provides a method that includes the steps of:

[0015] providing a structure including a plurality of patterned material stacks comprising a nitride layer on top of an oxide hardmask on a surface of semiconductor substrate and a plurality of patterned photomasks which cross over said plurality of patterned material stacks;

performing a chemical oxide removal step that laterally etches at least exposes sidewalls of said oxide hardmask of each material stack not protected by one of said patterned photomasks;

removing the plurality of patterned photomasks to expose patterned material stacks including a laterally etched oxide hardmask beneath said nitride layer;

[0016] performing an anisotropic etching process selective to the laterally etched oxide hardmask to remove said nitride layer and at least an upper portion of any semiconducting material of said semiconductor substrate not protected by said laterally etched oxide hardmask to form Fins; and

forming a plurality of gate regions that cross over said Fins.

[0017] Optionally, the laterally etched oxide hardmask is removed by exposing upper portions of the semiconducting

material of the semiconductor substrate previously protected by said laterally etched oxide hardmask, wherein portions of said exposed upper portions of the semiconducting material of the semiconductor substrate previously protected by said laterally etched oxide hardmask define the Fins.

[0018] Each of the Fins produced by the inventive method are then merged by forming a Si-containing material between each of the Fins. The Si-containing material prevents rounding of corners of each Fin with their corresponding source/drain region. The source/drain regions are located within wider end portions of each Fin that where previously protected by said plurality of patterned masks that cross over said plurality of patterned stacks. The wider end portions of each Fin are substantially square; i.e., little or no rounding of the corners of the wider end portions occurs in the present invention.

[0019] The present invention also relates to the semiconductor structure that is fabricated using the above processing steps. In general terms, the semiconductor structure of the present invention comprises.

[0020] a plurality of FinFET devices located on a surface of a semiconductor substrate, each of said FinFET devices including an elevated semiconducting layer that has wider end portions relative to its middle portion, a gate region that crosses said middle portion, and source/drain regions within said wider end portions; and

a Si-containing material located between said elevated semiconducting layer that joins each elevated semiconducting layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0021] FIG. **1**A is a pictorial representation (through a top-down view) and FIG. **1**B is a pictorial representation (through a cross-sectional view) showing a plurality of first patterned photomasks located over a structure including (from bottom to top) a semiconductor substrate, an oxide hardmask and a nitride layer.

[0022] FIG. **2** is a pictorial representation (through a top-down view) showing the structure of FIG. **1** after etching exposed regions of the nitride layer and the oxide layer stopping on an upper surface of the semiconductor substrate, removing the plurality of first patterned photomasks and forming a plurality of second patterned photomasks that lay across stripes of stacked oxide/nitride layers.

[0023] FIG. **3** is a pictorial representation (through a top-down view) showing the structure of FIG. **2** after performing a chemical oxide removal (COR) process which etches exposed sidewalls of the oxide hardmask to a desired distance undercutting both the nitride layer and the second patterned photoresist masks by the distance.

[0024] FIG. **4** is a pictorial representation (through a top-down view) showing the structure of FIG. **3** after removing the second patterned photoresist masks; an undercut oxide layer pattern is illustrated, although cover by the nitride layer.

[0025] FIG. **5** is a pictorial representation (through a top-down view) showing the structure of FIG. **4** after performing an anisotropic etch that is selective to the oxide layer, stopping within the semiconductor substrate, e.g., on a buried insulator layer within the substrate.

[0026] FIG. **6** is a pictorial representation (through a top-down view) showing the structure of FIG. **5** after forming a gate region including a gate dielectric and a gate electrode.

[0027] FIG. **7** is a pictorial representation (through a top-down view) showing the structure of FIG. **6** after spacer formation.

[0028] FIG. **8** is a pictorial representation (through a top-down view) showing the structure of FIG. **7** after selectively forming a Si-containing layer on exposed sidewalls of the substrate.

DETAILED DESCRIPTION OF THE INVENTION

[0029] The present invention, which provides a method of fabricating a semiconductor structure that includes at least multiple FinFET devices in which a single mask is used in defining the Fins as well as the resultant semiconductor structure, will now be described in greater detail by referring to the following discussion and drawings that accompany the present application. It is noted that the drawings of the present application are provided for illustrative purposes and, as such, they are not drawn to scale.

[0030] Reference will be made to FIGS. **1-8** which illustrate an embodiment in which a semiconductor-on-insulator (SOI) substrate is used. Although an SOI substrate is depicted and described in the following discussion, the present invention also contemplates utilizing a bulk semiconductor substrate. When a bulk semiconductor substrate is used, the bulk semiconductor substrate comprises one of Si, Ge alloys, SiGe, GaAs, InAs, InP, SiCGe, SiC as well as other III/V or II/VI compound semiconductors. Preferably, and when a bulk semiconductor is employed, the substrate includes a Si-containing semiconducting material, with Si being highly preferred.

[0031] As indicated above, the processing description provided herein utilizes an SOI substrate. An SOI substrate includes a bottom semiconductor layer and a top semiconductor layer (i.e., active semiconductor layer) that are electrically isolated from each other by a buried insulating layer. The top and bottom semiconductor layers may comprise one of the above mentioned bulk semiconductor materials, with Si-containing semiconductors, preferably, Si being highly preferred. The buried insulating material separating the two semiconducting layers may be a crystalline or non-crystalline oxide or nitride, with crystalline oxides being highly preferred. It is noted that SOI substrates are preferred over bulk substrates since they permit formation of devices having higher operating speeds. In particular, devices formed using SOI technology provide higher performance, absence of latch-up, higher packaging density and low voltage applications as compared with their bulk semiconductor counterparts.

[0032] The SOI substrate employed in the present invention may be formed utilizing conventional processing techniques well known in the art. For example, a layer transfer process including a bonding step can be used in providing the SOI substrate. Alternatively, an implantation process such as SIMOX (Separation by IMplantation of OXygen) can be used in forming the SOI substrate.

[0033] The thickness of the various layers of the SOI substrate may vary depending on the technique used in

forming the same. Typically, however, the top semiconductor layer has a thickness from about 3 to about 10 nm, the buried insulating layer has a thickness from about 10 to about 150 nm, and the thickness of the bottom semiconductor layer of the SOI substrate is inconsequential to the present invention.

[0034] Reference is now made to FIG. **1**B which is a pictorial representation (through a cross-sectional view) showing a plurality of first patterned photomasks **22** located over a structure **100** including (from bottom to top) an SOI semiconductor substrate **10**, an oxide hardmask **18** and a nitride layer **20**. As stated above, the SOI substrate **10** includes a bottom semiconductor layer **12**, a buried insulating layer **14** and a top semiconductor layer **16**. A top-down view of structure **100** is shown in FIG. **1**A. In the top-down views provided in the present application, only the patterned regions are highlighted.

[0035] The structure **100** is formed by first providing an SOI substrate (or bulk semiconductor substrate) by conventional techniques. Next, the oxide hardmask **18** is formed on the upper surface of the substrate, e.g., the upper surface of the top semiconductor layer **16**, utilizing a conventional deposition process such as, for example, chemical vapor deposition (CVD), plasma enhanced chemical vapor deposition (PECVD), atomic layer deposition (ALD), physical vapor deposition (PVD), evaporation, chemical solution deposition and other like deposition processes. Alternatively, the oxide hardmask **18** is formed utilizing a conventional oxidation process. The thickness of the oxide hardmask **18** formed at this point of the present invention may vary depending on the technique that was used in forming the same. Typically, the thickness of the oxide hardmask **18** employed in the present invention is from about 1 to about 50 nm, with a thickness from about 2 to about 30 nm being even more typical.

[0036] Following the formation of the oxide hardmask **18**, a nitride layer **20** such as Si_3N_4 is formed atop the oxide hardmask **18**. The nitride layer **20** can be formed utilizing a conventional deposition process such as CVD, PECVD, ALD, PVD, evaporation, chemical solution deposition or and other like deposition processes. Alternatively, the nitride layer **20** is formed utilizing a conventional nitridation process. The thickness of the nitride layer **20** formed at this point of the present invention may vary depending on the technique that was used in forming the same. Typically, the thickness of the nitride layer **20** employed in the present invention is from about 1 to about 20 nm, with a thickness from about 1.5 to about 4 nm being even more typical.

[0037] After nitride layer **20** formation, a blanket layer of photoresist material is deposited on the surface of the nitride layer **20** utilizing a conventional deposition process such as, for example, CVD, PECVD, evaporation or spin-on coating. The blanket layer of photoresist material is patterned into a plurality of first patterned photomasks **22** as shown in FIGS. **1**A and **1**B. Patterning of the photoresist material is achieved by utilizing a conventional lithographic process which includes exposing the photoresist material to a pattern of radiation and developing the exposed photoresist material utilizing a conventional resist developer.

[0038] To better highlight the inventive method, the fabrication process will make reference to top-down views from now on. With the plurality of first patterned photomasks **22** in place, the exposed nitride layer **20** and the underlying oxide hardmask **18** are removed from the structure **100** utilizing one or more etching processes. The one or more etching processes remove the unprotected portions of layers **20** and **18**, stopping on an upper surface of the SOI substrate **10**, i.e., atop the top semiconductor layer **16**. The one or more etching processes may include dry etching or wet etching. Preferably, dry etching such as reactive-ion etching (RIE) is used. Other examples of dry etching that can be used at this point of the present invention include ion beam etching, plasma etching or laser ablation.

[0039] After the one or more etching processes have been performed, the plurality of first patterned photomasks **22** are removed utilizing a conventional resist stripping process. The structure at this point of the present invention includes a plurality of material stacks **24** containing remaining portions of nitride layer **20** and oxide hardmask **18** on the SOI substrate **10**.

[0040] A plurality of second photomasks **26** is then formed so as to cross stripes of material stacks **24**. That is, the plurality of second photomasks **26** is formed such that each of the second photomasks **26** lay across the material stacks **24**. The plurality of second photomasks **26** are formed by first applying a second blanket photoresist material to the structure shown in FIGS. **1**A and **1**B and then subjecting that blanket photoresist layer to lithography. The area between the second photomasks, particularly the underlying top semiconductor layer **16** of the SOI substrate **10**, represents the location wherein the Fins of each FinFET device will be formed.

[0041] The structure including the plurality of second photomasks **26** and the material stacks **24** is shown in FIG. **2**. Note, that the plurality of second photomasks **26** protect some portions of the material stacks **24** as well as the adjacent SOI substrate **10**, e.g., the top semiconductor layer **18**.

[0042] The resultant structure shown in FIG. **2** is then subjected to a chemical oxide removal (COR) process. The COR process selectively etches (in a lateral direction) exposed vertical surfaces of the oxide hardmask **18** of each material stack **24** undercutting both the overlying nitride layer **20** and each of the second photomasks **26**. The lateral etch is performed to a predetermined distance of from about 5 to about 40 nm, which distance is substantially the same for the undercuts as well. FIG. **3** shows the structure after the COR process. Note that in FIG. **3** and FIG. **4** the pattern formed in the underlying oxide hardmask **18** is shown to emphasize the COR processing step of the present invention. Although the patterned oxide hardmask **18** is shown in these drawings of the present invention, nitride layer **20** remains atop the patterned hardmask **18** at these two stages of the present invention.

[0043] The COR process used in providing the structure shown in FIG. **3** comprises exposing the structure of FIG. **2** to a gaseous or vaporous mixture of HF and ammonia at a pressure of about 30 mTorr or below, preferably at a pressure from about 1 mTorr to about 30 mTorr. The COR process is typically performed at a temperature that is about nominal room temperature (20° C. to about 40° C.), with a temperature of about 25° C. being even more typical. The ratio of HF to ammonia employed in the COR process is typically from about 1:10 to about 10:1, with a ratio of about 2:1 being even more typical.

[0044] After performing the COR process, the plurality of second photomasks **26** are removed from the structure utilizing a conventional resist stripping processing step. FIG. **4** shows the resultant structure that is formed after the plurality of second photomasks **26** are removed from the structure. In this drawing, the undercut oxide layer **18** is again illustrated, although covered by nitride layer **20**.

[0045] An anisotropic Si etch, selective to the remaining oxide hardmask **18**, is used to remove the remaining nitride layer **20** as well as exposed top semiconductor layer **16** of SOI substrate **10**, stopping on buried insulating layer **14**. When a bulk substrate is used, this etch thins the substrate to a predetermined value. An example of an anisotropic Si etch that can be used at this point of the present invention includes reactive-ion etching with a fluorocarbon chemistry, such as CF_4. The resultant structure is shown, for example, in FIG. **5**. In FIG. **5**, oxide hardmask **18** remains, and buried insulating layer **14** is exposed. It is emphasized that the top semiconductor layer **16** underlying the patterned oxide hardmask **18** will now have the same pattern as layer **18**.

[0046] The remaining oxide hardmask **18** can be removed in one embodiments in which case the top surface of the Fin will become part of the FinFET channel once the structure is complete. Specifically, an etching process selective to the semiconducting material can be used to optionally remove the remaining oxide hardmask **18**. In the drawings, the remaining oxide hardmask **18** is shown as being removed from the structure. Although this is illustrated, the present invention also contemplates embodiments where the remaining oxide hardmask **18** remains in the structure during the following processing steps.

[0047] In some embodiments of the present invention, the patterned semiconductor layer **16** may need to be ion implanted at this point of the present invention. When ion implantation is needed, a conventional ion implantation process can be used to implant dopant ions (p- or n-type) into the patterned top semiconducting layer **16**.

[0048] FIG. **6** shows the structure of FIG. **5** forming a gate region **28** that includes a gate dielectric (not shown in this drawing of the present invention) and an overlying gate electrode **30**. The gate dielectric is formed first, followed by the gate electrode. Specifically, the gate dielectric is formed by first providing a sacrificial oxide (not shown) on the structure and then stripping the sacrificial oxide to remove imperfections in the structure. The gate dielectric is then formed by a thermal growth process such as, for example, oxidation, nitridation or oxynitridation. Alternatively, the gate dielectric can be formed by a deposition process such as, for example, chemical vapor deposition (CVD), plasma-assisted CVD, metalorganic chemical vapor deposition (MOCVD), atomic layer deposition (ALD), evaporation, reactive sputtering, chemical solution deposition and other like deposition processes. The gate dielectric may also be formed utilizing any combination of the above processes.

[0049] The gate dielectric is comprised of an insulating material having a dielectric constant of about 4.0 or greater, preferably greater than 7.0. The dielectric constants mentioned herein are relative to a vacuum. Note that SiO_2 typically has a dielectric constant that is about 4.0. Specifically, the gate dielectric employed in the present invention includes, but is not limited to: an oxide, nitride, oxynitride and/or silicates including metal silicates, aluminates, titanates and nitrides. In one embodiment, it is preferred that the gate dielectric is comprised of an oxide such as, for example, SiO_2, HfO_2, ZrO_2, Al_2O_3, TiO_2, La_2O_3, $SrTiO_3$, $LaAlO_3$, Y_2O_3 and mixtures thereof.

[0050] The physical thickness of the gate dielectric may vary, but typically, the gate dielectric has a thickness from about 1 to about 10 nm, with a thickness from about 1 to about 3 nm being more typical.

[0051] After forming the gate dielectric, a blanket layer of a conductive material which forms the gate electrode **30** of gate region **28** is formed on the gate dielectric utilizing a known deposition process such as physical vapor deposition (PVD), CVD or evaporation. The conductive material may comprise polysilicon, SiGe, a silicide, a metal or a metal-silicon-nitride such as Ta—Si—N. Examples of metals that can be used as the conductive material include, but are not limited to: Al, W, Cu, Ti or other like conductive metals. The blanket layer of conductive material may be doped or undoped. If doped, an in-situ doping deposition process may be employed. Alternatively, a doped conductive material can be formed by deposition, ion implantation and annealing.

[0052] The doping of the conductive material will shift the workfunction of the gate formed. Illustrative examples of doping ions include As, P, B, Sb, Bi, In, Al, Tl, Ga or mixtures thereof. The thickness, i.e., height, of the conductive material deposited at this point of the present invention may vary depending on the deposition process employed. Typically, the conductive material has a vertical thickness from about 20 to about 180 nm, with a thickness from about 40 to about 150 nm being more typical.

[0053] In some embodiments, an optional hardmask (not shown) may be formed atop the conductive material utilizing a conventional deposition process. The optional hardmask can be comprised of a dielectric such as an oxide or nitride.

[0054] After deposition of at least the gate dielectric and the conductive material, gate regions **28** including gate electrode **30** are formed. Specifically, the gate regions **28** are formed by first providing a patterned mask atop the conductive material by deposition and lithography and then transferring the pattern to the conductive material and optional the gate dielectric. The etching steps comprise one or more etching processes including dry etching such as RIE. It is noted that the region of patterned semiconductor **16** in which the gates cross over is the channel region of the Fin. The Fin is an elevated semiconductor layer **16** that includes wider end portions connected by a thinner middle portion as is shown in FIGS. **6-8**. It is observed that the patterned semiconductor layer **16** has a dumb bell or dog bone shape in which the outer, wider end portions are substantially square due to the processing steps of the present invention.

[0055] Next, source/drain extension regions (not shown) and/or halo regions (not shown) are formed into the semiconductor substrate utilizing conventional implantation processes well known to those skilled in the art.

[0056] Next, a gate spacer **32** comprising an oxide, nitride, oxynitride or combination thereof is formed around the

perimeter of the gate region **28** as is shown, for example, in FIG. **7**. The gate spacer **32** is formed by a conventional deposition process such as, for example, CVD or PECVD, followed by a directional etching process. It is noted that the gate dielectric is shown in this drawing and FIG. **8** to illustrate its position relative to the channel portion of the Fin; reference numeral **29** denotes the gate dielectric surrounding the channel position of the Fin.

[**0057**] Next, and as shown in FIG. **8**, a single crystalline Si-containing material **34** such as Si, SiGe or SiGeC is selectively grown from the exposed sidewalls of the top semiconductor layer **16** of the SOI substrate **10**. The single crystalline Si-containing material **34** is formed by CVD, PECVD or an UHVCV process. Source/drain regions (the term 'S/D' is used in FIG. **8** to represent the location of the source/drain regions) are then implanted into wider portion of the semiconductor material **16** adjoining each Fin utilizing conventional ion implantation techniques well known in the art.

[**0058**] The above processing steps provide a semiconductor structure such as shown in FIG. **8** that includes at least multiple FinFET devices **102** in which a single mask is used in defining the Fins **104** which avoids rounding of the corners where the Fins **104** join the source/drain regions.

[**0059**] While the present invention has been particularly shown and described with respect to preferred embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in forms and details may be made without departing from the spirit and scope of the present invention. It is therefore intended that the present invention not be limited to the exact forms and details described and illustrated, but fall within the scope of the appended claims.

What is claimed is:

1. A semiconductor structure comprising:

a plurality of FinFET devices located on a surface of a semiconductor substrate, each of said FinFET including an elevated semiconducting layer that has wider end portions relative to its middle portion, a gate region that crosses said middle portion, and source/drain regions within said wider end portions; and

a Si-containing material located between said elevated semiconducting layer which joins each elevated semiconducting layer.

2. The semiconductor structure of claim 1 wherein said elevated semiconducting layer is a top semiconducting layer of an SOI substrate, said SOI substrate including a buried insulating layer that is patterned or unpatterned and an unpatterned bottom semiconducting layer.

3. The semiconductor structure of claim 2 wherein said elevated semiconducting layer is a Si-containing semiconductor and said buried insulating layer is an oxide.

4. The semiconductor structure of claim 1 wherein each gate region comprises a gate dielectric and a gate electrode.

5. The semiconductor structure of claim 1 further comprising a gate spacer located around each gate region.

6. The semiconductor structure of claim 1 wherein said elevated semiconducting layer is an upper surface layer of a bulk semiconductor substrate.

7. The semiconductor structure of claim 1 wherein said Si-containing material comprises one of single crystalline Si, SiGe or SiGeC.

8. The semiconductor structure of claim 1 wherein said end portions of the elevated semiconducting layer are substantially square.

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