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(54) DATA RECOVERY USING DATA EYE TRACKING

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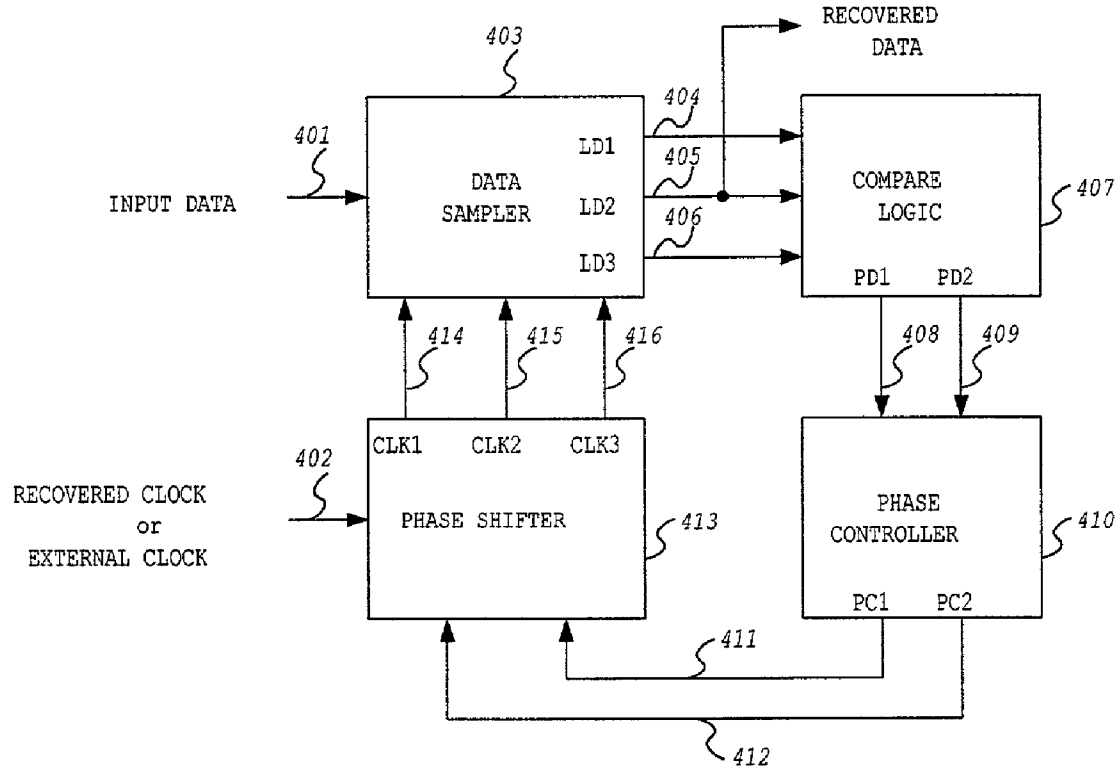
(57) ABSTRACT

A data recovery system for a serial digital data link includes a data sampler, compare logic, a phase controller, and a phase shifter. The data sampler samples input data three times in a bit time which time is determined by clock pulses generated by the phase shifter, and recovers digital data according to a predetermined decision criterion. Data sampling phases are split so as to track the data eye. The compare logic compares the output of the data sampler according to a predetermined method. Phase controller uses the output of the compare logic and generates phase control signals. These signals are set so as to control the sampling times of the data sampler and to attain near optimally recovered data stream. The phase shifter uses the phase control signals and makes three different phase clocks from input clock. The input clock can be an external clock, or can be recovered from the external clock or input data stream.



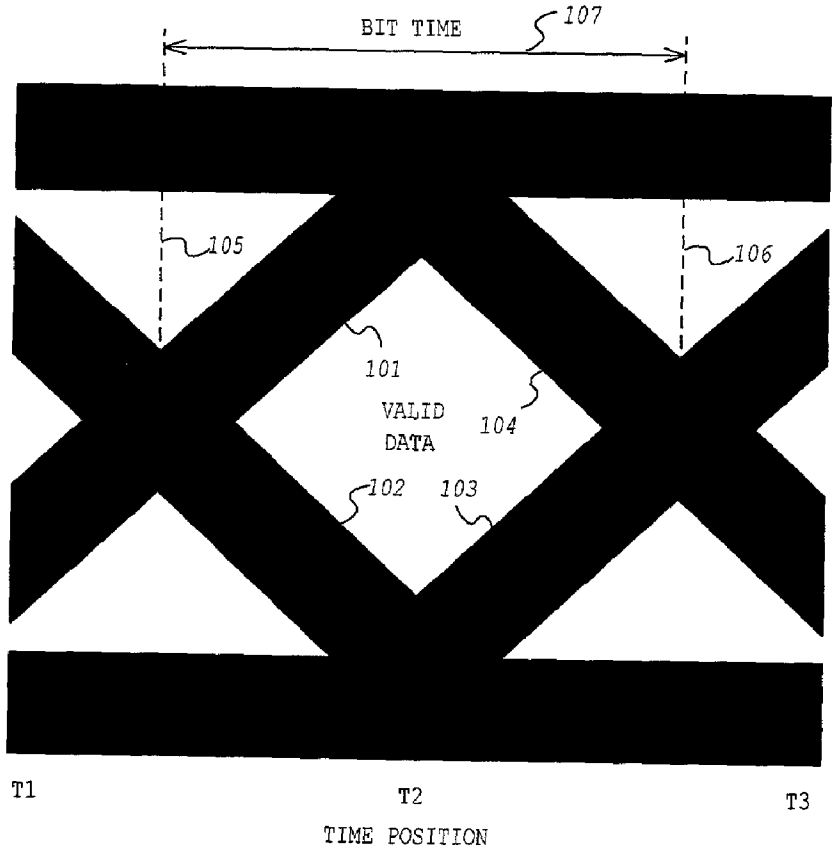

BIT TIME
107
105
106
101
VALID
DATA
104
102
103
T1
T2
T3
TIME POSITION

FIG. 1

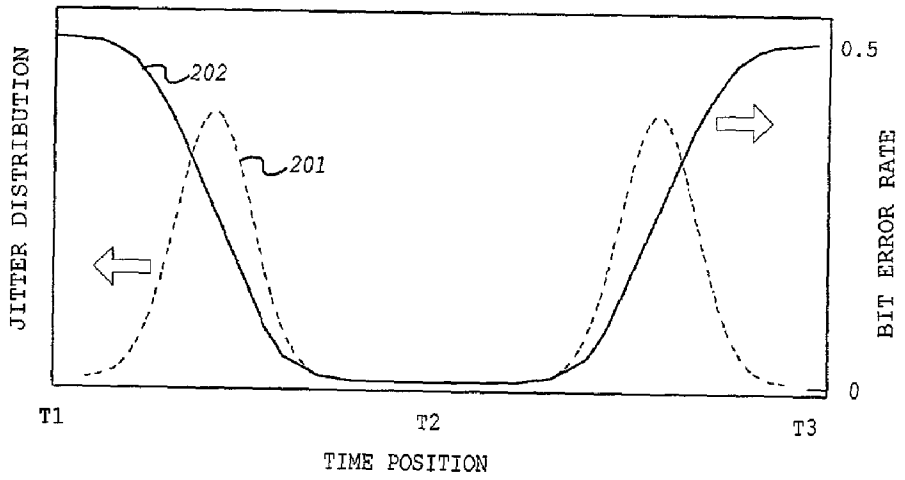

JITTER DISTRIBUTION
202
201
0.5
0
BIT ERROR RATE
T1
T2
T3
TIME POSITION

FIG. 2

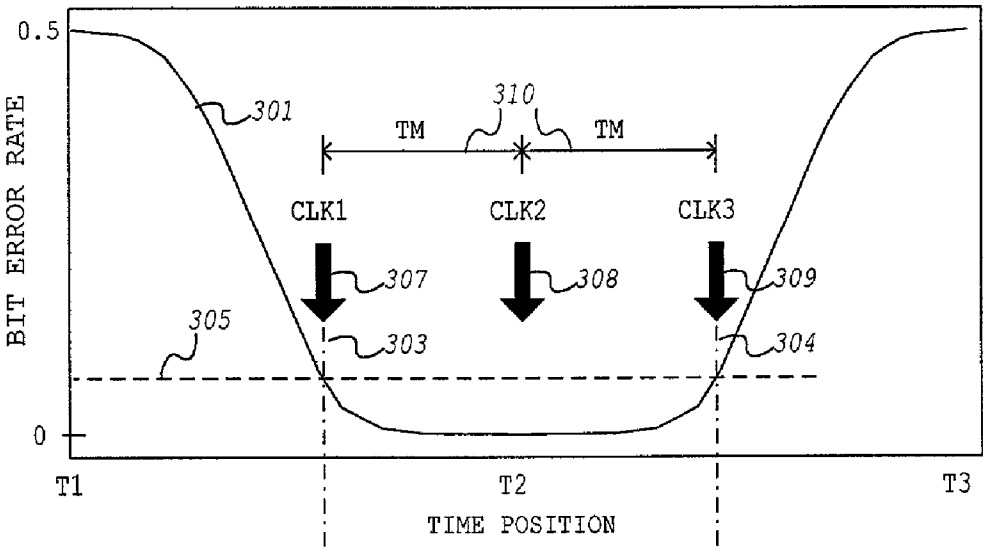

0.5
BIT ERROR RATE
0
301
310
TM
TM
CLK1
CLK2
CLK3
307
308
309
305
303
304
T1
T2
T3
TIME POSITION

FIG. 3a

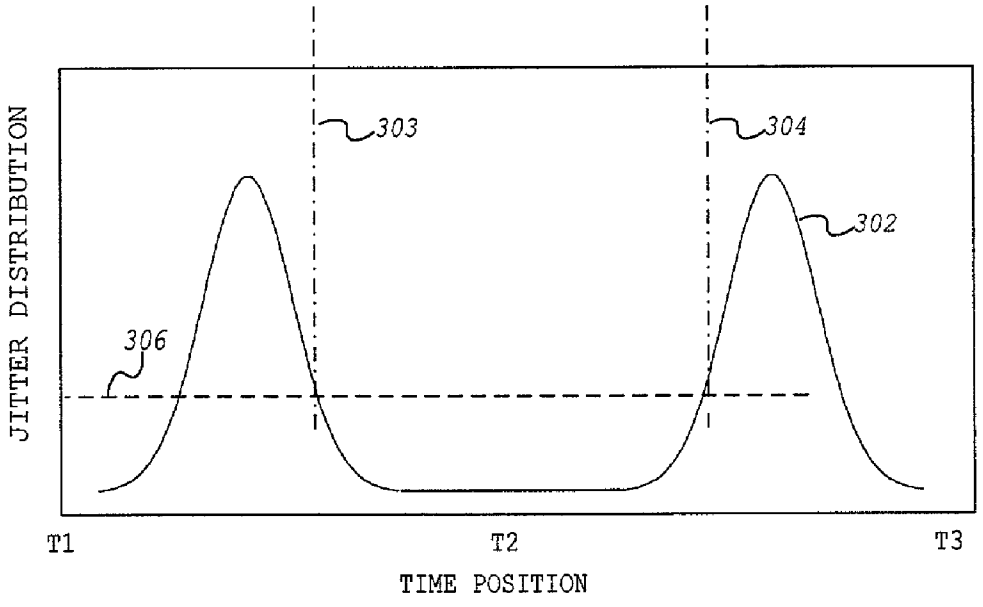

JITTER DISTRIBUTION
303
304
302
306
T1
T2
T3
TIME POSITION

FIG. 3b

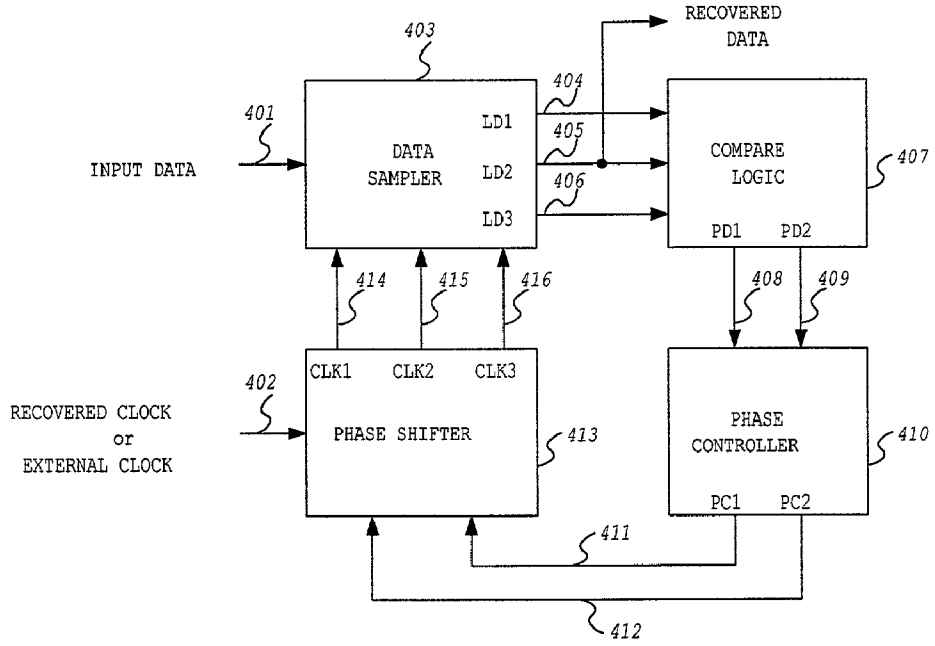

RECOVERED DATA
403
404
401
LD1
405
INPUT DATA
DATA SAMPLER
LD2
406
COMPARE LOGIC
407
LD3
PD1 PD2
414
415
416
408
409
CLK1 CLK2 CLK3
402
RECOVERED CLOCK or EXTERNAL CLOCK
PHASE SHIFTER
413
PHASE CONTROLLER
410
PC1 PC2
411
412

FIG. 4

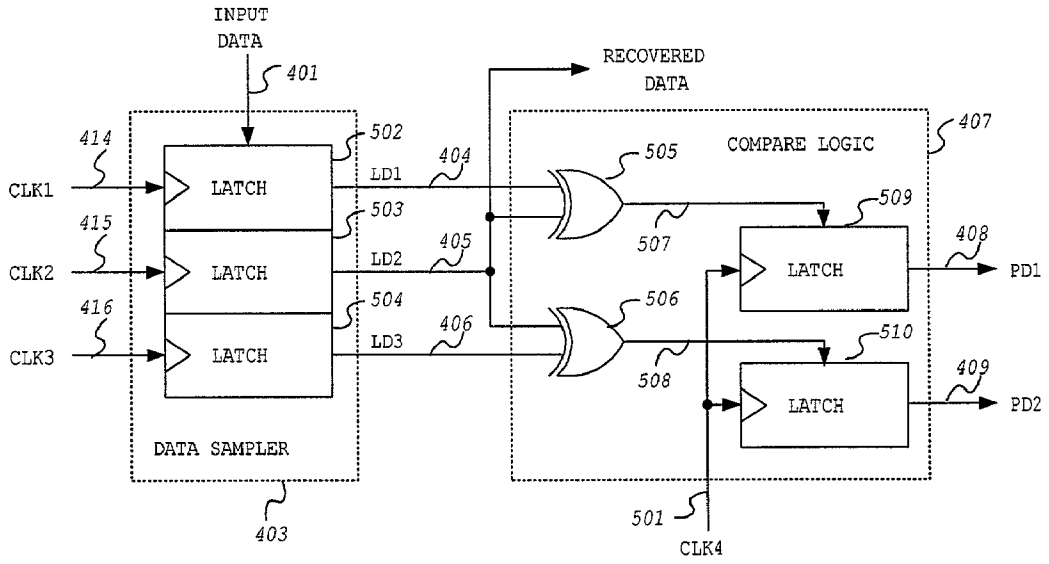

INPUT DATA
401
RECOVERED DATA
414
502
CLK1
LATCH
LD1
404
505
COMPARE LOGIC
407
503
509
415
CLK2
LATCH
LD2
405
507
408
PD1
504
506
416
CLK3
LATCH
LD3
406
510
508
409
LATCH
PD2
DATA SAMPLER
403
501
CLK4

FIG. 5

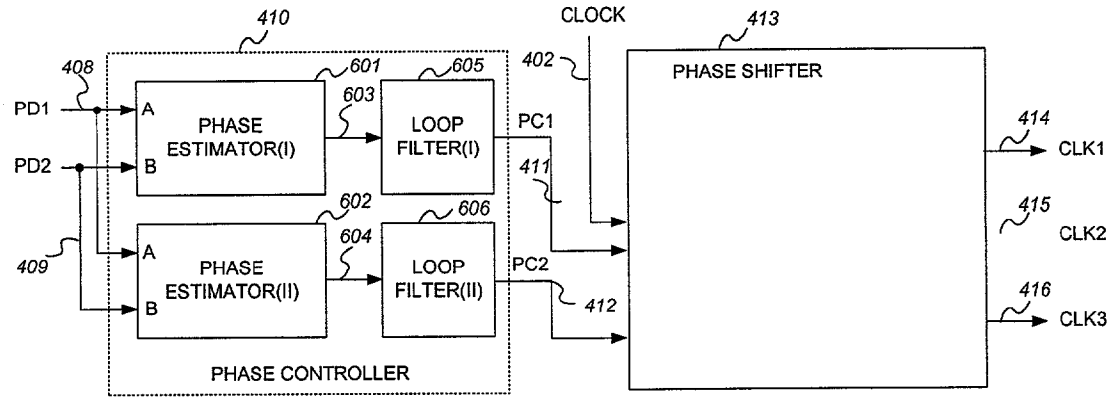

410
CLOCK
413
408
601
605
402
PHASE SHIFTER
PD1
A
PHASE ESTIMATOR(I)
603
LOOP FILTER(I)
PC1
414
CLK1
PD2
B
411
602
606
415
CLK2
409
A
PHASE ESTIMATOR(II)
604
LOOP FILTER(II)
PC2
416
412
CLK3
B
PHASE CONTROLLER

FIG. 6

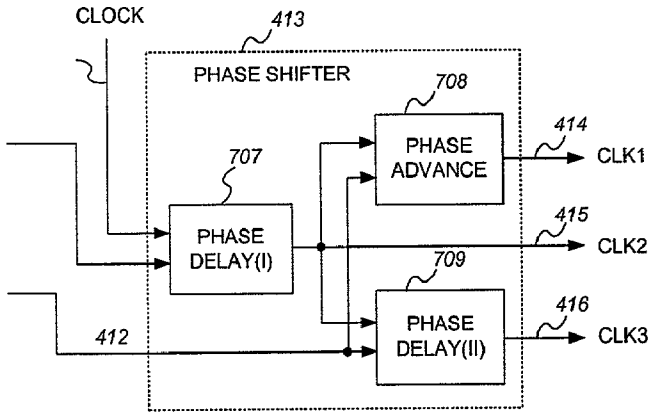

CLOCK
413
PHASE SHIFTER
708
414
PHASE ADVANCE
CLK1
707
PHASE DELAY(I)
415
CLK2
709
416
PHASE DELAY(II)
CLK3
412

FIG. 7

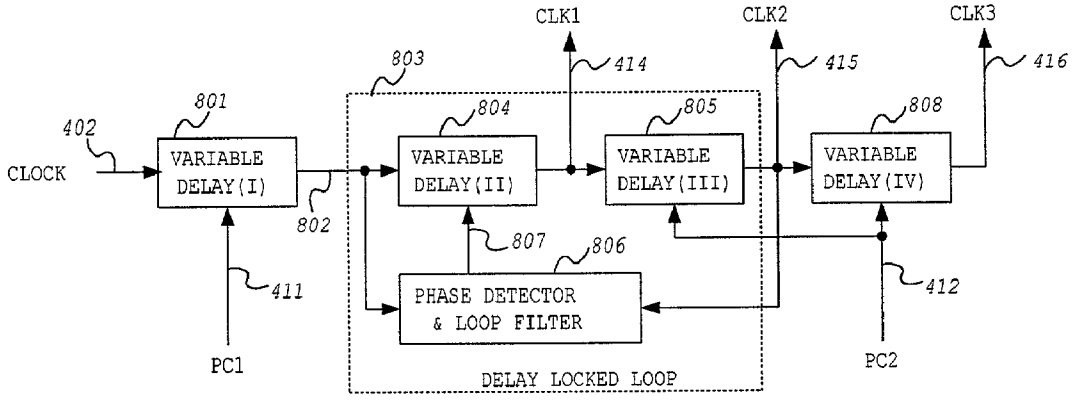

CLK1
CLK2
CLK3
803
414
415
416
801
804
805
808
402
CLOCK
VARIABLE DELAY(I)
VARIABLE DELAY(II)
VARIABLE DELAY(III)
VARIABLE DELAY(IV)
802
807
806
411
412
PHASE DETECTOR & LOOP FILTER
PC1
PC2
DELAY LOCKED LOOP

FIG. 8

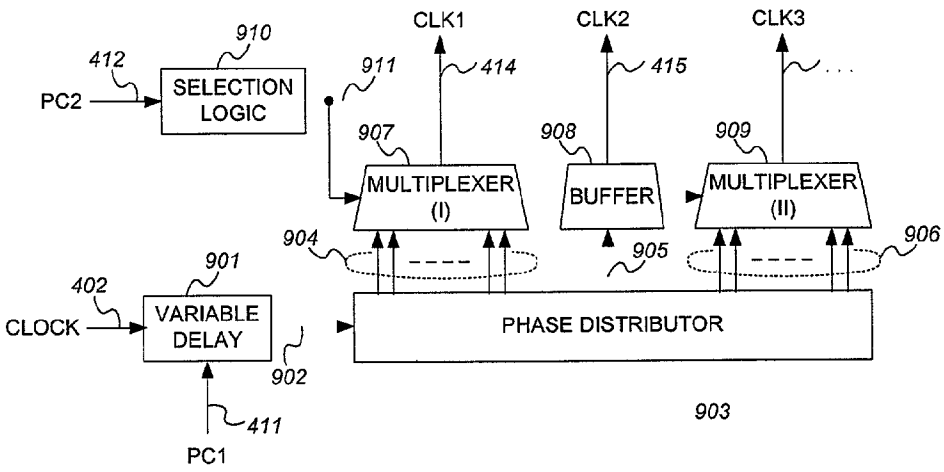

910
412
PC2
SELECTION LOGIC
911
CLK1
414
CLK2
415
CLK3
907
908
909
MULTIPLEXER (I)
BUFFER
MULTIPLEXER (II)
904
905
906
901
402
CLOCK
VARIABLE DELAY
902
PHASE DISTRIBUTOR
903
411
PC1

FIG. 9

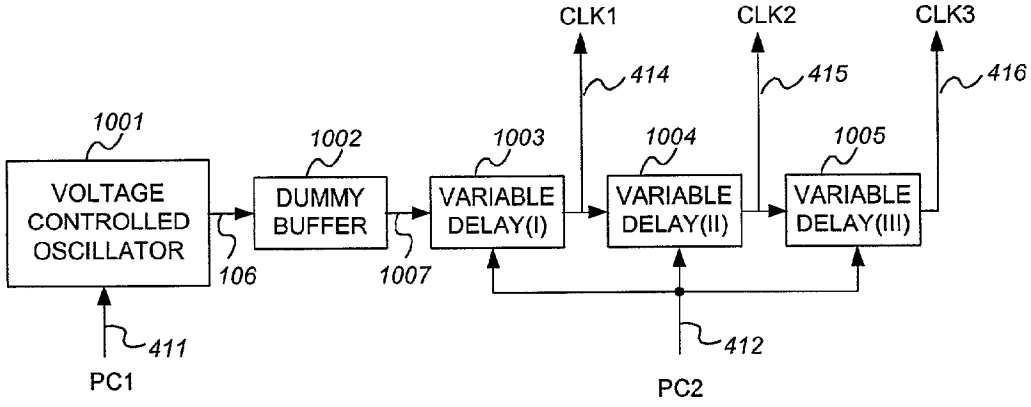

CLK1
CLK2
CLK3
414
415
416
1001
1002
1003
1004
1005
VOLTAGE CONTROLLED OSCILLATOR
DUMMY BUFFER
VARIABLE DELAY(I)
VARIABLE DELAY(II)
VARIABLE DELAY(III)
106
1007
411
PC1
412
PC2

FIG. 10

DATA RECOVERY USING DATA EYE TRACKING

RELATED APPLICATIONS

[0001] This application claims priority under 35 U.S.C. §119(e) to U.S. Application Serial No. 60/229,369 of Lee and Jeong, entitled "Data Recovery Using Data Eye Tracking" filed Aug. 30, 2000, which is incorporated by reference herein in its entirety.

BACKGROUND OF THE INVENTION

[0002] 1. Technical Field

[0003] This invention relates generally to data communications, and more specifically to data recovery for serial digital data link.

[0004] 2. Description of the Related Art

[0005] A number of digital data recovery systems are based on a sampling recovery method that uses sampled data to control the data sampling time. For example, Rau discloses a method for serial non-return-to-zero (NRZ) data transmission. See Rau et al., "Clock/Data Recovery PLL Using Half-Frequency Clock," IEEE Journal of Solid-State Circuits, pp.1156-1160, No.7, July 1997. Rau includes a general feature of phase-locked loops (PLLs) that includes a phase detector, a loop filter, and a voltage-controlled oscillator (VCO). The structures and operations of the loop filter and the VCO are the same as generally known to those skilled in the field. But, an unusual feature of the design is the phase detector, which uses a delay-locked loop (DLL) to generate multiple sampling clocks. The VCO can run at a clock rate lower than the data rate, specifically at half the data rate.

[0006] The PLL adjusts the clock to an incoming data stream. Because of the random nature of data, data transition does not necessarily occur at every clock cycle. The loop must handle a sequence of consecutive zeros or ones in the data stream. In general, for good loop performance, the control signal should be proportional to the phase error. However, at very high operating frequencies, analog signals depend on the data pattern and become highly nonlinear because they do not settle during the bit duration. On the other hand, clock recovery schemes based on sampling techniques result in uniform digital control pulses.

[0007] The data stream is sampled twice within a bit time (the time between received bits). The first of the sampled data are the recovered data, forming the output stream at the original data rate. The second sampled data, which are sampled at half of the bit time later than the first, are used for phase decision. If data transition occurs, and the second sampled data equal the first, it indicates that the sampling phase is early. The frequency of the VCO is then lowered and the sampling phase is delayed. On the contrary, if data transition occurs, and the second sampled data are not equal to the first, it indicates that the sampling phase is late. The frequency of the VCO is then raised and the sampling phase is advanced. If there is no data transition, the phase detector operates so that there is no control on the sampling phase. The stable operating point of the sampling loop is reached when the second sampling is done exactly at the data transition. This so-called bang-bang operation can make the clock jitter smaller than the one introduced by data dependent and nonlinear analog pulses at high frequencies.

[0008] Poulton discloses a similar data recovery scheme. See Poulton et al., "A Tracking Clock Recovery Receiver for 4 Gbps Signaling,"*IEEE Micro, pp.*25-26, January-February 1998. The system is aimed at a higher data rate and uses a demultiplexing receiver to recover high frequency data with a lower frequency clock. The clock rate is one tenth of the data rate. Therefore, the receiver produces 20 samples of the incoming bit stream. Half of the samples are used to output the recovered data stream, while the remaining half are used for phase control as in Rau. Up and Down signals are generated for each of the 10 sample pairs, and the results are summed by an analog summer to generate a differential analog phase control voltage pair. This operation is performed using a switched capacitor filter summer. In this system, the sampling phase is generated by a phase shifter and a delay-locked loop (DLL). The Up/Down signals control the bias voltage of the phase interpolator in the phase shifter and make the phase of the phase shifter output either advanced or delayed. The 20 phase clocks are generated as the outputs of the consecutive delay stage in the DLL.

[0009] The above-described systems are tracking receivers. They control sampling instants by using twice oversampled data. They find the transition edge of an input data stream using the bang-bang operation, and sample the valid data at the position that is half of the bit time distance from the transition edge. If the received data stream has no jitter and is not distorted by the channel, the sampling phase is not critical to the receiver performance. If the received data stream has a small jitter but is not distorted by the channel, the sampling phase may be deviated from the center of the data eye without any performance degradation. But if the received data stream has a jitter comparable to a bit time or is heavily distorted by the channel, the sampling phase deviation from the eye center has a great impact on the performance such as a bit-error-rate (BER). Furthermore, if the jitter is not distributed symmetrically around the transition center, the eye center cannot be correctly tracked by the above two methods.

SUMMARY OF THE INVENTION

[0010] A described embodiment of the present invention provides a data recovery apparatus that can give accurate phase tracking for a serial digital data link.

[0011] A described embodiment of the present invention provides a data recovery apparatus that is based on indirect statistical bit-error-rate measurements.

[0012] A described embodiment of the present invention provides a data recovery apparatus where the sampling phase tracks the practical data eye rather than the data transition center.

[0013] The foregoing are accomplished by the present invention providing data recovery that can be used for a serial digital data link. It is particularly suitable for a very high speed data link that suffers from jitter and signal shape distortion. The system is devised so that better data recovery is possible under the above conditions. The key idea is to make the timing loop track the center of data transition, instead of the practical eye-opening. The center of the data eye may not be matched to the half bit time distance from the transition center as discussed above. In this case, this invention could achieve much lower bit-error-rate than prior tracking receivers.

[0014] The eye opening is tracked by an indirect statistical method by measuring a pseudo bit-error-rate. Practically, there is no way for the receiver to measure a bit-error-rate directly because the receiver does not have information about the transmitted data stream while it samples it. Here, basically three-times oversampling in a bit time is used based on the assumption that the output stream made of center sampled data is the same as the transmitted data stream. The advanced and delayed sampling is used to compare the sampled data to the center sampled data. By summing and/or averaging the compared results over some bit time, a pseudo bit-error-rate is achieved. If one data bit is sampled in one clock cycle, the summing can be done by a charge pump or other types of integrating devices. Practically, this is a method used in a PLL including a charge pump. Or if multiple data bits are sampled in a clock cycle, the summing can be done by simply summing the comparison results in a clock cycle. The summing device can be implemented as a digital device or analog device. An example of this summing method is described in Poulton.

[0015] The assumption that the output stream made of center sampled data is the same as the transmitted data stream may seem unreasonable. But, under a steady locked state, if the signal-to-noise ratio (SNR) is high enough, this assumption gives good results on the pseudo bit-error-rate measurement. Under an out-of-lock state, although the pseudo bit-error-rate measured by this method will not match the real bit-error-rate, the timing loop can make the sampling phase go locked and track the eye opening.

[0016] The tracking ability depends greatly on the loop design. The loop is designed so that the three sampling phases are within the eye opening with some margin. This is accomplished by at least two loop control paths. The phase control signal from one path is used to control the phase width (time duration) from an advanced sampling phase to a delayed sampling phase. The signal is determined by the sum of the pseudo bit-error-rate at the advanced sampling position and that at the delayed sampling position. The phase control signal from the other path is used to control the position of the center sampling phase, which, of course, changes the positions of the advanced and delayed sampling phases. The signal is determined by the difference of the two pseudo bit-error-rates at the advanced and delayed sampling positions.

[0017] A described embodiment of the present invention comprises a data sampler, compare logic, a phase controller, and a phase shifter. The data sampler includes three latches. The latches latch outputs according to the input data when triggering occurs by a clock edge. Compare logic compares the three latched data and gives an output indicating whether the sampling phase is early or late compared to the eye opening. This output corresponds to the measurement of the pseudo bit-error-rates at the advanced and delayed sampling positions. The phase controller includes two loop control sub-blocks. One of the sub-blocks generates a control signal that controls the position of the center sampling phase. It calculates the difference of the two pseudo bit-error-rates and integrates by a loop filter, which can be made of a charge pump. The other sub-block generates a control signal that controls the phase width between the advanced and delayed sampling phases. It adds the two pseudo bit-error-rates and passes through a loop filter. The phase shifter makes the three sampling clocks under control of the two-phase control signals.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] **FIG. 1** shows the data eye diagram for a serial digital data link;

[0019] **FIG. 2** shows the jitter distribution and bit-error-rate with the same time base shown in **FIG. 1**;

[0020] **FIGS. 3***a* and **3***b* are illustrative diagrams showing the three sampling phases of an embodiment of the invention;

[0021] **FIG. 4** is a system block diagram illustrative of an embodiment of the invention;

[0022] **FIG. 5** is a detailed block diagram of the data sampler and compare logic of **FIG. 4**.

[0023] **FIG. 6** shows a block diagram of a phase controller and phase shifter of **FIG. 4**.

[0024] FIGS. **7-10** show more detailed block diagrams of embodiments of the phase shifter of **FIG. 6**.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0025] **FIG. 1** shows a typical data eye pattern that is a superposition of multiple data transitions with a horizontal displacement indicative of the jitter that may be observed in an actual data link. The source of the jitter may be: (1) transmitter clock jitter generated by power supply fluctuation or any other noise, (2) inter-symbol interference caused by the mixture of randomly transmitted data pattern and channel attenuation, or (3) a jitter source in a receiving device similar to that of a transmitting device. The first and second terms reflect direct jitter sources that can be measured by a measurement device. The last term is not measurable, but it also affects the receiving performance. In **FIG. 1**, the diamond shape surrounded by **101**, **102**, **103**, **104** and indicated by 'VALID DATA' is the eye opening area. The vertical length of the eye opening at a certain time position represents the signal strength (energy) at that time. So it is desired to sample the data stream at time position T2, the maximum eye position. If the sampling phase deviates from T2 to T1 or to T3, the bit-error-rate would be increased.

[0026] **FIG. 2** shows a typical jitter distribution probability **201** for the eye pattern of **FIG. 1** with the same horizontal axis, and it also shows the bit-error-rate **202** as a function of the sampling phase. In the figure, the jitter is shown to be distributed symmetrically around the center of data transition. In this case, the eye opening will be halfway between the left and right transition center. But, in some cases, the eye opening may not be symmetric, having a long tail in one direction when the jitter source is heavily biased in one direction. Therefore, the eye opening leads or lags the halfway position. The tracking receivers presented in Rau and Poulton make the sampling phase track the transition center. Those are well suited for a symmetric jitter distribution, but not for a non-symmetric distribution.

[0027] **FIGS. 3***a* and **3***b* show three sampling phases of an embodiment of the invention. 'CLK2'**308** is the clock for the center sampling phase of an embodiment of the invention.

'CLK1'**307** and 'CLK3'**309** represent the clocks for advanced and delayed sampling phases, respectively. Assuming that the center-sampled data by 'CLK2'**308** is correct, the bit-error-rate could be measured by comparing the two data sampled by 'CLK1'**307** and by 'CLK3'**309** to the center sampled data. The bit-error rate will be simply 'zero' or 'one' if the sampled results are compared for only one bit. The bit-error rate will be some number between 'zero' and 'one' if multiples of sampled results are compared for a predetermined time duration or for a predetermined number of bits given by a demultiplexing receiver such as that shown in Poulton. If the measured bit-error rate is greater than a predetermined value **305** (or a predetermined margin), the corresponding sampling phase would be apart from the eye opening, and be in the jitter region. The term 'predetermined margin' indicates that the phases of 'CLK1' and 'CLK3' do not exactly coincide to the edge of the data eye. The data eye is related to the probabillistic distribution of jitter. Furthermore, the phase controller has a low pass filter, which makes the phases of 'CLK1' and 'CLK3' determined by the past history of random jitters on the data.

[**0028**] In the present invention, 'CLK2'**308** is controlled by a phase control signal that is determined from the difference of the bit-error-rate measured at 'CLK1'**307** and the one measured at 'CLK3'**309**. 'CLK1'**307** and 'CLK3'**309** are advanced and delayed from 'CLK2'**308** by the time difference of 'TM'**310**, respectively. The time difference 'TM'**310** is controlled by another phase control signal that is determined from the summation of the two bit-error-rate. If bit-error-rate at 'CLK1'**307** is greater than the one at 'CLK3'**309**, it means that the overall sampling phase leads the eye opening. Therefore, the phase of 'CLK2'**308** is delayed until the two bit-error-rate becomes equal. On the contrary, if the bit-error-rate at 'CLK1'**307** is smaller, the phase of 'CLK2'**308** is advanced. If the sum of the two bit-error-rate exceeds a predetermined value, 'TM'**310** is decreased to shrink the sampling window to the eye opening. If the sum is less than predetermined value, 'TM'**310** is increased.

[**0029**] The mechanism described above on the dual phase control operates correctly when the data recovery loop is in a steady locked state. Although many other cases of the unlocked state may be considered, the mechanism can make the loop enter the locked state eventually. If it is desired to make the system operate more efficiently and go to lock faster, a certain lock-aiding apparatus could be added.

[**0030**] **FIG. 4** is a system block diagram of an embodiment of the present invention. The overall system includes a data sampler **403**, compare logic **407**, a phase controller **410**, and a phase shifter **413**. Input data **401** comes from the channel directly or is the output of any type of filter, pre-amplifier, buffer, etc which modifies the shape of the signal from the channel. The data sampler **403** oversamples and latches the input data **401** by a predetermined decision criterion. Compare logic **407** compares the latched data **404**, **405**, **406** and measures the pseudo bit-error-rate for the sampled data set. The phase controller **410** decides the phase relationship between the sampling clocks **414**, **415**, **416** and input data **401**, and outputs phase control signals **411**, **412** through a loop filter, which is a low pass filter such as charge pump, RC filter, etc. Phase shifter **413** splits and shifts the phase of the input clock **402** to make the desired three phase clocks **414**, **415**, **416**. The input clock **402** could be externally supplied from transmitter or other control device, or could be recovered from the input data stream **401**. The frequency of input clock **402** is matched to the input data rate so that the recovery loop does not lose lock owing to the frequency difference.

[**0031**] **FIG. 5** shows a detailed block diagram of the data sampler **403** and the compare logic **407**. The data sampler **403** has three latches **502**, **503**, **504**. They latch input data on triggering of the three clock signals 'CLK1'**414**, 'CLK2'**415**, 'CLK3'**416** respectively. The outputs of the data sampler, 'LD1'**404**, 'LD2'**405**, 'LD3'**406**, are provided to the compare logic **407**, while 'LD2'**405** makes an output stream as the recovered data.

[**0032**] Compare logic **407** compares 'LD1'**404** and 'LD3'**406** with 'LD2'**405** by comparing means, which is implemented as XOR gate **505**, **506** in the figure. Because of the different latching time for 'LD1'**404**, 'LD2'**405** and 'LD3'**406**, it is better to latch the comparison results **507**, **508** by another clock 'CLK4'**501** rather than directly output the results. This clock **501** should not overlap the meta-stable time duration during which the comparison results are meaningless. Therefore, 'CLK4'**501** should trigger the latch before 'LD1'**404** is latched or after 'LD3'**406** is latched.

[**0033**] **FIG. 6** shows a detailed block diagram of phase controller **410** and a block diagram representing phase shifter **413**. Phase controller **410** gets the outputs of compare logic **407**, 'PD1'**408** and 'PD2'**409**, and estimates the phase relationship between the latching clock **414**, **415**, **416** and input data **401**. The phase of 'CLK2'**415** could be estimated by phase estimator (I) **601**, which calculates the difference of 'PD1'**408** and 'PD2'**409**. This estimation result **603** is fed to loop filter (I) **605** to generate the low-pass filtered output 'PC1'**411**, which determines the phase delay of 'PLK2'**415**. The phase difference 'TM'**310** between 'CLK2'**415** and the other two clocks **414**, **416** could be estimated by phase estimator (II) **602**, which calculates the sum of 'PD1'**408** and 'PD2'**409**. This estimation result **604** is fed to loop filter (II) **606** and generates the other low-pass filtered output 'PC2'**412**. 'PC2'**412** determines the amount of phase advance and phase delay for 'CLK1'**414** and 'CLK3'**416** respectively. There are many different ways to implement the phase estimators **601**, **602**. We can determine the weighted difference or sum for faster lock-in time. Some offset may be added to the output **604** of phase estimator (II) **602** to modify the tracking behavior.

[**0034**] The phase shifter **413** comprises a phase delay.

[**0035**] **FIG. 7** shows a first embodiment of phase shifter **413**, including a phase delay (I) **707**, a phase advance **708**, and a phase delay (II) **709**. Phase delay (I) **707** is used to adjust the phase of 'CLK2'**415** under control of 'PC1'**411**. Phase delay **707** can be made up of a cascade of MOSFET inverters or a resistor-capacitor (RC) delay circuit, where 'PC1'**411** acts as the bias current or bias voltage. Phase advance **708** and phase delay (II) **709** are used to adjust the phase difference of 'CLK1'**414** and 'CLK3'**416** from 'CLK2'**415**.

[**0036**] **FIG. 8** shows a second embodiment of the phase shifter **413**, which comprises four variable delays **801**, **804**, **805**, **808** and further comprises a phase detector and a loop filter **806**. Variable delay (I) **801** is controlled by 'PC1'**411** and adjusts the phase of its output **802**. Variable delay (II)

804, variable delay (III) **805**, and phase detector and loop filter **806** make up delay-locked loop **803**, which makes the phase of 'CLK2'**415** tracks the phase of variable delay (I)'s output **802**. Variable delay (III) **805** is controlled by 'PC2'**412** and adjusts the phase difference between 'CLK1'**414** and 'CLK2'**415**. Variable delay (IV) **808** is a replica of variable delay (III) **805** and is also controlled by PC2'**412**. Therefore, the phase difference between 'CLK2'**415** and 'CLK3'**416** is the same as that between 'CLK1'**414** and 'CLK2'**415**.

[**0037**] **FIG. 9** shows a third embodiment of phase shifter **413**. It comprises variable delay **901**, phase distributor **903**, multiplexer (I) **907**, multiplexer (II) **909**, buffer **908**, and selection logic **910**. Variable delay **901** has the same function as variable delay (I) **801** in **FIG. 8**. Phase distributor **903** is a kind of delay-locked loop or phase-locked loop that makes multiples of different phase clocks **904**, **905**, **906**, where the phase of **905** tracks the phase of **902**. Here **904** is a bundle of clocks that lead **905** in phase, where the amount of phase leading lies between zero and half bit time. Selection logic **910** controls multiplexer (I) **907** so that it passes one of multiple input clocks **904**. Therefore, the phase difference of 'CLK1'**414** and 'CLK2'**415** can be adjusted by 'PC2'**412**. Bundle of clocks **906** that lag **905** in phase are input to multiplexer (II) **909**, where one of those is selected so that the phase difference between 'CLK2'**415** and 'CLK3'**416** is the same as that between 'CLK1'**414** and 'CLK2'**415**. The purpose of buffer **908** is that the propagation delay through itself **908** is the same as that through multiplexers **907**, **909** so the phase relationships between 'CLK1'**414**, 'CLK2 **415** and 'CLK3'**416** are more accurately controlled.

[**0038**] **FIG. 10** shows a fourth embodiment of phase shifter **413**. It comprises a voltage-controlled oscillator **1001**, variable delay circuits **1003**, **1004**, **1005**, and a dummy buffer **1002**. It does not need the input clock **402** because it uses a voltage-controlled oscillator as a clock source. A voltage-controlled oscillator is controlled by 'PC1'**411** and generates a clock whose frequency is adjusted so that the phase of 'CLK2'**415** is located at the optimum sampling position. Variable delay circuits **1003**, **1004**, **1005** are controlled by 'PC2'**412** and generates 'CLK1'**414**, 'CLK2'**415**, and 'CLK3'**416**, respectively. The dummy buffer **1002** is an optional circuit that could be included so as to match the phase difference between the three clocks **414**, **415**, **416** equally. For the embodiment of FIG. **10**, the phase of 'CLK2'**415** should be controlled by 'PC1'**411** only and should not be affected by the variation of 'PC2'**412**. And the phase differences between the three clocks **414**, **415**, **416** should be affected by 'PC2'**412** and should not be affected by the variation of 'PC1'**411**. If frequency range of the voltage controlled oscillator **1001** is wide, it may be difficult for the phase of 'CLK2'**415** to track the optimum sampling position because of the initial acquisition failure. To avoid this difficulty, we can add a reference loop. See Richard Gu et al, "A 0.5-3.5 Gb/s Low-Power Low-Jitter Serial Data CMOS Transceiver," ISSCC Digest of Technical Papers, pp.352-353, February 1999. Upon power-up or reset, the data recovery system is defaulted to the reference loop so that the frequency of the voltage controlled oscillator **1001** output is locked to an external reference clock. After initial lock is acquired, the loop containing the signals 'PC1'**411** and 'PC2'**412** is enabled.

[**0039**] This invention has been described in a considerable detail in order to provide those skilled in the art enough information to apply the principles and to implement the components. The system shown in **FIG. 4** through **FIG. 6** is applicable to data recovery which samples one bit data per clock. Skilled engineers can modify or expand this embodiment for use in a complex recovery system such as half-frequency receiver of Rau's or the demultiplexing receiver of Poulton's. The present invention can be applied to various types of coding such as NRZ, Manchester, binary PAM, M-ary (multi-level) PAM, etc. The invention can be carried out by different equipment and devices than those described herein, and various modifications, both as to the equipment details and operating procedures, can be accomplished without departing the scope of the invention itself.

[**0040**] While the invention has been described with reference to preferred embodiments, it is not intended to be limited to those embodiments. It will be appreciated by those of ordinary skilled in the art that many modifications can be made to the structure and form of the described embodiments without departing from the spirit and scope of this invention.

What is claimed is:

1. A data recovery apparatus for a digital data stream of input data, comprising: phase shifting means for outputting multiple sampling clocks in a bit time, where the phase of said sampling clocks are automatically adjustable;

data sampling means for sampling the input data using the sampling clocks as triggers, and for providing multiple sampled data signals, where one of said sampled data signals is used to output recovered data;

compare logic means for comparing said sampled data signals to said recovered data; and

phase controlling means for estimating the phase relationship between the input data and said sampling clocks using the comparison result of said compare logic means, and for providing control signals to said phase shifting means according to said estimation result.

2. The apparatus of claim 1 wherein the phase shifting means comprises:

phase delay means controlled by a first output of said phase controlling means for outputting a first sampling clock using an input clock which is one of an external clock and an internally recovered clock;

first circuit means controlled by a second output of said phase controlling means for outputting a second sampling clock that advances said first sampling clock in phase;

second circuit means controlled by the second output of said phase controlling means for outputting a third sampling clock that is delayed from said first sampling clock in phase; and

the phases of the three sampling clocks are arranged within an eye opening of the input data stream with a predetermined margin.

3. The apparatus of claim 2, wherein the first circuit means and the second circuit means receive the first sampling clock.

4. The apparatus of claim 1, wherein the phase shifting means comprises:

a phase distributor outputting a plurality of phase shift values;

a buffer receiving input from the phase distributor and outputting a first sampling clock in accordance with a first output of said phase controlling means; and

selection logic receiving input from the phase distributor and outputting a second and third sampling clock in accordance with a second output of said phase controlling means.

5. The apparatus of claim 1 wherein the phase shifting means comprises:

a voltage controlled oscillator controlled by a first output of the phase controlling means,

circuit means controlled by a second output of said phase controlling means for outputting three sampling clocks by delaying the output of the voltage controlled oscillator, where the phases of the three sampling clocks are arranged within an eye opening of input data stream with a predetermined margin.

6. A data recovery apparatus for a digital data stream of input data, comprising:

a phase shifter that outputs multiple sampling clocks in a bit time, where the phase of said sampling clocks are automatically adjustable;

a data sampler that samples the input data using the sampling clocks as triggers, and for providing multiple sampled data signals, where one of said sampled data signals is used to output recovered data;

compare logic that compares said sampled data signals to said recovered data; and

a phase controller that estimating the phase relationship between the input data and said sampling clocks using the comparison result of said compare logic means, and for providing control signals to said phase shifting means according to said estimation result.

7. The apparatus of claim 6 wherein the phase shifter comprises:

phase delay logic controlled by a first output of said phase controller for outputting a first sampling clock using an input clock which is one of an external clock and an internally recovered clock;

a first circuit, controlled by a second output of said phase controller, for outputting a second sampling clock that advances said first sampling clock in phase;

a second circuit, controlled by the second output of said phase controller, for outputting a third sampling clock that is delayed from said first sampling clock in phase; and

the phases of the three sampling clocks are arranged within an eye opening of the input data stream with a predetermined margin.

8. The apparatus of claim 6 wherein the phase shifter comprises:

a voltage controlled oscillator controlled by a first output of the phase controller,

a circuit,controlled by a second output of said phase control, for outputting three sampling clocks by delaying the output of the voltage controlled oscillator, where the phases of the three sampling clocks are arranged within an eye opening of input data stream with a predetermined margin.

9. A data recovery method for a digital data stream, comprising:

sampling input data at multiple points, where said sampling points are arranged by a predetermined order and adjustable time difference;

providing a first pseudo bit-error signal that is a result of comparison of data sampled at an early boundary with recovered data;

providing a second pseudo bit-error signal that is a result of comparison of data sampled at a late boundary with recovered data; and

using the first and second pseudo bit-error signals, so that the sampling boundary is marginally matched to the edge of an eye opening and one of the intermediate sampling points serves for data recovery.

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