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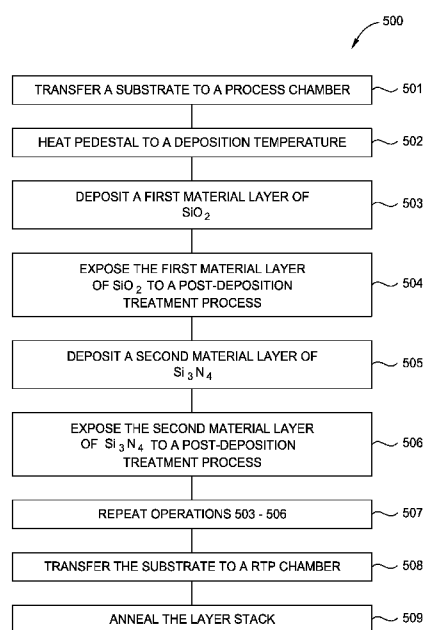


FIG. 5

(57) Abstract: Embodiments described herein relate to manufacturing layer stacks of oxide/nitride (ON) layers with minimized in-plane distortion (IPD) and lithographic overlay errors. A method of forming a layer stack ON layers includes flowing a first silicon-containing gas, an oxygen-containing gas, and a first dilution gas. A RF power is symmetrically applied to form a first material layer of SiO₂. A second silicon-containing gas, a nitrogen-containing gas, and a second dilution gas are flowed. A second RF power is symmetrically applied to form a second material layer of Si₃N₄. The flowing the first silicon-containing gas, the oxygen-containing gas, and the first dilution gas, the symmetrically applying the first RF power, the flowing the second silicon-containing gas, the nitrogen-containing gas, and the second dilution gas, and the symmetrically applying the second RF power is repeated until a desired number of first material layers and second material layers make up a layer stack.

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ON STACK OVERLAY IMPROVEMENT FOR 3D NAND

BACKGROUND

Field

[0001] Embodiments of the present disclosure generally relate to 3D NAND memory cell manufacturing processes. More particularly, embodiments of the present disclosure relate to apparatuses and methods of manufacturing layer stacks of oxide/nitride (ON) layers with minimized in-plane distortion (IPD) and lithographic overlay errors.

Description of the Related Art

[0002] Growing demands continue to drive the need for high-capacity, high performance computer memory devices with smaller geometries at lower costs. To this end, components of memory cells are stacked on top of each other to create three-dimensional (3D) memory cells, such as vertical gate 3D memory cells. One such technology is NAND flash memory, which is generally found in memory cards, USB flash drives, solid-state drives, and other similar devices for data storage and transfer. In NAND flash memory, memory cells made from transistors are connected in series and stacked in vertical layers to create densely-packed, high-capacity memory devices. Flash drives generally use less power and are more durable than ordinary hard drives because they do not contain moving parts. As such, there is great interest in increasing the capacity of flash drives.

[0003] As flash technology has progressed, challenges have continued to exist in how to create high-capacity devices on a small scale. One such challenge is that 3D NAND memory cells require 64x or more layer stacks of oxide/nitride (ON) layers that are subject to in-plane distortion (IPD) and lithographic overlay errors. Therefore, there is a need in the art for an apparatus and methods of manufacturing layer stacks of ON layers with minimized IPD and improved lithographic overlay.

SUMMARY

[0004] In one embodiment, a method of forming a layer stack of oxide/nitride (ON) layers is provided. The method includes transferring a substrate to a process chamber, heating a pedestal retaining the substrate to a deposition temperature, and flowing a first silicon-containing gas at a first silicon-containing gas flow rate, an

oxygen-containing gas at an oxygen-containing gas flow rate, and a first dilution gas at a first dilution gas flow rate into the process chamber. A first radio frequency (RF) power is symmetrically applied to the first silicon-containing gas, the oxygen-containing gas, and the first dilution gas to form a first material layer of silicon dioxide (SiO_2). The method further includes flowing a second silicon-containing gas at a second silicon-containing gas flow rate, a nitrogen-containing gas at a nitrogen-containing gas flow rate, and a second dilution gas at a second dilution gas flow rate into the process chamber. A second RF power is symmetrically applied to the second silicon-containing gas, the nitrogen-containing gas, and the second dilution gas to form a second material layer of silicon nitride (Si_3N_4). The flowing the first silicon-containing gas, the oxygen-containing gas, and the first dilution gas, the symmetrically applying the first RF power, the flowing the second silicon-containing gas, the nitrogen-containing gas, and the second dilution gas, and the symmetrically applying the second RF power is repeated until a desired number of material layer pairs of the first material layer and the second material layer make up a layer stack.

[0005] In another embodiment, a method of forming a layer stack of oxide/nitride (ON) layers is provided. The method includes transferring a substrate to a first process chamber, heating a first pedestal of the first process chamber retaining the substrate to a deposition temperature, and flowing a first silicon-containing gas at a first silicon-containing gas flow rate, an oxygen-containing gas at an oxygen-containing gas flow rate, and a first dilution gas at a first dilution gas flow rate into the first process chamber. A first radio frequency (RF) power is symmetrically applied to the first silicon-containing gas, the oxygen-containing gas, and the first dilution gas to form a first material layer of silicon dioxide (SiO_2). The method further includes flowing a second silicon-containing gas at a second silicon-containing gas flow rate, a nitrogen-containing gas at a nitrogen-containing gas flow rate, and a second dilution gas at a second dilution gas flow rate into the first process chamber. A second RF power is symmetrically applied to the second silicon-containing gas, the nitrogen-containing gas, and the second dilution gas to form a second material layer of silicon nitride (Si_3N_4). The flowing the first silicon-containing gas, the oxygen-containing gas, and the first dilution gas, the symmetrically applying the first RF power, the flowing the second silicon-containing gas, the nitrogen-containing gas, and the second dilution gas, and the symmetrically applying the second RF power is repeated until a first portion of a desired number of material layer pairs of the first material layer and the second material

layer make up a layer stack. The method further includes transferring the substrate from the first process chamber to a second process chamber, heating a second pedestal of the second process chamber retaining the substrate to the deposition temperature, and repeating the flowing the first silicon-containing gas, the oxygen-containing gas, and the first dilution gas, the symmetrically applying the first RF power, the flowing the second silicon-containing gas, the nitrogen-containing gas, and the second dilution gas, and the symmetrically applying the second RF power until a second portion of the desired number of the material layer pairs of the first material layer and the second material layer make up a layer stack.

[0006] In yet another embodiment, a showerhead is provided. The showerhead includes a symmetric radio frequency (RF) circuit disposed in the showerhead connected to a RF power source by a RF feed having a four portions connected to the symmetric RF circuit at 90 degree intervals.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] So that the manner in which the above recited features of the present disclosure can be understood in detail, a more particular description of the disclosure, briefly summarized above, may be had by reference to embodiments, some of which are illustrated in the appended drawings. It is to be noted, however, that the appended drawings illustrate only exemplary embodiments and are therefore not to be considered limiting of its scope, as the disclosure may admit to other equally effective embodiments.

[0008] Figure 1 is a schematic cross-sectional view of a memory device according to an embodiment.

[0009] Figure 2 is a schematic view of a processing system according to an embodiment.

[0010] Figure 3 is a schematic cross-sectional view of a plasma-enhanced chemical vapor deposition system according to an embodiment.

[0011] Figure 4 is a top, schematic cross-sectional view of a showerhead of a process chamber according to an embodiment.

[0012] Figure 5 is a flow diagram of a method of forming a layer stack of ON layers with minimized IPD and improved lithographic overlay according to an embodiment.

[0013] Figure 6 is a flow diagram of a method of forming a layer stack of ON layers with minimized IPD and improved lithographic overlay according to an embodiment.

[0014] To facilitate understanding, identical reference numerals have been used, where possible, to designate identical elements that are common to the figures. It is contemplated that elements and features of one embodiment may be beneficially incorporated in other embodiments without further recitation.

DETAILED DESCRIPTION

[0015] Embodiments described herein relate to manufacturing layer stacks of oxide/nitride (ON) layers with minimized in-plane distortion (IPD) and lithographic overlay errors. A method of forming a layer stack ON layers includes flowing a first silicon-containing gas, an oxygen-containing gas, and a first dilution gas. A RF power is symmetrically applied to form a first material layer of SiO_2 . A second silicon-containing gas, a nitrogen-containing gas, and a second dilution gas are flowed. A second RF power is symmetrically applied to form a second material layer of Si_3N_4 . The flowing the first silicon-containing gas, the oxygen-containing gas, and the first dilution gas, the symmetrically applying the first RF power, the flowing the second silicon-containing gas, the nitrogen-containing gas, and the second dilution gas, and the symmetrically applying the second RF power is repeated until a desired number of first material layers and second material layers make up a layer stack.

[0016] Figure 1 is a schematic cross-sectional view of a memory device 100 according to embodiments of the present disclosure. The memory device 100 includes a substrate 102 with a plurality of first material layers 104 and a plurality of second material layers 106 thereon. Material layer pairs 108a, 108b, 108c, ... 108n, also known as a plurality of material layer pairs 108 of a first material layer of the plurality of first material layers 104 and a second material layer of the plurality of second material layers 106, make up a layer stack 110. In the embodiment of an ON stack memory device, each of the first material layers 104 is generally a silicon dioxide layer (O layer) and each of the second material layers 106 is generally a silicon nitride layer (N layer). While Figure 1 depicts the second material layer 106 deposited over the first material layer 104, the deposition order may be reversed such that the first material layer 104

(O layer) is deposited over the second material layer 106 (N layer). In an embodiment in which the memory device 100 is a 3D NAND memory cell, the memory device 100 further includes a source and a drain (not shown) disposed on opposite ends of a first surface 112 of the substrate 102. For use as flash memory, multiple NAND flash cells are generally connected in series with the adjacent cells sharing a source or drain, and each cell is connected to a bitline and a wordline. In operation, each cell can store data, such as a "0" or "1," therein.

[0017] The methods of manufacturing layer stacks of ON/OP films with minimized IPD and improved lithographic overlay include plasma-enhanced chemical vapor deposition (PECVD) processes, which can be used to form silicon films at relatively low temperatures. The methods can be performed by one or more twin PECVD systems, such as a PRODUCER® plasma enhanced CVD (PECVD) system, available from Applied Materials, Inc. of Santa Clara, Calif. The PECVD systems may be incorporated into a processing system 200, available from Applied Materials, Inc. of Santa Clara, Calif. It is to be understood that the processing system described below is an exemplary processing system and other processing systems, including processing systems from other manufacturers, may be used with or modified to accomplish aspects of the present disclosure. It is to be understood that the PECVD system below is an exemplary PECVD system and other PECVD systems, including PECVD systems from other manufacturers, may be used with or modified to accomplish aspects of the present disclosure.

[0018] Figure 2 is a schematic view of a processing system 200 utilized for methods of manufacturing layer stacks of ON/OP layers with minimized IPD and improved lithographic overlay. As shown in Figure 2, a pair of front opening unified pods (FOUPs) 202 supplies substrates that are received by robotic arms 204 and placed into the holding area 206 before being placed into one of the process chambers 214a-214d of PECVD systems 208a, 208b and/or Rapid Thermal Processing (RTP) chambers 210a, 210b. A second robotic arm 212 may be used to transport the substrates from the holding area 206 to the PECVD systems 208a-208d and/or RTP chambers 210a, 210b and back. The PECVD systems 208a, 208b are utilized to deposit ON/OP layer stacks and the RTP chambers 210a, 210b are utilized to anneal the ON/OP layer stacks.

[0019] Figure 3 is a schematic cross-sectional view of a PECVD system 208a utilized for methods of manufacturing layer stacks of ON/OP layers with minimized IPD and improved lithographic overlay. As shown in Figure 3, the PECVD system 208a includes the process chambers 214a, 214b, wherein the process chambers 214a, 214b share resources, for example, such as a shared vacuum pump 304, a first gas source 306, a second gas source 332, and a third gas source 334. The process chamber 214a (e.g., a first process chamber) and the process chamber 214b (e.g., a second process chamber) are similarly configured.

[0020] Each process chamber 214a, 214b has a processing volume 307, 308 that includes a pedestal 309, 310 disposed therein to support a substrate 102. The pedestal 309, 310 includes a heating element (not shown) and a mechanism (not shown) that retains the substrate 102 on the pedestal 309, 310, such as an electrostatic chuck, a vacuum chuck, a substrate retaining clamp, or the like. The pedestal 309, 310 is coupled to and movably disposed in the processing volume 307, 308 by a stem 311, 312 connected to a lift system (not shown) that moves the pedestal 309, 310 between an elevated processing position and a lowered position that facilitates transfer of the substrate 102 to and from the process chamber 214a, 214b through an opening 315, 316.

[0021] A flow controller 317, 318, such as a mass flow control (MFC) device, is disposed between the first gas source 306 and the process chamber 214a, 214b to control a flow rate of a first process gas from the first gas source 306 to a showerhead 319, 320 used for distributing the first process gas across the processing volume 307, 308. A flow controller 328, 329 is disposed between the second gas source 332 and the process chamber 214a, 214b to control a flow rate of a second process gas from the second gas source 332 to a showerhead 319, 320 used for distributing the second process gas across the processing volume 307, 308. A flow controller 330, 331 is disposed between the third gas source 334 and the process chamber 214a, 214b to control a flow rate of a third process gas from the third gas source 334 to a showerhead 319, 320 used for distributing the third process gas across the processing volume 307, 308. A valve 325, 326 can be disposed between the shared vacuum pump 304 and the process chamber 214a, 214b for controlling the pressure within the processing volume 307, 308.

[0022] The showerhead 319, 320 includes a symmetric radio frequency (RF) circuit (shown in Figure 4) connected to a RF power source 321, 322 by a RF feed 323, 324 having a plurality of portions 344, 345 for striking a substantially uniform plasma in the processing volume 307, 308 from the process gas. The pedestal 309, 310 includes a bottom tuner assembly 340, 341. The bottom tuner assembly 340, 341 includes a tuning electrode 313, 314 coupled to a tuning circuit 342, 343. The tuning circuit 342, 343 is utilized to modulate the impedance on the tuning electrode 313, 314 provide further control of the plasma in the processing volume. For example, modulating the impedance of the tuning electrode 313, 314 increases plasma bombardment on the substrate 102.

[0023] As shown in Figure 4, a cross-sectional top view of the showerhead 319 of the process chambers 214a. The showerhead 319 has a symmetric RF circuit 402 disposed therein coupled to the RF feed 323. Each portion of the plurality of portions 344 is connected to the symmetric RF circuit 402 so that the supply of RF power to the symmetric RF circuit 402 is symmetric. For example, the RF feed 323 has four portions connected to the symmetric RF circuit 402 at 90 degree intervals. A symmetric supply of RF power to the symmetric RF circuit 402 allows for striking the substantially uniform plasma in the processing volume 307. The symmetric RF circuit 402 is symmetric so the plasma in the processing volume 307 is substantially uniform to reduce IPD of the layer stacks of ON layers.

[0024] Figure 5 is a flow diagram of a method 500 of forming a layer stack of ON layers with minimized IPD and improved lithographic overlay. At operation 501, a substrate 102 is transferred to a process chamber 214a of a PECVD system 208a. In one embodiment, a second robotic arm 212 transfers the substrate 102 from the holding area 206 of the processing system 200 to a process chamber 214a of the PECVD system 208a. At operation 502, the pedestal 309 is heated to a deposition temperature of about 500 degrees Celsius (°C) to about 600 °C. At operation 503, a first material layer 104 of silicon dioxide (SiO₂) is deposited. During operation 503, a first silicon-containing gas at a first silicon-containing gas flow rate, an oxygen-containing gas at an oxygen-containing gas flow rate, and a first dilution gas at a first dilution gas flow rate are delivered to the process chamber 214a.

[0025] In one embodiment, the flow controller 317 disposed between the first gas source 306 and the process chamber 214a controls the first silicon-containing gas flow rate of the first silicon-containing gas provided to showerhead 319 that distributes the first silicon-containing gas across the processing volume 307 of the process chamber 214a. The first silicon-containing gas may include at least one of silane (SiH_4), tetraethyl orthosilicate (TEOS), and disilane (Si_2H_6). In another embodiment, the flow controller 328 disposed between the second gas source 332 and the process chamber 214a controls the oxygen-containing gas flow rate of the oxygen-containing gas provided to showerhead 319 that distributes the oxygen-containing gas across the processing volume 307 of the process chamber 214a. The oxygen-containing gas may include at least one of nitrous oxide (N_2O), oxygen gas (O_2), and trioxygen (O_3). In yet another embodiment, the flow controller 330 disposed between the third gas source 334 and the process chamber 214a controls the first dilution gas flow rate of the first dilution gas provided to showerhead 319 that distributes the first dilution gas across the processing volume 307 of the process chamber 214a. The first dilution gas may include at least one of nitrogen gas (N_2), argon (Ar), and helium (He). In some embodiments, the first silicon-containing gas flow rate is about 600 standard cubic centimeters per minute (sccm) to about 5000 sccm, the oxygen-containing gas flow rate is about 500 sccm to about 15000 sccm, and the first dilution gas flow rate is about 100 sccm to about 20000 sccm.

[0026] During the deposition of the first material layer 104 of SiO_2 , a first RF power is applied to the first silicon-containing gas, the oxygen-containing gas, and the first dilution gas. In one embodiment, the showerhead 319 having a symmetric RF circuit 402 disposed therein connected to a RF power source 321 by a RF feed 323 having a plurality of portions 344 to allow for a symmetric application of the first RF power. Each portion of the plurality of portions is connected to the symmetric RF circuit 402 so that the supply of RF power to the symmetric RF circuit 402 is symmetric. A symmetric application of the first RF power allows for deposition of the first material layer 104 of SiO_2 with improved residual uniformity to minimize IPD and improve lithographic overlay of the layer stack 110 of ON layers. In one embodiment, IPD of the layer stack 110 of ON layers is reduced by 10 percent.

[0027] In one embodiment, the first material layer 104 is exposed to a post-deposition treatment process. At optional operation 504, after the deposition of the first

material layer 104 of SiO_2 , the flow of the first silicon-containing gas is discontinued, and the flow of the oxygen-containing gas and the flow of the first dilution gas are continued. The flow of the first silicon-containing gas is discontinued, and the flow of the oxygen-containing gas and the flow of the first dilution gas are continued to stabilize the plasma. The tuning circuit 342 of the bottom tuner assembly 340 is utilized to modulate the impedance on the tuning electrode 313 to increase bombardment of the remaining plasma in the processing volume 307 on the substrate 102. Increasing bombardment of the remaining plasma in the processing volume 307 on the substrate 102 reduces the stress non-uniformity of the first material layer 104. Reducing the stress non-uniformity of the first material layer 104 minimizes IPD and improves lithographic overlay of the layer stack 110 of ON layers.

[0028] At operation 505, a second material layer 106 of silicon nitride (Si_3N_4) is deposited. During operation 505, a second silicon-containing gas at a second silicon-containing gas flow rate, a nitrogen-containing gas at a nitrogen-containing gas flow rate, and a second dilution gas at a first dilution gas flow rate are delivered to the process chamber 214a.

[0029] In one embodiment, the flow controller 317 disposed between the first gas source 306 and the process chamber 214a controls the second silicon-containing gas flow rate of the second silicon-containing gas provided to showerhead 319 that distributes the second silicon-containing gas across the processing volume 307 of the process chamber 214a. The second silicon-containing gas may include at least one of SiH_4 and Si_2H_6 . In another embodiment, the flow controller 328 disposed between the second gas source 332 and the process chamber 214a controls the nitrogen-containing gas flow rate of the nitrogen-containing gas provided to showerhead 319 that distributes the nitrogen-containing gas across the processing volume 307 of the process chamber 214a. The nitrogen-containing gas may include at least one of ammonia (NH_3) and N_2 . In yet another embodiment, the flow controller 330 disposed between the third gas source 334 and the process chamber 214a controls the second dilution gas flow rate of the second dilution gas provided to showerhead 319 that distributes the second dilution gas across the processing volume 307 of the process chamber 214a. The second dilution gas may include at least one of N_2 , Ar, and He. The second dilution gas flow rate is selected to improve the residual uniformity of the second material layer 106 of Si_3N_4 and reduce IPD by 50 percent. In one embodiment,

the second dilution gas is N_2 and the second dilution gas flow rate is greater than about 2000 sccm. Increasing the flow of N_2 or Ar may improve the plasma uniformity during deposition to reduce IPD. In some embodiments, the second silicon-containing gas flow rate is about 30 standard cubic centimeters per minute (sccm) to about 300 sccm, the nitrogen-containing gas flow rate is about 200 sccm to about 7000 sccm, and the first dilution gas flow rate is about 500 sccm to about 3000 sccm.

[0030] During the deposition of the second material layer 106 of Si_3N_4 , a second RF power is applied to the second silicon-containing gas, the nitrogen-containing gas, and the second dilution gas. In one embodiment, the showerhead 319 having the symmetric RF circuit 402 disposed therein is connected to the RF power source 321 by the RF feed 323 to allow for a symmetric application of the second RF power. A symmetric application of the second RF power allows for deposition of the second material layer 106 of Si_3N_4 with improved residual uniformity to minimize IPD and improve lithographic overlay of the layer stack 110 of ON layers.

[0031] In one embodiment, the second material layer 106 is exposed to a post-deposition treatment process. At optional operation 506, after the deposition of the second material layer 106 of Si_3N_4 , the flow of the second silicon-containing gas is discontinued, and the flow of the nitrogen-containing gas and the flow of the second dilution gas are continued. The flow of the second silicon-containing gas is discontinued, and the flow of the nitrogen-containing gas and the flow of the second dilution gas are continued to stabilize the plasma. The tuning circuit 342 of the bottom tuner assembly 340 is utilized to modulate the impedance on the tuning electrode 313 to increase bombardment of the remaining plasma in the processing volume 307 on the substrate 102. Increasing bombardment of the remaining plasma in the processing volume 307 on the substrate 102 reduces the stress non-uniformity of the first material layer 104. Reducing the stress non-uniformity of the first material layer 104 minimizes IPD and improves lithographic overlay of the layer stack 110 of ON layers.

[0032] At operation 507, operation 503, optional operation 504, operation 505, and optional operation 506 are repeated until a desired number of material layer pairs 108 of the first material layer 104 of SiO_2 and the second material layer 106 of Si_3N_4 make up a layer stack 110. In one embodiment, 64 material layer pairs 108 make up the layer stack 110.

[0033] At operation 508, the substrate 102 is transferred to a RTP chamber 210a. In one embodiment, the second robotic arm 212 transfers the substrate 102 from the process chamber 214a of the PECVD system 208a to a RTP chamber 210a of the processing system 200. At operation 509, the layer stack 110 is annealed at an annealing temperature greater than about 800 °C. Annealing at the annealing temperature greater than about 800 °C improves the residual uniformity of the layer stack 110 of ON layers by stress relaxation to minimize IPD and improve lithographic overlay. In one embodiment, IPD of the layer stack 110 of ON layers is reduced by 50 percent.

[0034] Figure 6 is a flow diagram of a method 600 of manufacturing layer stacks of ON layers with minimized IPD and improved lithographic overlay. At operation 601 a substrate 102 is transferred to a process chamber 214a of a PECVD system 208a. At operation 602, the pedestal 309 is heated to a deposition temperature of about 550 °C to about 650 °C. At operation 603, a first material layer 104 of silicon dioxide (SiO_2) is deposited. During operation 603, a first silicon-containing gas at a first silicon-containing gas flow rate, an oxygen-containing gas at an oxygen-containing gas flow rate, and a first dilution gas at a first dilution gas flow rate are delivered to the process chamber 214a. During the deposition of the first material layer 104 of SiO_2 , a first RF power is applied symmetrically to the first silicon-containing gas, the oxygen-containing gas, and the first dilution gas. A symmetric application of the first RF power allows for deposition of the first material layer 104 of SiO_2 with improved residual uniformity to minimize IPD and improve lithographic overlay of the layer stack 110 of ON layers.

[0035] At operation 604, a second material layer 106 of silicon nitride (Si_3N_4) is deposited. During operation 604, a second silicon-containing gas at a second silicon-containing gas flow rate, a nitrogen-containing gas at a nitrogen-containing gas flow rate, and a second dilution gas at a first dilution gas flow rate are delivered to the process chamber 214a. The second dilution gas flow rate is selected to improve the residual uniformity of the second material layer 106 of Si_3N_4 and reduce IPD by 50 percent. In one embodiment, the second dilution gas is N_2 and the second dilution gas flow rate is greater than about 2000 sccm. During the deposition of the second material layer 106 of Si_3N_4 , a second RF power is applied symmetrically to the second silicon-containing gas, the nitrogen-containing gas, and the second dilution gas. A symmetric application of the second RF power allows for deposition of the second

material layer 106 of Si_3N_4 with improved residual uniformity to minimize IPD and improve lithographic overlay of the layer stack 110 of ON layers.

[0036] At operation 605, operation 603, depositing the first material layer 104 of SiO_2 , and operation 604, depositing the second material layer 106 of Si_3N_4 , are repeated until a first portion of a desired number of material layer pairs 108 of the first material layer 104 of SiO_2 and the second material layer 106 of Si_3N_4 that make up a layer stack 110 is deposited. In one embodiment, 64 material layer pairs 108 make up the layer stack 110 and the first portion of the desired number of material layer pairs 108 is 32 material layer pairs 108. In another embodiment, the substrate 102 is rotated 180° after half of the first portion of the desired number of material layer pairs 108 is deposited. Rotating the substrate 102 accounts for non-uniformity within the process chamber 214a to reduce the IPD of the layer stack 110. At operation 606, the substrate 102 is transferred to a process chamber 214b of a PECVD system 208a. In one embodiment, the second robotic arm 212 transfers the substrate 102 from the process chamber 214a of the PECVD system 208a to the process chamber 214b of a PECVD system 208a.

[0037] At operation 607, the pedestal 310 is heated to the deposition temperature of about 550°C to about 650°C . Transferring the substrate 102 during the method 600 of forming a layer stack of ON layers allows for improved matching of IPD of the layer stack 110 formed on each pedestal of the process chambers 214a-214d for improved lithographic overlay. For example, the IPD of a layer stack 110 of ON layers formed in the process chamber 214a may be different the IPD of a layer stack 110 of ON layers formed in the process chamber 214b. Transferring the substrate 102 during the method 600 of forming a layer stack of ON layers averages the variation of IPD of the process chamber 214a and the process chamber 214b to match the IPD of the layer stack 110 formed in each process chamber.

[0038] At operation 608, operation 603, depositing the first material layer 104 of SiO_2 , and operation 604, depositing the second material layer 106 of Si_3N_4 , are repeated until a second portion of a desired number of material layer pairs 108 of the first material layer 104 of SiO_2 and the second material layer 106 of Si_3N_4 that make up a layer stack 110. In one embodiment, 64 material layer pairs 108 make up the layer stack 110 and the second portion of the desired number of material layer pairs 108 is

32 material layer pairs 108. In another embodiment, the substrate 102 is rotated 180° after half of the second portion of the desired number of material layer pairs 108 is deposited. Rotating the substrate 102 accounts for non-uniformity within the process chamber 214b to reduce the IPD of the layer stack 110. At operation 609, the substrate 102 is transferred to a RTP chamber 210a. In one embodiment, the second robotic arm 212 transfers the substrate 102 from the process chamber 214b of the PECVD system 208a to a RTP chamber 210a of the processing system 200. At operation 610, the layer stack 110 is annealed at an annealing temperature greater than about 800 °C. Annealing at the annealing temperature greater than about 800 °C improves the residual uniformity of the layer stack 110 of ON layers by stress relaxation to minimize IPD and improve lithographic overlay. In one embodiment, IPD of the layer stack 110 of ON layers is reduced by 50 percent.

[0039] In summation, methods of manufacturing layer stacks of ON layer with minimized IPD and improved lithographic overlay and a showerhead configured to form a substantially uniform plasma are described herein. During the deposition of the first material layer of SiO₂ and the second material layer of Si₃N₄ RF power is applied symmetrically by the showerhead to the first silicon-containing gas, the oxygen-containing gas, and the first dilution gas. A symmetric application of the RF power allows for deposition of the first material layer of SiO₂ and the second material layer of Si₃N₄ with improved residual uniformity to minimize IPD and improve lithographic overlay of the layer stack of ON layers. The second dilution gas flow rate is selected to improve the residual uniformity of the second material layer of Si₃N₄ and reduce IPD. Transferring the substrate allows for differences of IPD of the layer stack formed on each pedestal of the process chambers to be eliminated for improved lithographic overlay. Annealing at the annealing temperature greater than about 800 °C improves the residual uniformity of the layer stack of ON layers by stress relaxation to minimize IPD and improve lithographic overlay.

While the foregoing is directed to examples of the present disclosure, other and further examples of the disclosure may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.

What is claimed is:

1. A method of forming a layer stack of oxide/nitride (ON) layers, comprising:
transferring a substrate to a process chamber;
heating a pedestal retaining the substrate to a deposition temperature;
flowing a first silicon-containing gas at a first silicon-containing gas flow rate, an oxygen-containing gas at an oxygen-containing gas flow rate, and a first dilution gas at a first dilution gas flow rate into the process chamber;
symmetrically applying a first radio frequency (RF) power to the first silicon-containing gas, the oxygen-containing gas, and the first dilution gas to form a first material layer of silicon dioxide (SiO_2);
flowing a second silicon-containing gas at a second silicon-containing gas flow rate, a nitrogen-containing gas at a nitrogen-containing gas flow rate, and a second dilution gas at a second dilution gas flow rate into the process chamber;
symmetrically applying a second RF power to the second silicon-containing gas, the nitrogen-containing gas, and the second dilution gas to form a second material layer of silicon nitride (Si_3N_4); and
repeating the flowing the first silicon-containing gas, the oxygen-containing gas, and the first dilution gas, the symmetrically applying the first RF power, the flowing the second silicon-containing gas, the nitrogen-containing gas, and the second dilution gas, and the symmetrically applying the second RF power until a desired number of material layer pairs of the first material layer and the second material layer make up a layer stack.
2. The method of claim 1, further comprising:
transferring the substrate from the process chamber to a Rapid Thermal Processing (RTP) chamber; and
annealing at an annealing temperature greater than about 800 °C.
3. The method of one of claims 1 or 2, wherein the deposition temperature is about 500 degrees (°C) to about 650 °C.
4. The method of one of claims 1-3, wherein the first silicon-containing gas comprises at least one of silane (SiH_4), tetraethyl orthosilicate (TEOS), and disilane (Si_2H_6), the oxygen-containing gas comprises at least one of nitrous oxide (N_2O),

oxygen gas (O_2), and trioxxygen (O_3), and the first dilution gas comprises at least one of nitrogen gas (N_2), argon (Ar), and helium (He).

5. The method of one of claims 1-4, wherein the second silicon-containing gas comprises at least one of SiH_4 and Si_2H_6 , the nitrogen-containing gas comprises at least one of ammonia (NH_3) and N_2 , and the second dilution gas comprises at least one of N_2 , Ar, and He.

6. The method of one of claims 1-5, wherein the first silicon-containing gas flow rate is about 600 standard cubic centimeters per minute (sccm) to about 5000 sccm, the oxygen-containing gas flow rate is about 500 sccm to about 15000 sccm, and the first dilution gas flow rate is about 100 sccm to about 20000 sccm.

7. The method of one of claims 1-6, wherein the second silicon-containing gas flow rate is about 30 sccm to about 300 sccm, the nitrogen-containing gas flow rate is about 2000 sccm to about 7000 sccm, and the second dilution gas flow rate is about 500 sccm to about 3000 sccm.

8. A method of forming a layer stack of oxide/nitride (ON) layers, comprising:
transferring a substrate to a first process chamber;
heating a first pedestal of the first process chamber retaining the substrate to a deposition temperature;

flowing a first silicon-containing gas at a first silicon-containing gas flow rate, an oxygen-containing gas at an oxygen-containing gas flow rate, and a first dilution gas at a first dilution gas flow rate into the first process chamber;

symmetrically applying a first radio frequency (RF) power to the first silicon-containing gas, the oxygen-containing gas, and the first dilution gas to form a first material layer of silicon dioxide (SiO_2);

flowing a second silicon-containing gas at a second silicon-containing gas flow rate, a nitrogen-containing gas at a nitrogen-containing gas flow rate, and a second dilution gas at a second dilution gas flow rate into the first process chamber;

symmetrically applying a second RF power to the second silicon-containing gas, the nitrogen-containing gas, and the second dilution gas to form a second material layer of silicon nitride (Si_3N_4);

repeating the flowing the first silicon-containing gas, the oxygen-containing gas, and the first dilution gas, the symmetrically applying the first RF power, the flowing the

second silicon-containing gas, the nitrogen-containing gas, and the second dilution gas, and the symmetrically applying the second RF power until a first portion of a desired number of material layer pairs of the first material layer and the second material layer make up a layer stack;

transferring the substrate from the first process chamber to a second process chamber;

heating a second pedestal of the second process chamber retaining the substrate to the deposition temperature; and

repeating the flowing the first silicon-containing gas, the oxygen-containing gas, and the first dilution gas, the symmetrically applying the first RF power, the flowing the second silicon-containing gas, the nitrogen-containing gas, and the second dilution gas, and the symmetrically applying the second RF power until a second portion of the desired number of the material layer pairs of the first material layer and the second material layer make up the layer stack.

9. The method of claim 8, further comprising:

transferring the substrate from the second process chamber to a Rapid Thermal Processing (RTP) chamber; and

annealing at an annealing temperature greater than about 800 °C.

10. The method of one of claims 10 or 11, wherein the first silicon-containing gas comprises at least one of silane (SiH_4), tetraethyl orthosilicate (TEOS), and disilane (Si_2H_6), the oxygen-containing gas comprises at least one of nitrous oxide (N_2O), oxygen gas (O_2), and trioxygen (O_3), and the first dilution gas comprises at least one of nitrogen gas (N_2), argon (Ar), and helium (He).

11. The method of one of claims 8-10, wherein the second silicon-containing gas comprises at least one of SiH_4 and Si_2H_6 , the nitrogen-containing gas comprises at least one of ammonia (NH_3) and N_2 , and the second dilution gas comprises at least one of N_2 , Ar, and He.

12. The method of one of claims 8-11, wherein the first silicon-containing gas flow rate is about 600 standard cubic centimeters per minute (sccm) to about 5000 sccm, the oxygen-containing gas flow rate is about 500 sccm to about 15000 sccm, and the first dilution gas flow rate is about 100 sccm to about 20000 sccm.

13. The method of one of claims 8-12, wherein the second silicon-containing gas flow rate is about 30 sccm to about 300 sccm, the nitrogen-containing gas flow rate is about 200 sccm to about 7000 sccm, and the second dilution gas flow rate is about 500 sccm to about 3000 sccm.

14. The method of one of claims 8-13, wherein the second dilution gas is N₂ and the second dilution gas flow rate is greater than about 2000 sccm.

15. A showerhead, comprising:

a symmetric radio frequency (RF) circuit disposed in the showerhead connected to a RF power source by a RF feed having a four portions connected to the symmetric RF circuit at 90 degree intervals.

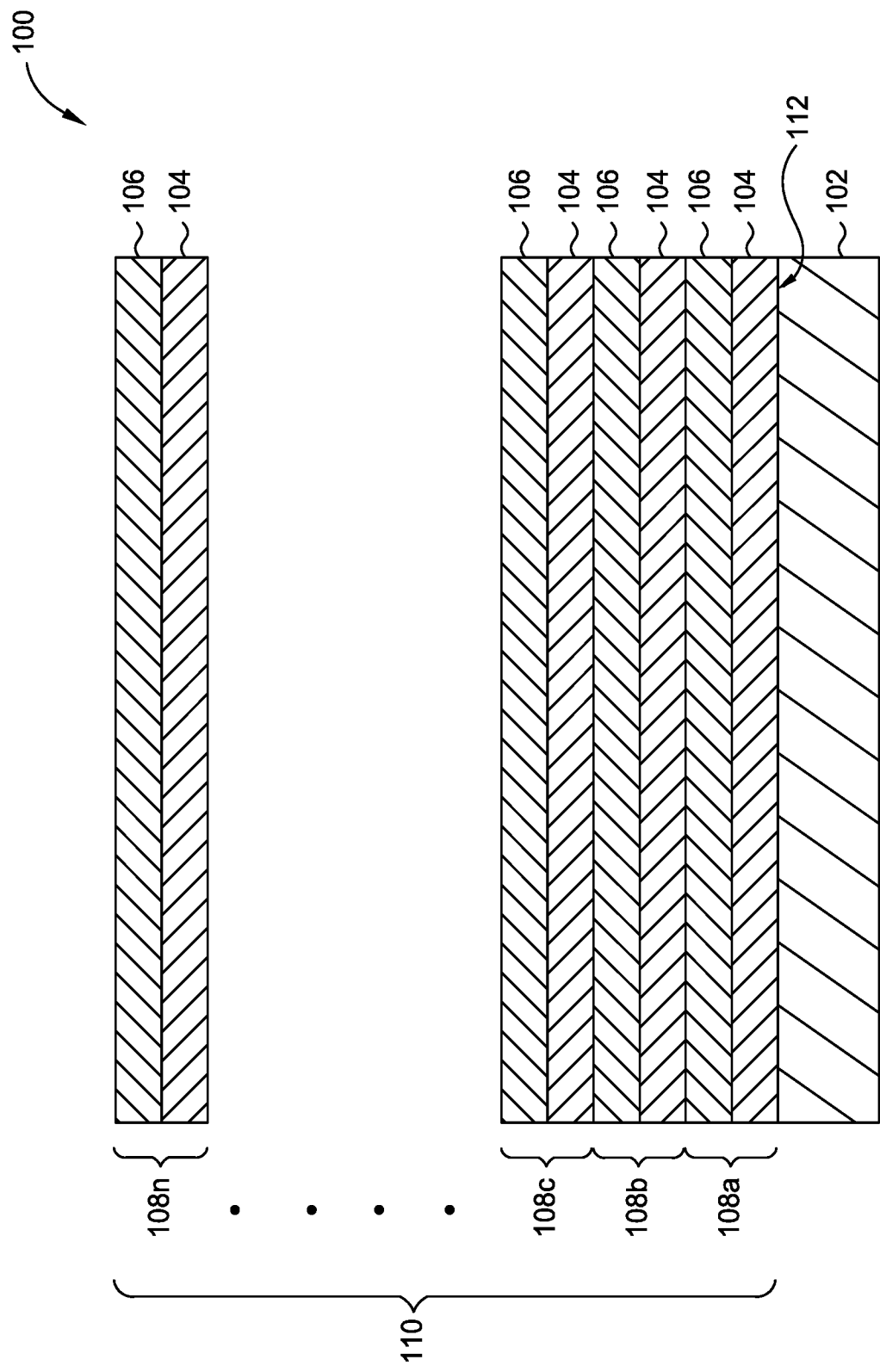


FIG. 1

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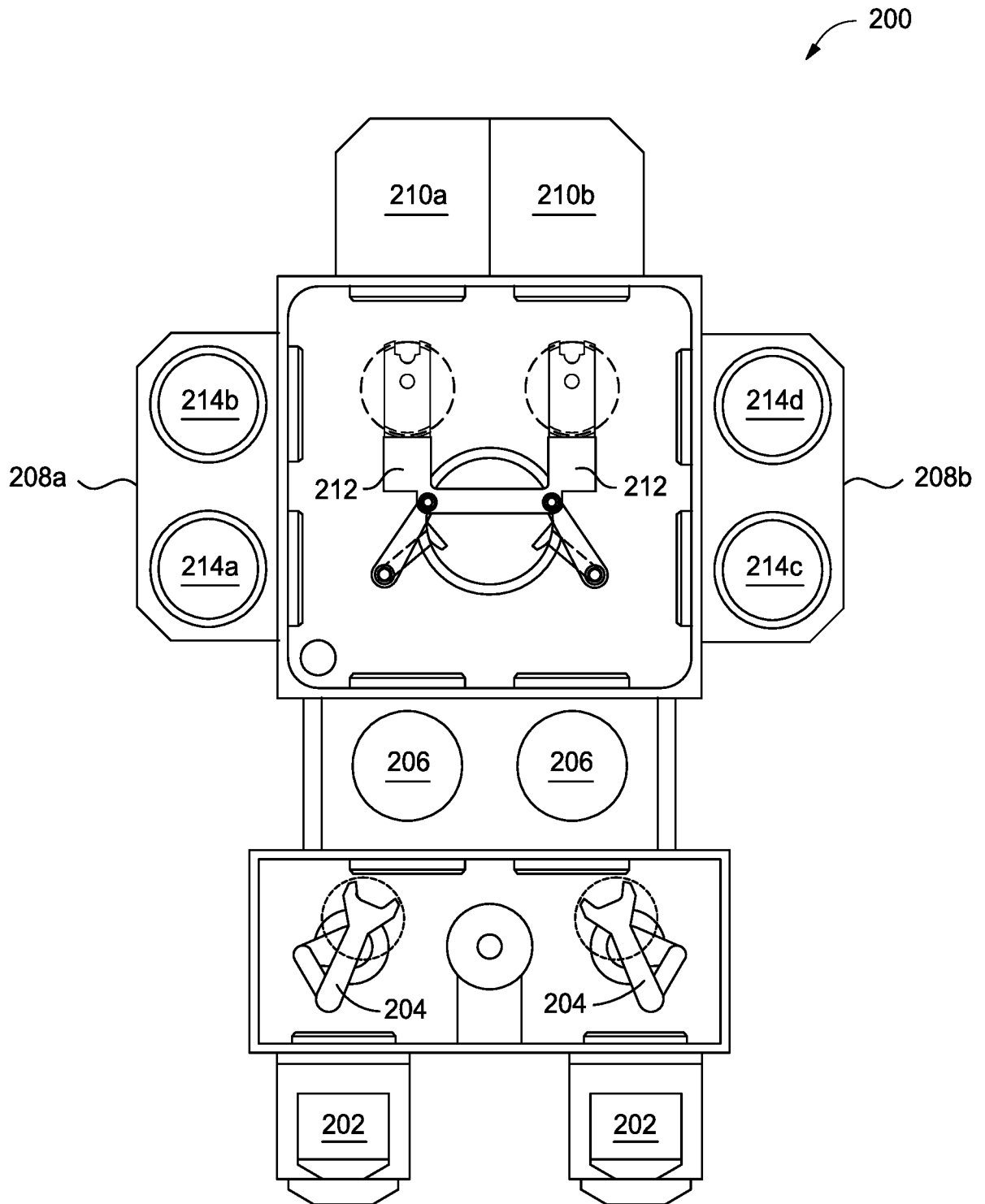


FIG. 2

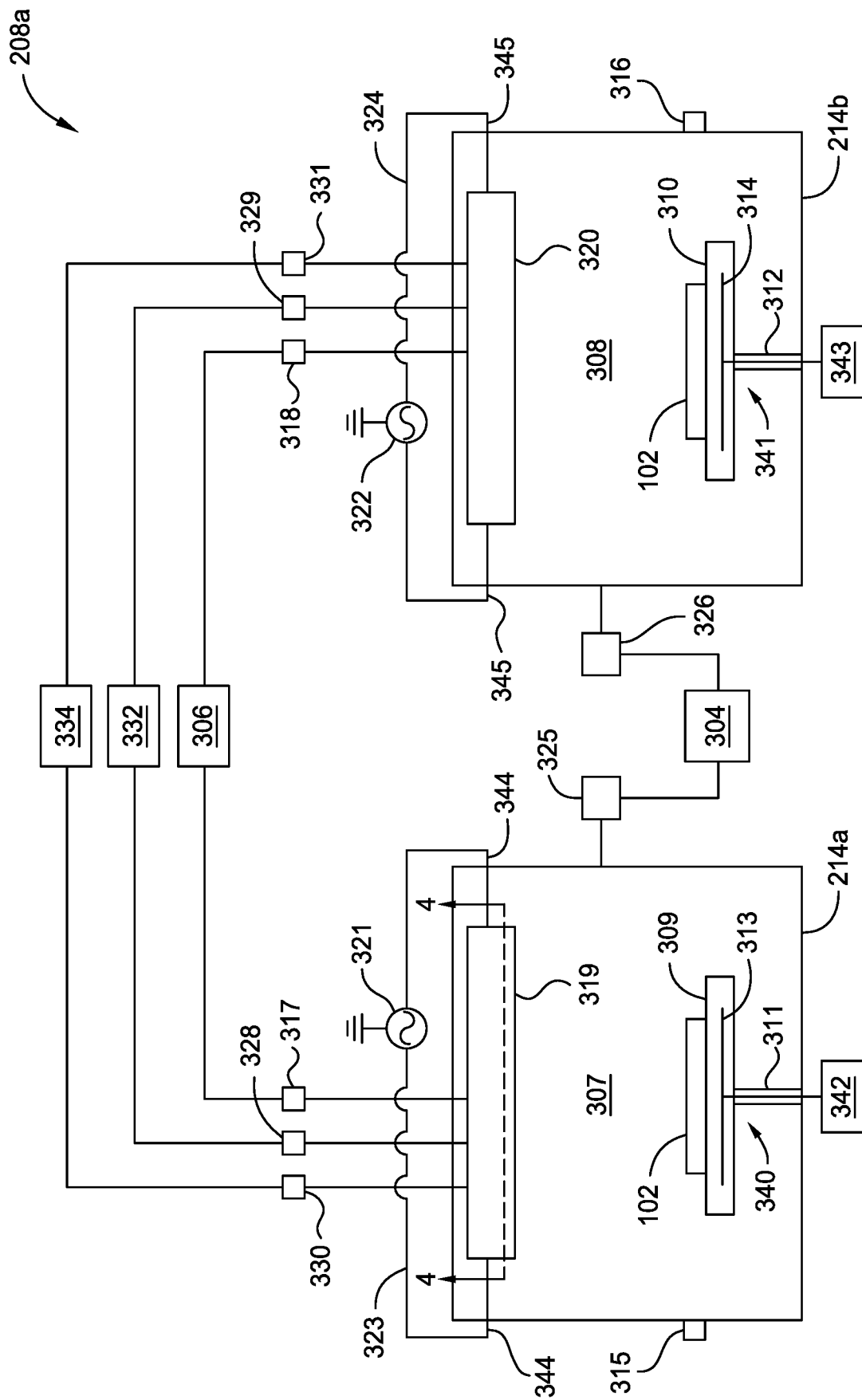


FIG. 3

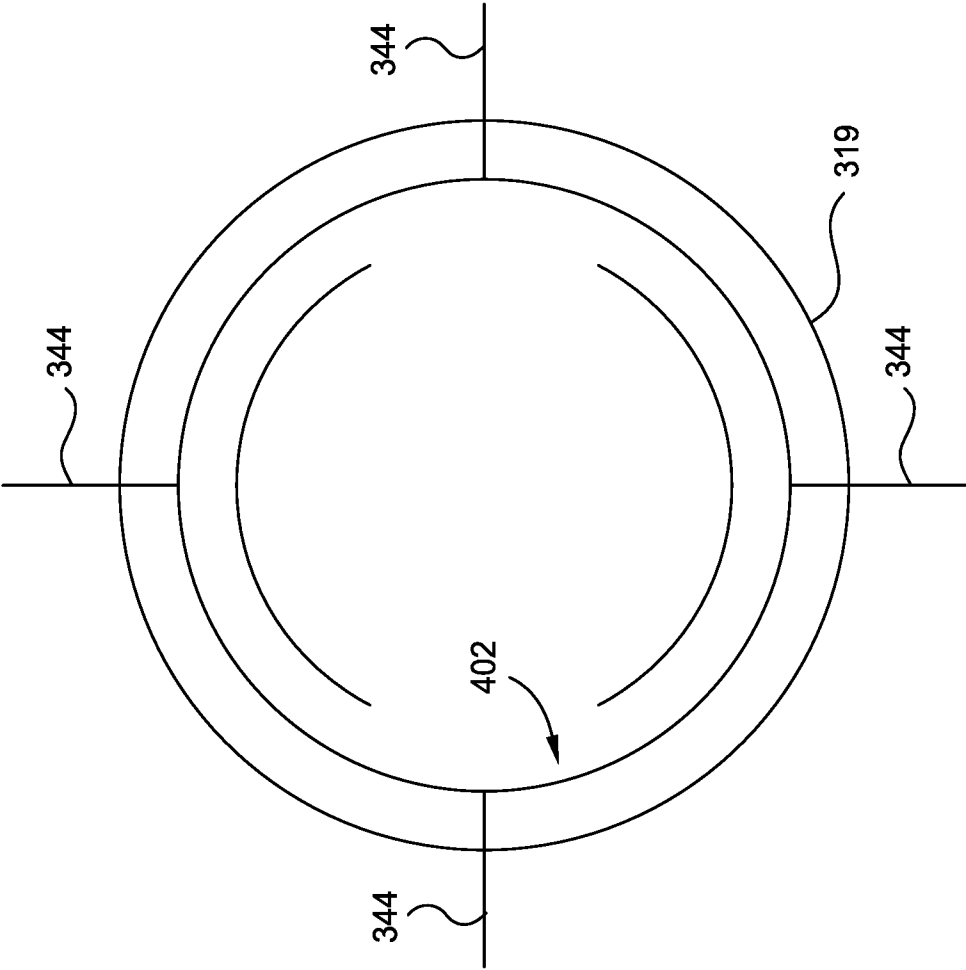


FIG. 4

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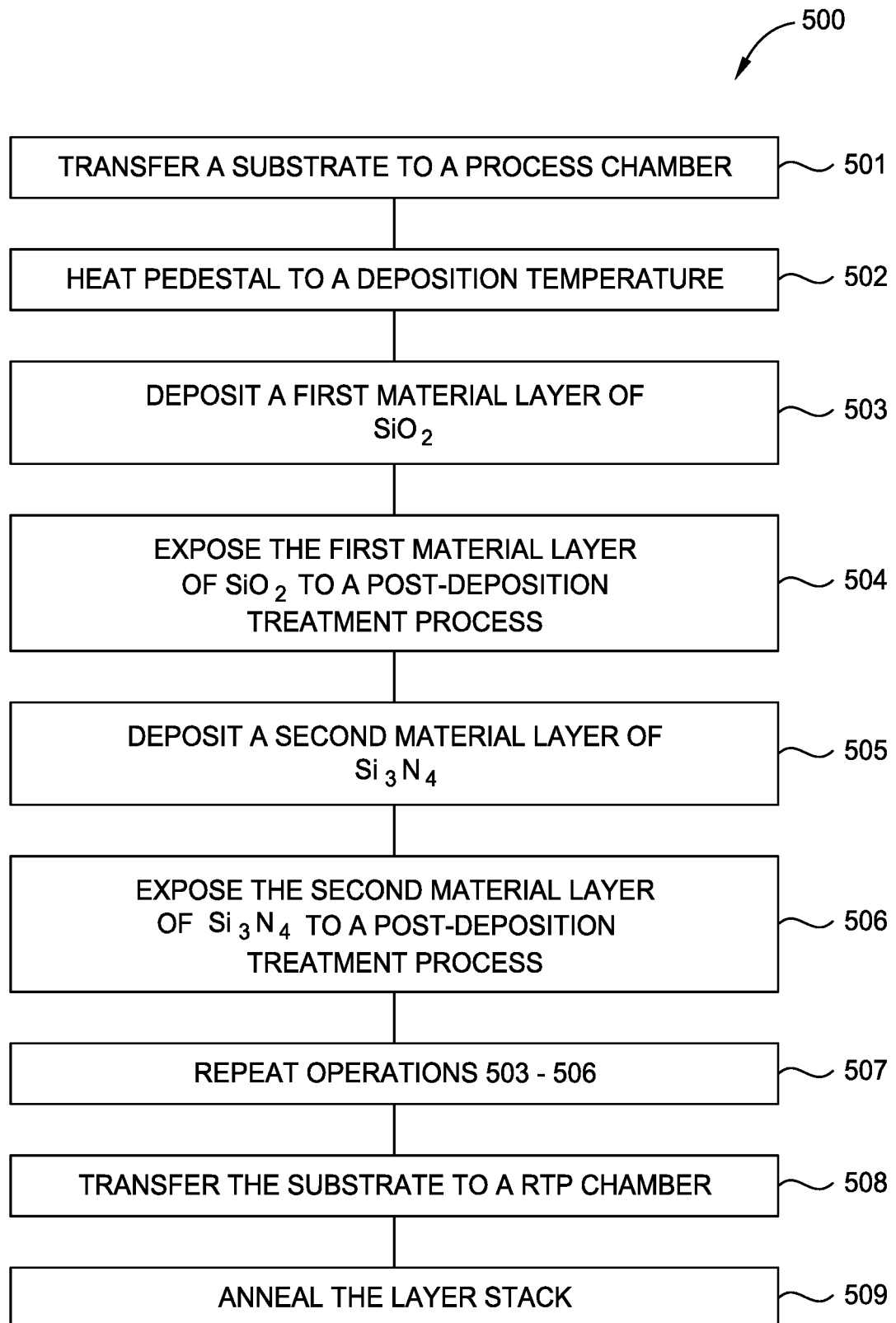


FIG. 5

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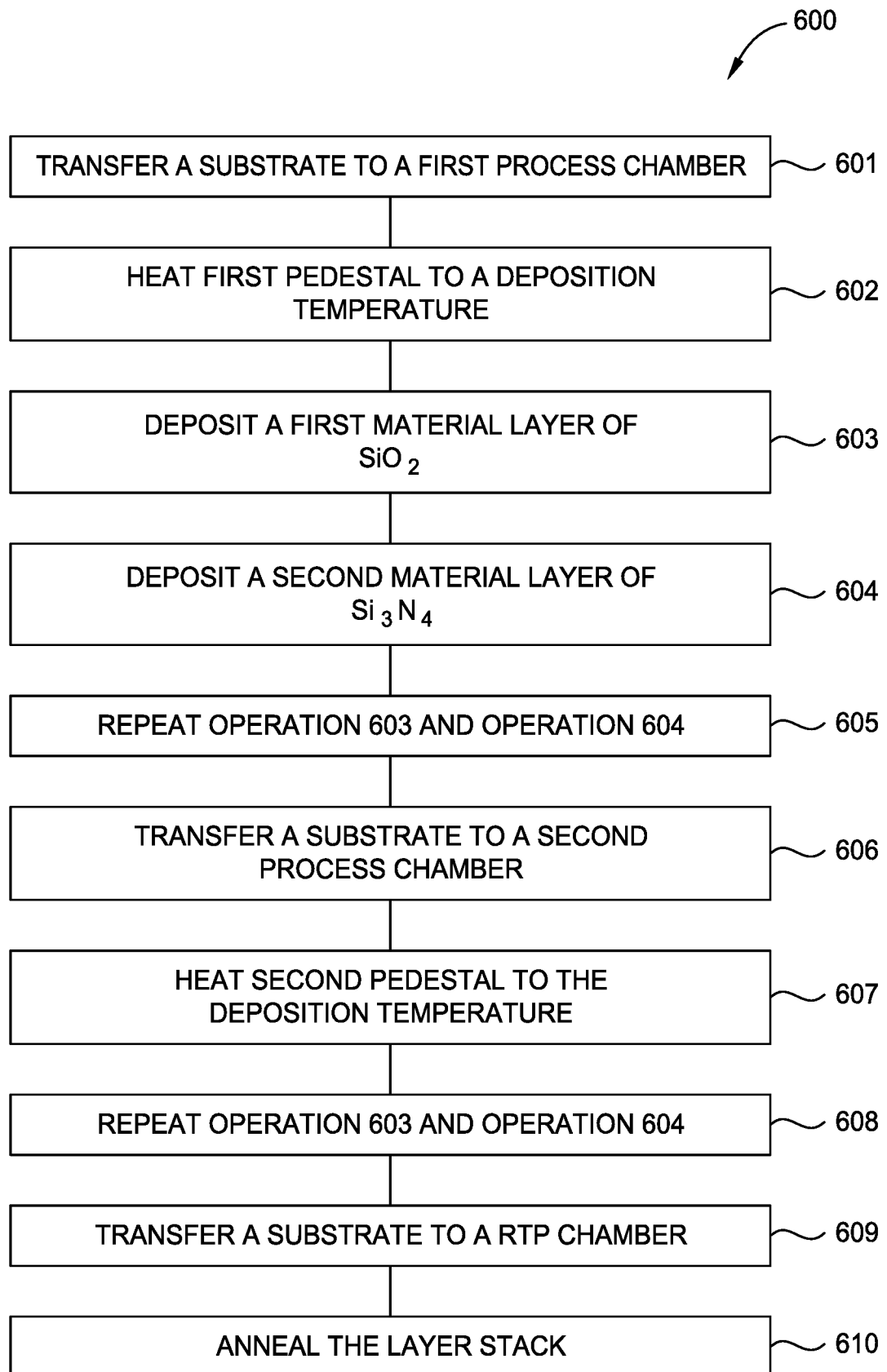


FIG. 6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2019/042489**A. CLASSIFICATION OF SUBJECT MATTER****H01L 21/02(2006.01)i, H01L 21/768(2006.01)i, H01L 27/11524(2017.01)i, H01L 21/67(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/02; C23C 16/505; H01J 37/32; H01L 21/316; H01L 21/318; H01L 21/336; H01L 21/67; H01L 29/786; H05H 1/24; H01L 21/768; H01L 27/11524

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: PECVD, silicon, oxide, nitride, RF, symmetric, showerhead

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2012-0009356 A1 (SOO YOUNG CHOI et al.) 12 January 2012 See paragraphs [0011], [0027], claims 16-17 and figure 1A.	15
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A	US 2016-0027667 A1 (APPLIED MATERIALS, INC.) 28 January 2016 See the whole document.	1-15



Further documents are listed in the continuation of Box C.



See patent family annex.

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

06 November 2019 (06.11.2019)

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Information on patent family members

International application No.

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