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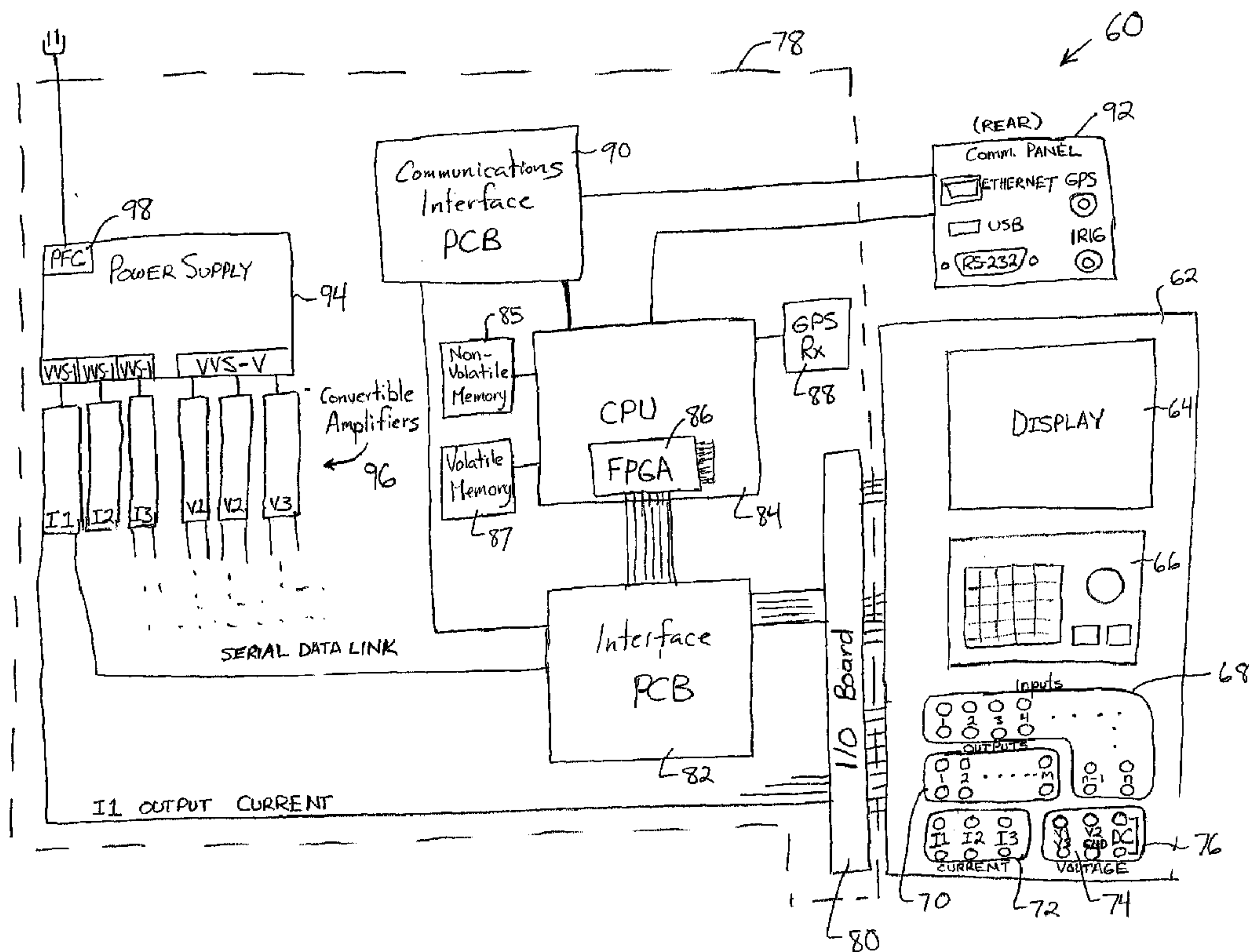
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(54) **Titre : SYSTEME ET PROCEDE POUR MODULER UNE ALIMENTATION EN ELECTRICITE DANS UN SYSTEME D'ESSAI A
RELAIS**

(54) **Title: SYSTEM AND METHOD FOR MODULATING A POWER SUPPLY IN A RELAY TEST SYSTEM**



(57) **Abrégé/Abstract:**

A system and method are provided for modulating a power supply in a relay test system having an amplifier. The system includes a control system separating the power supply and the amplifier and is configured to operate according to a class H modulation



(57) Abrégé(suite)/Abstract(continued):

scheme. The system also includes a gate drive sense circuit for providing a gate drive intensity signal input to the control system indicative of the extent to which an output switching mechanism for the amplifier is being operated, and a voltage difference circuit for monitoring a difference between an output of the amplifier and a power supply rail from the power supply to provide a voltage difference signal to the control system. The control system is operated according to the class H modulation scheme using readings taken from the voltage difference signal and the gate drive intensity signal to generate a control signal for the power supply.

ABSTRACT

A system and method are provided for modulating a power supply in a relay test system having an amplifier. The system includes a control system separating the power supply and the amplifier and is configured to operate according to a class H modulation scheme. The system also includes a gate drive sense circuit for providing a gate drive intensity signal input to the control system indicative of the extent to which an output switching mechanism for the amplifier is being operated, and a voltage difference circuit for monitoring a difference between an output of the amplifier and a power supply rail from the power supply to provide a voltage difference signal to the control system. The control system is operated according to the class H modulation scheme using readings taken from the voltage difference signal and the gate drive intensity signal to generate a control signal for the power supply.

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1 techniques becomes difficult because while attempting to test the characteristics of a particular
2 element, other elements often operate.

3 **[0006]** Accordingly, modern testing of relays has become an exercise in how to minimize the
4 number of times that the settings are altered, and/or to minimize the number of times needed to
5 block an element. This can be not only a waste of time, but may pose a risk in that a relay could
6 potentially be put back in service with incorrect settings or have incorrect functionality.

7 **[0007]** Some utilities have recognized the apparent futility of routine testing of the relay
8 algorithms. Also, some utilities are beginning to test in a more sensible fashion where the focus
9 is now on verifying correct operation of the protection scheme as a whole instead of the
10 individual relays. The protection scheme typically includes the protective relays, the remote
11 tripping communication equipment, the breaker trip and breaker failure circuits, as well as all
12 interconnection wiring. This type of testing is often referred to as end to end testing.

13 **[0008]** End to end testing typically requires more sophisticated testing equipment and set up.
14 When performing end to end testing, the response from the relay and auxiliary equipment is
15 dependent both on the nature of the fault simulated, as well as the response from the remote
16 equipment. As such, it may be necessary to generate numerous fault scenarios simultaneously at
17 all ends of the line or element in the circuit to verify correct operation of the protection scheme.

18 **[0009]** End to End practices vary from utility to utility. In general the following steps are
19 taken: the generation of fault data (the "fault study"); fault data distribution; outage, blocking,
20 and test equipment preparation; coordinated fault playback; analysis of results; and protection
21 restoration.

22 **[0010]** In most situations, the fault cases are generated using one of the established industry
23 standard power system modeling programs such as Electro Magnetic Transient Program
24 (EMTP), or Computer-Aided Protection Engineering (CAPE). These programs can accurately
25 calculate all the relevant power system quantities for any type of fault regardless of the
26 complexity of the system. This often requires a significant amount of time for entering all of the
27 required data to accurately model a particular portion of the power system. These programs can

1 be considered complex, and are usually only used by a senior protection engineer that is
2 responsible for the overall system. Numerous fault studies may be done to simulate typical “in-
3 and-out-of-zone” fault scenarios.

4 **[0011]** Once the various fault conditions have been simulated, the fault data is transferred
5 from the simulation computer to the test equipment, which then plays back the scaled down
6 secondary quantities seen by the protective relays. Many utilities store and/or transfer the fault
7 data using the industry standard Common Format for Transient Data Exchange (COMTRADE).
8 Most if not all of the major test-set manufacturers support COMTRADE because it is flexible,
9 scalable, and accommodates non-sinusoidal waveform data. Using COMTRADE does present a
10 few problems. One such problem is that files are often very large, and in some cases
11 incompatible with other vendor equipment due to ongoing changes in the standard. Also, in most
12 cases, the end user is forced to calculate and enter scale factors to scale the data to secondary
13 values.

14 **[0012]** Some utilities have resorted to a more straightforward method to record and transfer
15 the fault data required for end to end testing. For example, a spreadsheet may be developed for
16 each fault case, which tabulates the data in a simple table showing the amplitude and phase angle
17 for the various stages of the fault. This method has several benefits, such as being intuitive, using
18 industry standard software, having a relatively small file size, and not requiring scaling in the
19 field to name a few. The data in the spreadsheet may then be extracted for or by the test
20 equipment to run the test(s).

21 **[0013]** A typical line protection scheme may rely on a redundant protection system having
22 two nearly identical protection schemes often referred to as the “A” and “B” protection. Each
23 protection is independent of the other with separate transducers, wiring, power supply (batteries),
24 trip coils in the circuit breaker etc. The “A” and “B” protections often use relays from different
25 manufacturers. In an ideal scenario, the routine protective relay maintenance (protection outage)
26 would occur while the line is out of service for maintenance (line outage), eliminating the
27 possibility of an inadvertent trip. On many lines the ideal situation described above rarely occurs
28 anymore for several reasons such as construction of new transmission lines that would allow line

1 outages is severely limited due to economic (construction costs) and/or environmental
2 (acquisition of new rights-of-way) issues; and the power system and particularly transmission
3 lines are being pushed to the limit, so line outages even if possible from a power transfer
4 perspective, reduce power system stability to an unacceptable level.

5 [0014] One result of such line outage limitations is that protective relay maintenance often
6 needs to be done while the line is in service. This type of testing is inherently more risky
7 because: 1) One of the two protections is temporarily blocked, eliminating the redundant
8 protection; and 2) The trip outputs of the relay being tested is exercised numerous times during
9 the maintenance test, and if a trip signal from the out of service relay is not blocked correctly, the
10 protection outage will quickly become an inadvertent line outage.

11 [0015] Outages are typically scheduled well in advance of the actual outage date. In some
12 cases an approved outage planned a year in advance is cancelled at the last moment due to
13 unexpected demand on the power system due to weather or unanticipated system conditions.
14 Assuming the outage proceeds, the protection technician sets up the test equipment and then
15 isolates the protection by opening the blocking switches connected to the trip outputs of the
16 relay. Next, the current transformer (CT) and potential transformer (PT) signals are isolated
17 from the relay. The output signals from the test set are then connected in place of the now
18 isolated CT and PT signals. Finally, the output signals from the relay are connected to the status
19 inputs of the test set.

20 [0016] At this stage, the technicians on either end of the line set up the test equipment with
21 the agreed upon test case. The two ends then simultaneously (with the help of a timing signal
22 provided by linked global positioning system (GPS) equipment) apply the fault. The various
23 relays operate, or do not operate, depending on the nature of the fault. The actual test is
24 performed most typically in less than one second.

25 [0017] The analysis of the resulting relay operations, targets, etc is then performed to verify
26 that the protection system operated as expected. This step varies from utility to utility, and even
27 within a utility. In the simplest case, the technician simply verifies the correct targets are
28 displayed on the relay and that the basic trip output of the relay operated or did not operate. More

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sophisticated users will analyze the sequence of events in more detail. However, detailed analysis can be time consuming and, more importantly, such analysis relies on the knowledge and experience of the technicians doing the test, which requires an understanding of how the system is supposed to respond to the particular fault case. Since technicians' skill levels can vary to a large degree, the analysis may be prone to error, or require the input of a more senior person.

[0018] When all testing is complete, the test equipment is disconnected, the CT and PT circuits are restored, and then the blocking switches are closed to restore the protection.

[0019] In one aspect, it is an object of the following to obviate or mitigate the above-noted disadvantages.

[0020] In another aspect, it is an object of the following to provide modulation for a power supply in an amplifier used in testing equipment for testing the above-described protective relays that minimizes power dissipation and noise, while balancing overall weight of the amplifier.

SUMMARY OF THE INVENTION

[0021] In one aspect, there is provided a system for modulating a power supply in a relay test system comprising an amplifier, the system comprising a control system separating the power supply and the amplifier and configured to operate according to a class H modulation scheme; an output switching mechanism connected to the control system; a drive intensity signal input into the digital signal processor indicative of the extent to which the output switching mechanism is being operated; and a voltage difference circuit for monitoring a difference between an output of the amplifier and a power supply rail; wherein the class H modulation scheme is operated according to readings taken from the voltage difference circuit and the drive intensity signal.

[0022] In another aspect, there is provided a method for performing an end-to-end test on a power system is provided comprising: obtaining a test case comprising end-to-end test parameters and at least one expected result for at least one corresponding test parameter; running the end-to-end test according to the test case; displaying an output indicative of actual results of

the end-to-end test; and for the at least one expected result, providing an indicator with the output showing how a corresponding one of the actual results differed from the expected result.

[0023] In yet another aspect, there is provided a computer readable medium comprising computer executable instructions for performing the method described above.

BRIEF DESCRIPTION OF THE DRAWINGS

[0024] An embodiment of the invention will now be described by way of example only with reference to the appended drawings wherein:

[0025] Figure 1 is a schematic diagram of an end to end testing arrangement for a high voltage power line.

[0026] Figure 2 is a waveform illustrating pre-fault, fault and post-fault current and voltage signals.

[0027] Figure 3 is a schematic block diagram of a protective relay under test and test equipment therefor.

[0028] Figure 4 is a schematic block diagram of a protective relay test system.

[0029] Figure 5 is a waveform illustrating a class H modulation scheme for a variable voltage power supply.

[0030] Figure 6 is a schematic block diagram of a portion of an amplifier for implementing class H.

[0031] Figure 7 is an electrical schematic for implementing the block diagram shown in Figure 6.

[0032] Figure 8 is a screen shot of a spreadsheet comprising fault test data.

[0033] Figure 9 is a screen shot of the spreadsheet shown in Figure 8 with predictive result data appended thereto.

[0034] Figure 10 provides a screen shot of a test result report for a passed fault test in view (a) and for a failed fault test in view (b) according to the test data defined in the spreadsheet of Figure 9.

[0035] Figure 11 is a screen shot of a test report menu for a fault test operated according to the test data defined in the spreadsheet of Figure 9.

[0036] Figure 12 is a screen shot of a graphical sequence of events displayed for manual fault test data.

[0037] Figure 13 is a screen shot of an input/output (I/O) set up menu for the sequence of events display.

DETAILED DESCRIPTION OF THE INVENTION

[0038] Referring first to Figure 1, an exemplary protective relay testing arrangement is generally denoted by numeral 10. In this example, a high voltage transmission line 12 between a power source 14 and a load 16 is protected by a first protective relay 18 towards the source end of the line 12 (denoted by "A"), and a second protective relay 20 towards the load end of the line 12 (denoted by "B"). It will be appreciated that the line 12 is shown as a single phase or "1 line" transmission line for clarity only and that the line 12 may be instead (and is typically) a three phase or "3 line" transmission line. It will also be appreciated that the testing arrangement 10 is applicable to any portion of a power system infrastructure such as a generator, transformer etc.

[0039] Endpoint A of the testing arrangement 10 comprises an inline current transformer (CT) 22 for measuring current in the line 12, and a circuit breaker 24 for isolating the line 12. Similarly, endpoint B comprises a breaker 26 and CT 28 to complete the isolation. Each end also comprises a potential transformer (PT) 30 and 32 respectively for measuring voltage in the line 20. The first relay 18 at end A is connected to the CT 22 to measure current through push switch 34, is connected to the circuit breaker 36 to provide a trip signal for tripping the breaker 36 through on/off switch 36, and is connected to the PT 30 to measure voltage through on/off switch 38. It will be appreciated that the second relay 20 is connected to the circuit breaker 26,

1 CT 28 and PT 32 in a similar manner, namely through push switch 40, on/off switch 42, and
 2 on/off switch 44 respectively.

3 **[0040]** The protective relays 18, 20 are complex electromechanical apparatus, often having
 4 more than one coil, and are designed to calculate operating conditions on the transmission line
 5 12, and trip the circuit breakers 24, 26 when a fault is found. Unlike switching type relays with
 6 fixed and usually ill-defined operating voltage thresholds and operating times, the protective
 7 relays 18, 20 typically have well-established, selectable, time/current (or other operating
 8 parameter) curves. The protective relays 18, 20 are generally important to the reliability of the
 9 transmission infrastructure (including transmission line 12) and thus it is important that they are
 10 operating correctly.

11 **[0041]** Figure 2 shows voltage and current waveforms in a pre-fault stage 46 where the
 12 normal, expected sinusoidal waveforms are shown, during a common fault 48 (e.g. where an
 13 obstruction contacts the line 12), where the current rises dramatically as the voltage decreases,
 14 until a post fault stage 50 where the protection trips the breakers associated with the faulted
 15 section of the line 12 isolating the faulted section and causing the current and voltage to
 16 effectively go to zero.

17 **[0042]** As discussed above, and shown generally by way of example only in Figure 3, end to
 18 end testing may be accomplished by connecting the protective relay 18, 20 to a protective relay
 19 testing system or tester 60. As shown in Figure 3, a voltage output from the tester 60 is
 20 connected to the switch 38, a current output from the tester 60 is connected to switch 34 and the
 21 trip signal provided through switch 36 on the relay 18 is connected to an input to the tester 60. It
 22 will be appreciated that typically the voltage and current outputs are for three phase circuits and
 23 thus such connections would typically include three connections per voltage and three
 24 connections per current. The input and voltage and current outputs are shown in general in
 25 Figure 3 and further detail regarding these connections is provided below.

26 **[0043]** The tester 60 is shown in greater detail in Figure 4. The tester 60 is housed in a
 27 structural casing or box, the front panel of which is shown in Figure 4 and denoted by numeral
 28 62. The front panel 62 of the box provides, for the user, a display 64 for displaying textual and

graphical interfaces. The display 64 is preferably a liquid crystal display (LCD) and may itself provide an input mechanism by being a touch-screen (not shown). In the example shown in Figure 4, the tester 60 comprises an input panel 66 which may comprise any number of and/or combination of input mechanisms such as a keypad, scroll wheel, trackball, rotary knob, push buttons, arrow keys, touch screen etc. The input panel 66 enables the user, in conjunction with the display 62, to interact with the tester 60, provide commands, give feedback, receive feedback etc.

[0044] The front panel 62 also provides n status inputs 68, e.g. $n = 12$, for measuring various signals during the fault test; and m output contacts 70, e.g. $m = 4$, for outputting various signals to simulate events that would be seen by the relay 18 in an actual fault. An example would be feedback indicating whether or not the breaker is open or closed. In this example, the tester 60 performs fault testing on a 3 phase transmission line 12 and thus the front panel 62 also comprises 3 AC current outputs 72, and 3 AC voltage outputs 74. The front panel 62 further comprises a DC voltage output 76 for powering the relay under test 18 or for providing voltage to the output contacts 70 for powering other devices.

[0045] The tester 60 houses various electronic components, shown within the dashed lines in Figure 4. An input/output (I/O) board 80 provides a bridge between the inputs 68, outputs 70-76, input panel 66 and display 64, on the front panel 62, and an interface printed circuit board (PCB) 82. The interface PCB 82 is used to translate external connections to internal connections and routes the signals to the appropriate locations. Central to the operation of the tester 60 is a central processing unit (CPU) 84, which includes a field programmable gate array (FPGA) 86 connected thereto. The CPU 84 and FPGA 86 communicate with the interface PCB 82 for interacting with inputs and outputs; a GPS receiver 88 for receiving accurate time signals for end to end testing routines; and a communications interface PCB 90 and external communications panel 92, for uploading and downloading data and communicating with various media. As shown in Figure 4, the communication panel may be compatible with various communication standards, such as Ethernet, universal serial bus (USB), GPS, RS-232 (serial) and Inter-Range Instrumentation Group (IRIG). The CPU 84 also has access to non-volatile memory 85 such as flash or a hard drive and to volatile memory 87 such as random access memory (RAM).

1 [0046] The tester 60 also includes a variable voltage power supply 94, which connects to an
2 external power source through a power factor correction (PFC) circuit 98. The power supply 94
3 powers a series of convertible amplifiers 96. In this example, the tester 60 comprises three
4 current amplifiers (I1, I2 and I3), and three voltage amplifiers (V1, V2 and V3). As shown for
5 I1, each amplifier has a serial data link to the interface PCB 82 to obtain waveform data
6 information, and provides an output to the appropriate contact on the front panel 62, through the
7 I/O board 80.

8 [0047] It is generally desirable in a testing system such as those using the tester 60, to
9 modulate the power supply 94 to decrease losses in the amplifiers 64. Previous modulation
10 schemes have used either a class G arrangement (linear), or a class D arrangement (switched
11 mode). In a class G amplifier, "rail switching" is used to decrease power consumption and
12 increase efficiency. The class G amplifier has several power rails at different voltages, and
13 switches between rails as the signal output approaches each. Thus the amplifier increases
14 efficiency by reducing the "wasted" power at the output transistors. Despite the rail switching
15 used, class G amplifiers still tend to dissipate a significant amount of power and are often
16 relatively large in size as they require heat sinks to dissipate the resultant heat. Where high
17 power amplifiers such as the amplifiers 94 are used in relay testing, this can be exacerbated. In a
18 class D amplifier, although the power dissipation may be lower when compared to class G, noise
19 can be a problem, which is generally undesirable. There are two problems with noise, namely
20 the overall noise itself that can naturally be problematic, and consequently, such noise makes it
21 more difficult to provide accurate measurements at lower output levels.

22 [0048] It has been recognized that a low dissipation rate, lower overall weight for the tester,
23 and manageable noise can be achieved by modulating the power supply 94 using a class H
24 arrangement. In a class H arrangement, the idea of Class G efficiencies are taken one step
25 further creating an infinite number of supply rails. This is done by modulating the supply rails in
26 the power supply 94 so that the rails are only a few volts larger than the output signal at any
27 given time such that less power is wasted without clipping the signal. The output stage operates
28 near its maximum efficiency all of the time. The variable voltage switched (VVS) power supply

94 shown in Figure 4 is used to create the tracking rails. It has been found that significant gains may be achieved while avoiding the drawbacks of class G and class D arrangements.

[0049] Figure 5 shows an implementation of class H, which is substantially similar to the ideal waveform in standard class H. In the implementation shown, the non-loaded power supply rail approaches full output during the non-output portion of the waveform. This modulation scheme simplifies the power supply 94 and has been found to have only a negligible effect on efficiency, since the output field-effect transistor (FET) connected to the "high" rail (see Figures 6 and 7 explained below) is biased off during this period.

[0050] To implement class H to behave as shown in Figure 5, the amplifiers 96 can be constructed as shown in general terms in Figure 6. Typical implementations of class H are analog, which in this example would not provide adequate separation between the amplifier 96 and the power supply 94. In order to provide such separation along with several other benefits discussed below, a digital signal processor (DSP) 100, dealing with digital quantities, is used as a control system for implementing the class H scheme. The DSP 100 measures and analyzes numerous signals within the amplifier to determine the optimum drive signal required to drive the programmable power supply 94 in class H operation. Although the reaction time of a DSP 100 may be relatively slower than some analog solutions, the DSP 100 provides a suitable compromise due to its inherent programmability (and resultant intelligence) and by realizing efficiencies in the programmed algorithms used to modify the output. In this way, the DSP 100 is able to at least partially predict where the output is going. Moreover, the DSP 100 is flexible in that various algorithms can be programmed into the software and subsequently changed or updated. Two circuit portions that are important in implementing class H operation when using the DSP 100, are a gate drive sense circuit 102 and a delta-V measurement circuit 104. Implementations of circuits 102 and 104 are shown by way of example only in Figure 7.

[0051] The gate drive sense circuit 102, which in this embodiment comprises components U1a, R15, C19, R18, U8, R22, and the DSP 100, provides a gate drive intensity signal to the DSP 100 that is required to control the power supply 94 for class-H operation. The gate drive intensity signal tells the DSP 100 the extent to which the FET is being driven so that it knows

1 how to increase or decrease the operation of the FET to achieve the desired output. This enables
2 the DSP 100 to know and control how close the circuit is to the waveform without clipping the
3 waveform. U1a is configured as a standard differential amplifier with unity gain. U8 is an
4 isolated linear current sensing IC. The U1a with U8 sub-circuit scales the Q3 gate drive signal to
5 an appropriate level for the analog to digital converters 106 on the DSP 100. U8 is used because
6 the differential voltage between the DSP 100 and FET output circuit can range from a few volts
7 to several hundred volts depending on the instantaneous rail voltage.

8 **[0052]** The delta-V measurement circuit 104, which in this embodiment comprises
9 components U3, U31b, and the DSP 100, provides a signal proportional to the difference
10 between the power supply rail 108 and the amplifier output 110. As can be seen best in Figure 7,
11 VMON is a scaled down representation of the amplifier output voltage 110, and VDDMON is a
12 scaled down representation of the power supply positive rail voltage 108. In this embodiment,
13 U31b is configured as an adder with an output voltage proportional to the difference between the
14 rail and amplifier output.

15 **[0053]** It can therefore be seen that using class H operation with the amplifiers 96 can reduce
16 power dissipation (with the possibility of decreasing overall weight by requiring fewer or smaller
17 heat sinks) and decrease noise. Prior relay test sets have not realized that class H is particularly
18 suitable in the environment discussed above. As noted, the use of class H provides a
19 compromise between linear (class D) and switch mode (class G) solutions by providing a lower
20 power solution than class G and lower noise than class D. Moreover, the use of a DSP 100
21 provides separation between the amplifier 96 and the power supply 94 as well as offering the
22 flexibility in being able to program algorithms that can realize efficiencies in achieving the
23 desired output. Since the output levels for relay testing are generally high, a lower power
24 solution is an advantage in that it can minimize overloading on the power supply line to the test
25 set when the tester 60 is used in end-to-end testing as discussed below. Further, the lower power
26 solution dissipates less heat, and thus the heat sinks needed can be reduced in size and/or
27 number. The lower noise is beneficial in that the noise floor is reduced as well as enabling a
28 more accurate measurement at lower output levels. Moreover, the class H arrangement
29 described herein is particularly suitable in this environment as the duration of high power tests,

1 to which a lower power solution is beneficial, is specific to electro-mechanical relays such as
2 those being tested by the tester 60. The combination of using class H and the control thereof
3 using the DSP 100 also enables the output to follow as close as possible to the output rails
4 without clipping the waveform.

5 **[0054]** As discussed above, the complexity of power system protection systems used to
6 safeguard power systems has grown such that many modern power system protections use
7 testing equipment (e.g. tester 60) that are synchronized via GPS satellites to properly perform the
8 test, e.g. using timing signals. Power system end to end testing involves coordinated
9 simultaneous synthesis and generation of predetermined fault case(s) at various locations. When
10 performing this type of test, the response from the relay 18, 20 and auxiliary equipment (e.g. CT
11 22) is dependent on both the nature of the fault being simulated, and the response from the
12 remote equipment. Therefore, it may be necessary to generate numerous fault scenarios
13 simultaneously at all ends of the line 12 to verify the correct operation of the protection scheme.

14 **[0055]** The actual test typically takes only a fraction of a second, however, as also discussed
15 above, the preparation and subsequent analysis can be very time consuming and may even
16 require several days. Proper analysis of the test results should be performed by an expert or
17 experienced professional and such analysis can consume a significant portion of their time.

18 **[0056]** It has been recognized that using the hardware and software capabilities already
19 included in the tester 60, the results and analysis can be realized in mere seconds and can be
20 done instantaneously following a fault simulation. Figure 8 shows an example of a test file 116,
21 which specifies a fault case 112 that has been prepared by a professional ahead of the actual fault
22 simulation. It has been realized that the preparation of the test file 116 can be extended to
23 include pre-programmed, expected results 114 so that this knowledge is known ahead of time,
24 and can then be used to analyze a test case 112. As such, the expected results 114 can be used to
25 generate instantaneous test reports and graphical "pass/fail" outputs by comparing test results
26 with expected results 114 and applying predefined analytical operations. In this way, every time
27 a test case is run, the predefined expected results can be used to perform an instantaneous
28 analysis and avoid having to manually interpret the resultant test data, which can be time

1 consuming and may be prone to human error. Moreover, by having the appropriate professional
2 define the expected results beforehand, a technician who is inexperienced in the analysis can still
3 obtain the results and convey those back to the professional.

4 **[0057]** Figure 9 illustrates a modified version of the spreadsheet shown in Figure 8 with
5 expected result data 114 in the lower portion. It will be appreciated that the result data 114 may
6 be added to an existing test case 112 (e.g. Figure 8) or can be prepared by an experienced
7 professional at the same time as preparing the test file 116. The number of test points being
8 monitored is entirely up to the professional designing the test and an additional row in the
9 spreadsheet can be added to add an additional test point as desired. Descriptive information may
10 be included in the fault case, which can then be loaded automatically into the test report to
11 provide more meaningful information.

12 **[0058]** It will be appreciated that the example shown in Figure 9 is for illustrative purposes
13 only and that any type of test file 116 can be created and used to run fault test data 112 and
14 generate reports. Other formats such as a text file, database file, XML, etc. may used to create
15 the test file 116. By creating expected result data 114, and including it with the fault case 112 as
16 shown in Figure 9, the time consuming task of determining the expected results 114 only needs
17 to be performed once, by the appropriate professional, is properly documented and/or
18 standardized in the test file 116, and may be verified instantaneously by the test equipment every
19 time the test is performed.

20 **[0059]** The test result analysis is in one embodiment performed by the CPU 84. The test
21 files 116 are typically stored in memory, either the non-volatile memory 85 (hard drive or flash)
22 or the volatile memory 87 (RAM), and accessed and run by the CPU 84 upon receiving an
23 appropriate input from the user at the input panel 66. The fault test may then be performed by
24 the tester 60 and the results compared to the expected results 114 stored in the test file 116. An
25 analysis module stored preferably in a software program operated by the CPU 84 may then
26 create an output for displaying the results of the test as shown in Figures 10 and 11. In order to
27 prepare a test, the user would prepare a test case and save it into non-volatile memory 85 within
28 the tester 60. In order to subsequently run the test, the user would transfer the test case into

1 volatile memory 87, run the test on the tester 60, and review reports and/or display the results
2 graphically.

3 **[0060]** Figure 11 illustrates a test report menu 126 which provides an overview of the results
4 for the test case shown in Figure 10 (b). As can be seen in Figure 11, each test point is clearly
5 identified and an “OK” or “FAIL” identifier included to show where the failure occurred. An
6 overall test result 128 may also be provided. The report menu 126 enables the user to first
7 review/save/print the results and provides an option for displaying the results graphically.

8 **[0061]** As can be seen in Figure 10, a graphical user interface 118 is provided that can be
9 displayed on the display 64 upon completing a fault test. The interface 118 comprises graphical
10 waveforms to illustrate voltage and current in pre-fault, fault and post-fault stages. Below the
11 waveforms, a graphical bar 120 is provided for each test point. The darker portions 122 of the
12 bars shown in view (a) indicate that the expected result for the particular test point occurred
13 within the acceptable range, which is represented by the lighter colour. In this way, the user can
14 immediately and visually, identify when and what went wrong, should the test fail. View (b) in
15 Figure 10 shows such a failure where it is clear that test point 4 did not occur within the
16 acceptable time range. In this case, it can be seen that the occurrence of the test point, shown as
17 a darkened bar 124, was outside (before) the graphical bar 120. Along each side of the display
18 64, a number of options such as zoom ratio may be provided to adjust settings and manipulate
19 and explore the output graphically. Since the test case is preloaded with the expected results,
20 the graphical display can not only show what happened during the test, it can also, by way of the
21 bars 122, 124 show the user how far away they were from what should have happened. This can,
22 e.g., enable an inexperienced user to easily determine what went wrong so that they can report
23 this to the more experienced professional without requiring analysis to do so. This can save time
24 and reduce errors in interpreting the data. In other words, the expected results can be
25 intelligently used so that the actual results are more meaningful.

26 **[0062]** Testing equipment such as tester 60 may be used for manual tests in addition to end-
27 to-end testing. Manual testing involves a single tester 60 running a series of test cases on a
28 particular piece of equipment in the power system, such as a protective relay 10.

1 [0063] Protective relay test instruments, e.g. tester 60, generate waveforms using a set of
2 voltage and current waveform generators (e.g. amplifiers 96). These waveforms are typically
3 connected to the voltage and current inputs of a protective relay (at switches 34 and 38, see
4 Figure 3), or similar equipment. The outputs of the equipment under test are typically connected
5 to digital inputs on the instrument (e.g. through switch 36), and digital outputs on the instrument
6 are used to control aspects of the operation of the equipment under test.

7 [0064] A common requirement for such an instrument is the ability to measure timing
8 relationships. For example, the instrument might generated a high level of current, interpreted
9 by an overcurrent relay as a fault condition. The instrument would monitor the "trip" output of
10 the overcurrent relay, and measure the time between the start of the high-current waveform and
11 the closure of the trip output (typically known as the relay's "operate time"). A typical fault
12 scenario contains many events that occur very quickly (e.g. within milliseconds) making it
13 difficult if not impossible for the naked eye to follow the sequence of events. Traditionally, the
14 data captured during a test is recorded and then used for later analysis.

15 [0065] The test result data can used at run time to provide meaningful displays for the user.
16 This can be accomplished by capturing the sequence of events data and converting it into a
17 useable, graphical form so that the user can evaluate the various operations, as shown in Figure
18 12. The tester 60 uses a concept that may be referred to as "fault states", where each fault state
19 defines a set of generation parameters (current and voltage magnitudes, phase angles,
20 frequencies, etc.) and rules for making transitions to other states. The active fault state may
21 change due to user-initiated commands, digital input changes or the expiration of a timer.

22 [0066] To understand the test results, users of the tester may need to see the actual generated
23 waveforms, along with state changes of digital inputs, digital outputs and fault states. That way,
24 analysis of the results can include, for example, waveform phase angle information. One way of
25 obtaining the required waveform data is to connect a measuring and recording instrument (not
26 shown). However, that approach requires the user to obtain and connect at least two instruments
27 for the test.

1 **[0067]** The sequence of events recorder described herein allows such analysis to be
2 performed without requiring external recording equipment or computers, so the user only needs
3 one instrument, e.g. the tester 60. In this way, the capabilities already provided by the tester 60
4 such as display 64 and processing capabilities can be harnessed to provide meaningful output for
5 the user.

6 **[0068]** As discussed and shown in Figure 4, the tester 60 has numerous status inputs 68 that
7 are used to monitor the status points of interest. The user can assign relevant names to the
8 various input points to clarify the graphical sequence of events diagram as shown in the screen
9 shot of Figure 13. The sequence of events record is configured such that the user does not have
10 to setup any parameters to use this feature, all relevant data is captured automatically when ever
11 a test is executed. The sequence of events record is preferably stored in volatile memory 87 and
12 displayed upon selection by the user.

13 **[0069]** Whenever the tester 60 generates output waveforms, it may record every sample of
14 the generated waveform in volatile memory 87. A software setting determines whether these
15 samples represent the programmed levels or currents and voltages measured at the outputs using
16 analog-to-digital converters. The buffer also stores the states of all the digital inputs and outputs,
17 as well as the active fault state. The data capture operation continues until the end of the test
18 shot (i.e. a short time after the instrument stops generating waveforms), or when the buffer
19 becomes full, whichever occurs first. The buffer should be large enough to capture data for a
20 typical protective relay test (30 seconds, for example).

21 **[0070]** Once the test is complete, a selection option can be presented to the user that allows
22 the user to display a list of all the recorded events, in chronological order, with enough timing
23 information to allow analysis of the sequence as shown in Figure 12. Another selection option
24 can be used to cause the tester 60 to display the sequence information and waveform data
25 graphically on display 64. As can be seen in Figure 12, waveforms and digital input/output
26 states are shown in an oscilloscope-like fashion on an X-Y plot where the horizontal axis is time
27 and the vertical axis for each trace is magnitude or state. Waveforms are grouped as appropriate
28 to the test. For example, all three voltages in a three-phase set may be superimposed on each

1 other. The waveform traces may be shown in different colors so they can be differentiated while
2 superimposed.

3 **[0071]** The graphical display also shows the active fault state by drawing a box illustrating
4 the time during which each state was active. Each box is labelled with the name of the fault
5 state. The fault state name is abbreviated if the width of the box is too small to show the entire
6 fault state name. Controls are provided to control the information display, as described below.

7 **[0072]** A "zoom" button allows the user to zoom the time scale in or out using a rotary knob
8 on the instrument. A "horizontal position" button allows the user to pan back and forth along the
9 time line using, e.g., a rotary knob. A box at the bottom of the screen, graphically illustrates
10 which portion of the time scale is being shown in the main graphics area, based on the zoom and
11 horizontal position settings.

12 **[0073]** Preferably, buttons are provided for "cursor 1", "cursor 2" and "point of fault", which
13 allows the user to move the associated cursor lines back and forth using a rotary knob. The time
14 is displayed for each cursor and for the horizontal position, relative to the point of fault. The
15 time of the point of fault is shown relative to the start of the captured data buffer. The difference
16 between the cursor 1 and cursor 2 positions is shown, allowing the user to make relative time
17 calculations. A button is also provided to show the instantaneous waveform voltage and current
18 levels at the "cursor 1" position, so that the user can move cursor 1 back and forth to make
19 waveform measurements.

20 **[0074]** Buttons may be provided for "next event" and "previous event" when adjusting the
21 horizontal position, point of fault, or a cursor. These keys may move to the next or previous
22 time, relative to the present setting of the cursor or position, at which an event occurred. The
23 event may be, for example, a change of active fault state, or a transition of a digital input.

24 **[0075]** As shown in detail in Figure 13, the various test points may be configured in a setup
25 menu 170, e.g. to name the test point for ease of reference. The fault state control, outputs,
26 timers and input settings should be configurable by providing suitable option buttons as shown in
27 Figure 13.

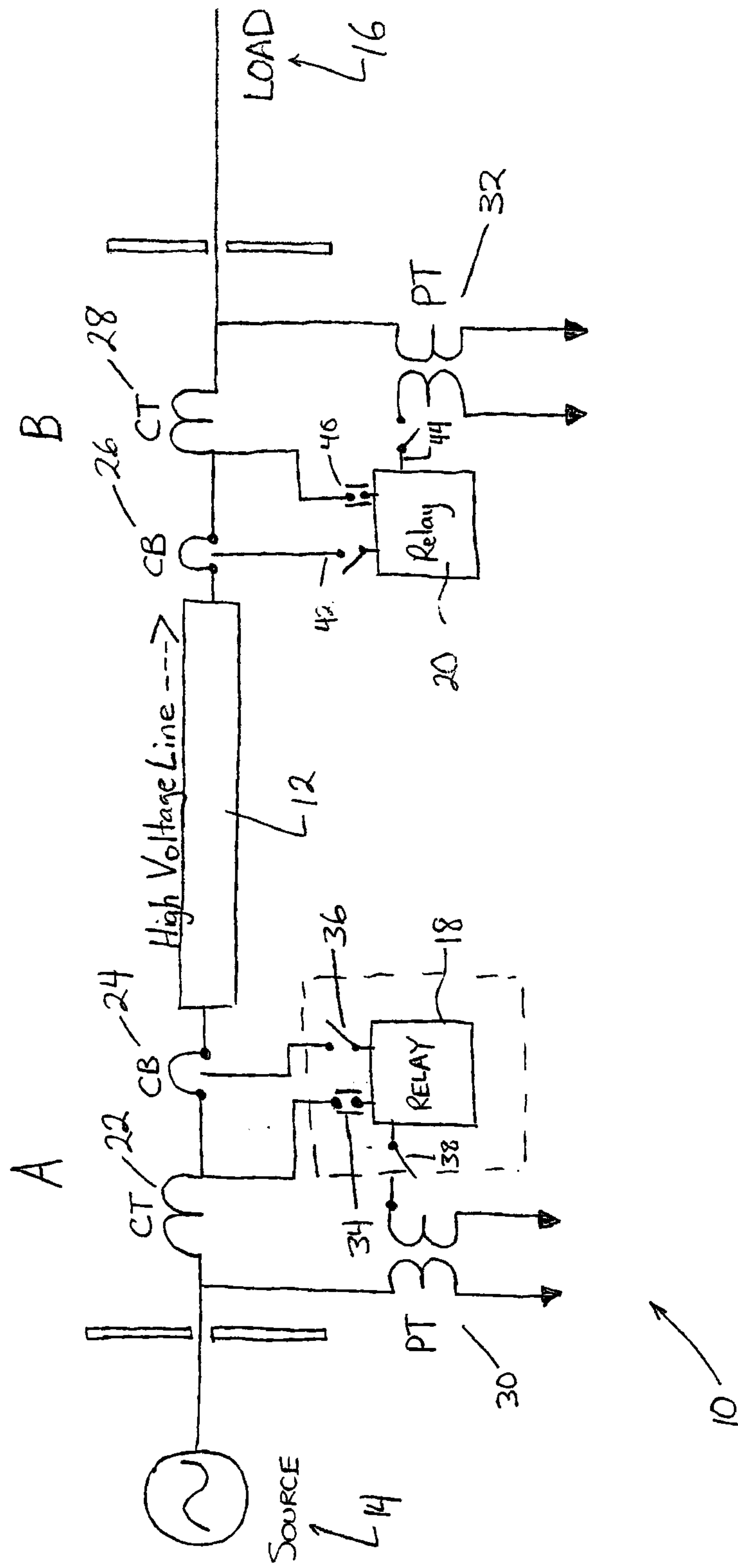
1 [0076] It can therefore be seen that the data recorded during a manual equipment test can be
2 captured and displayed in a usable form on the tester 60 to provide instantaneous results for the
3 user in the field. In this way, data which has previously been underutilized can be taken
4 advantage of.

5 [0077] Although the invention has been described with reference to certain specific
6 embodiments, various modifications thereof will be apparent to those skilled in the art without
7 departing from the spirit and scope of the invention as outlined in the claims appended hereto.

Claims:

1. A system for modulating a power supply in a relay test system comprising an amplifier, said system comprising:
 - a digital control system separating said power supply and said amplifier and configured to operate according to a class H modulation scheme;
 - a gate drive sense circuit for providing a gate drive intensity signal to said control system indicative of the extent to which an output switching mechanism for said amplifier is being operated; and
 - a voltage difference circuit for monitoring a difference between an output of said amplifier and a power supply rail from said power supply to provide a voltage difference signal to said control system;wherein said control system is operated according to said class H modulation scheme using readings taken from said voltage difference signal and said gate drive intensity signal to generate a control signal for said power supply.
2. The system according to claim 1 wherein said control system comprises a digital signal processor.
3. The system according to claim 1 or claim 2 wherein said output switching mechanism is a transistor.
4. The system according to claim 3 wherein said transistor is a field effect transistor (FET).
5. The system according to any one of claims 2 to 4 wherein said digital signal processor comprises a pre-programmed algorithm to predict changes in said power supply rail.
6. The system according to any one of claims 1 to 5 wherein said voltage difference signal is proportional to a difference between said power supply rail and said output of said amplifier.

7. A method of modulating a power supply in a relay test system comprising an amplifier, said method comprising:
- during operation of said power supply:
- obtaining, at a digital control system separating said power supply and said amplifier, a drive intensity signal from a gate drive sense circuit, said drive intensity signal input indicative of the extent to which an output switching mechanism for said amplifier is being operated, said control system configured to operate according to a class H modulation scheme;
- obtaining, at said control system, a voltage difference signal from a voltage difference circuit, said voltage difference signal indicative of a difference between an output of said amplifier and a power supply rail from said power supply; and
- operating said control system according to said class H modulation scheme using readings taken from said voltage difference signal and said drive intensity signal to generate a control signal for said power supply.
8. The method according to claim 7 wherein said control system comprises a digital signal processor.
9. The method according to claim 7 or claim 8 wherein said output switching mechanism is a transistor.
10. The method according to claim 9 wherein said transistor is a field effect transistor (FET).
11. The method according to any one of claims 8 to 10, wherein said digital signal processor comprises a pre-programmed algorithm to predict changes in said power supply rail.
12. The method according to any one of claims 7 to 11, wherein said voltage difference signal is proportional to a difference between said power supply rail and said output of said amplifier.

FIGURE 1

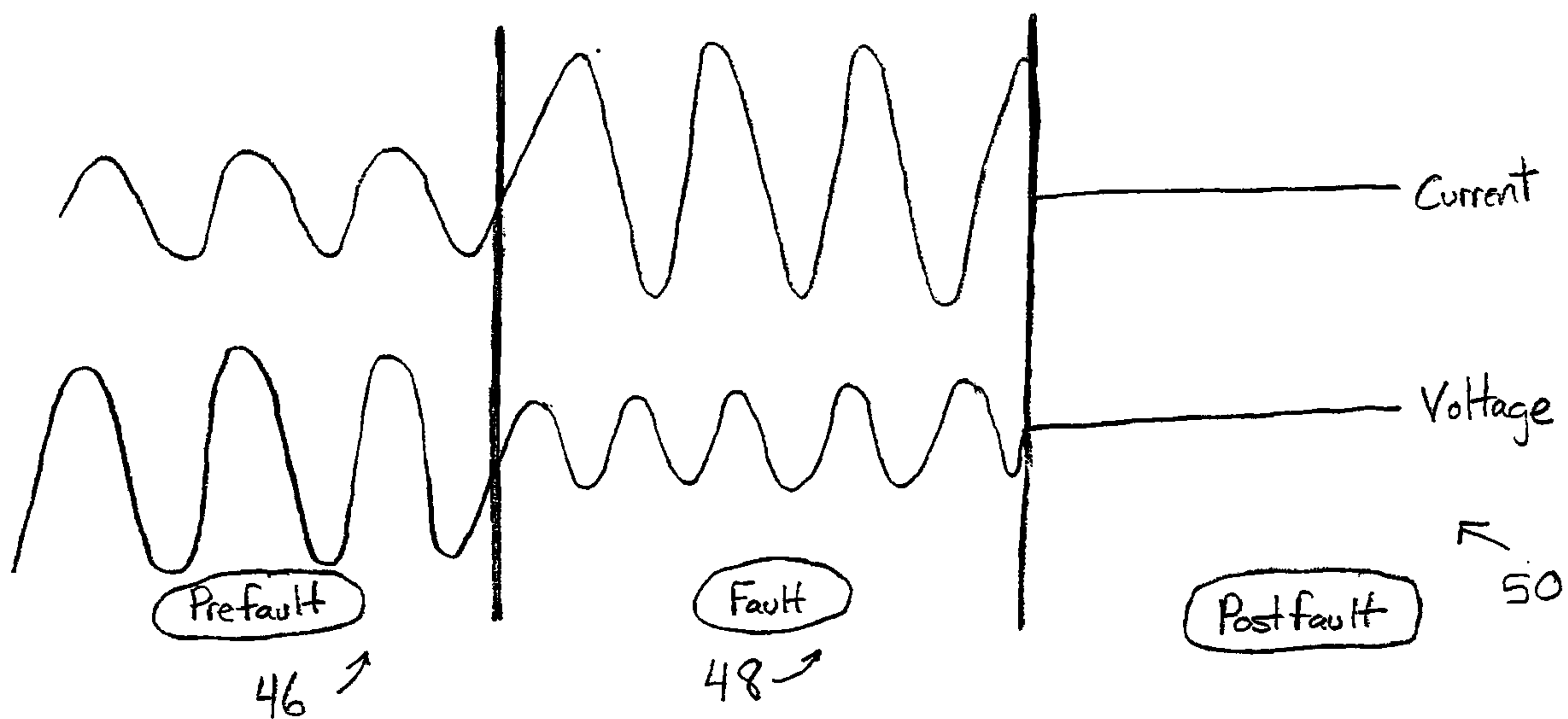


FIGURE 2

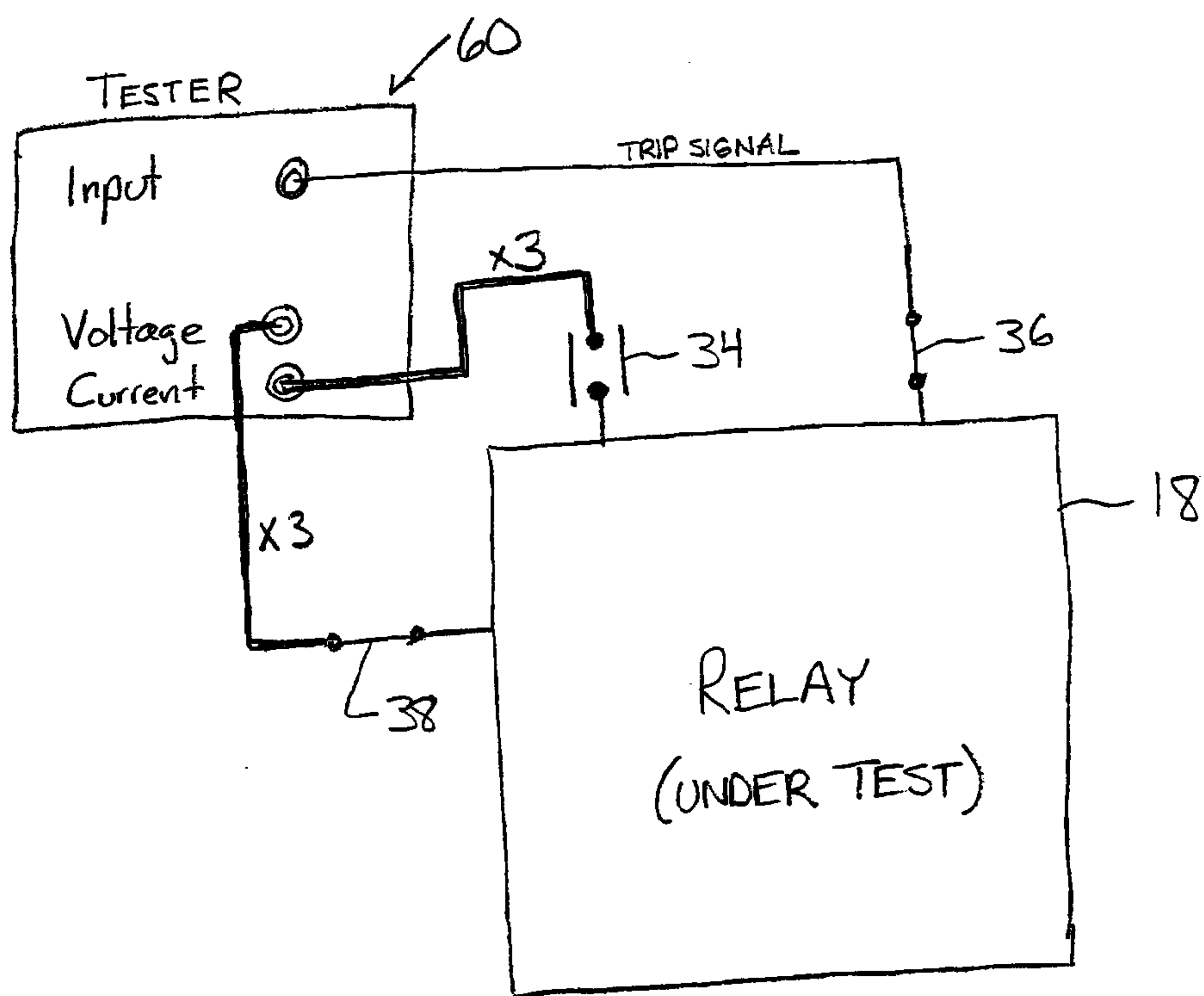


FIGURE 3

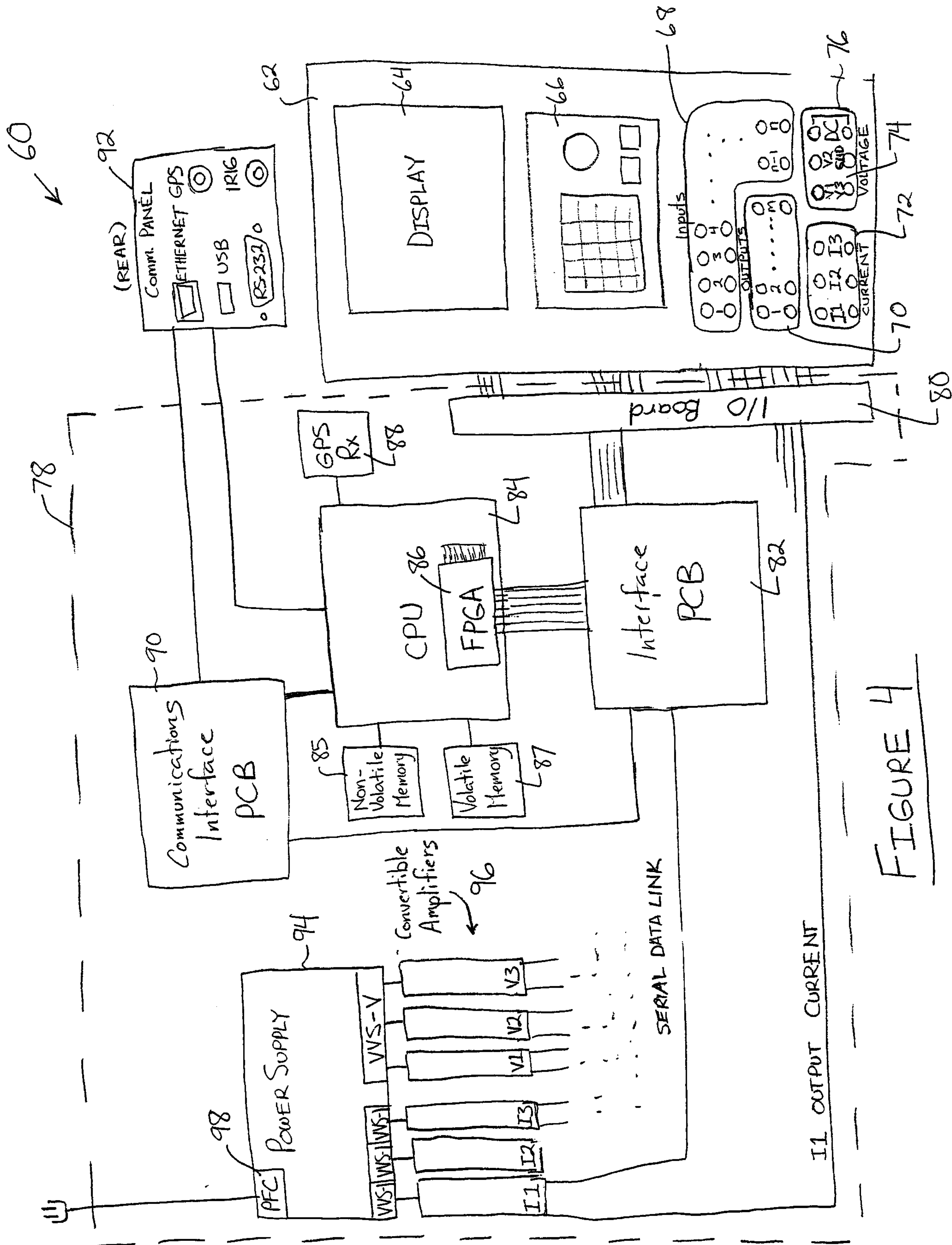


FIGURE 4

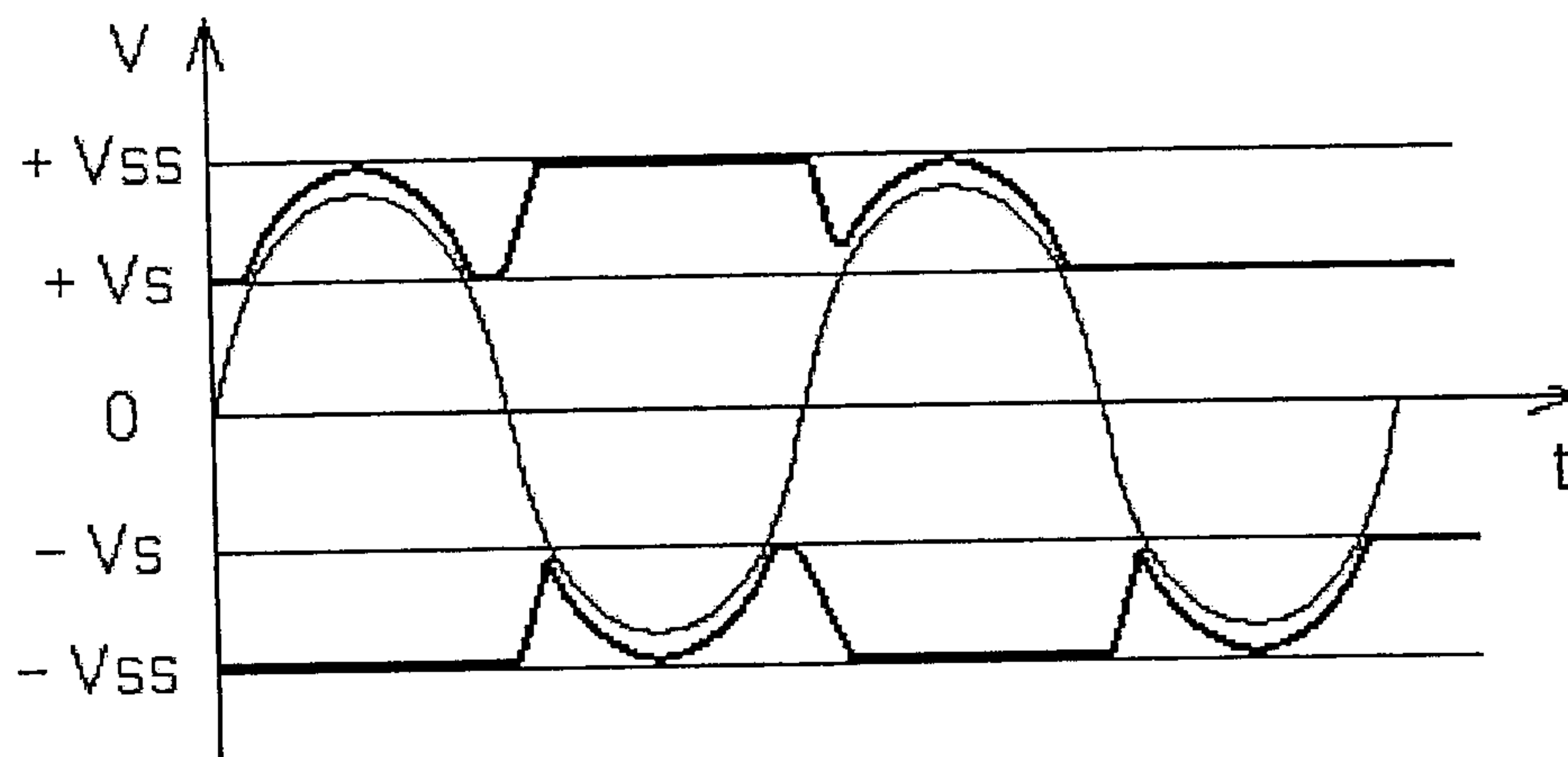


Figure 5

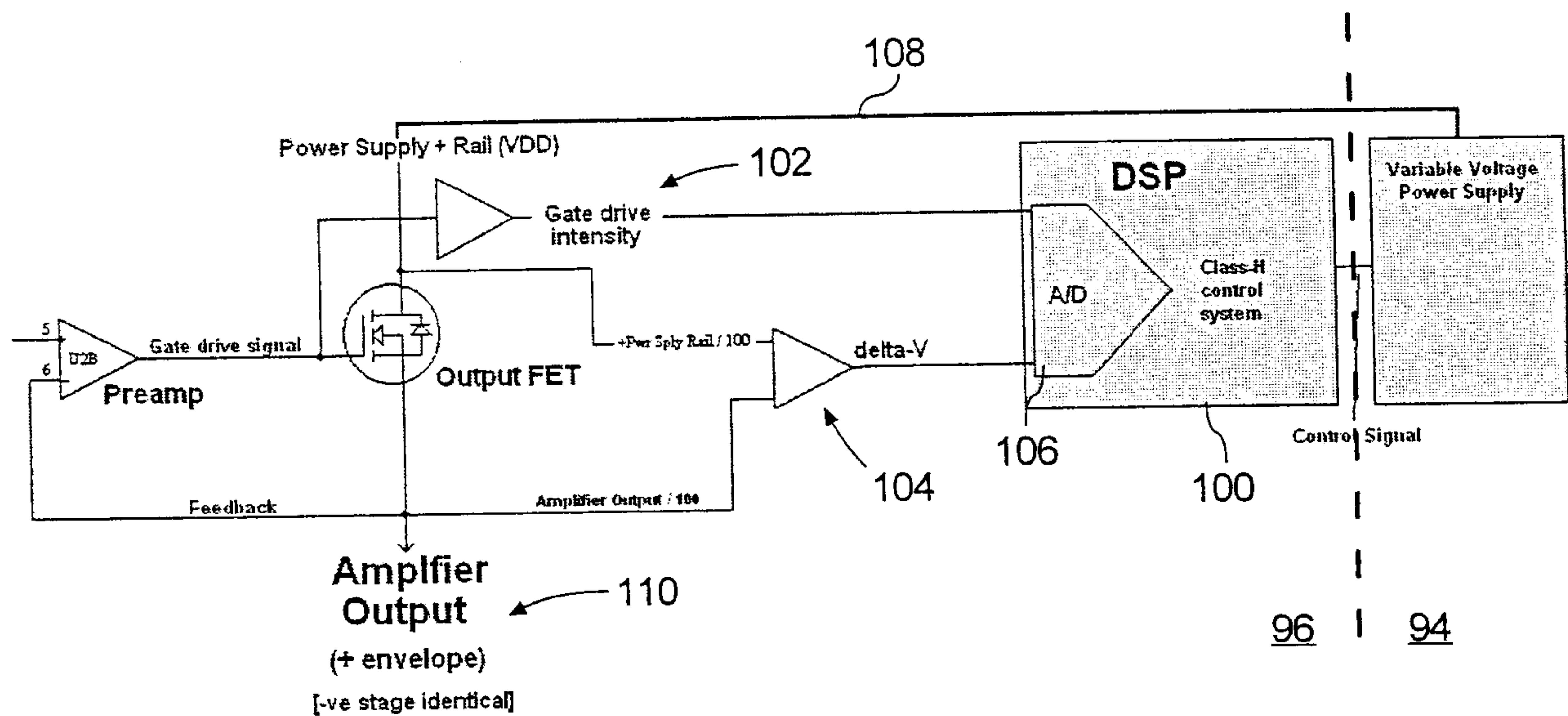


Figure 6

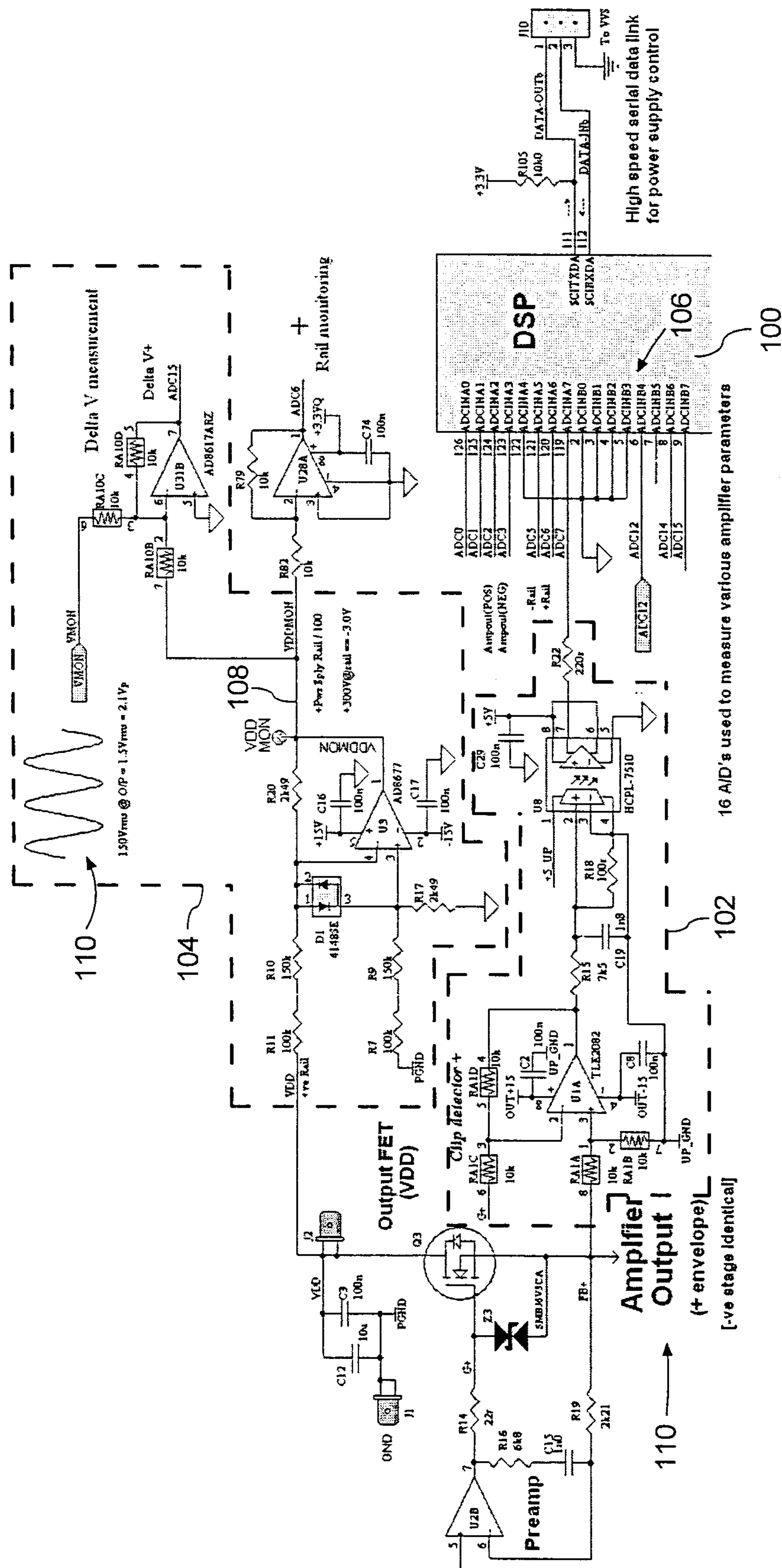


Figure 7

Microsoft Excel - GATES_MIDWAY EndtoEndCalc5.XLS															
	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
1		1													
3	GATES CB 272	CT: 400	PT: 2000												
4	MIDWAY CB 222	CT: 600	PT: 2000												
5	SYSTEM VOLTAGE:	230	kV												
6															
7	CB 282	Load from Bus to Line (SOURCE BUS for Prefault)													
8		Aspen Output Pre Fault	Aspen Output Fault 1	Aspen Output Fault 2	Aspen Output Post Fault										
9		Values Angle	Values Angle	Values Angle	Values Angle										
10	VA	132.79 0	110.9 -1		132.79 0										
11	VB	132.79 -120	110.9 -121		132.79 -120										
12	VC	132.79 120	110.9 119		132.79 120										
13	IA	200 -10	4452 -81		0 0										
14	IB	200 -130	4452 159		0 0										
15	IC	200 110	4452 39		0 0										
17	CB 222	Load from Line to Bus (LOAD BUS for Prefault)													
		Aspen Output	Aspen Output	Aspen Output	Aspen Output										
General Info 1 2 3 4 5 6 7 8 9															

Figure 8

Microsoft Excel - GATES_MIDWAY EndtoEndCalc5.XLS															
	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
1		1													
3	GATES CB 272	CT: 400	PT: 2000												
4	MIDWAY CB 222	CT: 600	PT: 2000												
5	SYSTEM VOLTAGE:	230	kV												
6															
7	CB 282	Load from Bus to Line (SOURCE BUS for Prefault)													
8		Aspen Output Pre Fault	Aspen Output Fault 1	Aspen Output Fault 2	Aspen Output Post Fault										
9		Values Angle	Values Angle	Values Angle	Values Angle										
10	VA	132.79 0	110.9 -1		132.79 0										
11	VB	132.79 -120	110.9 -121		132.79 -120										
12	VC	132.79 120	110.9 119		132.79 120										
13	IA	200 -10	4452 -81		0 0										
14	IB	200 -130	4452 159		0 0										
15	IC	200 110	4452 39		0 0										
16															
17															
18	Status Input	Description	PRE initial	PRE final	PRE t(min)	PRE t(max)	FAULT 1 initial	FAULT 1 final	FAULT 1 t(min)	FAULT 1 t(max)	POSTFAULT initial	POSTFAULT final	POSTFAULT t(min)	POSTFAULT t(max)	
19	1	Trip	0	0	0	0	0	1	0.012	0.032	1	0	0.010	0.018	
20	2	BFI	0	0	0	0	0	1	0.014	0.040	1	0	0.000	0.015	
21	3	Per. Tx	0	0	0	0	0	1	0.012	0.032	1	0	0.000	0.020	
22	4	Per. Rx	0	0	0	0	0	1	0.016	0.038	1	0	0.000	0.025	
23															

Figure 9

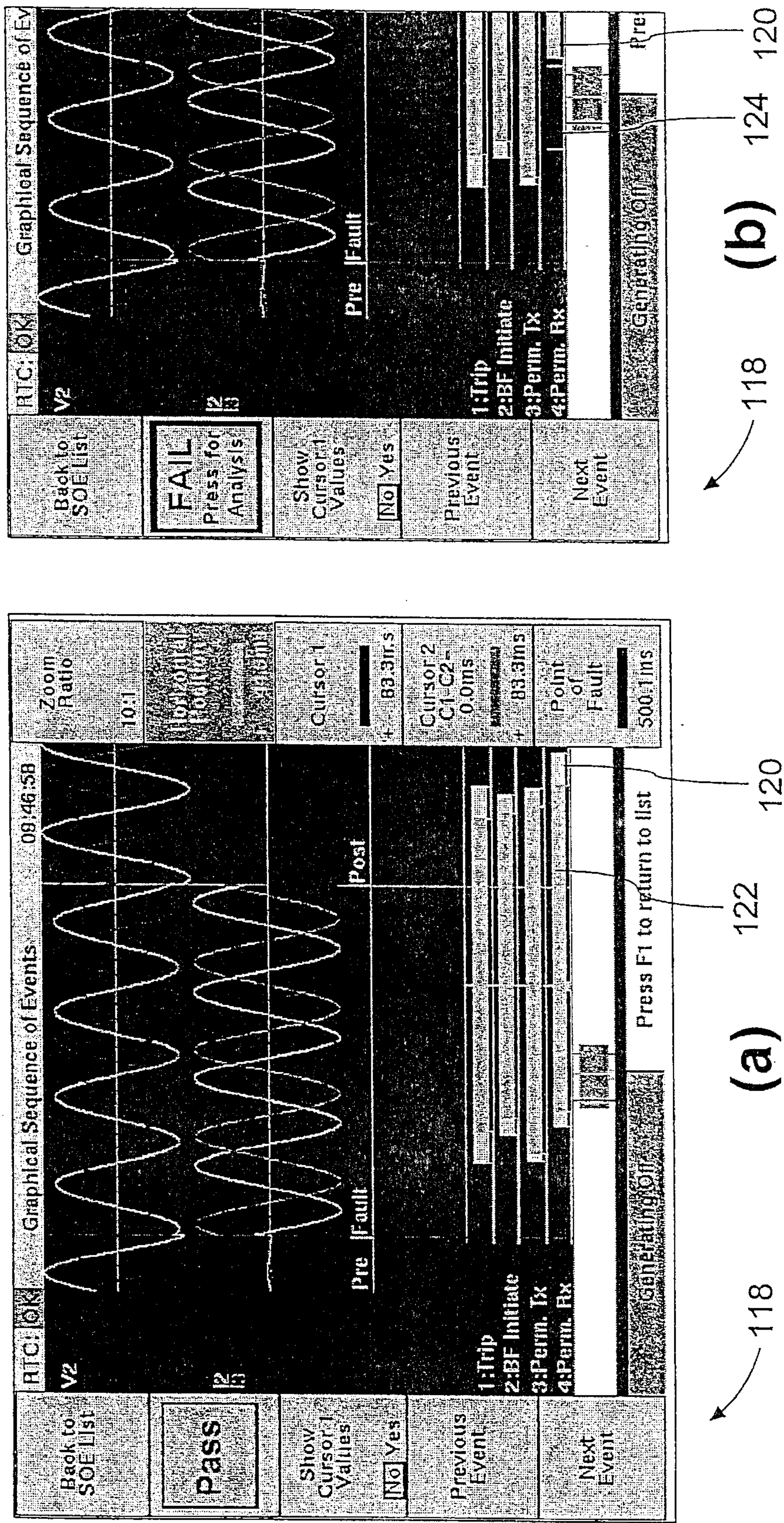


Figure 10

Press F1 When Done Viewing	RTC: OK	Test Reports Menu	17:31:08
	End - to - End Test Results March 1, 2006 17:30:46		
	File: CB 282 / 1 : GATES_MIDWAY EndToEndCalcs		
	Result: Fail 128		
	OK 1) Trip OK 2) BFI OK 3) Permissive Tx FAIL 4) Permissive Rx (channel#4) failed to assert 0.038s after FAULT		
	Report Ends		

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Figure 11

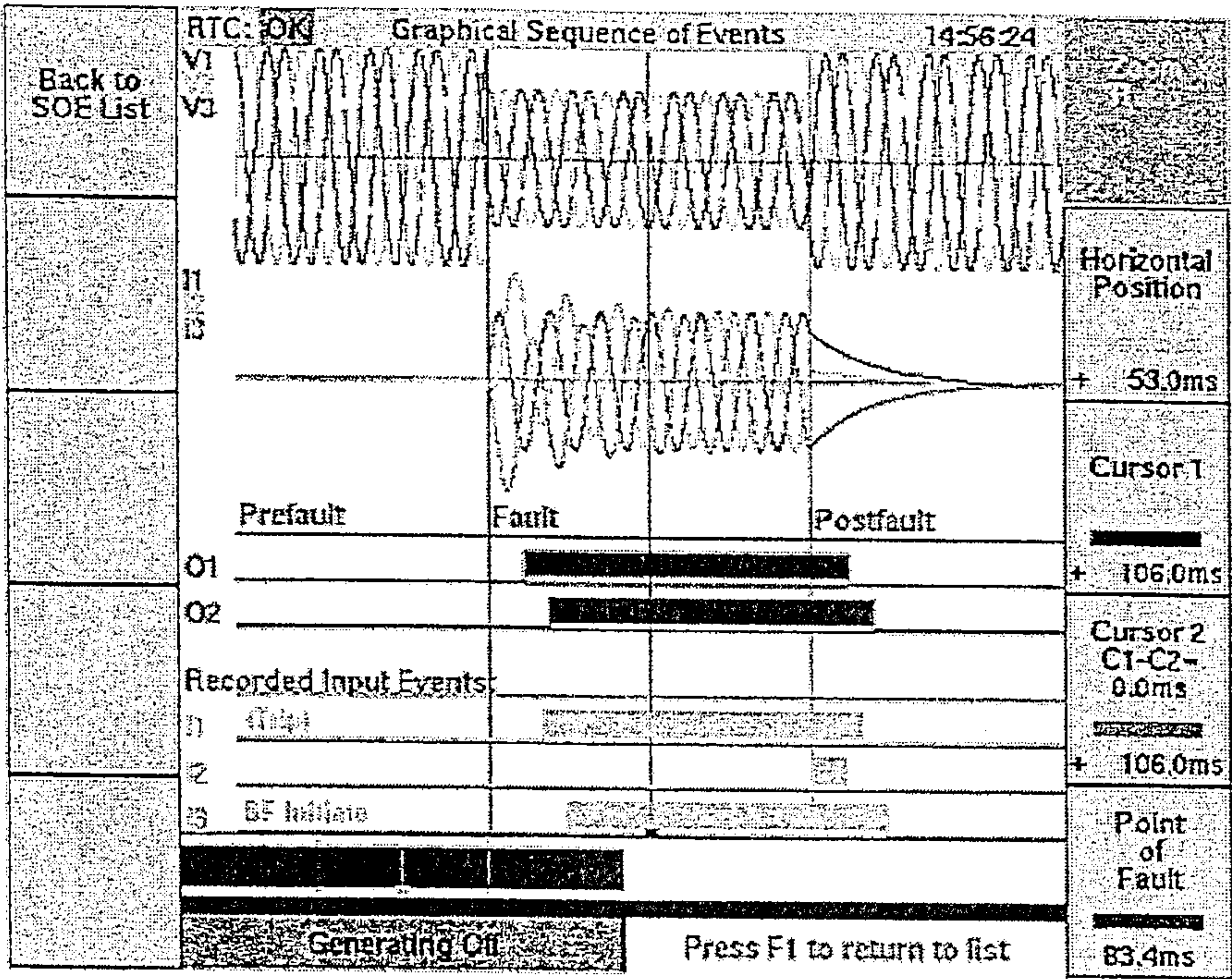


Figure 12

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Back to Advanced Settings Menu	RTC: OK I/O Setup Menu 13:39:46						
	Inputs						
Use Input 8 for Footswitch No Yes	#	Name	Type	Level	Debounce	Tone	Configure Fault State Control
	1	Trip	Dry	N/A	0.0 ms	Yes	
	2	Permissive Tx	Dry	N/A	0.0 ms	Yes	
	3	Custom 1	Dry	N/A	0.0 ms	Yes	
	4	Custom 2	Dry	N/A	0.0 ms	Yes	
	5	Slow Trip	Dry	N/A	0.0 ms	Yes	
		6	Fast Trip	Dry	N/A	0.0 ms	Yes
		7	Initiate Fault	Dry	N/A	0.0 ms	Yes
		8	52A	Dry	N/A	0.0 ms	No
		9	52B	Dry	N/A	0.0 ms	No
		10	BF Initiate	Dry	N/A	0.0 ms	No
		11	Block	Wet	10V	0.0 ms	Yes
Set all Inputs to Wet	12	Bus Blocking	Wet	10V	0.0 ms	Yes	Configure Outputs
		Bus Initiate	Wet	10V	0.0 ms	Yes	
		Close	Wet	10V	0.0 ms	Yes	
Set all Inputs to Dry		Echo	Wet	10V	0.0 ms	Yes	Configure Timers
		Fault Detector					
		Local/Remote Lockout					
The first five names are customizable, via the Customization Menu. Press HELP for more details.			basic operational characteristics of 7 to configure the state transitions				Reset Input Settings to Factory Defaults
			each status input channel. The sequence of events screens, sequence of events display.				
Generating Off			Adjusting Prefault				

Figure 13

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