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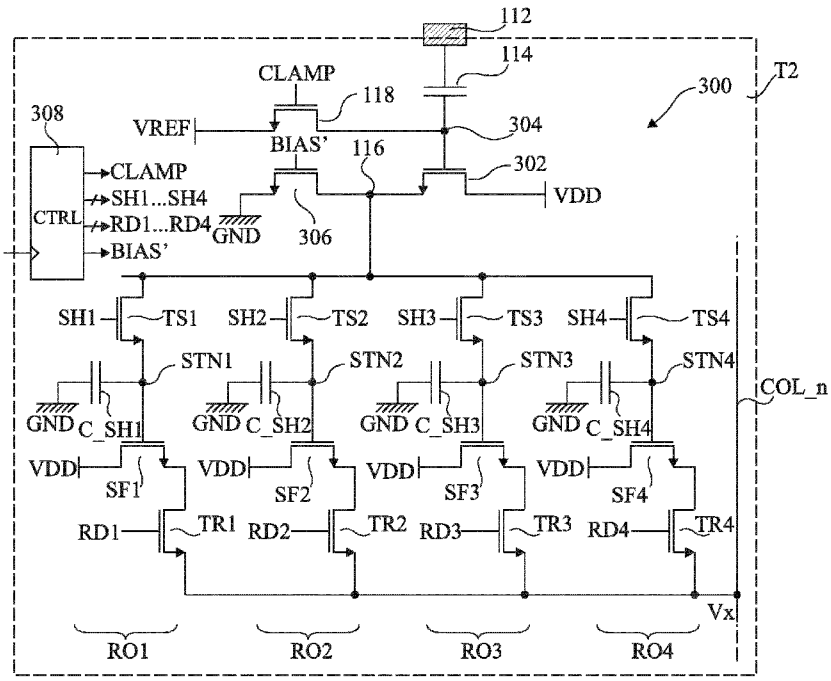


Fig 3

(57) Abstract: The present disclosure relates to a pixel readout circuit comprising:a clamping capacitor (114) having a first terminal coupled to an output node of a pixel circuit; first and second readout paths (RO1, RO2) each comprising a selection transistor (TS1, TS2) and a readout capacitor (C_SH1, C_SH2) for storing a voltage level captured by the pixel circuit; and a source follower transistor (302) having its control node coupled to a second terminal of the clamping capacitor (114), a first of its main conducting nodes coupled to a first supply voltage rail (VDD, GND), and a second of its main conducting nodes coupled to the first and second readout paths (RO1, RO2).

[Continued on next page]

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DESCRIPTION

VOLTAGE MODE GLOBAL SHUTTER PIXEL

[0001] The present patent application claims priority from the French patent application filed on August 28, 2018 and assigned application no. FR 18/57694, the contents of which is hereby incorporated by reference.

Technical field

[0002] The present disclosure relates generally to the field of image sensors, and in particular to a pixel circuit of an image sensor and method of forming the same.

Background art

[0003] Image sensors capable of performing a global shutter operation generally comprise pixel circuits that locally store one or more signals captured by one or more photodiodes until the signals can be read. The storage of the one or more signals within each pixel circuit can generally be achieved using either a voltage mode or a charge mode. In charge mode, the captured signals are represented by quantities of charge stored on capacitors within each pixel circuit. In voltage mode, the captured signals are represented by voltages present across capacitors within each pixel circuit. Voltage mode storage has advantages in terms of the signal dynamic and parasitic light sensitivity.

[0004] The photo response non-uniformity (PRNU) in a pixel array is a measure of undesirable non-uniformity among the pixels of an image sensor, and in particular the non-uniformity among the gains between the received optical power and the resulting output voltage generated by a readout path of each pixel. For example, the PRNU can be calculated as the standard deviation of the gain, expressed as a percentage

with respect to the full dynamic range of output signal of the pixels.

[0005] It would be desirable to provide an image sensor comprising voltage mode pixels having readout paths with relatively low PRNU.

Summary of Invention

[0006] It is an aim of embodiments of the present disclosure to at least partially address one or more needs in the prior art.

[0007] According to one aspect, there is provided a pixel readout circuit comprising a clamping capacitor having a first terminal coupled to an output node of a pixel circuit; a first readout path comprising a first selection transistor and a first readout capacitor for storing a first voltage level captured by the pixel circuit; a second readout path comprising a second selection transistor and a second readout capacitor for storing a second voltage level captured by the pixel circuit; and a source follower transistor having its control node coupled to a second terminal of the clamping capacitor, a first of its main conducting nodes coupled to a first supply voltage rail, and a second of its main conducting nodes coupled to the first and second readout paths.

[0008] According to a further aspect, there is provided an image sensor comprising: a pixel circuit having a first photodiode coupled to a sense node via a first transfer gate; and the above pixel readout circuit.

[0009] According to one embodiment, the photodiode is a pinned photodiode.

[0010] According to one embodiment, the pixel circuit further comprises a second photodiode coupled to the sense node via a second transfer gate, the first voltage level being captured

by the first photodiode and the second voltage level being captured by the second photodiode.

[0011] According to one embodiment, the pixel readout circuit further comprises a third transistor coupling the second terminal of the clamping capacitor to a second supply voltage rail.

[0012] According to one embodiment, the pixel readout circuit further comprises a current source coupled between the second main conducting node of the transistor and the second supply voltage rail.

[0013] According to one embodiment, the clamping capacitor is of a first type, and each of the first and second readout capacitors is of a second type different to the first type.

[0014] According to one embodiment, the clamping capacitor is a metal-insulator-metal capacitor.

[0015] According to one embodiment, the first and second readout capacitors are capacitive trench capacitors.

[0016] According to one embodiment, the first readout path further comprises a source follower transistor having its control node coupled to a first storage node connected to a first terminal of the first readout capacitor, the source follower transistor of the first readout path having one of its main conducting nodes coupled to a column line via a first readout transistor; and the second readout path further comprises a source follower transistor having its control node coupled to a second storage node connected to a first terminal of the second readout capacitor, the source follower transistor of the second readout path having one of its main conducting nodes coupled to the column line via a second readout transistor.

[0017] According to one embodiment, the pixel readout circuit further comprises one or more further readout paths coupled to the second main conducting node of the source follower transistor.

[0018] According to a further aspect, there is provided an image sensor comprising: a first tier comprising an array of pixel circuits including the above pixel circuit, the pixel circuits being configured to operate in a global shutter mode; and a second tier comprising, for each of the pixel circuits, at least part of the above pixel readout circuit.

[0019] According to one embodiment, the second tier comprises, for each of the pixel circuits, the above pixel readout circuit, each pixel readout circuit being coupled to the output node of a corresponding one of the pixel circuits via a corresponding inter-tier connection.

[0020] According to one embodiment, the first and second readout capacitors are part of the first tier, the first readout capacitor being coupled to part of a corresponding readout circuit via a first inter-tier connection and the second readout capacitor being coupled to part of a corresponding readout circuit via a second inter-tier connection.

[0021] According to one embodiment, the second tier further comprises a further source-follower transistor having its gate coupled to the sense node of the pixel circuit and one of its main conducting terminals coupled to the first terminal of the clamping capacitor.

[0022] According to a further aspect, there is provided a method of reading a pixel value from a pixel circuit using a pixel readout circuit, the pixel circuit for example comprising a first photodiode coupled to a sense node via a first transfer gate, the method comprising: controlling

a first selection transistor of a first readout path of the pixel readout circuit to couple a sense node of the pixel circuit to a first readout capacitor of the first readout path via a clamping capacitor and via a source follower transistor having its control node coupled to a terminal of the clamping capacitor; and controlling a second selection transistor of a second readout path of the pixel readout circuit to couple a sense node of the pixel circuit to a second readout capacitor of the second readout path via the clamping capacitor and the source follower transistor.

Brief description of drawings

[0023] The foregoing features and advantages, as well as others, will be described in detail in the following description of specific embodiments given by way of illustration and not limitation with reference to the accompanying drawings, in which:

[0024] Figure 1 is a circuit diagram illustrating an example of part of an image sensor;

[0025] Figure 2 is a timing diagram representing an example of signals in the circuit of Figure 1;

[0026] Figure 3 is a circuit diagram of a readout circuit of pixels of an image sensor according to an example embodiment of the present disclosure;

[0027] Figure 4 is a circuit diagram of a capacitor ratio in the circuit of Figure 1;

[0028] Figure 5 is a circuit diagram of a capacitor ratio in the circuit of Figure 3;

[0029] Figure 6 is a cross-section view of a clamping capacitor and part of the readout circuit of Figure 3 according to an example embodiment;

[0030] Figure 7 is a circuit diagram illustrating part of an image sensor according to an example embodiment of the present disclosure;

[0031] Figure 8 is a cross-section view of a pixel of an image sensor; and

[0032] Figure 9 is a graph representing an example of gain measurements in the circuits of Figures 1 and 3.

Description of embodiments

[0033] Like features have been designated by like references in the various figures. In particular, the structural and/or functional features that are common among the various embodiments may have the same references and may dispose identical structural, dimensional and material properties.

[0034] Unless indicated otherwise, when reference is made to two elements connected together, this signifies a direct connection without any intermediate elements other than conductors, and when reference is made to two elements linked or coupled together, this signifies that these two elements can be connected directly, or they can be connected via one or more other elements.

[0035] In the following disclosure, unless indicated otherwise, when reference is made to absolute positional qualifiers, such as the terms "front", "back", "top", "bottom", "left", "right", etc., or to relative positional qualifiers, such as the terms "above", "below", "higher", "lower", etc., or to qualifiers of orientation, such as "horizontal", "vertical", etc., reference is made to the orientation shown in the figures.

[0036] Unless specified otherwise, the expressions "around", "approximately", "substantially" and "in the order of" signify within 10%, and preferably within 5%.

[0037] Figure 1 is a circuit diagram of part of an image sensor according to one example.

[0038] In the example of Figure 1, the image sensor is implemented in two tiers T1 and T2 of a 3D circuit. The tier T1, which is for example a top tier of the image sensor, comprises an array of pixel circuits 100, one of which is shown in Figure 1. The tier T2, which is for example a bottom tier of the image sensor, for example comprises an array of readout circuits 102, one of which is shown in Figure 1, a readout circuit 102 being provided for each pixel circuit 100.

[0039] The pixel circuit 100 in the example of Figure 1 comprises four photodiodes PD1, PD2, PD3 and PD4, these photodiodes for example being pinned photodiodes having their anode coupled to a ground rail (GND), and their cathode coupled to a corresponding detection node DN1, DN2, DN3, DN4. Each of the detection nodes has a capacitance, represented by capacitors C_PD1, C_PD2, C_PD3 and C_PD4 respectively, which may correspond to parasitic capacitances and/or actual capacitors formed at these nodes.

[0040] The detection nodes DN1 to DN4 are respectively coupled to a sense node SN of the pixel circuit 100 via transfer gates Tg1, Tg2, Tg3 and Tg4, respectively controlled by transfer gate signals TG1, TG2, TG3 and TG4.

[0041] Of course, while an example of a pixel circuit having four photodiodes is provided in Figure 1, in alternative embodiments there could be any plurality of photodiodes each coupled to the sense node SN via a corresponding transfer gate.

[0042] The sense node SN for example has a capacitance represented by a capacitor C_SN, which for example results from parasitic capacitances or could be implemented by a

capacitor coupled between the sense node SN and the ground rail.

[0043] The sense node SN is for example coupled to a reset voltage rail VRST via a reset transistor 104 controlled by a reset signal RST. The sense node SN is further coupled to the control node of a source-follower transistor 106, having its main conducting nodes respectively coupled to a supply voltage rail VSF and to an output node 108 of the pixel circuit 100. In some embodiments, the source-follower transistor 106 is biased by a transistor 110 controlled by a signal BIAS and coupled between the output node 108 and the ground rail.

[0044] The output node 108 is for example coupled to the corresponding readout circuit 102 via a 3D inter-tier connection 112, which is for example a via or a Cu-Cu hybrid bonding connection.

[0045] The tier T1 further for example comprises a control circuit (CTRL) 113 generating the control signals TG1 to TG4, RST and BIAS.

[0046] The readout circuit 102 for example comprises a clamping capacitor 114, having one of its terminals coupled to the output node 108 of the pixel circuit 100 via the inter-tier connection 112, and its other terminal coupled to a common node 116 of the readout circuit. The common node 116 is for example coupled to a reference voltage rail VREF via a transistor 118, controlled at its control node by a signal CLAMP. The common node 116 is further coupled to four readout paths RO1, RO2, RO3 and RO4. More generally, the number of readout paths is for example equal to the number of photodiodes in the pixel circuit 100.

[0047] Each readout path RO1 to RO4 for example respectively comprises a selection transistor TS1 to TS4 coupling the common node 116 to a storage node STN1 to STN4 of each readout

path RO1 to RO4 respectively, the transistors TS1 to TS4 being respectively controlled by control signals SH1 to SH4. Each storage node STN1 to STN4 has a capacitance provided by a respective readout capacitor C_SH1 to C_SH4, each readout capacitor for example having one of its terminals coupled to ground. The storage nodes STN1 to STN4 are further coupled to control terminals of source-follower transistors SF1 to SF4 of the readout paths RO1 to RO4 respectively. The transistors SF1 to SF4 each have one of their main conducting nodes coupled to a supply voltage rail VDD, and their other main conducting node coupled, via a corresponding readout transistors TR1 to TR4 of the readout paths RO1 to RO4, to an output column line COL_n, where n is the column number, there for example being two or more columns in the array. The column line COL_n provides an output voltage signal Vx. The readout transistors TR1 to TR4 are controlled by control signals RD1 to RD4 respectively.

[0048] While not illustrated in Figure 1, the readout circuit 102 may further comprise a control circuit for generating the control signals CLAMP, SH1 to SH4 and RD1 to RD4.

[0049] The transistors of the pixel circuit 100 and of the readout circuit 102 are for example all NMOS transistors. However, in alternative embodiments, it would equally be possible to implement the pixel circuit and/or readout circuit 102 using only PMOS transistors, or a mixture of NMOS and PMOS transistors.

[0050] The advantage of positioning the clamping capacitor 114 between the pixel circuit 100 and the readout circuit 102 is that it can be used in order to perform a double sampling of the pixel circuit, also known in the field as correlated double sampling, as will be apparent from the following

description of the operation of the pixel circuit 100 and readout circuit 102 made with reference to Figure 2.

[0051] Figure 2 is a timing diagram illustrating examples of the signals of Figure 1 of TG1, RST, Vpx at the output node 108, CLAMP, SH1 and Vsh1 at the node STN1 according to an example embodiment.

[0052] The signals TG1, RST and CLAMP are initially high, causing the detection node DN1 to be reset to the reset voltage of the supply rail VRST and the nodes 108 and 116 to be at high voltages. An integration period INT1 starts at a time t1 when the signal TG1 goes low, isolating the detection node DN1 from the sense node SN1.

[0053] At a time t2, the reset signal RST goes low, causing, due to capacitive coupling, a slight drop in the voltage Vpx to a level VBLK corresponding to a reference voltage of the sense node SN. This corresponds therefore to a sampling of the reference level of the sense node SN. The node 116 being coupled to the voltage VREF via the transistor 118, the capacitor 114 is charged at a voltage VBLK-VREF.

[0054] At a time t3, the signal SH1 goes high, causing the voltage Vsh1 at the node STN1 to be set to the reference voltage VREF.

[0055] At a time t4, the signal CLAMP goes low, and the signal TG1 goes high shortly thereafter to initiate a transfer phase TRSF1, causing the charge at the node DN1 to be transferred to the sense node SN. This results in a decrease in the voltage at the sense node SN, and also causes a corresponding drop in the voltage Vpx at the output node 108, a corresponding drop in the voltage at the common node 116 and a corresponding drop in the voltage Vsh1 at the storage node STN1. This corresponds to a second sampling of the sense node SN, this time after the captured voltage signal has been transferred

to the sense node. Thus the node 108 falls to a level VSIG, and the node STN1 falls to a level V1. Since the capacitor 114 was previously charged at VBLK-VREF and the sampling capacitor C_SH1 was charged at VREF, the resulting voltage V1 present at the storage node STN1 is the equal to VREF minus the difference between the voltages VBLK and VSIG, attenuated by the capacitance ratio ACL. Thus the voltage V1 is equal for example to VREF-(VSIG-VBLK)*ACL, where the capacitance ratio ACL is for example equal to C_CL/(C_CL+C_SH1), where C_CL is the capacitance of the capacitor 114.

[0056] At a time t5, the signal TG1 goes low again. At a time t6, the signals RST and CLAMP are brought high. At a time t7 the signal SH1 is brought low, so that the voltage V1 is stored at the storage node STN1. The read sequence from time t2 to t7 is then for example repeated for the photodiode PD2, and again for the photodiode PD3 and then again for the photodiode PD4. The integration periods for the photodiodes PD2, PD3 and PD4 for example each start with an offset chosen such that the integration periods for each of the photodiodes of the pixel circuit are of substantially the same duration. The voltage V1 stored at each of the storage nodes STN1 to STN4 is then for example sequentially read via the common column line COL_n and the source follower transistors SF1 to SF4, enabled by its respective read transistor TR1 to TR4. A conventional double read can be performed in order to subtract VREF from V1. The second read operation is for example used to obtain VREF by asserting the signal CLAMP and the respective signal SH1 to SH4. Thus we measure:

[0057] VREF-V1=VREF-(VREF-(VSIG-VBLK)*ACL)=(VSIG-VBLK)*ACL

[0058] It should be noted that even if the integration within each pixel circuit 100 and the readout by each readout circuit 102 corresponds to a type of rolling shutter operation, the

time interval between the readouts of each pixel will be very short. Furthermore, the integration periods for the photodiode PD1 of each pixel circuit 100 of the array are for example synchronized with each other, and equally for the photodiodes PD2, for the photodiodes PD3 and for the photodiodes PD4. Thus, the operation corresponds to that of a global shutter.

[0059] The present inventor has found that the readout circuit 102 of Figure 1 results in a relatively high PRNU, for example of over 1 percent, resulting from process variations between the capacitor 114 and each of the capacitors C_SH1 to C_SH4. This problem is particularly notable when the capacitor 114 is of a different type to the capacitors C_SH1 to C_SH4. Indeed, in such a case, the process variations among the capacitors will be uncorrelated. Given that the capacitor 114 should generally be chosen to be considerably larger than each of the capacitors C_SH1 to C_SH4 in order to obtain a relatively high attenuation factor ACL, it would be desirable that the capacitor 114 is a MIM (metal-insulator-metal) capacitor, whereas the capacitors C_SH1 to C_SH4 are for example implemented by the gate of MOS transistors having their source and drains connected together, or by capacitive trench capacitors as described in more detail below. Thus the ratio between the capacitance of the capacitor 114 and that of each of the capacitors C_SH1 to C_SH4 will be variable, leading to a non-uniform pixel-pixel gain within a same readout circuit.

[0060] Figure 3 is a circuit diagram of a readout circuit 300 according to an example embodiment of the present disclosure. This readout circuit 300 for example replaces the readout circuit 102 of Figure 1, and is for example implemented in an array in a tier T2 of an image sensor, like the circuit 102. An advantage of implementing the image sensor in two tiers is

that the transistor technology used in each tier can differ. For example, the pixel circuits 100 (not shown in Figure 3) can be implemented in the transistor technology known in the field as GO2, also called "thick oxide", due to the thicker gate oxides of the transistors with respect to those of the tier T2. The technology GO2 is compatible with relatively high supply voltages commonly used for pinned photodiode technologies, for example up to substantially 3 V. Thanks to the presence of the series capacitor 114, the readout circuits 300 can be implemented in the transistor technology known in the field as GO1, which is compatible with relatively low supply voltages for example up to substantially 1.2 V. In alternative embodiments, the readout circuit 300 could be implemented in a 2D or single-tier image sensor.

[0061] The readout circuit 300 has many features in common with the readout circuit 102 of Figure 1, and these features have been labelled with like reference numerals and will not be described again in detail. With respect to the readout circuit 102, the circuit 300 additionally comprises a further transistor 302 having its control node coupled to a node 304, which is in turn connected to a terminal of the clamping capacitor 114. The transistor 302 is coupled by its main conducting nodes between the supply rail VDD and the common node 116. In some embodiments, a current source, for example implemented by a further transistor 306, is coupled between the node 116 and the ground rail, and controlled by a biasing voltage BIAS'. This voltage for example causes the transistor 306 to conduct a current that saturates the transistor 302 and thus causes the transistor 302 to operate in its linear operating region.

[0062] In the example of Figure 3, the transistors of the readout circuit 300 are all NMOS transistors. More generally, each of the transistors of the readout circuit 300 could be

implemented by an NMOS or a PMOS transistor, except for the transistors 302 and 306, which are for example both implemented by NMOS transistors, or both implemented by PMOS transistors.

[0063] A control circuit (CTRL) 308 for example generates the clamp signal CLAMP, the control signals SH1 to SH4 and RD1 to RD4, and the bias signal BIAS', these signals for example being common for a row of readout circuits.

[0064] Operation of the readout circuit 300 is for example similar to that of the readout circuit 102 as described above, and the timing diagram of Figure 2 for example applies equally to the circuit of Figure 3.

[0065] In particular, a method of reading a pixel value using the pixel readout circuit 300 for example involves the following operations:

- storing a first voltage level captured by the pixel circuit to the readout capacitor C_SH1 via the clamping capacitor 114, the transistor 302 and the selection transistor TS1 of the readout path RO1; and
- storing a second voltage level captured by the pixel circuit to the readout capacitor C_SH2 via the clamping capacitor 114, the transistor 302 and the selection transistor TS2 of the readout path RO2.

[0066] An advantage of providing the transistor 302 in a source-follower configuration between the clamping capacitor 114 and the common node 116 is that it provides a significant improvement in the PRNU, as will now be described with reference to Figures 4 and 5.

[0067] Figure 4 is a circuit diagram of a capacitor ratio in the circuit of Figure 1 between the clamping capacitor 114 and the readout capacitor C_SH1. Calling C_CL the capacitance

of the capacitor 114 and C_SH the capacitance of the capacitor C_SH1, the gain is thus equal to C_CL/(C_CL+C_SH).

[0068] Figure 5 is a circuit diagram of a capacitor ratio in the circuit of Figure 3. The gain in this circuit is now based on the ratio between the capacitance of the clamping capacitor 114 and the parasitic capacitance of the transistor 302. Calling the latter capacitance C_GS, the gain becomes equal to ASF*C_CL/(C_CL+C_GS), where ASF is the attenuation introduced by the source-follower configuration, typically equal to around 0.9. The capacitance C_GS being typically far smaller than the capacitance C_SH, this leads to a strong increase in the gain. Furthermore, the gain is no longer dependent on the capacitance C_SH, meaning that it no longer varies with variations in the capacitances among the readout capacitors.

[0069] Figure 6 is a cross-section view of part of readout circuit 300 comprising the capacitor 114 according to an example embodiment in which this capacitor is a MIM capacitor.

[0070] The structure for example comprises a substrate 602 on which is formed a device layer 604 comprising transistor devices 605. One of these devices for example corresponds to the source-following transistor 302 of the readout circuit 300. A metal interconnection layer 606 is formed over the device layer 604, and comprises layers 608 of metal interconnected by vias 610 formed for example of copper. The MIM capacitor 114 is for example formed above the metal interconnection layer 606, and for example comprises metal plates 612 and 614 sandwiching an insulating layer 616 for example formed of oxide. The metal plate 614 is for example connected, by a via 618 formed in an upper interconnection layer 620, to the inter-tier connection 112, which is for example a wafer-to-wafer copper bond.

[0071] An advantage of the circuit configuration of Figure 3 is that the inter-tier connection 112 is connected directly to the MIM capacitor, without first descending to the surface of the substrate. This makes an implementation like that of Figure 6 possible in which the metal interconnection layer 606 is not used to connect the interconnect 112 to the MIM capacitor 114, thereby avoiding the loss in surface area and allowing the MIM capacitor 114 to be relatively large.

[0072] Figure 7 is a circuit diagram of part of an image sensor according to a further example embodiment. The circuit of Figure 7 implements a pixel circuit similar to the circuit 100 of Figure 1 and a readout circuit similar to the circuit of Figure 3. However, there is a different distribution of the components between the tiers T1 and T2, as will now be described in more detail (for ease of illustration, the photodiode capacitances C_PD1 to C_PD4 and the control circuits 113 and 308 are not represented in Figure 7).

[0073] The circuit of Figure 7 is for example fabricated using 3D sequence layering, this technique being described in more detail below with reference to Figure 8.

[0074] Figure 8 is a cross-section view of a pixel of an image sensor and substantially reproduces Figure 4 of the US patent published as US 7,417,268 in the name of STMicroelectronics S.A. While the circuit of this pixel is not the same as that of Figure 7, the process used to form the image sensor of Figure 8 can be applied to the circuit of Figure 7.

[0075] The image sensor of Figure 8 comprises a lower semiconductor substrate 800 and an upper semiconductor substrate 801 separated from each other by an intermediary insulating layer 802. The two substrates are for example p-type doped and connected to ground GND. The pixel comprises

a photodiode 803 and a transfer gate 804 formed in a tier T1, and three read transistors formed in a tier T2. Photodiode 803 comprises a heavily-doped p-type area 805 positioned at the surface of lower substrate 800, and an n-type doped buried area 806 positioned under p+ area 805. A heavily-doped n-type contact area 821 is positioned on one side of the transfer gate 804. The contact area 821 is connected to a source/drain area of one of the transistors of the tier T2 via an inter-tier connection formed by a metallization 850 comprising a portion passing through an opening in the insulating layer 802 and in the upper substrate 801, and a portion formed in an insulating layer 860 covering the upper substrate 801, this portion for example corresponding to part of a standard metal layer.

[0076] Although not shown, a row line RL connected to the transfer gate 804 is for example coupled to a metal layer of the tier T2 via a metallization similar to the metallization 850.

[0077] To increase the sensitivity of an image sensor, a heavily-doped P-type area 870 at the level of the lower surface of lower substrate 800 may be provided. Furthermore, filter portions 880 that allow incident photons in the green, blue, or red wavelength ranges may be placed against the p+ area 870 on the lower surface of lower substrate 800.

[0078] An image sensor comprising pixels such as that shown in Figure 8 may be obtained according to the following manufacturing method.

[0079] The transfer gates and the photodiodes are first formed above a lower substrate. An ion implantation of n-type dopant elements is performed to form n-type buried areas 806 of the photodiodes. Insulating spacers may be formed on the sides of the transfer gate according to a conventional method.

An ion implantation of P-type dopant elements is then performed to form at the surface of the lower substrate heavily-doped P-type areas 805. An ion implantation of n-type dopant elements is then performed to form at the substrate surface heavily-doped n-type contact areas 821. The lower substrate and transfer gates are then covered by an insulating layer on which a semiconductor layer is deposited to form an upper substrate. The upper substrate may be obtained by a deposition of a semiconductor bonding layer, for example made of silicon, on the intermediary insulating layer, then by epitaxial growth of a semiconductor layer on this bonding layer in an epitaxy furnace.

[0080] The read transistors are then conventionally formed in and above the upper substrate. Finally, the upper substrate and the read transistors are covered with the upper insulating layer 860.

[0081] The metallizations connecting the access transistors and the read transistor may be formed in various ways. One way comprises, after the previously-described steps, forming openings in the upper insulating layer, in the upper substrate, and in the intermediary insulating layer separating the two substrates, and of filling the openings with a conductive material. Alternatively, the metallizations could be formed in stages following the formation of each of the insulating layer 802, the substrate 801 and the insulating layer 860.

[0082] Once the upper insulating layer has been deposited, the lower substrate may be thinned down, for example, according to a chemical-mechanical polishing method. A heavily-doped p-type area is then formed by ion implantation on the lower surface side of the lower substrate, after which a deposition of filters according to a conventional method is performed.

[0083] A sequential 3D process is also discussed in more detail in the publication by Perceval Coudrain et al. entitled "Investigation of a Sequential Three-Dimensional Process for Back-Illuminated CMOS Image Sensors With Miniaturized Pixels", IEEE Transactions on Electron Devices, Vol. 56, No. 11, November 2009.

[0084] With reference again to Figure 7, the sensor tier T1 comprises only transfer gates, photodiodes and capacitors, the transistors 104, 106 and 110 having been moved to the tier T2. Furthermore, the capacitors C_SH1 to C_SH4 of the readout circuit 300 are for example implemented in the tier T1.

[0085] In the example of Figure 7, there are fourteen inter-tier connections 701 to 714, which are for example formed by metallizations similar to the metallization 850 of Figure 8. The inter-tier connections 701 to 704 respectively couple the transfer gates Tg1 to Tg4 of the sensor tier to the readout tier T2. The inter-tier connections 705 to 708 respectively supply the control signals TG1 to TG4 to the transfer gates Tg1 to Tg4. Indeed, in the embodiment of Figure 7, the control circuit 113 is for example implemented in the tier T2. The inter-tier connections 709 to 712 respectively connect the storage nodes STN1 to STN4 to the corresponding capacitors C_SH1 to C_SH4. The inter-tier connections 713 and 714 are for example used to connect the substrate of tier T1 to a fixed voltage source or to ground to provide a drain sink or source for free carrier evacuation.

[0086] In the example of Figure 7, the transistors 106, 110, 302 and 306 are implemented by PMOS transistors, but could be NMOS transistors in alterative embodiments.

[0087] An advantage of forming the capacitors C_SH1 to C_SH4 in the tier T1 is that the technology employed in this tier

for example permits relatively high density capacitors to be formed, for example of the CDTI (capacitive deep trench isolation) type. Furthermore, thanks to the sequential stacking technology, the vias implementing the inter-tier connections can for example be of significantly smaller dimensions than the interconnection 112 of Figure 1, for example in the order of 90 nm compared to around 2 μm in the case of the interconnection 112.

[0088] Figure 9 is a graph representing an example of simulated gain measurements in the circuits of Figures 1 and 3. Performance of the circuit of Figure 7 is similar to that of Figure 3. The x-axis represents the input voltage VIN, corresponding to the voltage present at the sense node SN, while the y-axis represents the output voltage VOUT, corresponding to the voltage stored at the storage node. A region 902 in the graph shows simulated measurements in the circuit of Figure 1, while a region 904 shows simulated measurements in the circuit of Figure 3. It can be seen that the region 904 not only corresponds to higher gains when compared to those of the region 902, but also the dispersion 906 of the gain in the region 904 for a given input voltage is significantly less than the dispersion 908 of the gain in the region 902 for the corresponding input voltage. The amount of gain dispersion is a measure of the PRNU, and thus the circuit of Figure 3 leads to a significantly lower PRNU than the circuit Figure 1.

[0089] Various embodiments and variants have been described. Those skilled in the art will understand that certain features of these embodiments can be combined and other variants will readily occur to those skilled in the art. For example, it will be apparent to those skilled in the art that while circuits implemented using MOS transistor technology have been described, in alternative implementations other

transistor technologies could be used. Furthermore, one or more of the NMOS transistors in the various circuit could be implemented by PMOS transistors in alternative embodiments, and/or one or more of the PMOS transistors in the various embodiments could be implemented by NMOS transistors.

[0090] Finally, the practical implementation of the embodiments and variants described herein is within the capabilities of those skilled in the art based on the functional description provided hereinabove. In particular, those skilled in the art will understand how to implement the pixel circuit 100, and in particular how to implement suitable photodiodes and transfer gates for capturing and transferring pixel readings.

CLAIMS

1. An image sensor comprising:
   a pixel circuit (100) having a first photodiode (PD1) coupled to a sense node (SN) via a first transfer gate (Tg1); and
   a pixel readout circuit (102) comprising:
   - a clamping capacitor (114) having a first terminal coupled to an output node (108) of the pixel circuit (100);
   - a first readout path (RO1) comprising a first selection transistor (TS1) and a first readout capacitor (C_SH1) for storing a first voltage level captured by the pixel circuit (100);
   - a second readout path (RO2) comprising a second selection transistor (TS2) and a second readout capacitor (C_SH2) for storing a second voltage level captured by the pixel circuit (100); and
   - a source follower transistor (302) having its control node coupled to a second terminal of the clamping capacitor (114), a first of its main conducting nodes coupled to a first supply voltage rail (VDD, GND), and a second of its main conducting nodes coupled to the first and second readout paths (RO1, RO2).

2. The image sensor of claim 1, wherein the photodiode (PD1) is a pinned photodiode.

3. The image sensor of claim 1 or 2, wherein the pixel circuit (100) further comprises a second photodiode (PD2) coupled to the sense node (SN) via a second transfer gate (Tg2), the first voltage level being captured by the first photodiode (PD1) and the second voltage level being captured by the second photodiode (PD2).

4. The image sensor of any of claims 1 to 3, wherein the pixel readout circuit further comprises a third transistor

(118) coupling the second terminal of the clamping capacitor (114) to a second supply voltage rail (GND, VDD).

5. The image sensor of any of claims 1 to 4, wherein the pixel readout circuit further comprises a current source (306) coupled between the second main conducting node of the source follower transistor (302) and the second supply voltage rail (GND, VDD).

6. The image sensor of any of claims 1 to 5, wherein the clamping capacitor (114) is of a first type, and each of the first and second readout capacitors (C_SH1, C_SH2) is of a second type different to the first type.

7. The image sensor of claim 6, wherein the clamping capacitor (114) is a metal-insulator-metal (MIM) capacitor.

8. The image sensor of claim 6 or 7, wherein the first and second readout capacitors (C_SH1, C_SH2) are capacitive trench capacitors.

9. The image sensor of any of claims 1 to 8, wherein:
- the first readout path (RO1) further comprises a source follower transistor (SF1) having its control node coupled to a first storage node (STN1) connected to a first terminal of the first readout capacitor (C_SH1), the source follower transistor (SF1) of the first readout path having one of its main conducting nodes coupled to a column line (COL_n) via a first readout transistor (TR1); and
- the second readout path (RO2) further comprises a source follower transistor (SF2) having its control node coupled to a second storage node (STN2) connected to a first terminal of the second readout capacitor (C_SH2), the source follower transistor (SF2) of the second readout path having one of its main conducting nodes coupled to the column line (COL_n) via a second readout transistor (TR2).

10. The image sensor of any of claims 1 to 9, wherein the pixel readout circuit further comprises one or more further readout paths (RO1, RO2) coupled to the second main conducting node (304) of the source follower transistor (302).

11. The image sensor of any of claims 1 to 10, comprising:
- a first tier (T1) comprising an array of pixel circuits including said pixel circuit (100), the pixel circuits being configured to operate in a global shutter mode; and
- a second tier (T2) comprising, for each of the pixel circuits (100), at least part of the pixel readout circuit (102) of any of claims 1 to 10.

12. The image sensor of claim 11, wherein the second tier comprises, for each of the pixel circuits (100), the pixel readout circuit (102) of any of claims 1 to 10, each pixel readout circuit being coupled to the output node (108) of a corresponding one of the pixel circuits (100) via a corresponding inter-tier connection (112).

13. The image sensor of claim 11, wherein the first and second readout capacitors (C_SH1, C_SH2) are part of the first tier (T1), the first readout capacitor (C_SH1) being coupled to part of a corresponding readout circuit (102) via a first inter-tier connection (709) and the second readout capacitor (C_SH2) being coupled to part of a corresponding readout circuit (102) via a second inter-tier connection (710).

14. The image sensor of claim 11 or 13, wherein the second tier further comprises a further source-follower transistor (106) having its gate coupled to the sense node of the pixel circuit (100) and one of its main conducting terminals coupled to the first terminal of the clamping capacitor.

15. A method of reading a pixel value from a pixel circuit (100) using a pixel readout circuit (300), the pixel circuit (100) comprising a first photodiode (PD1) coupled to a sense node (SN) via a first transfer gate (Tg1), the method comprising:

- controlling a first selection transistor (TS1) of a first readout path (RO1) of the pixel readout circuit (300) to couple a sense node (SN) of the pixel circuit (100) to a first readout capacitor (C_SH1) of the first readout path (RO1) via a clamping capacitor (114) and via a source follower transistor (302) having its control node coupled to a terminal of the clamping capacitor (114); and
- controlling a second selection transistor (TS2) of a second readout path (RO2) of the pixel readout circuit (300) to couple a sense node (SN) of the pixel circuit (100) to a second readout capacitor (C_SH2) of the second readout path (RO2) via the clamping capacitor (114) and the source follower transistor (302).

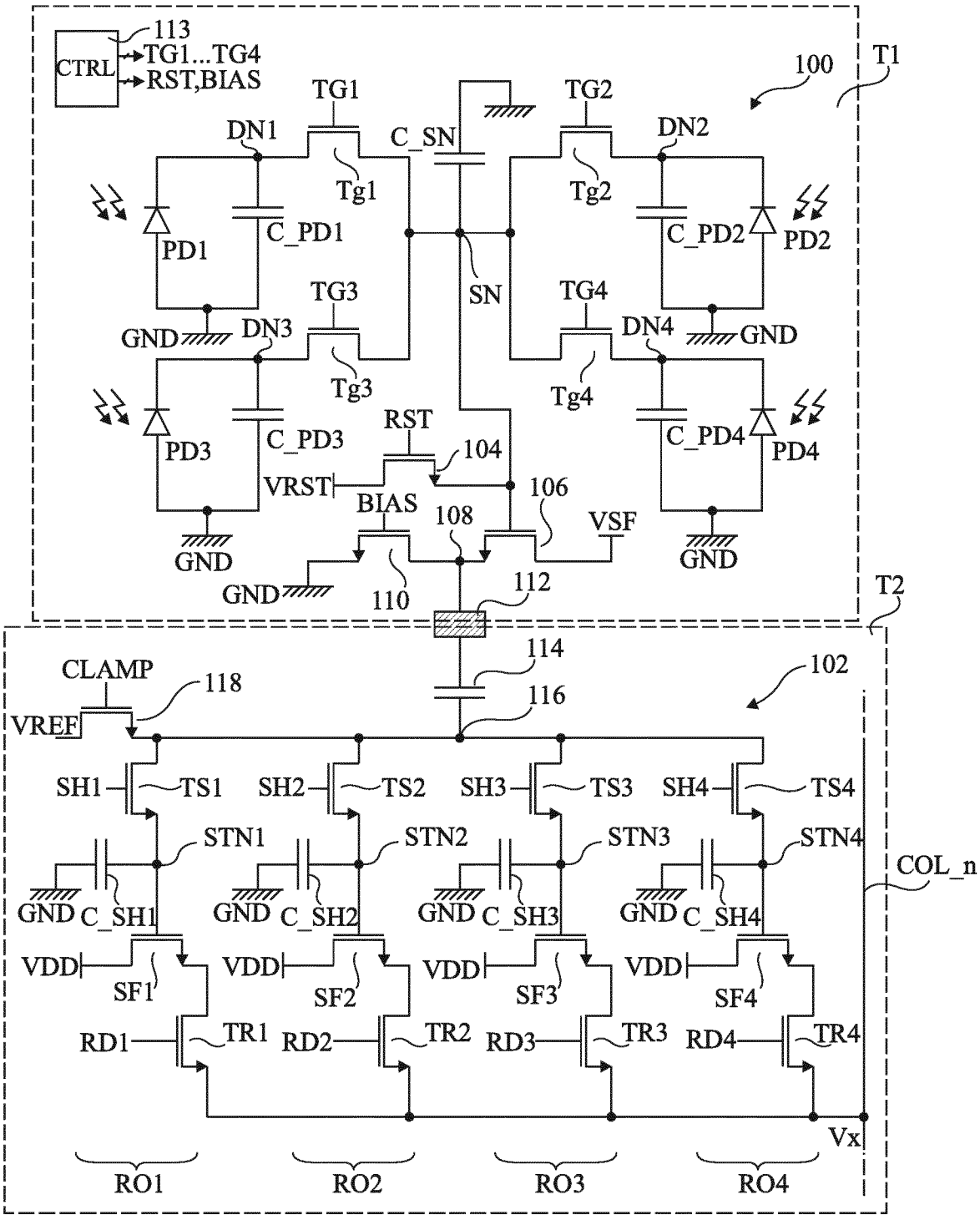

CTRL
113
TG1...TG4
RST,BIAS
100
T1
TG1
TG2
DN1
C_SN
DN2
Tg1
Tg2
PD1
C_PD1
C_PD2
PD2
SN
TG3
TG4
GND
DN3
DN4
GND
Tg3
Tg4
PD3
C_PD3
RST
C_PD4
PD4
104
VRST
106
BIAS
108
VSF
GND
GND
GND
110
112
T2
114
CLAMP
118
102
VREF
116
SH1
TS1
SH2
TS2
SH3
TS3
SH4
TS4
STN1
STN2
STN3
STN4
COL_n
GND
C_SH1
GND
C_SH2
GND
C_SH3
GND
C_SH4
VDD
VDD
VDD
VDD
SF1
SF2
SF3
SF4
RD1
TR1
RD2
TR2
RD3
TR3
RD4
TR4
Vx
RO1
RO2
RO3
RO4

Fig 1

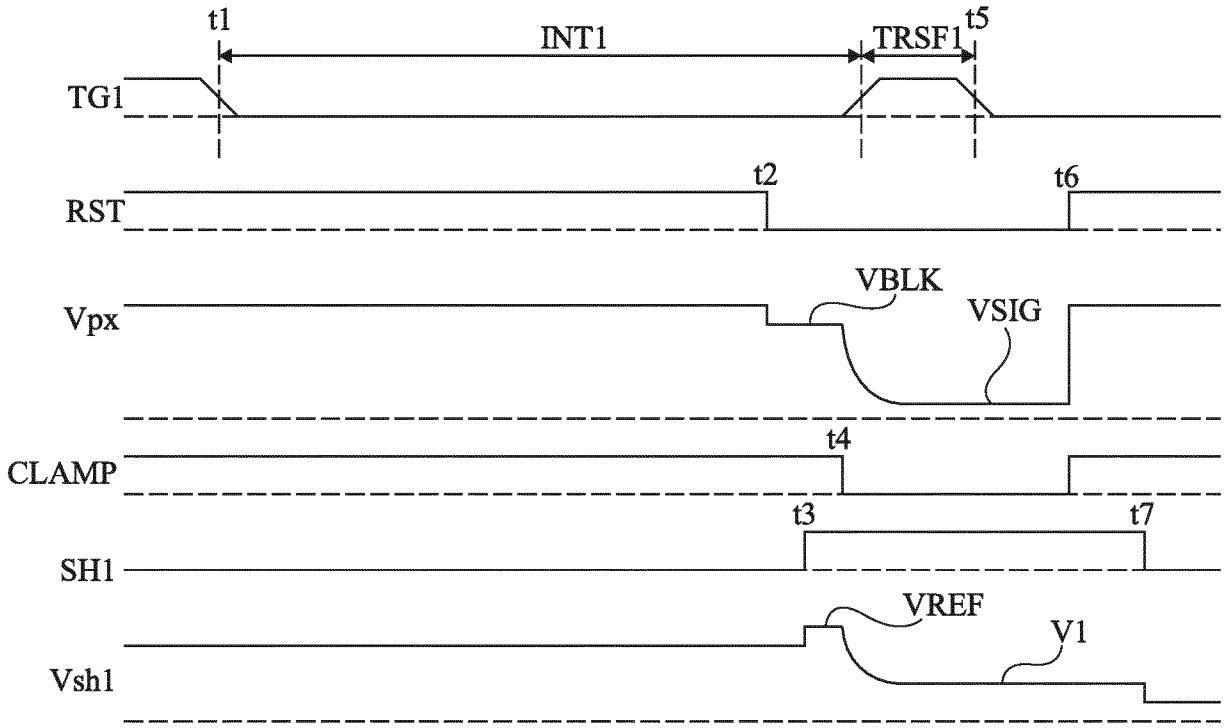

t1
INT1
TRSF1
t5
TG1
t2
t6
RST
VBLK
VSIG
Vpx
t4
CLAMP
t3
t7
SH1
VREF
V1
Vsh1

Fig 2

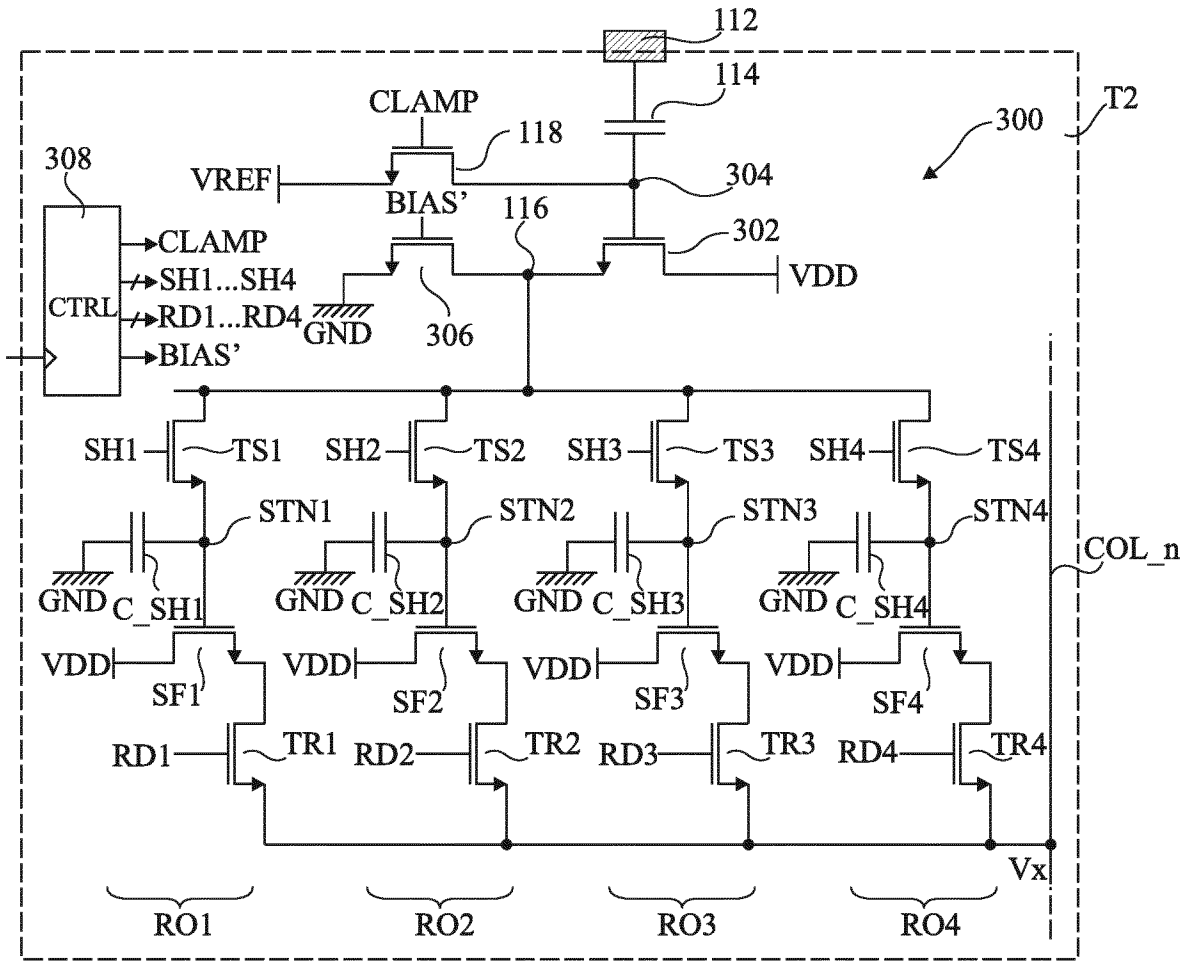

112
114
CLAMP
118
300
T2
308
VREF
BIAS'
116
304
302
CLAMP
SH1...SH4
RD1...RD4
BIAS'
CTRL
GND
306
VDD
SH1
TS1
SH2
TS2
SH3
TS3
SH4
TS4
STN1
STN2
STN3
STN4
COL_n
GND
C_SH1
C_SH2
C_SH3
C_SH4
VDD
SF1
SF2
SF3
SF4
RD1
TR1
RD2
TR2
RD3
TR3
RD4
TR4
Vx
RO1
RO2
RO3
RO4

Fig 3

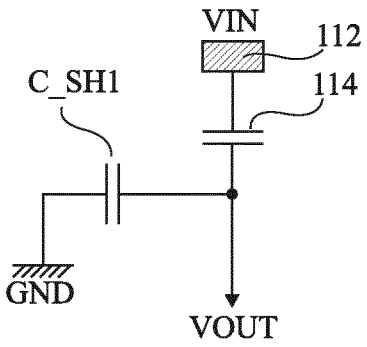


Fig 4

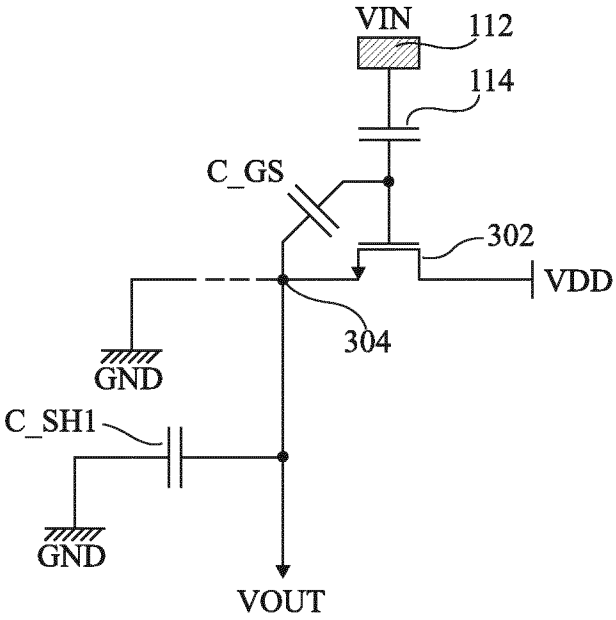


Fig 5

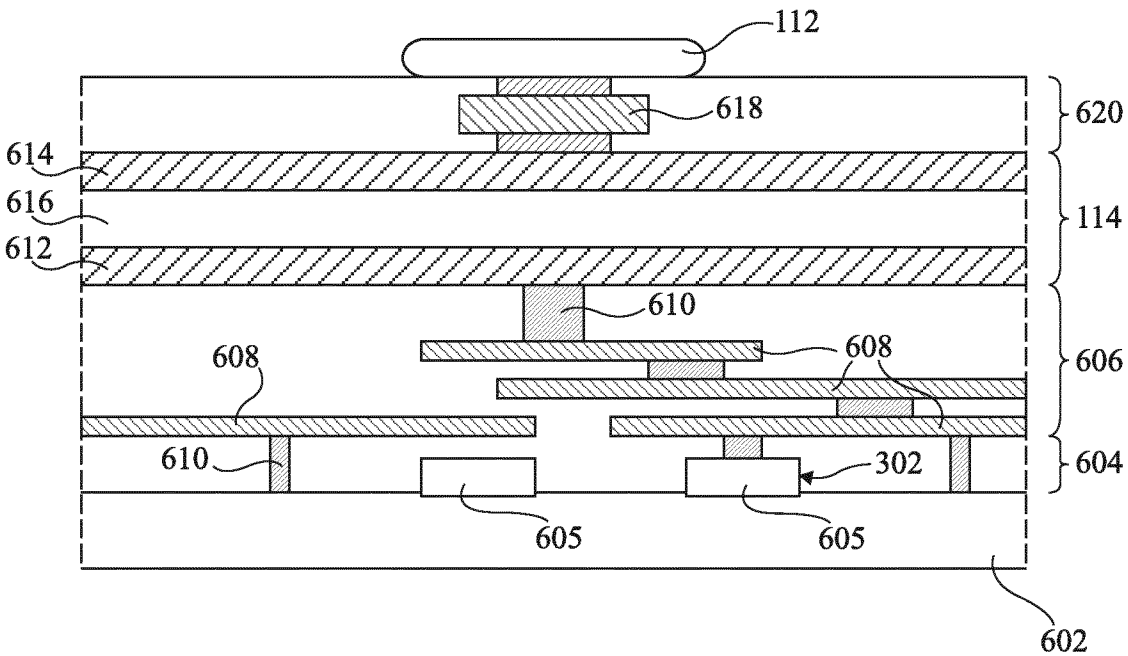


Fig 6

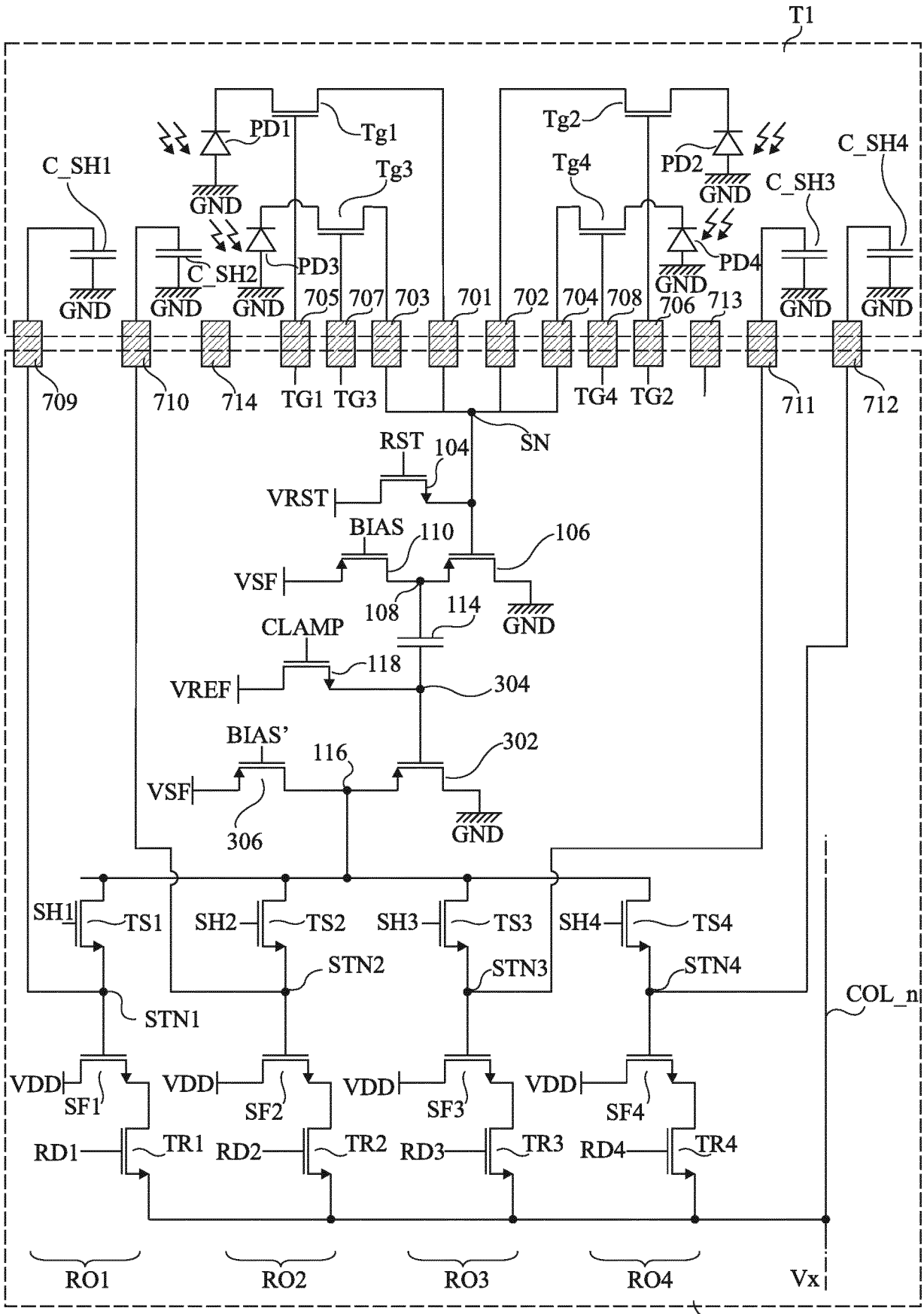

T1
PD1
Tg1
Tg2
PD2
C_SH4
C_SH1
Tg3
Tg4
GND
C_SH3
C_SH2
PD3
PD4
705
707
703
701
702
704
708
706
713
709
710
714
TG1
TG3
TG4
TG2
711
712
SN
RST
104
VRST
BIAS
110
106
VSF
108
114
CLAMP
118
VREF
304
BIAS'
116
302
306
SH1
TS1
SH2
TS2
SH3
TS3
SH4
TS4
STN2
STN3
STN4
STN1
COL_n
VDD
SF1
SF2
SF3
SF4
RD1
TR1
RD2
TR2
RD3
TR3
RD4
TR4
RO1
RO2
RO3
RO4
Vx
T2

Fig 7

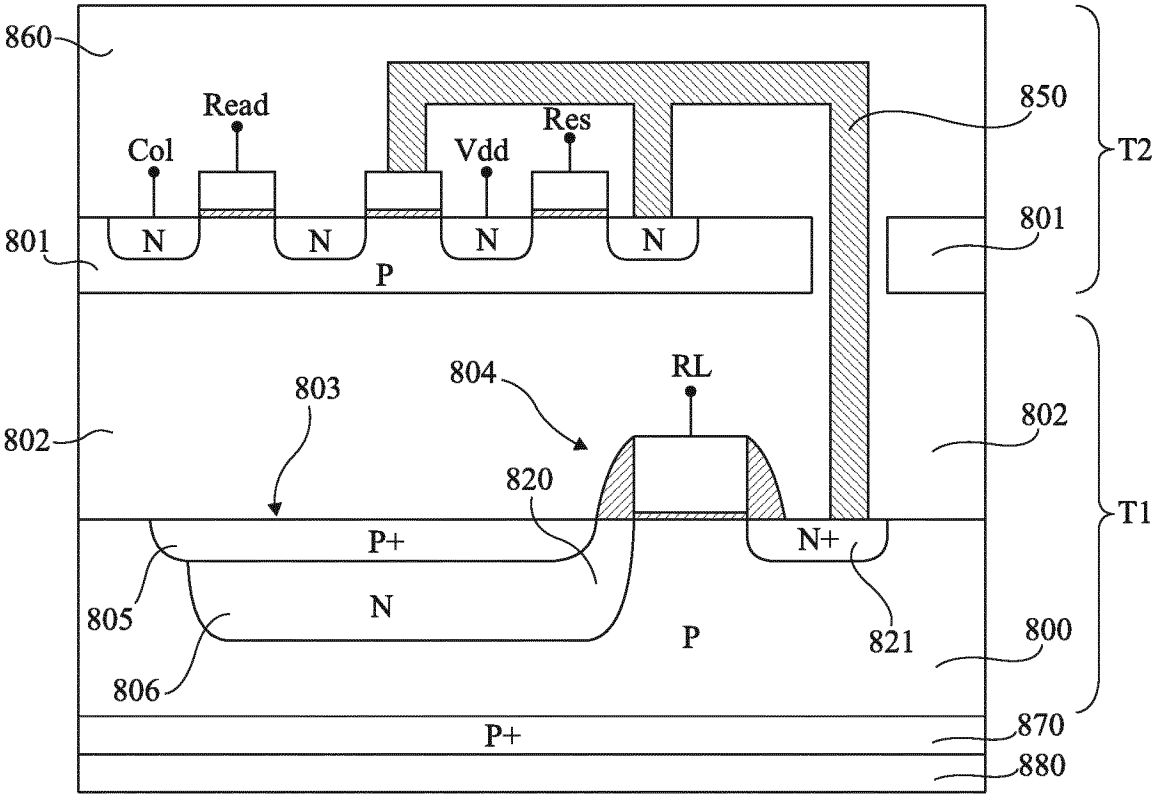

860
Read
Col
Res
Vdd
850
T2
801
N
N
N
N
P
801
803
804
RL
802
802
820
T1
P+
N+
805
N
P
821
800
806
P+
870
880

Fig 8

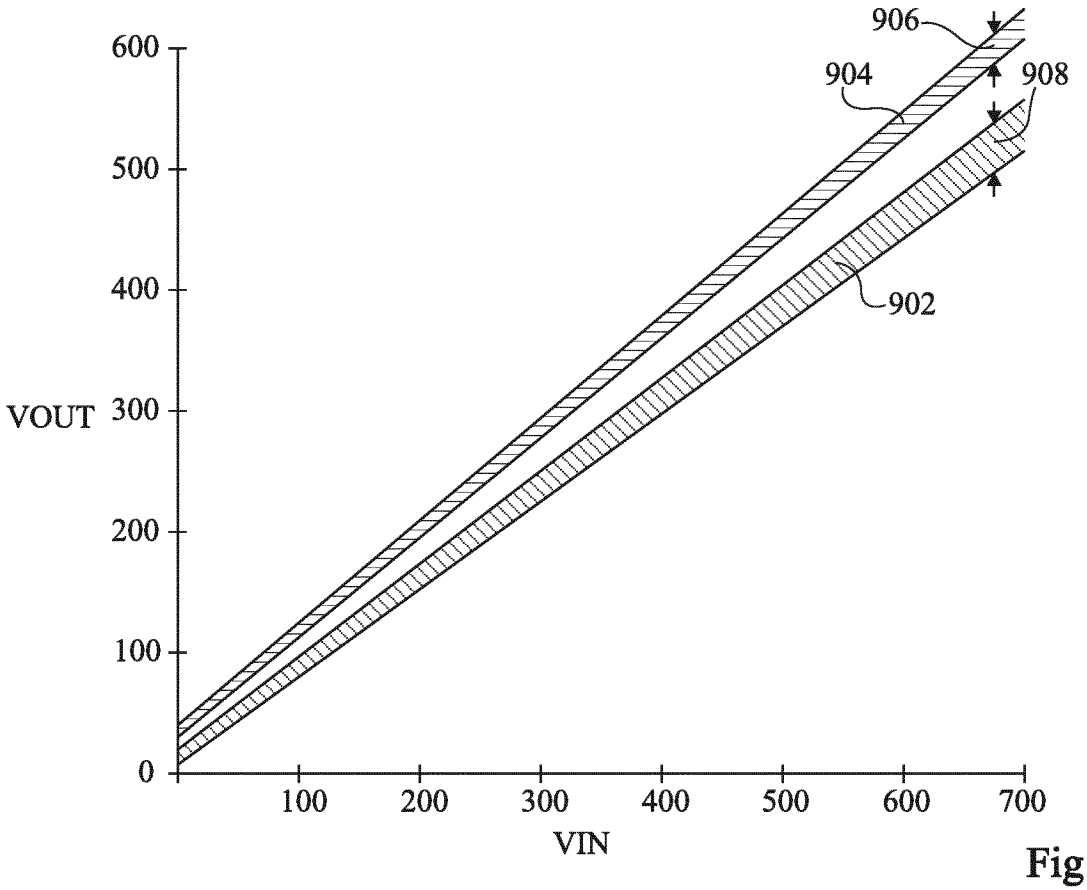

906
904
908
600
500
400
VOUT
300
200
100
0
902
100
200
300
400
500
600
700
VIN

Fig 9

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2019/072189

A. CLASSIFICATION OF SUBJECT MATTER
INV. H04N5/378 H04N5/3745
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2013/141618 A1 (KOBAYASHI KENJI [JP]) 6 June 2013 (2013-06-06) paragraphs [0137] - [0142] paragraphs [0151] - [0153] paragraphs [0160] - [0163]; figure 17	1-15
Y	US 2012/075515 A1 (DOWAKI KANAKO [JP] ET AL) 29 March 2012 (2012-03-29) paragraphs [0020] - [0025]; figure 1 paragraph [0026]; figure 2A	1-15
A	US 2013/161487 A1 (SAKAGUCHI NAOFUMI [JP] ET AL) 27 June 2013 (2013-06-27) paragraphs [0083] - [0099]; figure 6 paragraph [0111]	1-15

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
14 October 2019	23/10/2019

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Berne, Jean-François

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2019/072189

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US 2013161487 A1	27-06-2013	NONE	