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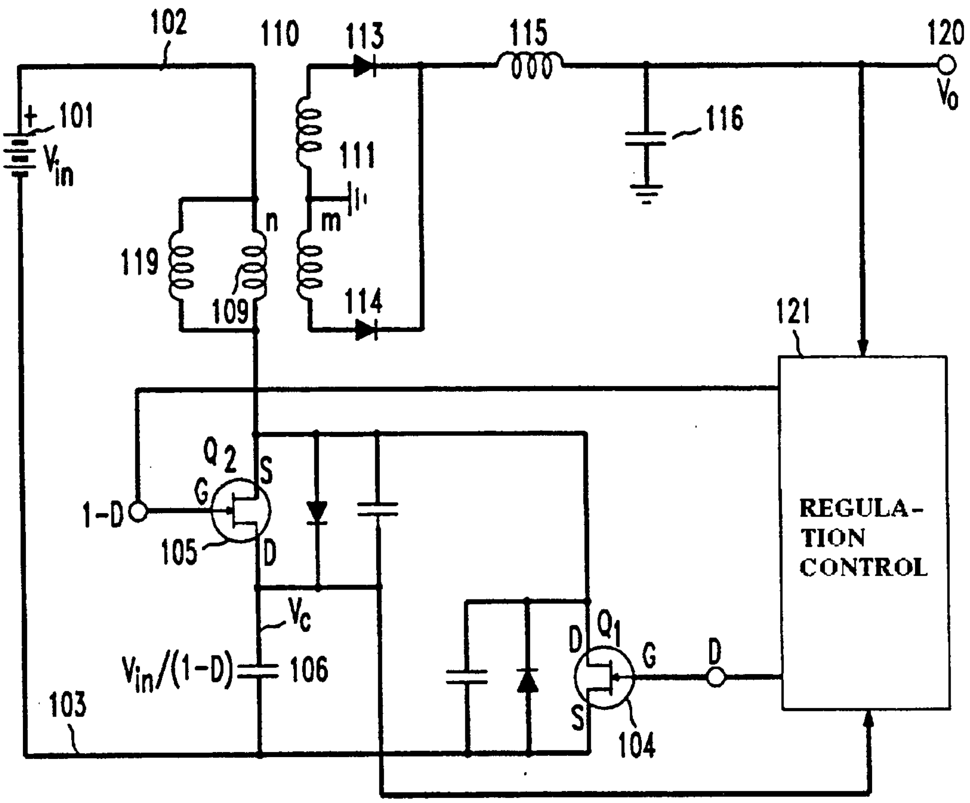
(54) Title: CONTROL APPARATUS FOR LIMITING VOLTAGE ON A CORE RESET CAPACITOR



(57) Abstract

A power converter circuit requiring the periodic reset of a core of a power transformer (110) includes a control circuit (121) operative to alter a response of the converter's voltage regulation feedback loop to limit and/or control the power switch (104) duty cycle to regulate a voltage of the reset capacitor (106) whenever the reset capacitor (106) sustains a voltage above a preset threshold.

CONTROL APPARATUS FOR LIMITING VOLTAGE ON A CORE RESET CAPACITOR

Field of the Invention

This invention relates to power converters in which a magnetic core in the converter's power train requires active control of a flux therein and in particular to the control of the voltage of a capacitor used in circuitry for achieving this control.

Background of the Invention

Forward, push-push, flyback and similar converter topologies require that the power transformer core be periodically reset in each cycle of operation. The core reset voltage is supplied by a voltage reset capacitor which is periodically charged each cycle to provide the needed reset voltage.

The voltage due to charge stored on the reset capacitor is dependent on the duty cycle of the converter's power switch. Accordingly, the circuitry is designed so that the proper reset voltage is stored by the reset capacitor during normal operation (i.e., normal duty cycles).

The input voltage to the converter may drop below the low limit operating voltage for which the converter is designed. These low input voltage conditions can be caused by "brownout" conditions in the ac mains, or batteries discharged beyond their capacity, or system faults. At low input voltages, outside the normal designed input voltage range of the converter, the duty cycle of the power switches tends toward unity. This causes abnormally high voltages to be supplied by the reset capacitor, which may cause a failure of the converter circuit.

Similarly, if the input voltage rises above the high limit voltage of the input voltage range, the reset capacitor can attain a very high voltage level which may also destroy components of the converter.

Summary of the Invention

A power converter utilizing a charge storage capacitor for periodic reset of a transformer core monitors the voltage of the voltage storage capacitor and controls the feedback regulation of the converter to limit the maximum voltage which may be attained by the voltage storage capacitor substantially as claimed in claim 1.

Brief Description of the Drawing

In the drawing:

FIG. 1 is a schematic of a power converter circuit requiring periodic core reset;

FIG. 2 is another schematic of a power converter circuit requiring periodic core reset;

FIG. 3 is a block schematic of a control system for regulating a voltage of a reset capacitor voltage;

FIG. 4 is a block schematic of an illustrative regulation circuit for the power converters of FIGS. 1 and 2 which regulates a voltage of the reset capacitor when this voltage exceeds a predetermined limit;

FIG. 5 is a block schematic of a control system for limiting a voltage of a reset capacitor voltage to some safe threshold value;

Detailed Description

Two push push topology power converter schematics requiring periodic transformer core reset are shown in FIGS. 1 and 2. In the converter of FIG. 1 DC input voltage supplied by a voltage source 101, to input lead 102, is periodically applied to a primary winding 109 of the power transformer 110 in response to periodic switching of the power switch FETs 104 and 105. FET 104 is directly connected to a return lead 103 to the voltage source 101. FET 105 is connected to the return lead 103, via a reset capacitor 106. In operation the flux in the core of transformer 110 is driven by FET 104 in one direction and hence the core may saturate. This reset capacitor 106 accumulates a stored voltage during operation of the converter and is connected to the transformer primary winding 109 when the FET 105 is conducting and in order to reset the core of the transistor 110 by recycling the flux stored in its magnetizing inductance 119.

Power output to an output terminal 120 is supplied by a tapped secondary 111 of the power transformer 110 through the rectifying diodes 113 and 114 and a filter including inductor 115 and capacitor 116.

A regulation control 121 is connected to monitor the output voltage at terminal 120 and the voltage of reset capacitor 106. These inputs are utilized to generate the drive signals applied to the FETs 104 and 105. These drive signals modulate the FETs to control one of the monitored voltages. The output voltage is regulated when the sensed reset capacitor voltage is deemed satisfactory and when the reset capacitor voltage exceeds a threshold level the FETs are modulated to control the voltage of the reset capacitor.

A second push push converter topology in FIG. 2 has the reset capacitor 106 connected, via lead 212, to the input lead 102 instead of the return lead.

The reset capacitor voltage in these converters (FIGS. 1, 2) can be described in the steady state by Equations 1 or 2. (Equation 1 applies to circuits configured similar to FIG. 1, and Equation 2 to circuits configured similar to FIG. 2. In these equations, D is the duty cycle, which is the fraction of cycle time that the FET switch 104 is conducting.)

$$V_c = V_{in}/(1-D) \qquad (1)$$

for the topology at FIG. 1. and

$$V_c = (V_{in} \cdot D)/(1-D) \qquad (2)$$

for the topology at FIG. 2.

For low dc input voltages, sustained outside the normal operating range of the converter, the duty cycle D can approach unity, in an attempt to maintain the regulated output voltage, resulting in arbitrarily high values for the voltage of the reset capacitor 106, causing circuit failure. The high reset capacitor voltage, occurring at low input voltage, is caused by the duty cycle of the power switch, increasing arbitrarily close to unity. In instances where the input voltage is high exceeding the input range upper voltage value the reset capacitor also assumes a high voltage above a prescribed limit. The duty cycle, of the power switching in both instances, is limited to reduce this reset capacitor voltage by altering the feedback control loop when the reset capacitor sustains a voltage higher than a prescribed limit. The regulation control 121, hence, limits the reset capacitor voltage when the dc input voltage falls outside the normal operating range for the converter.

The functional implementation of a feedback regulation control, embodying the principles of the invention, is shown in the FIG. 3. In FIG. 3, V_o, applied to the terminal 301, is the output voltage of the dc-dc converter represented in either FIG. 1 or FIG. 2. Each converter is required to be regulated so that its output voltage is equal to a regulated output voltage. Following commonly used control practice for power supplies, a V_{ref}, on lead 302, is subtracted from the monitored output voltage V_o (or a voltage related to V_o) in the summing circuit 303 and the difference voltage is then amplified. The resulting amplified difference signal is then modified by a network 305 to alter its frequency-dependent gain and phase characteristics. This frequency-dependent network is represented on FIG. 3 by the network 305. This signal is then used by a PWM control process to set the switching frequency and duty cycle D for the main power switching FET 105 shown in FIGS. 1 and 2. The characteristics of the network 305 and the PWM controller are selected so that the resulting system is stable and so that it exhibits desirable response characteristics such as response time, ringing, and overshoot.

In a similar manner, the reset capacitor voltage V_c in FIG. 3 is applied to the input lead 311. This voltage, representing the reset capacitor voltage, is required to be less than a maximum value V_{max} applied to a summing circuit 313 on lead 312. The signal path on FIG. 3 begins with the input V_c on lead 311 and ends in the duty cycle control pulse D on outer lead 321. When the reset capacitor voltage V_c exceeds V_{max}, the value of the reset capacitor voltage is regulated to the value V_{max} , the value of the reset capacitor voltage is regulated to the value V_{max} . The frequency-dependent gain and phase network 315, in conjunction with PWM controller, is selected to provide stable operation of this circuit, also with desirable response characteristics.

The output of the gain and phase networks 305 and 315 is applied to a switch 310, which is operative to transmit the maximum value, applied to it by the networks 305 and 315. This allows the PWM controller 320 to regulate the output voltage, to the voltage specified by V_{ref} , as long as the reset capacitor voltage is less than V_{max} . Otherwise, the PWM controller regulates the reset capacitor voltage to the regulated value determined by V_{max} . Thus, whenever the output voltage is the operative variable in the feedback control loop, the reset capacitor voltage is regulated, and whenever the reset capacitor voltage is the operated variable, the output voltage is regulated. In this illustrative embodiment these regulated values are V_{max} and V_{ref} .

A more detailed implementation of the regulation control circuitry shown in FIG. 3 is shown in FIG. 4. Two operational amplifiers 405 and 415 are shown which provide the amplification functions for the networks 305 and 315 shown in FIG. 3. Simple R-C networks, 407 and 417, connected to the operational amplifiers provide means of controllably shaping the frequency characteristics of these circuits. A particular circuit implementation may require the diodes 408 and 418, to be connected to the amplifier outputs, select the minimum of the two error signals, δV_1 and δV_2 supplied by the two operational amplifiers 405 and 415.

The circuit details will become apparent to those skilled in the art from the following description of its operation. When the input voltage to the DC-DC converter lies within its specified operating range of input voltages for the converter, the DC voltage sustained by the reset capacitor $106C_{reset}$ will be less than a maximum preset threshold value. In general, for any input voltage V_{in}, the steady-state DC voltage sustained by the reset capacitor is

$$V_C = \frac{V_{in}}{1-D} \tag{3}$$

where D is the duty cycle, which is necessarily in the range $0 \leq D \leq 1$. The duty cycle is related to the input and output voltages V_0 and V_{in}, and to the transformer turns ratios m and n by the equation:

$$D = \frac{V_0}{V_{in}} \cdot \frac{n}{m+1} \tag{4}$$

Thus, from Equation 3, when the input voltage V_{in} decreases to

$$V_{in} = V_o \cdot \frac{n}{m+1} \tag{5}$$

then D = 1, and the reset capacitor voltage V_c becomes arbitrarily large, as indicated by Equation 3; this condition of high reset capacitor voltage must be prevented to provide reliable operation of the converter. Additionally, if the input voltage becomes larger than the high voltage level input voltage, the reset capacitor voltage must become larger in value than a desired maximum value dictated by other design considerations.

To prevent the reset capacitor voltage from becoming too large, the reference voltage V_{max}, at input lead 401 in FIG. 4 is selected to be less than a maximum design voltage of the reset capacitor. When the reset capacitor voltage V_c is less than V_{max}, the output voltage from the lower operational amplifier is a high value, and reverse biases diode 418. The bias resistor 419 connects a source voltage to the cathodes of the diodes 408 and 418. The resulting bias voltage causes the anode voltage of diode 408 to be slightly higher (approximately 0.7 volt) than the output voltage of the upper operational amplifier 405 under these conditions, and will thus track the output voltage of the upper operational amplifier 405. Thus the feedback path from the output voltage V_o from the DC-DC converter output to the input to the PWM controller is the operational control path when the reset capacitor voltage is less than V_{max}. This is the normal operational mode of the converter.

If the reset capacitor voltage rises above V_{max} under abnormal input voltage conditions for the converter as described above, then the output voltage of the lower operational amplifier 415 decreases until diode 418 becomes forward biased, and diode 408 becomes back biased. Under these conditions the feedback path from the reset capacitor voltage to the input to the PWM controller becomes the operational feedback path, and the duty cycle D is controlled by the PWM controller to regulate the voltage on the reset capacitor, rather than the output voltage of the converter.

For operational compatibility, the two operative feedback loops are arranged with the same input-output polarity, i.e., an increase of the controlled voltage (i.e., either the output voltage of the converter, or the reset capacitor voltage) results in the same polarity of the change in the error voltage applied to the input of the PWM controller. From Equation 3, the reset capacitor voltage can be decreased by a decrease in the value of D. From Equation 4, the output voltage of the converter can also be decreased by a decrease in the value of D.

Another functional implementation of a feedback control for limiting the reset capacitor voltage, embodying the principles of the invention, is shown in the FIG. 5. The output voltage is applied to the input lead 501, differenced (i.e. summed) with the reference voltage on lead 502 and coupled via the gain and phase network 505 to the PWM control 520 in order to control the power switches to regulate the output. The reset capacitor voltage is applied to the lead 511 and differenced (i.e. summed) with a threshold voltage on lead 512. The differenced (i.e. summed) output is connected, via a gain and phase network to a comparator 516 which converts the output of network 515 to a digital state of either one or zero. If the reset capacitor voltage exceeds an allowable limit the output of the comparator 516 is one state which is applied to the PWM control 520 to limit its output to a low duty cycle until the reset capacitor voltage drops below the threshold value.

Claims:

1. A power converter circuit including:

a power transformer (110) providing galvanic isolation between an input (102) and an output (120); the power transformer requiring a periodic reset of a core flux with the voltage stored on a reset capacitor (106);

a power switch (105) connecting the input to the power transformer;

a voltage regulation feedback control (121) to control a duty cycle of the power switch to regulate a voltage at the output;

CHARACTERIZED BY;

a reset capacitor voltage control circuit (310, 311, 312, 321) operative to alter a response of the converter's voltage regulation feedback control to control the duty cycle of the power switch to limit a voltage of the reset capacitor whenever the reset capacitor sustains a voltage above a preset threshold.

2. A power converter circuit as claimed in claim 1, comprising:

the reset capacitor voltage control circuit including:

means to compare the reset capacitor voltage with a threshold voltage defining a maximum allowable reset capacitor voltage and means (320) responsive to the means to compare to operate the voltage regulation feedback control to control a duty cycle of the power switch to regulate the reset capacitor voltage.

3. A power converter circuit as claimed in claim 1, comprising:

a reset capacitor voltage control circuit including:

means to compare the reset capacitor voltage with a threshold voltage defining a maximum allowable reset capacitor voltage and means (320) responsive to the means to compare to operate the voltage regulation feedback control to limit a duty cycle of the power switch to a low value to limit the reset capacitor voltage.

FIG. 1

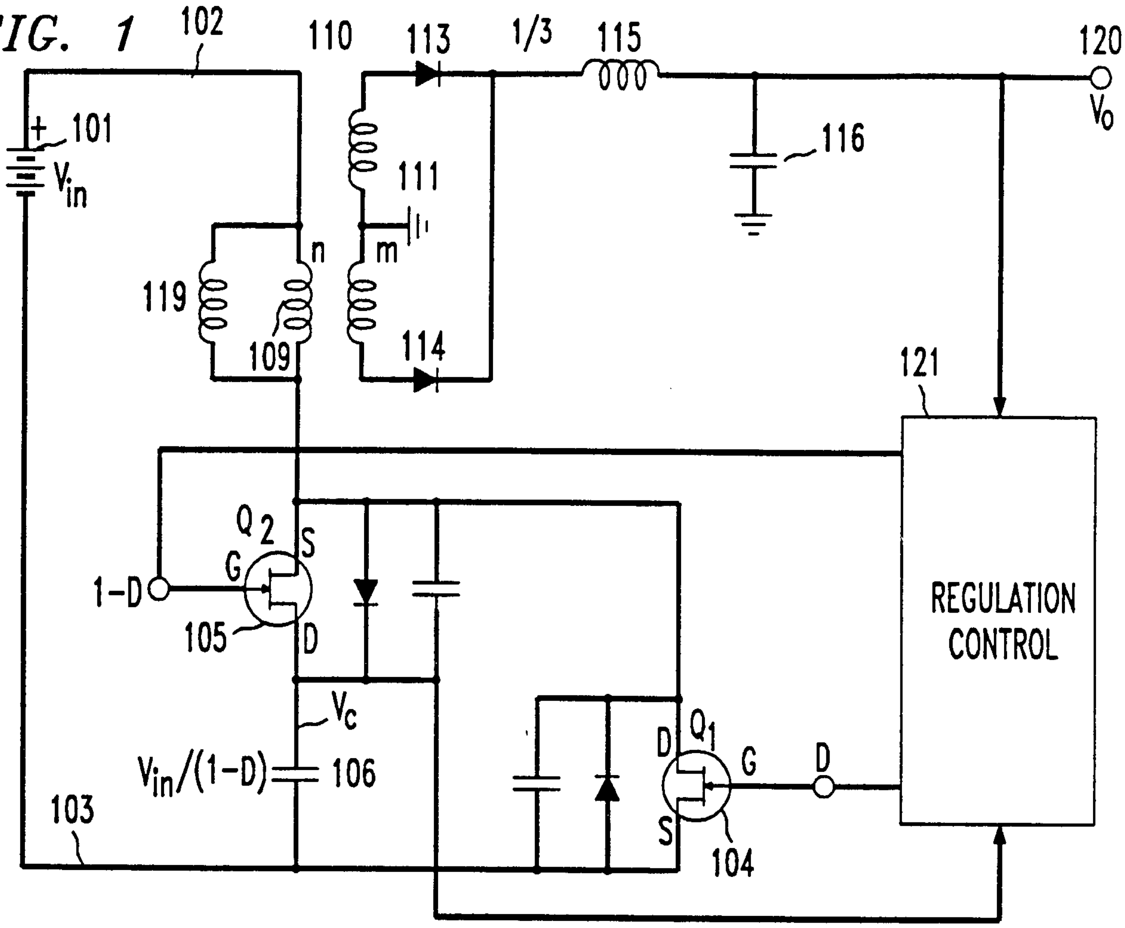

102
110
113
1/3
115
120
V_0
101
V_{in}
116
111
m
n
119
109
114
121
REGULATION CONTROL
Q_2
S
G
1-D
105
D
V_c
$V_{in}/(1-D)$
106
103
D
Q_1
G
D
S
104

FIG. 2

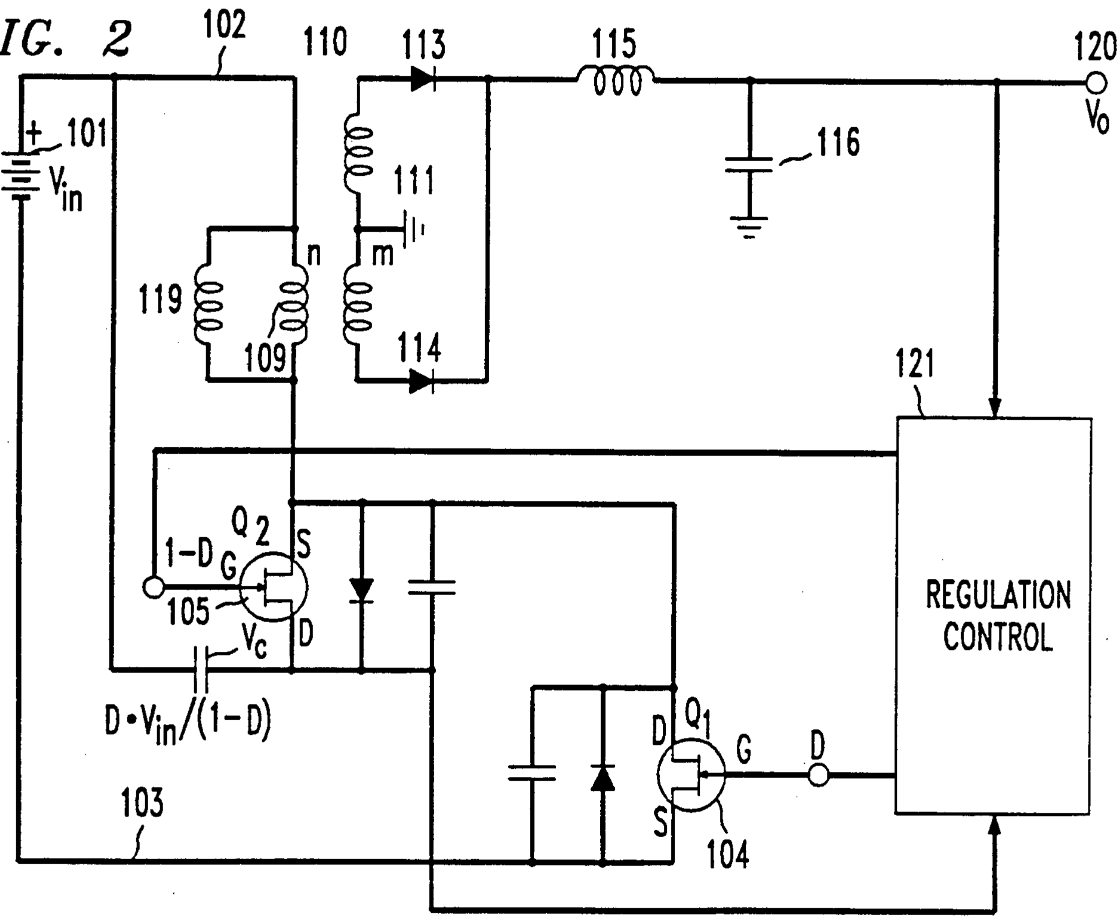
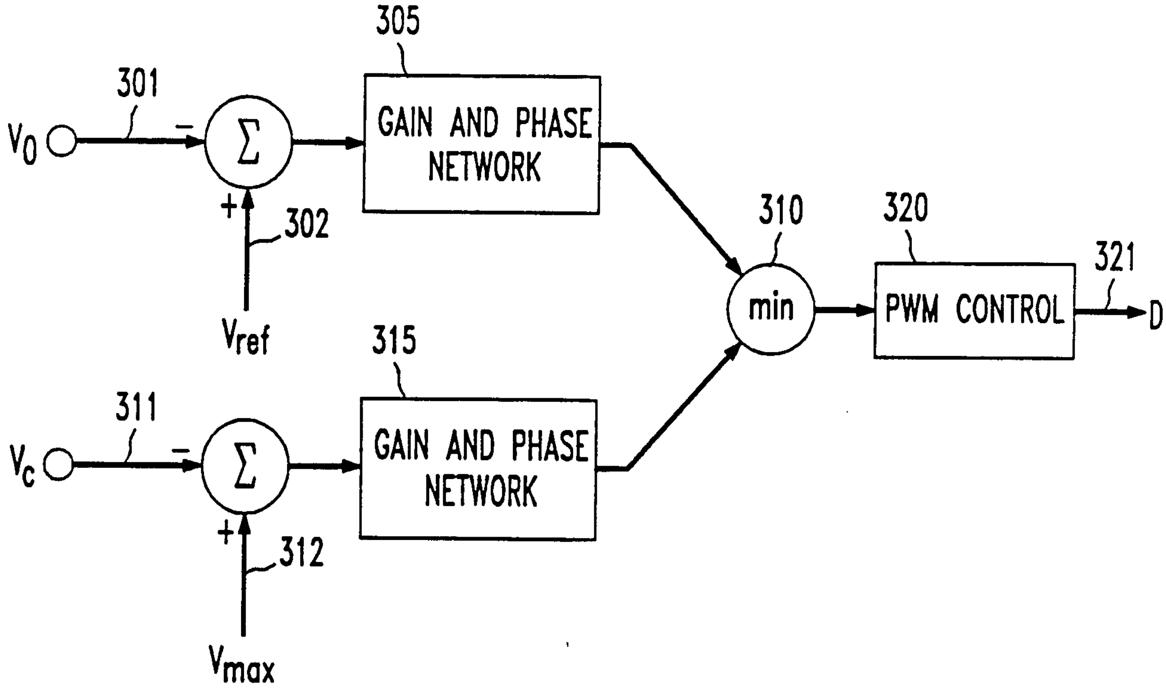
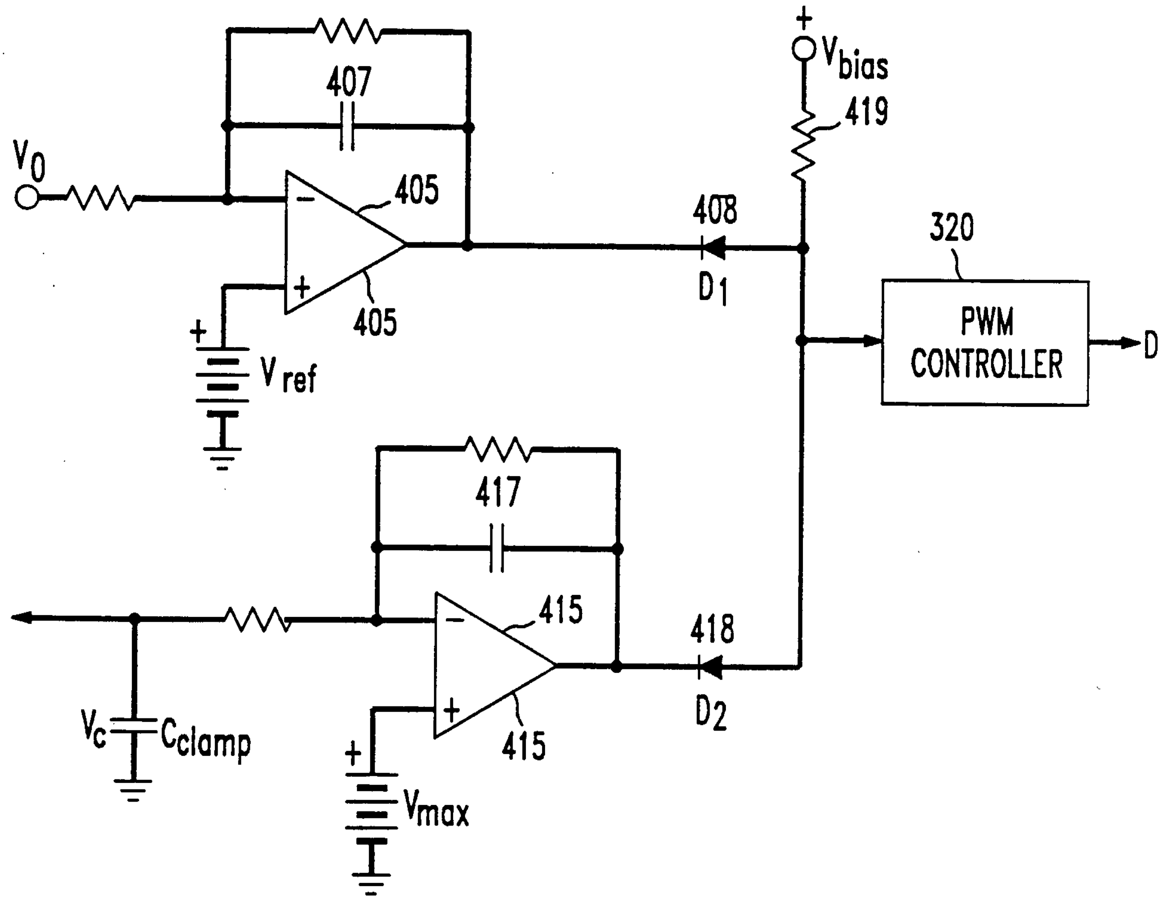

102
110
113
115
120
V_0
101
V_{in}
116
111
m
n
119
109
114
121
Q_2
1-D
G
S
105
V_c
D
$D \cdot V_{in}/(1-D)$
REGULATION CONTROL
D
Q_1
G
D
S
103
104

FIG. 3



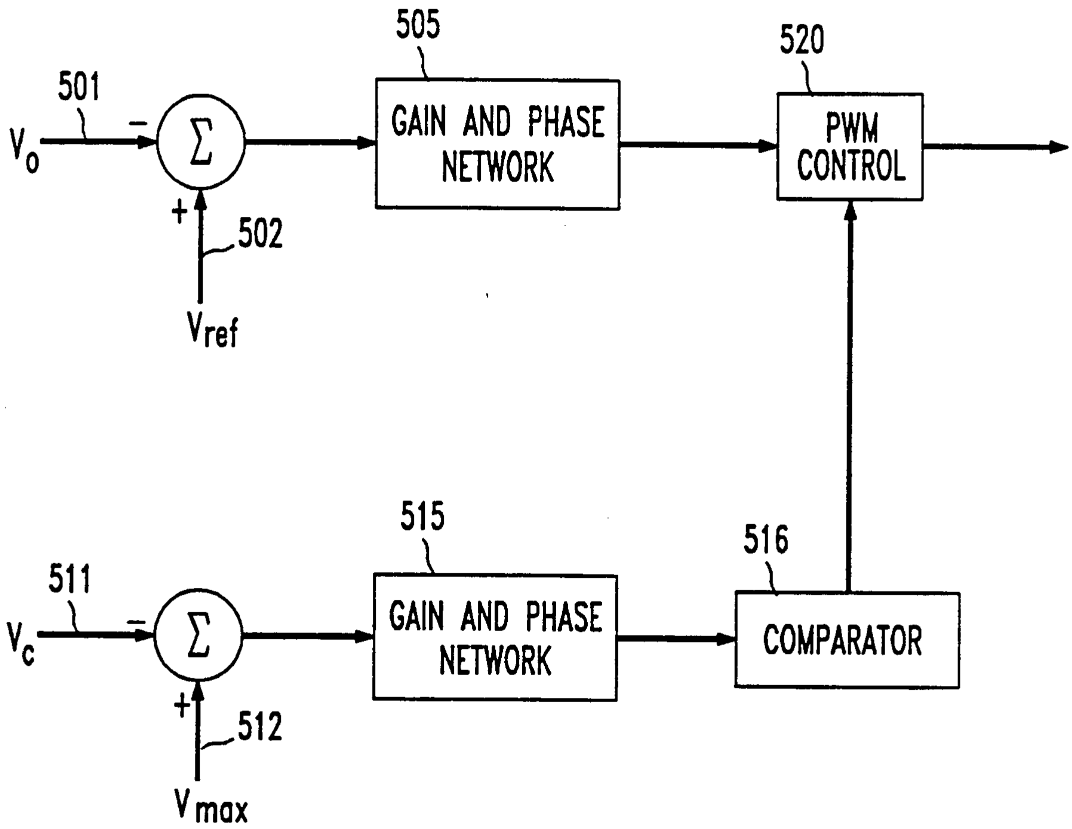
301
305
V_0
GAIN AND PHASE NETWORK
302
V_{ref}
310
320
321
min
PWM CONTROL
D
315
311
V_c
GAIN AND PHASE NETWORK
312
V_{max}

FIG. 4



407
V_{bias}
419
V_0
405
405
408
D_1
320
PWM CONTROLLER
D
V_{ref}
417
415
418
D_2
415
V_c
Cclamp
V_{max}

FIG. 5


505
520
501
V_o
−
Σ
+
502
V_{ref}
GAIN AND PHASE NETWORK
PWM CONTROL
515
516
511
V_c
−
Σ
+
512
V_{max}
GAIN AND PHASE NETWORK
COMPARATOR

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US93/12217

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) :H02M 3/335
US CL : 363/21,56
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 363/20,21,56,79,97

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS
search terms: core reset, reset and core and transformer, capacitor#, feedback

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US, A, 4,809,148 (Barn) 28 February 1989, figures 7 and 8.	1-3
Y	US, A, 4,760,512 (Loftus) 26 July 1988, abstract-first sentence, and figure 2.	1-3
Y	JP, A, 58-66578 (Kikuchi) 20 April 1983, figure 3-comparator 2.	1-3

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

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