

APPLICATION FOR A STANDARD PATENT

We KONE ELEVATOR GMBH a Swiss company whose registered office is situate at Rathausstrassel, CH-6340 Baar, Switzerland

XX

hereby apply for the grant of a Standard Patent for an invention entitled
~~Patent of Addition~~

PROCEDURE AND APPARATUS FOR TRANSMITTING BINARY MESSAGES
IN A SERIAL COMMUNICATION BUS

which is described in the accompanying ~~provisional~~ ^{complete} specification.

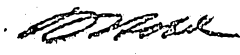
For a Convention application — details of basic application(s) —

NUMBER	COUNTRY	DATE OF APPLICATION
884500	FINLAND	30th September, 1988

Our ~~my~~ address for service is COLLISON & CO., Patent Attorneys, 117 King William Street, Adelaide, South Australia, 5000.

Dated this 22nd day of June, 1989

KONE ELEVATOR GMBH
By their Patent Attorneys,
COLLISON & CO.


(Signature)
G.E. HABEL
Attorney for the Applicant

A001618 22/06/89



To

THE COMMISSIONER OF PATENTS

38482

Commonwealth of Australia
The Patents Act 1952
DECLARATION IN SUPPORT

In support of the (Convention) Application made by: Kone Elevator GmbH
Rathausstrasse 1
CH-6340 Baar, Switzerland

for a patent for an invention entitled: PROCEDURE AND APPARATUS FOR TRANSMITTING
BINARY MESSAGES IN A SERIAL COMMUNICATION BUS

I(We) Heimo Mäkinen and Kimmo Laukas
of and care of the applicant company do solemnly and sincerely declare as follows:

a) ~~I am (We are) the applicant(s) for the patent~~
~~XXXXXXXXXXXXXXXXXXXXXXXXXXXX~~

or

b) ~~XXX~~ (We are) authorised by the applicant(s) for the patent to make this declaration on its behalf.

Delete the following if not a Convention Application.

The basic application(s) as defined by section 141 (142) of the Act was (~~were~~) made

in Finland on September 30, 1988

in on

in on

by Kone Oy of Munkkiniemen Puistotie 25, 00330 Helsinki, Finland

The basic application(s) referred to in this paragraph is (~~are~~) the first application(s) made in
a Convention country in respect of the invention the subject of the application.

a) ~~I am (We are) the actual inventor(s) of the invention.~~

or

b) Kimmo Selin, Niinipuuntie 2 B 19, 05460 Hyvinkää, Finland

is (~~are~~) the actual inventor(s) of the invention and the facts upon which Kone Elevator GmbH

is (~~are~~) entitled to make the application are as follows:

The Applicant is the assignee of Kone Oy who is the assignee of
the actual inventor.

Declared at Helsinki this 20th day of June 1989

Signed Status

Declarant's Name KONE Elevator GmbH

Heimo Mäkinen

director

Kimmo Laukas

director

This form is suitable for any type of Patent Application. No legalisation required.

(12) PATENT ABRIDGMENT (11) Document No. AU-B-36754/89
(19) AUSTRALIAN PATENT OFFICE (10) Acceptance No. 618103

(54) Title
PROCEDURE AND APPARATUS FOR TRANSMITTING BINARY MESSAGES IN A SERIAL
COMMUNICATION BUS

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884500	30.09.88	FI FINLAND

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(56) Prior Art Documents
AU 583316 49284/85 H04L 11/16 H04B3/04

(57) Claim.

1. Procedure for transmitting binary messages in a serial communication bus, several transmitting stations being connected to said bus, in which procedure each station is able to transmit a signal when the bus is free, and in which procedure, in a signal collision situation when several stations attempt to transmit messages simultaneously, each station monitors the message which is passing through the bus and only the station which has the highest priority is allowed to go ahead and transmit its message while each station having a lower priority transmitting a signal of a logic state assigned a recessive status, receives a signal of a logic state assigned a dominating status cancels its transmission attempt, characterized in that all stations transmit a dominating signal with the same polarity by recognizing the polarity of the signal present in the bus and by sending the dominating signal with that polarity and not when it is a recessive signal.

7. Apparatus applying the procedure of claim 1, designed for transmitting binary messages through a serial communication bus, several apparatus being connected to said bus for transmitting and receiving messages, each apparatus being able to transmit a message when the bus is free, said apparatus comprising a receiver (6,8) by means of which, in a signal collision situation when several apparatus attempt to transmit messages simultaneously, each apparatus monitors the message passing through the bus, and a transmitter (3,4) which is so controlled that in a collision situation only the apparatus which has the highest priority is able to transmit its

(11) AU-B-36754/89
(10) 618103

-2-

message while each apparatus of a lower priority transmitting a signal of a logic state assigned a recessive status, receives a signal of a logic state assigned a dominating status cancels its transmission attempt, characterized in that the apparatus incorporates a polarity testing unit (7) which recognizes the polarity of the signal present in the bus and causes the transmitter to transmit a dominating signal with that polarity but not to transmit a recessive signal.

Patents Act 1952-1969

COMPLETE SPECIFICATION

(ORIGINAL)

6 1 8 1 0 3

FOR OFFICE USE:

Class

Int. Class

Application Number :
Lodged :Complete Application No. :
Specification Lodged :
Published :

Priority:

Related art:

TO BE COMPLETED BY APPLICANT

Name of Applicant: KONE ELEVATOR GMBH

Address of Applicant: Rathausstrassel, CH-6340 Baar,
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Actual Inventor: KIMMO SELIN

Address for Service: Care of COLLISON & CO., 117 King William Street,
Adelaide, South Australia, 5000

Complete Specification for the invention entitled:

PROCEDURE AND APPARATUS FOR TRANSMITTING BINARY
MESSAGES IN A SERIAL COMMUNICATION BUSThe following statement is a full description of this invention, including the best method of performing it
known to ~~me~~ us:

PROCEDURE AND APPARATUS FOR TRANSMITTING BINARY MESSAGES IN A SERIAL COMMUNICATION BUS

5 The present invention relates to a procedure and an apparatus for transmitting binary messages in a serial communication bus, several transmitting stations being connected to said bus, in which procedure each station is able to transmit a message when the bus is free, and in which procedure, in a signal collision situation when several stations attempt to transmit messages simultaneously, each station monitors the message which is passing through the bus and only the station which has the highest priority is allowed to go ahead and transmit its message while each station having a lower priority which, when transmitting a signal of a logic state assigned a recessive status, receives a signal of a logic state assigned a dominating status cancels its transmission attempt.

15 The multimaster serial bus is based on the idea that each station is allowed to start a transmission any time when the bus is free. Therefore, collisions occur in the bus when two or more stations start transmission simultaneously. Using the bit arbitration method, a signal collision in a multimaster bus can be managed in such manner that the message of the highest priority is transmitted while the other stations wait until said high-priority message has been passed through. This is implemented by assigning one of the logic states a recessive status and the other a dominating status. The so-called AMI (Alternate Mark Inversion) code meets the requirement that a dominating bit have precedence over a recessive bit. In AMI coding, every second dominating bit is transmitted with a different polarity and a recessive bit is equivalent to a free bus. The first bit of each message is transmitted with a different polarity form that of the previous message. This means that it is necessary to know which way the bus connection leads are to be mounted to allow control of the collision.

The object of the present invention is to eliminate the aforesaid drawback.

- 5 The procedure of the invention for transmitting binary messages in a serial communication bus is characterized in that all stations transmit a dominating signal with the same polarity by recognizing the polarity of the signal passing through the bus and by sending the dominating signal with that polarity and not transmitting a recessive signal.

10

- The apparatus designed for applying the procedure of the invention for transmitting binary messages through a serial communication bus, several apparatus being connected to said bus for transmitting and receiving messages, each apparatus being able to transmit a message when the bus is free, each apparatus comprising a receiver which, in a signal collision situation when several apparatus attempt to transmit messages simultaneously, monitors the message passing through the bus, and a transmitter which is so controlled that in a collision situation only the apparatus which has the highest priority is able to go ahead and transmit its message while each apparatus of a lower priority transmitting a signal of a logic state assigned a recessive status, receives a signal of a logic state assigned a dominating status cancels its transmission attempt, is characterized in that the apparatus incorporates a polarity testing unit which recognizes the polarity of the signal present in the bus and causes the transmitter to transmit a dominating signal with the polarity of the signal present in the bus but not to transmit a recessive signal.

25

The characteristics of other preferred embodiments of the invention are as presented in the claims.

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The insensibility to signal polarity, which means that the signal leads may be cross-connected at different points of connection, is an important feature especially in the case of a serial bus implemented using a twisted pair. Connecting a station to the bus becomes easier because one need



not consider which lead is to be coupled to which connector. Besides, since individual leads need not be recognized, the invention makes it possible to use a larger variety of conductors. If the signals are transmitted through a pulse transformer, the power consumption of the transformer is reduced since the signal transmitted consists of a pulse pair considerably shorter in duration than the complete signal. Moreover, the invention allows the transmission speed to be varied without altering the configuration of the apparatus.

In the following, the invention is described by the aid of an example with reference to the drawings attached:

Fig. 1 is a block diagram of the modulator.

Fig. 2 is a block diagram representing the internal operation of the modulator.

Fig. 3 illustrates the transmission signals.

Fig. 4a illustrates the reception signals.

Fig. 5 illustrates the coding principle.

Fig. 6 shows the timing diagram for the transmission logic.

Fig. 7a shows the timing diagram for the reception logic.

Fig. 7b shows the reception logic timing diagram as applied in another case.

Fig. 8 illustrates the bus interface.

Fig. 9 presents a diagram of the logic circuitry.

The modulator, shown as a block diagram in Fig. 1, imple-

ments polarity-sensitive bit coding in a multimaster serial bus accessed via a pulse transformer on the basis of bit arbitration. Such a bus can be used as a serial communication bus e.g. in the device control system of an elevator.

5 The modulator constitutes the coding logic between the controller and the pulse transformer. The modulator consists of two sections: a logic section 1, which contains the coding logic, and a controller section 2, which contains a control stage and a receiver comparator. The modulator signals shown in Fig. 1 are discussed below.

10 In the description below, the zero bit has been selected as the dominating bit. In the event of signal collision, each station monitors the bus and, if the station receives a dominating bit when sending a recessive bit, it cancels its transmission attempt.

15 In this bus accessing procedure, all stations send a dominating signal with the same polarity into the bus. Moreover, the coding is so implemented that a dominating bit being transmitted has precedence over a recessive bit.

20 The data to be transmitted is so encoded that only the dominating bits will be transmitted. Each dominating bit is sent in the same way in such manner that the polarity determines the pulse shape. The polarity is monitored during each bit, so that the polarity can be changed very swiftly. 25 Once the first bit of a message has entered the bus, each station immediately changes to the correct polarity. The basic idea is to turn the transmitter to the correct polarity as soon as the receiver has recognized a signal. The bus is monitored continuously, which means that the change to the correct polarity is effected fully dynamically. 30

The apparatus illustrated in Fig. 2 comprises a transmission logic 3, an output controller 4, a pulse transformer

5, a receiver 6, a polarity testing unit 7 and a receiver logic 8. The inputs to the transmission logic 3 are the transmission data TXD, the baud clock signal TXC and the clock pulse CLK, supplied by the controller. The baud clock signal and the clock pulses are also input to the polarity testing unit 7. The transmission logic 3 provides the output signal OUT1 of channel 1 and the output signal OUT2 of channel 2, both of which are fed into the output controller 4, which transmits the message through the pulse transformer 5. The bus interface consists of the output controller 4, the pulse transformer 5 and the receiver 6. The receiver 6 monitors the line via the pulse transformer, and the message received, consisting of signals IN1 and IN2, proceeds from the receiver to the polarity testing unit 7 and to the receiver logic 8, which outputs the signal RXD. The polarity testing unit provides a polarity signal POL, which is input to the transmission logic 3, and a HOLD signal, which is input to the receiver logic 8. Fig. 3 shows the corresponding signals as transmission signals and Figs 4a and 4b as reception signals. Fig. 5 illustrates the coding principle, showing also the reception signal RXD which is input to the controller.

Fig. 6 shows the transmitter logic timing diagram. There are two internal timing signals TT1 and TT2, of which the first one, TT1, is low during the first output pulse OUT1 when POL is 1, and the second one, TT2, is low during the first and the second output pulses OUT1 and OUT2 when POL is 1. The polarity signal POL determines which channel is transmitted first.

The main features of the transmission logic are presented in Fig. 9. The TXD signal is passed via two OR gates 15 and 16 to AND gates 17 and 18, from which the output signals OUT1 and OUT2 of the two channels are obtained. The other input of the first OR gate 15 receives the TXC signal, while the other input of the second OR gate 16 receives the

second internal timing signal TT2. The AND gates 17 and 18 also receive timing signals, which are obtained by first inverting the TXC signal in a NOT circuit 19 to produce the XTXC signal, which is then applied to the R-inputs of two D-flip-flops 20 and 21. These flip-flops are also fed by the clock signal CLK and by signals obtained from the T8, T16 and T32 signals by passing these through AND gates 22 and 23 and then, together with the flip-flop feedback signals, through OR gates 24 and 25 and then into the flip-flops. These provide the internal timing signals TT1 and TT2. In each channel, the first timing pulse signal TT1 is fed into unconditional OR gates 26 and 27, which are also fed by the polarity signal POL obtained from the receiver, the POL signal for channel 2 being inverted by circuit 28. From these OR gates 27 and 28, the timing signals are passed into the aforesaid AND gates 17 and 18. Signals T8, T16 and T32 are provided by a counter 50 that counts 8, 16 and 32 clock pulses CLK.

In accordance with the above description, the transmission signal is so encoded that logic ones are not transmitted at all while logic zeros are transmitted as signal pair OUT1, OUT2. If the polarity POL signal is one, the first signal OUT1 is transmitted first, and vice versa. The TXC signal is transmitted at the beginning of each bit. It resets the counter 50, which then starts counting up again from zero. If the TXD signal is zero, the TT1 and TT2 signals are used to generate the output signals OUT1 and OUT2, which together are considerably shorter in duration than the complete signal.

The operation of the logic is exemplified by the following truth table, in which the first line represents the starting situation and «X» stands for a state in which the logic state of the signal is irrelevant. TXD, TXC, POL, TT1 and TT2 are the input signals, OUT1 and OUT2 being the output signals.

	TXD	TXC	POL	TT1	TT2	OUT1	OUT2	TIME
	X	1	X	0	0	0	0	
	1	0	X	0	0	0	0	0-T1
	1	0	X	1	0	0	0	T1-T2
5	1	0	X	1	1	0	0	T2-
	0	0	1	0	0	1	0	0-T1
	0	0	1	1	0	0	1	R1-T2
	0	0	1	1	1	0	0	T2-
	0	0	0	0	0	0	1	0-T1
	0	0	0	1	0	1	0	T1-T2
	0	0	0	1	1	0	0	T2-

Figs 7a and 7b show the timing diagrams for the receiver logic in two different cases. The first reception signal IN1 is obtained from channel 1 of the comparator, which is described below, and the second reception signal IN2 from channel 2. Signal RXD is the receiver signal for the controller, HOLD1 is the receiver hold signal for channel 1, HOLD2 the receiver hold signal for channel 2, POL1 is the polarity signal for channel 1 and POL2 for channel 2.

Fig. 9 shows the main features of the receiver logic and the polarity testing logic. The logic circuitry comprises four D-flip-flops 29-32, each of which receives the XTXC signal in port R. The outputs of the first and the second receiver flip-flops 29 and 30 provide the polarity change signals POL1 and POL2 for the two channels. These signals are passed via OR gates 33 and 34 to flip-flops 35 and 36, from whose outputs feedback signals are returned into said OR gates 33 and 34. The inverted output of the flip-flop 35 of the first channel and the output of the flip-flop 36 of the second channel are applied to the inputs of AND gate 37, whose output is the polarity signal POL.

In each channel, the first and the second flip-flops receive signals generated from the timing signals R1.16 and R2.16 as follows. The timing signals are inverted by circuits 38 and 39, from where they are passed through AND gates 40 and 41 and then through OR gates 42 and 43 to the flip-flop 31 and 32, whose R-inputs are fed by the TXTC signal. The other inputs of AND gates 40 and 41 are fed by the inverted outputs of flip-flops 31 and 32, and the other inputs of OR gates 42 and 43 are fed by the non-inverted outputs of the same flip-flops, i.e. by the hold signals HOLD1 and HOLD2. The inverted output of flip-flop 31 of the first channel and the inverted timing signal of the second channel are input to OR gate 44, whose output and the inverted output of the first flip-flop 29 are applied to the inputs of AND gate 46, whose output and the hold signal HOLD2 of the second channel are fed into OR gate 48. The output of this gate is input to flip-flop 29. The corresponding input signal for the second flip-flop 30 is obtained in a similar manner through OR gates 45 and 49 and AND gate 47. The timing signals R1.16 and R2.16 are produced by counters 51 and 53 by counting 16 clock pulses CLK when the IN1 signal is low. The first counter 51 obtains its RST signal from OR gate 52, whose inputs are fed by the input signal IN1 and the baud clock signal TXC. Similarly, the second counter 53 obtains its RST signal from OR gate 54, whose inputs are the second input signal IN2 and the baud clock signal.

As shown by Fig. 9, the reception signal RXD is produced by an OR circuit 56 whose inputs are fed by the hold signals HOLD1 and HOLD2 and a signal obtained from an AND gate 55 fed by the input signals IN1 and IN2.

The receiver logic is activated when one of the input signals IN1 and IN2 goes low. If the first reception signal IN1 goes low first, the reception counter 51 of channel 1 starts counting. For a certain time, which is shorter than

the pulse duration T1 shown in Fig. 6, the incoming bit is defined as a logic zero, which causes the HOLD1 signal to go high. This signal remains in the high state throughout the duration of the bit until the next TXC pulse occurs. For the polarity testing operation, also the second input signal IN2 is required. In order for the polarity signal POL to change to the 1-state, after the first input signal IN1 has been low for the time indicated above, the second input signal IN2 also has to remain low for an equal time during the same bit. This causes the polarity signal POL1 to go high, resulting in the polarity signal POL changing to the 1-state. If the second input signal IN2 goes low first, the same sequence is required for the POL signal to change to zero, but the signals involved are the hold and polarity signals of channel 2, i.e. HOLD2 and POL2.

Fig. 8 is a diagram of the modulator controller circuit, comprising a transmitter and a receiver. In each channel, the transmitter is implemented using a MOS-FET Q1,Q2. Connected in series with the drain of each transistor is a diode D1,D2 to ensure that the transistor will not constitute a load on the line when power is off. The pulse transformer 5 is connected to the terminals of these diodes via resistors R1 and R2. In series with each winding L1 and L2 on the modulator side of the transformer is a series circuit of a Zener diode D3,D4 and a diode D5,D6, which serve to reduce the interference generated by the transformer. The midpoint between these series circuits is connected to the positive voltage V+ and via capacitor C to ground, and via resistor R3 to the transformer midpoint between windings L1 and L2. The resistors protect the transformer against short circuits in the transistors. The bus signal VBUS is obtained from the transformer winding L3 connected to the line.

The receiver is implemented using comparators 9, 10, 13 and 14. The positive terminal of the first comparator 9 is con-

5 nected to the midpoint of two resistors R4 and R5, one of which connects to the diode D1 protecting transistor Q1 and the other to ground, and the second comparator 10 is similarly connected to the second channel via resistors R6 and R7. The negative terminal of each of these two comparators is connected to a reference voltage, which is obtained from the V+ voltage from the midpoint of a series circuit consisting of resistors R8 and R9. From the comparator, the signal proceeds in each channel through an RC filter 11 or 12 to the positive terminal of another comparator 13 or 14, which compares the signal to a reference voltage obtained as above by means of resistors R10 and R11. These comparators 13 and 14 produce the input signals IN1 and IN2 for the two channels.

15 Let us consider the circuit action in channel 1 when a signal is being received from the line. When the transformer produces a negative signal - polarity being indicated by the dots at the windings - the signal proceeds through resistors R1 and R4 to the first comparator 9, where it is compared to the reference voltage. The comparator output now goes low. The signal then proceeds through the filter into the second comparator 13, which again compares it to the reference voltage. This comparator outputs a negative pulse IN1 as shown e.g. in Fig. 7a. The other channel functions in a corresponding manner. By means of the comparators and filters, in addition to the counters described above, the receiver checks the amplitude and duration of the incoming pulses.

25 30 It is obvious to a person skilled in the art that different embodiments of the invention are not restricted to the examples discussed above, but that they may instead be varied within the scope of the following claims.

THE CLAIMS DEFINING THE INVENTION ARE AS FOLLOWS:

5

1. Procedure for transmitting binary messages in a serial communication bus, several transmitting stations being connected to said bus, in which procedure each station is able to transmit a signal when the bus is free, and in which procedure, in a signal collision situation when several stations attempt
10 to transmit messages simultaneously, each station monitors the message which is passing through the bus and only the station which has the highest priority is allowed to go ahead and transmit its message while each station having a lower priority transmitting a signal of a logic state assigned a recessive status, receives a signal of a logic state assigned a dominating
15 status cancels its transmission attempt, characterized in that all stations transmit a dominating signal with the same polarity by recognizing the polarity of the signal present in the bus and by sending the dominating signal with that polarity and not when it is a recessive signal.

2. Procedure according to claim 1, characterized in that the message to be transmitted is so encoded that the recessive signals are not transmitted and only the dominating signals are transmitted, and that each dominating signal is transmitted in the same way, the shape of the pulse to be transmitted being
25 determined by its polarity.

3. Procedure according to claim 1 or 2, characterized in that the signal polarity is monitored during every signal and that this monitoring function is continuously active as long as the station remains connected to the bus.

30 4. Procedure according to any one of the previous claims, characterized in that the signal to be transmitted through the bus is formed from two pulses



5 (OUT1,OUT2), and that the signal to be transmitted is fed into the bus through
a pulse transformer (5) in such manner that the signal produces an equal
transformer voltage in both positive and negative directions.

5. Procedure according to any one of the previous claims, characterized in
that the sum of the durations of said two pulses (OUT1,OUT2) is essentially
10 less than the duration of the signal.

6. Procedure according to any one of the previous claims, characterized in
that the amplitude and duration of the received pulse (IN1,IN2) are checked to
ensure that they are within preset limits before the pulse is accepted.

15 7. Apparatus applying the procedure of claim 1, designed for transmitting
binary messages through a serial communication bus, several apparatus
being connected to said bus for transmitting and receiving messages, each
apparatus being able to transmit a message when the bus is free, said
20 apparatus comprising a receiver (6,8) by means of which, in a signal collision
situation when several apparatus attempt to transmit messages
simultaneously, each apparatus monitors the message passing through the
bus, and a transmitter (3,4) which is so controlled that in a collision situation
only the apparatus which has the highest priority is able to transmit its
25 message while each apparatus of a lower priority transmitting a signal of a
logic state assigned a recessive status, receives a signal of a logic state
assigned a dominating status cancels its transmission attempt, characterized
in that the apparatus incorporates a polarity testing unit (7) which recognizes
the polarity of the signal present in the bus and causes the transmitter to
30 transmit a dominating signal with that polarity but not to transmit a recessive
signal.



8. Apparatus according to claim 7, characterized in that it incorporates a pulse transformer (5) through which the message is transmitted into the bus, and that the transmitter (3,4) generates the signal to be sent into the bus from two pulses (OUT1,OUT2) in such manner that the signal produces an equal transformer voltage in both positive and negative directions.

9. Apparatus according to claim 7 or 8, characterized in that the transmitter is so controlled that the sum of the durations of said two pulses (OUT1,OUT2) is essentially less than the duration of the signal.

10. Apparatus according to any one of the claims 7 - 9, characterized in that it incorporates comparators (9,10,13,14), filters (11,12) and counters (51,53) by means of which the amplitude and duration of the received pulse (IN1,IN2) are checked to ensure that they are within preset limits before the pulse is accepted.

11. Apparatus according to any one of the claims 7 - 10, characterized in that it constitutes part of a serial communication bus in the device control system of an elevator.

12. Procedure for transmitting binary messages in serial communication bus substantially as described herein with references to and as illustrated in the accompanying drawings.

Dated this 22nd day of June 1989

KONE ELEVATOR GMBH
By their Patent Attorneys,
COLLISON & CO.



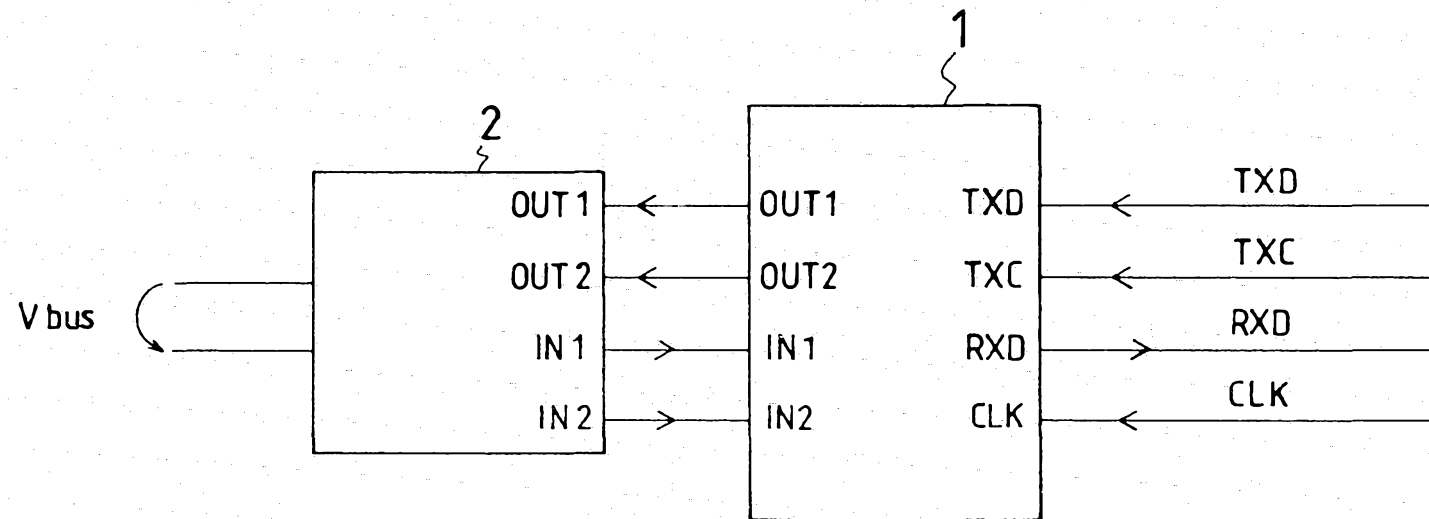


Fig.1

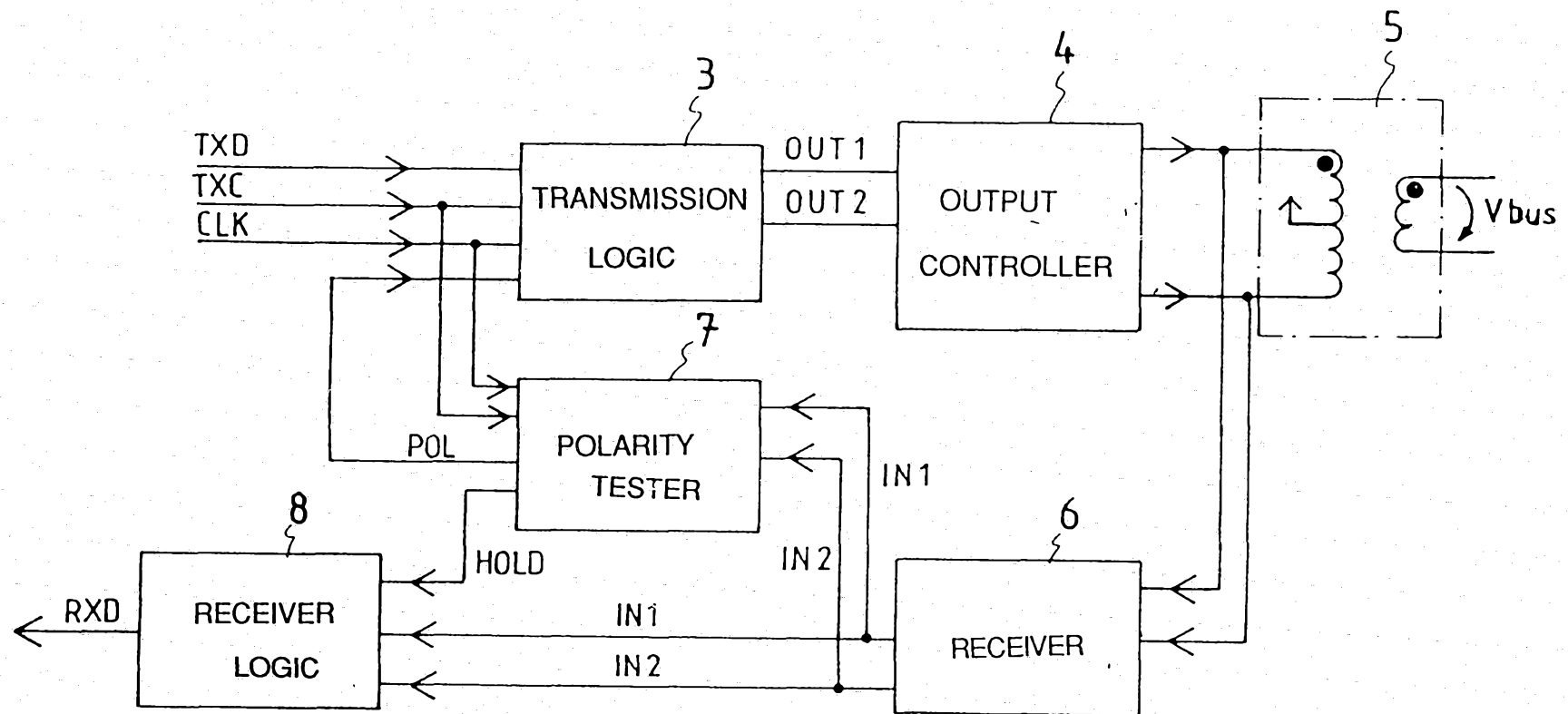


Fig. 2

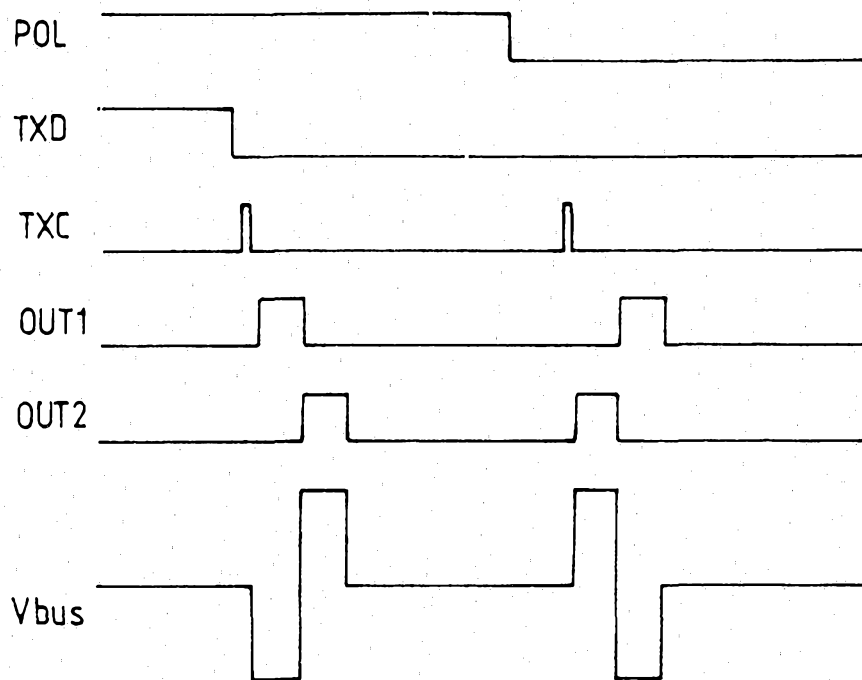


Fig.3

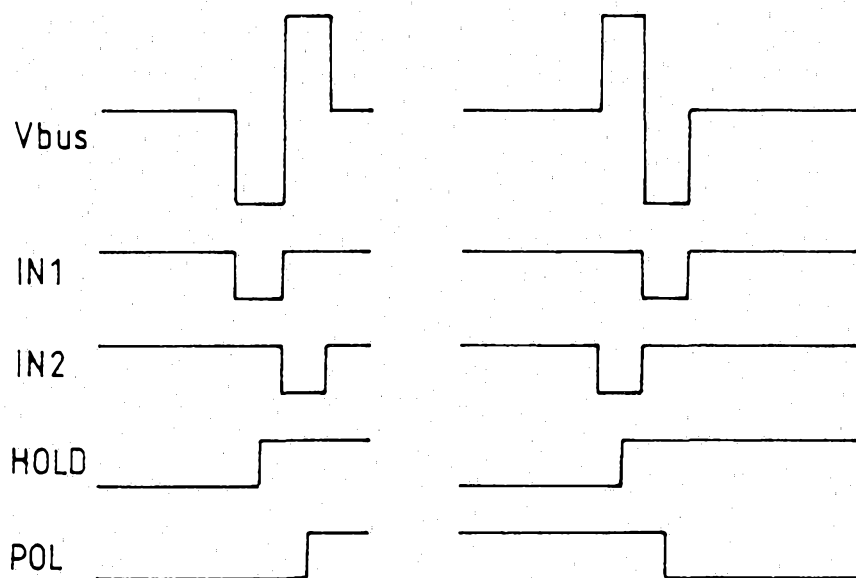


Fig.4a

Fig.4b

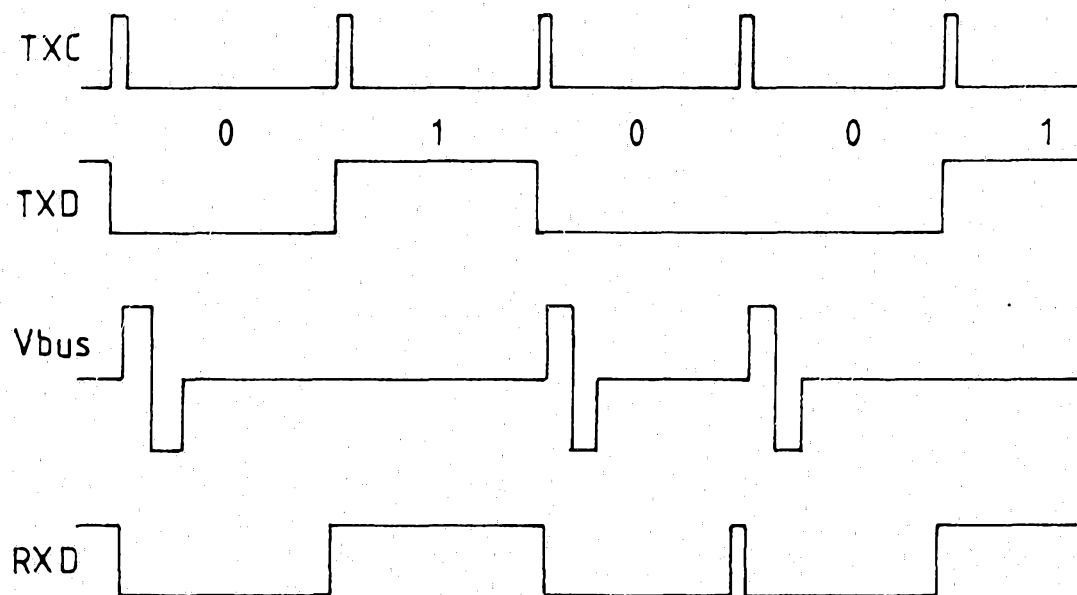


Fig5

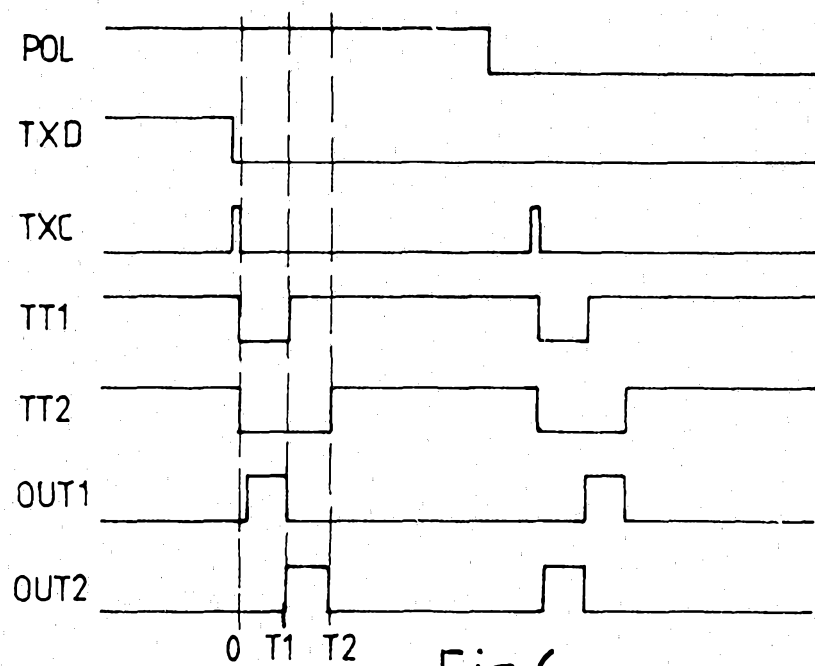


Fig. 6

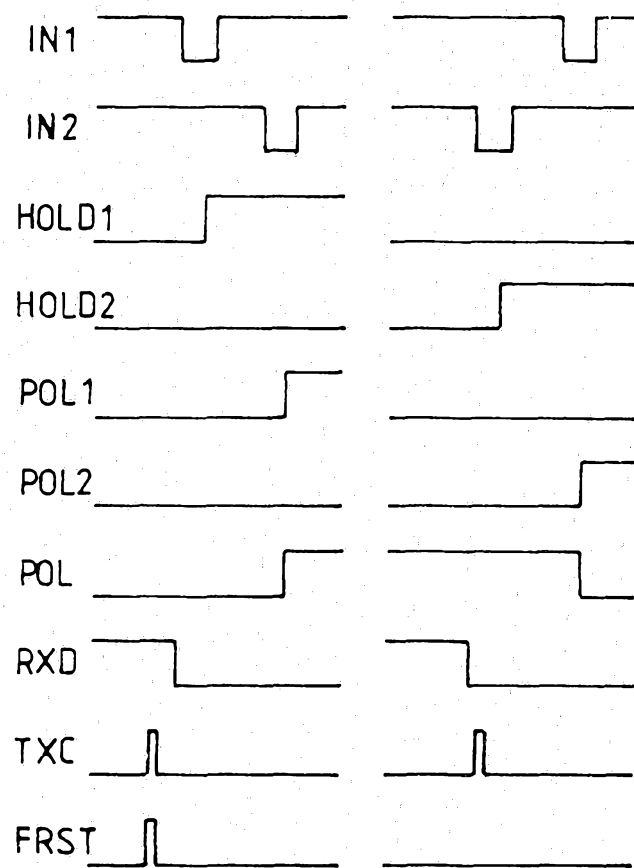


Fig. 7a

Fig. 7b

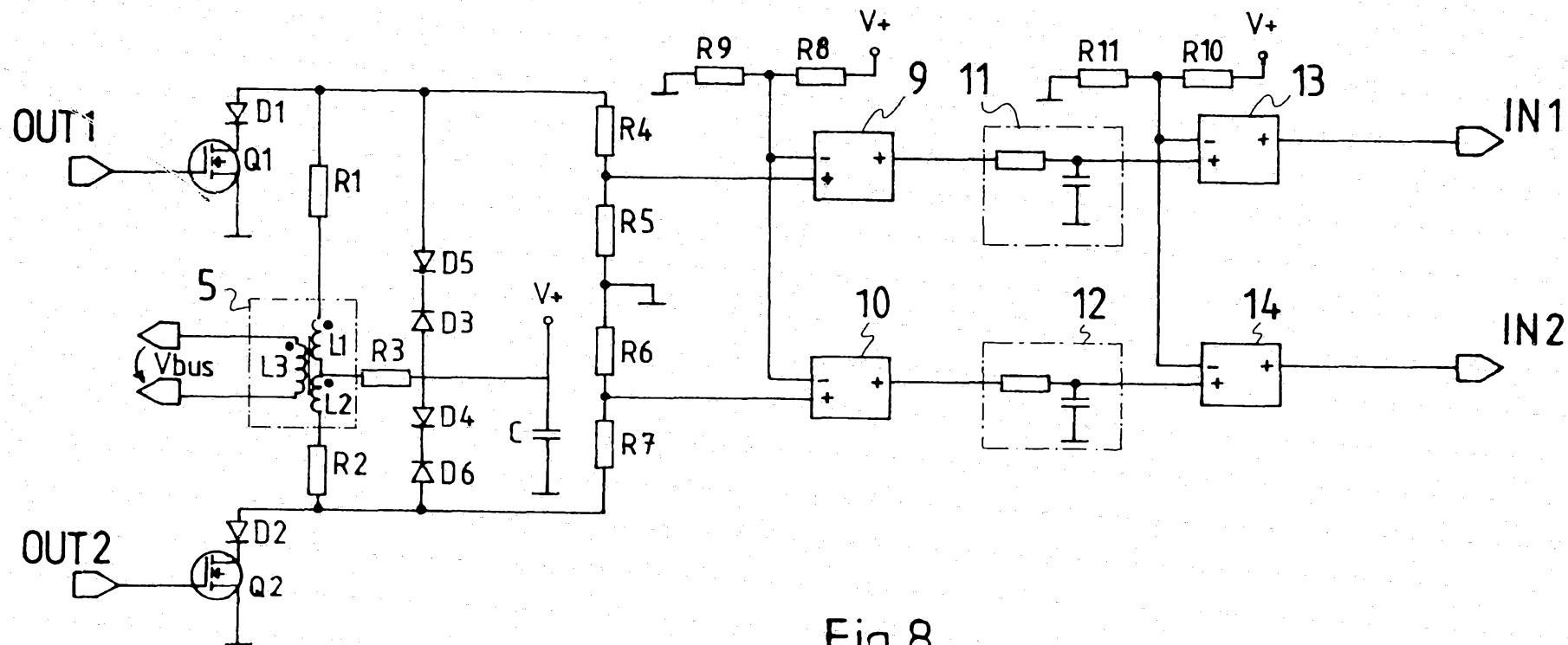


Fig. 8

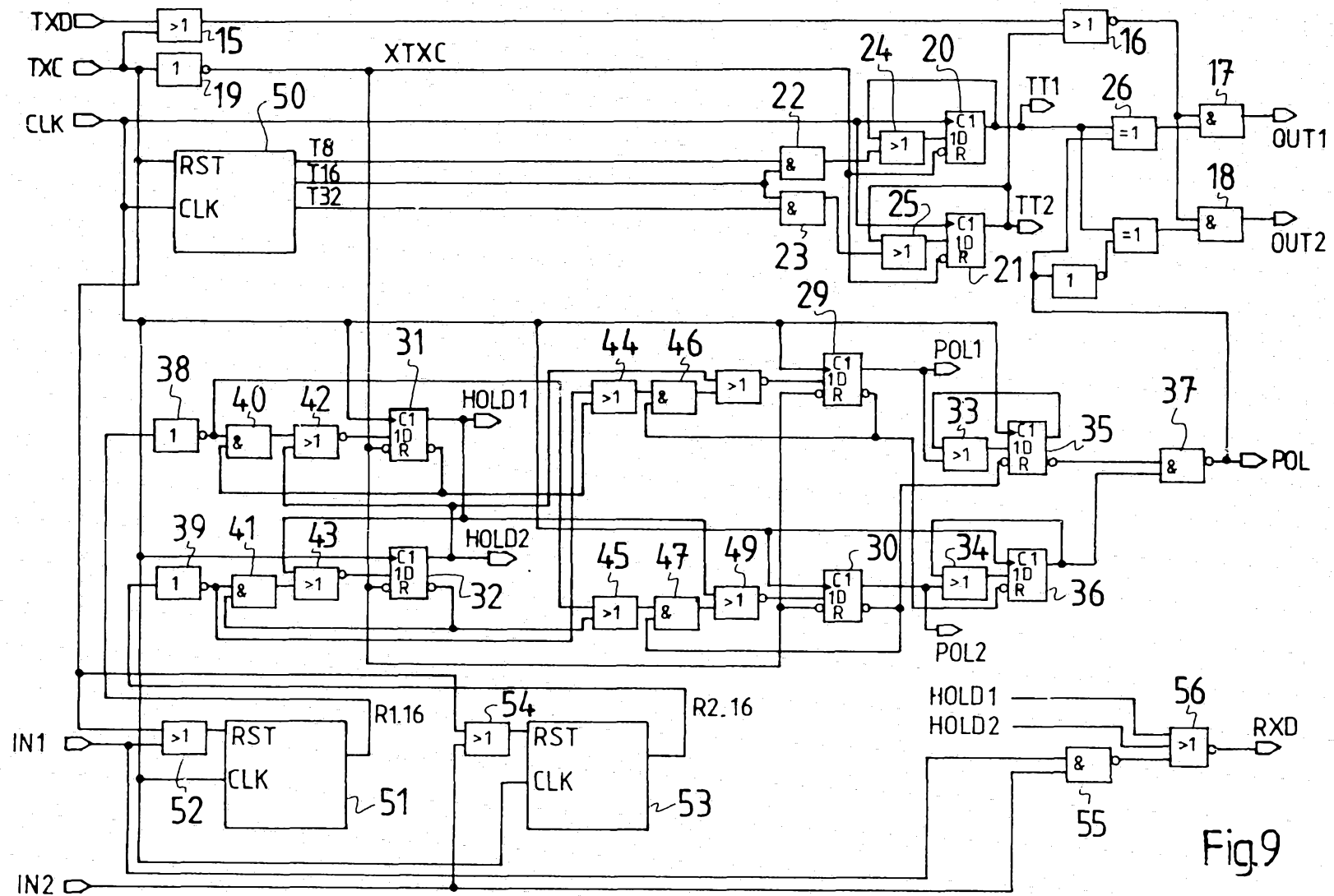


Fig.9