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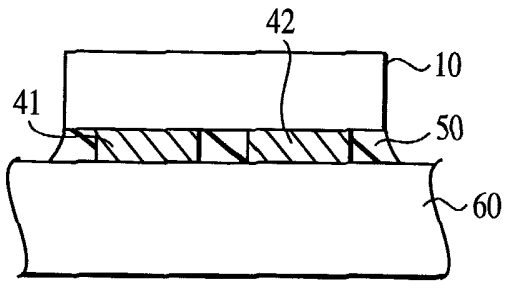
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(54) Title: WAFER LEVEL UNDERFILL AND INTERCONNECT PROCESS



(57) Abstract: A chip scale package and a method for its manufacture which include providing sticky interconnects (41, 42) on a surface of a semiconductor die (60), the interconnects being surrounded by a layer of thermal epoxy (EO).

WO 03/019628 A1

WAFER LEVEL UNDERFILL AND INTERCONNECT PROCESS

RELATED APPLICATION

[0001] This application is based on and claims priority to U.S. Provisional Application No. 60/314,818 entitled Wafer Level Underfill and Interconnect Process, which was filed on August 24, 2002, the subject matter and disclosure of which is incorporated by reference.

FIELD OF THE INVENTION

[0002] This application relates to a semiconductor device and more particularly to a chip-scale semiconductor device and a method for manufacturing thereof.

BACKGROUND OF THE INVENTION

[0003] Semiconductor devices such as power switches are a common part of electronic devices. Such devices are often packaged so that they may be practically incorporated into an electronic circuit. Due to the desire for smaller electronic devices there is a demand for electronic packages of smaller size. Chip scale packages thus have been developed which are the size of or nearly the size of a semiconductor device.

[0004] Also known are semiconductor device packages in which all electrodes are located on a common die surface and are connectable to corresponding conductive pads or traces on a support surface such as a printed circuit board.

[0005] The proper placement and attachment of a semiconductor package to a circuit board is an important step in manufacturing of electronic circuits. At the present time, such devices are first soldered down to the board and in a separate step a liquid epoxy is applied around the periphery of the device

which is pulled into the space between the device bottom and the top of the board by capillary action to form an underfill to improve device temperature cycling capability. Often, such a process requires the device to be first soldered in an automated step before the underfill material is applied. Thus, if during the soldering process the device is placed less than perfectly there is a chance that the underfill material will not be deposited accurately and may unintentionally spill over to the other areas of the board. This of course is undesirable and may require the circuit board to be designed in such a way to accommodate spillage due to misplacement of the semiconductor package. For example, the area on the circuit board intended for the semiconductor package may be enlarged to accommodate the spillage of the underfill material. This solution of course requires the enlargement of the circuit board which is contrary to the desire for a smaller electronic device.

[0006] It would be desirable to provide a semiconductor package which can be accurately placed on a circuit board and attached thereto without the drawbacks of the conventionally known devices discussed above.

BRIEF DESCRIPTION OF THE INVENTION

[0007] A semiconductor device according to the present invention is prepared to include the materials needed for board attach and underfill so that the user need only provide a thermal excursion to complete the attach process thus avoiding the problems encountered by prior art packages and attach methods.

[0008] In accordance with the invention a novel attach system, which can be made at wafer level, employs a silver loaded epoxy for the interconnects and a thermal epoxy which is disposed between the silver loaded interconnects for an underfill.

[0009] The preferred embodiment of the invention is a flip chip type semiconductor device which is processed at wafer level before singulation.

[0010] Specifically, a wafer having a plurality of identical die is first coated with a suitable photo-sensitive epoxy passivation layer. This layer is then processed to open windows over contacts of each one of the die. Then

interconnects will be disposed on and connected to each contact of each die through a respective window.

[0011] According to an aspect of the present invention the interconnects are composed of a silver loaded epoxy having certain advantageous characteristics. Specifically, the silver loaded epoxy has a resin as a matrix material that is semi-solid and will be sticky to the touch at room temperature. The silver loaded epoxy may also include fillers which give the interconnects structural integrity both at room temperature and at higher temperatures.

[0012] To allow the silver loaded epoxy to be deposited on the contents of respective die it can be reduced using solvents. These solvents, when evaporated, leave the interconnects with a sticky exterior surface.

[0013] Next, a thermal epoxy is laid down across the surface of the wafer. The thermal epoxy, which will constitute the underfill layer, is solid at room temperature (staying solid to a slightly higher temperature than that used for the interconnects) and is reduced with a solvent. The thermal epoxy layer may be formed through a process of repeated deposition and evaporation to a thickness of slightly less than the height of the interconnects.

[0014] Once the thermal epoxy layer is formed the die are singulated by, for example, sawing thus forming a plurality of chip-scale semiconductor devices.

[0015] To achieve the intended purposes of the present invention, according to one aspect of the present invention, during a solder reflowing process such as that commonly used for SMT (surface mount) assembly, a semiconductor device according to the present invention is first subjected to a reflow process and then the thermal epoxy is cured to form the underfill structure. Specifically, when the device is first placed on the board the sticky interconnects of the device serve to keep the device in a proper place on the circuit board. As the temperature is elevated the interconnect resin starts to become mobile, but the fillers will prevent these interconnects from slumping at this stage. As the temperature increases still further, the thermal epoxy becomes mobile, and, having no structuring fillers, will become less viscous. Thus, the

thermal epoxy flows readily and by capillary action is pulled toward the center of the semiconductor device.

[0016] In a preferred embodiment of the invention, once the temperature exceeds about 110°C the epoxy starts to cure. If necessary, however, this cure temperature can be increased. The epoxy resin and the hardener system of the thermal epoxy used in a semiconductor device according to the present invention are selected to be capable of fully curing within the solder reflow cycle.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] Figure 1 shows a top plan view of a semiconductor wafer having a plurality of identical semiconductor die formed on a top surface thereof.

[0018] Figure 2 shows a top plan view of a representative portion of the wafer shown by Figure 1.

[0019] Figure 3 shows the representative portion of the wafer as shown by Figure 2 having a passivation layer with windows over the electrical contacts of the die in the wafer.

[0020] Figure 4 shows part of the portion shown in Figure 3 as viewed looking in the direction of and between arrows 4-4.

[0021] Figure 5 shows the representative portion of the wafer as shown by Figure 3 having silver loaded epoxy interconnects formed in its windows.

[0022] Figure 6 shows part of the portion shown in Figure 5 as viewed looking in the direction of and between arrows 5-5.

[0023] Figure 7 shows the representative portion of the wafer as shown by Figure 5 having a thermal epoxy layer deposited around the interconnects of each die.

[0024] Figure 8 shows part of the portion shown in Figure 7 as viewed looking in the direction of and between arrows 8-8.

[0025] Figure 9 is a side view of a semiconductor device according to the present invention disposed over a circuit board prior to heating.

[0026] Figure 10 shows a side view of a semiconductor device according to the present invention as connected to a circuit board after the appropriate heating step.

DETAILED DESCRIPTION OF THE DRAWINGS

[0027] Figure 1 shows a wafer 100 of monolithic silicon which includes a plurality of identical die 10 formed therein. The die 10 formed in wafer 100 may be power switching devices such as MOSFETs or IGBTs or power diodes.

[0028] Figure 2 shows a representative portion 105 of wafer 100 which includes a plurality of adjacently disposed die 10. Each die 10 is isolated from its neighboring die 10 by intersecting streets 110. According to the preferred embodiment, die 10 is a MOSFET that includes all its major electrical contacts 11, 12, 13, 14 on only one of its major surfaces. Specifically, each die 10 includes on only one major surface thereof source contacts 11, 12, drain contact 13 and gate contact 14. Other varieties of die may also be processed into a semiconductor device according to the present invention.

[0029] Referring next to Figures 3 and 4, a passivation layer 30 is deposited over the entire surface of wafer 100, a representative portion 105 of which is shown by Figure 3. Passivation layer 30 is composed of photosensitive epoxy.

[0030] Next, using a photolithographic method, which may include an imaging step followed by a curing step, passivation layer 30 is processed to provide windows 31, 32, 33, 34 over source contacts 11, 12, drain contact 13 and gate contact 14 respectively of each die. Each window 31, 32, 33, 34 extends from the top of passivation layer 30 to the top surface of a respective contact thereby exposing it.

[0031] Referring next to Figures 5 and 6, silver loaded epoxy is deposited inside windows 31, 32, 33, 34 of each die to form interconnects 40, 41, 42, 43 therein which are electrically connected respectively to electrical contacts 11, 12, 13, 14 of each die 10. The silver loaded epoxy can be deposited in any desired way, such as by screening or by dispensing. The silver loaded epoxy

according to the preferred embodiment includes 60% to 85% silver by weight of silver particles of 3 to 40 microns in size. Also, in the preferred embodiment, the silver epoxy used in the interconnects 40, 41, 42, 43 will contain a suitable solvent such as Dowanol PMA (propylene glycol) or a similar chemical. The selection of the solvent will depend on its speed and volatility. That is, there will be a balance between being slow enough to process the material and yet fast enough to result in a shorter drying time. Also, it should be noted that the solvent content will determine the shrinkage experienced by the interconnects 40, 41, 42, 43. Further, the evaporation temperature of the solvent in the preferred embodiment is kept well below the curing temperature of the epoxy. Preferably, the solvent speed is about one hour. Significantly, when the solvent has evaporated, and the epoxy is still uncured, the surfaces of the interconnects 40, 41, 42, 43 will be slightly sticky.

[0032] In the preferred embodiment, the silver loaded epoxy will contain a suitable amount of filler material such as micronized glass, mica or barium sulphate in addition to the silver particles. The filler material will prevent the epoxy that forms the interconnects 40, 41, 42, 43 from slumping when the epoxy is semiliquid such as when the interconnects are heated.

[0033] Referring next to Figures 7 and 8, a thermal epoxy layer 50 is deposited over the top surface of wafer 100, a representative portion 105 of which is shown by Figure 7. The solvent in the thermal epoxy 50 is then evaporated leaving an uncured solid thermal epoxy layer 50. The thermal epoxy layer 50 when dried, surrounds the interconnects 40, 41, 42, 43 of each die 10, and extends to a height below that of interconnects 40, 41, 42, 43 as shown schematically by Figure 8. The thermal epoxy 50 layer may be deposited in one step followed by a drying step or by multiple deposition steps each followed by a drying step. Epoxies that may be used in the conductive interconnects and the thermal epoxy include epoxy novalac or mixes of bisphenyl A and bisphenyl F.

[0034] Wafer 100 is then singulated into individual semiconductor devices by, for example, sawing along streets 110. A semiconductor device so manufactured may be then packaged as in a tape and reel and shipped to the user, with interconnects 40, 41, 42, 43 of each device

being formed of sticky and uncured silver loaded epoxy, and each including a layer of dry and uncured thermal epoxy 50 surrounding its interconnects 40, 41, 42, 43.

[0035] Referring to Figures 9 and 10, the sticky or adhesive surfaces of interconnects 40, 41, 42, 43 hold the die in place on a board 60. Thereafter, the board (which may also be loaded with other components to be soldered down) is reflowed, using a traditional solder reflow process.

[0036] The interconnects 40, 41, 42, 43 become slightly softer at approximately 80°C and allow a connection to form with conductive pads (not shown) on board 60. At the same time the thermal epoxy 50 layer becomes fairly fluid (to the consistency of thick oil) and flows to form a connection between the die 10 and the top surface of board 60. The viscosity of the thermal epoxy 50 continues to reduce until the temperature exceeds about 150°C. At this point the catalyst in the external epoxy 50 starts a cure reaction. The catalyst is controlled by the use of known cure initiators and retardants to stop lower temperature curing. When the board 60 emerges from the end of the reflow oven, the epoxy system is cured and the device has silver interconnects connected to the conductive pads of the board 60. The thermal epoxy 50 has flown out forming a bond between the die 10 surface and the board 60 everywhere except where the interconnections 40, 41, 42, 43 are (underfilled) as best shown in Figure 10.

[0037] Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. It is preferred, therefore, that the present invention be limited not by the specific disclosure herein.

What is claimed is:

1. A method for manufacturing a semiconductor device, comprising:

depositing a passivation layer over a major surface of a semiconductor wafer, said semiconductor wafer including a plurality of identical semiconductor die isolated from one another by streets, each die having a major electrical contact on a major surface thereof;

creating a plurality of windows in said passivation layer, each window being positioned over and exposing said major electrical contact of a respective die;

depositing conductive epoxy containing conductive particles in each of said windows to form an interconnect over each of said major electrical contacts;

forming a layer of thermal epoxy around each of said interconnects; and

dicing said wafer along said streets to form a plurality of semiconductor devices.

2. A method for manufacturing of a semiconductor device according to claim 1, wherein said layer of thermal epoxy is formed to a maximum height which is below that of said interconnects.

3. A method for manufacturing of a semiconductor device according to claim 1, wherein said layer of thermal epoxy is formed by multiple deposition steps of thermal epoxy each step followed by an evaporation step.

4. A method for manufacturing of a semiconductor device according to claim 1, wherein said passivation layer comprises a photosensitive epoxy.

5. A method for manufacturing of a semiconductor device according to claim 1, wherein said windows are created by a photolithographically imaging step followed by a curing step.

6. A method for manufacturing of a semiconductor device according to claim 1, wherein said conductive particles comprise of silver.

7. A method for manufacturing of a semiconductor device according to claim 1, wherein said conductive epoxy comprises of 60% to 85% silver particles by weight, said particles being 3 to 40 microns.

8. A method for manufacturing of a semiconductor device according to claim 1, wherein said conductive epoxy comprises solvent.

9. A method for manufacturing of a semiconductor device according to claim 1, wherein said conductive epoxy is deposited by one of screening and dispensing.

10. A method for manufacturing of a semiconductor device according to claim 1, wherein all major electrical contacts of each respective die are disposed on only one major surface thereof, and wherein interconnects are formed on all major electrical contacts of each respective die before forming said layer of thermal epoxy.

11. A semiconductor device, comprising:

a semiconductor die having a major surface;

an electrical contact on said major surface of said semiconductor die;

an interconnect on said electrical contact, said interconnect being composed of a sticky epoxy containing conductive particles; and

a layer of thermal epoxy disposed on said major surface and surrounding said interconnect.

12. A semiconductor device according to claim 11, wherein said layer of thermal epoxy has a maximum height below that of said interconnect.

13. A semiconductor device according to claim 11, wherein said conductive particles comprise of silver.

14. A semiconductor device according to claim 11, wherein said conductive epoxy comprises of 60% to 85% silver particles by weight, said particles being 3 to 40 microns.

15. A semiconductor device according to claim 11, wherein all major electrical contacts of said die are disposed on said major surface, and wherein interconnects are formed on all major electrical contacts of said die.

16. A method for attaching a semiconductor die having a major electrical contact on a major surface thereof to a conductive pad, comprising:

disposing an interconnect on said major electrical contact, said interconnect being comprised of a sticky epoxy containing conductive particles;

surrounding said interconnect with a layer of thermal epoxy;

sticking said interconnect to said conductive pad;

heating said interconnect to a reflow temperature to form a connection between said interconnect and said conductive pad; and

further heating said thermal epoxy to a curing temperature, said curing temperature being above said reflow temperature.

17. A method according to claim 16, wherein said conductive pad is on a power circuit board.

18. A method according to claim 16, wherein said thermal epoxy includes initiators and retardants to ensure that said curing temperature will not be below said reflow temperature.

19. A method according to claim 16, wherein said reflow temperature is approximately 80 and said curing temperature is approximately 150.

20. A method according to claim 16, wherein said thermal epoxy becomes fluid upon further heating and wherein said die is spaced from said conductive pad to allow said thermal epoxy flows to a central portion of said die by capillary action.

21. A method according to claim 16, wherein said sticky epoxy comprises filler material.

22. A method according to claim 16, wherein said conductive particles comprise 60% to 85% of said sticky epoxy by weight and are comprised of silver particles that are 3 to 40 microns.

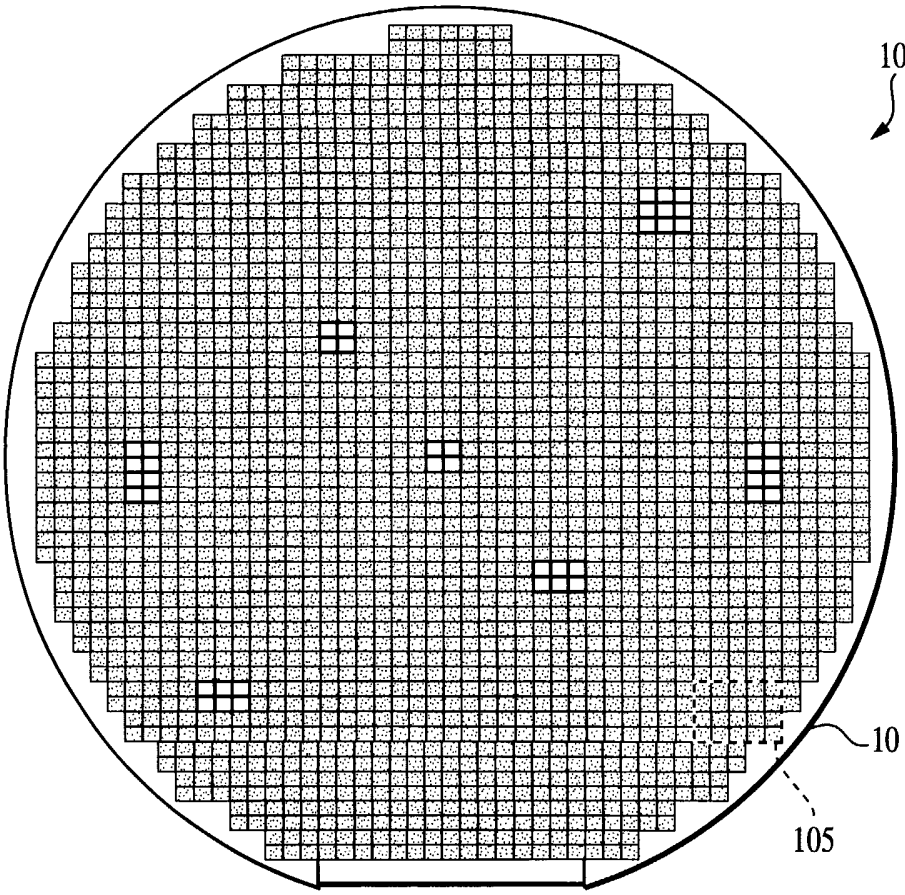


FIG. 1

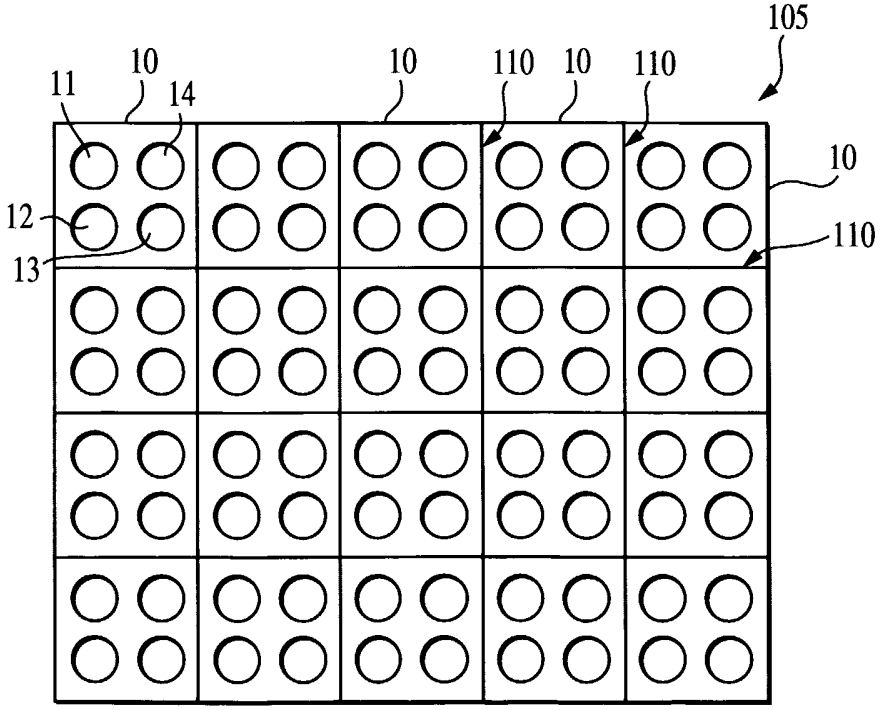


FIG. 2

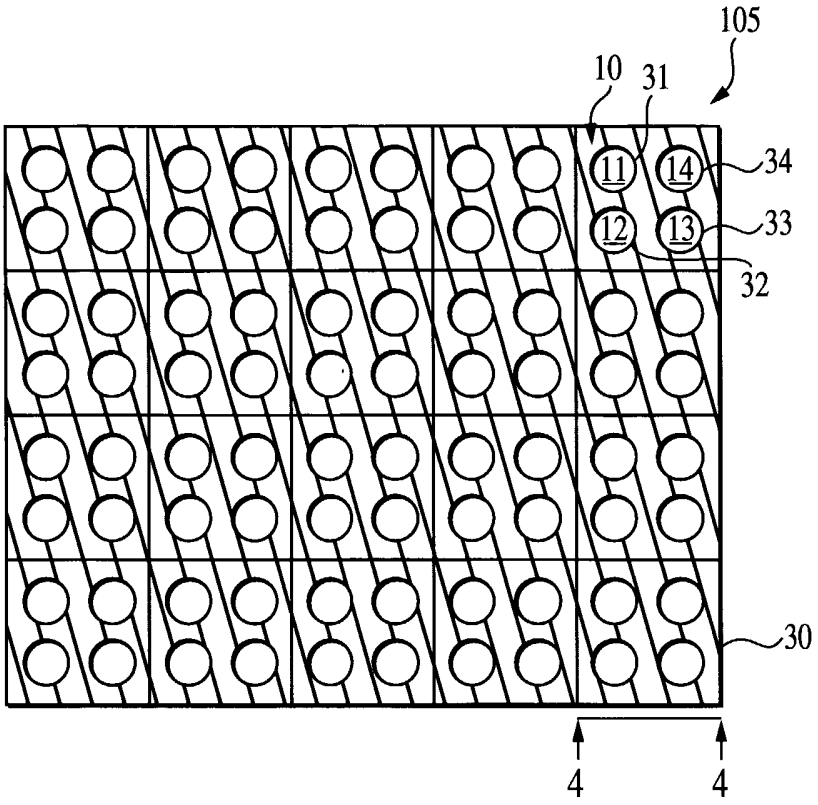


FIG. 3

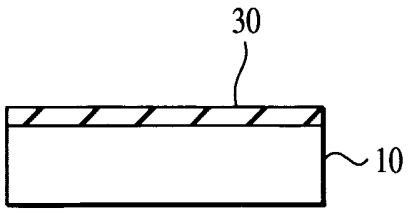


FIG. 4

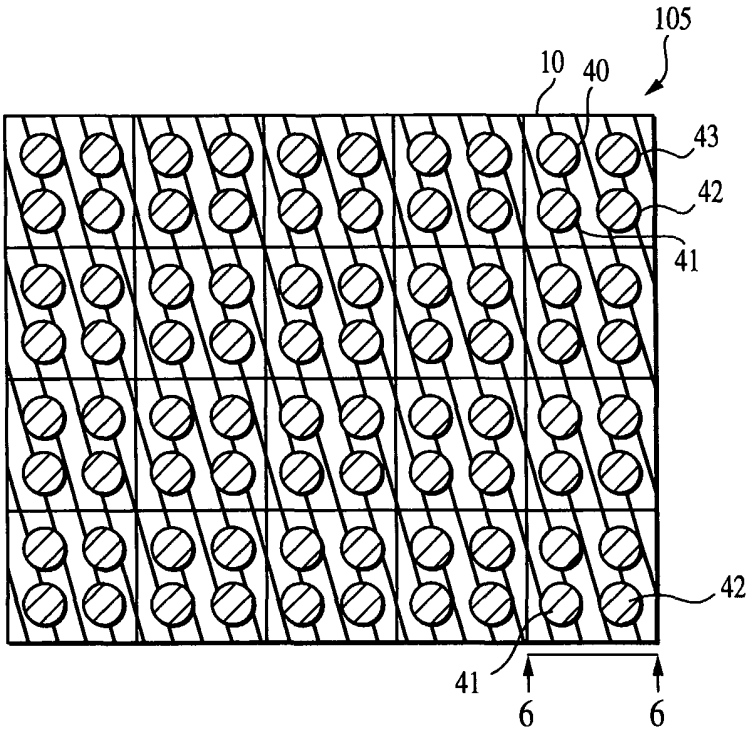


FIG. 5

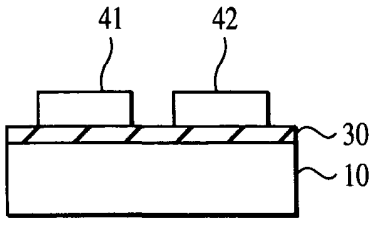


FIG. 6

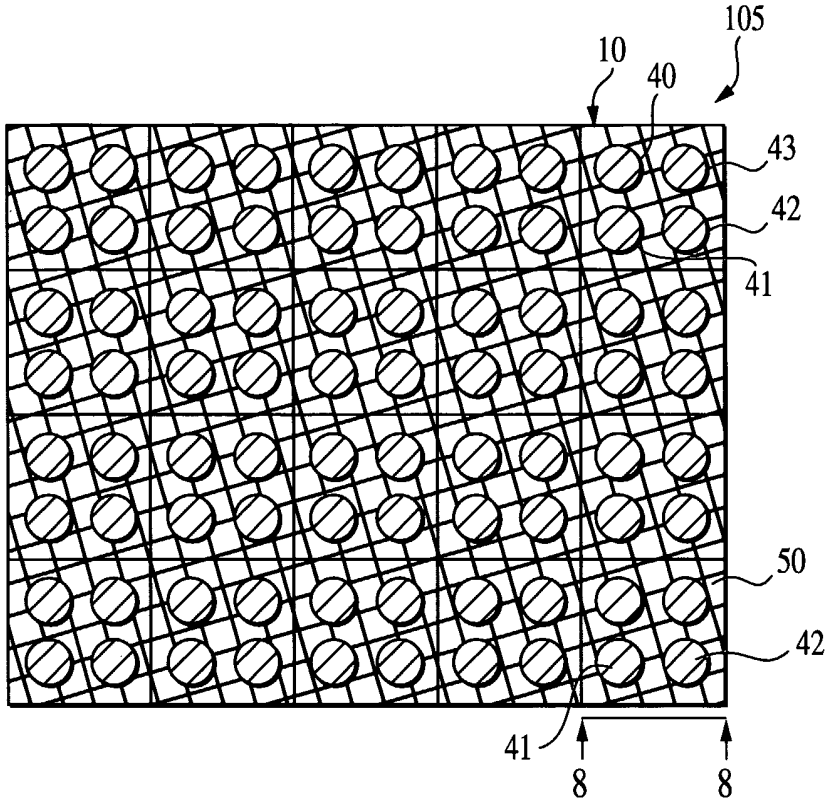


FIG. 7

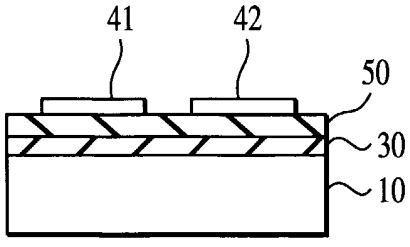


FIG. 8

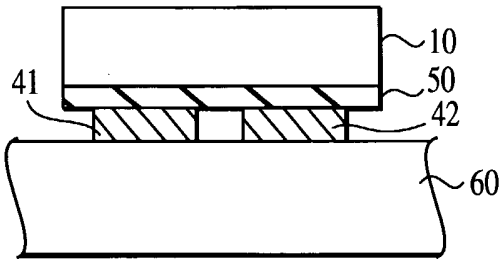


FIG. 9

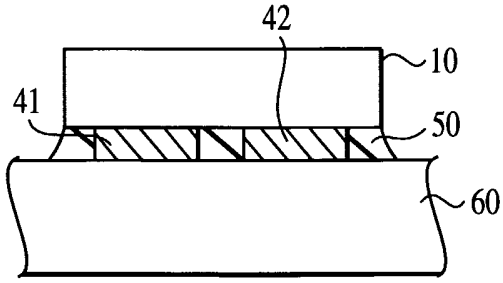


FIG. 10

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US02/27065

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) :H01L 21/00
US CL :438/113, 610

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 216/17, 18, 19, 33, 39; 438/113, 14, 610, 669, 690, 691, 754

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EAST

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 3,494,023 A (DORENDORF) 10 February 1970 (10/02/70), see entire document.	1-22

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
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"P"	document published prior to the international filing date but later than the priority date claimed		

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