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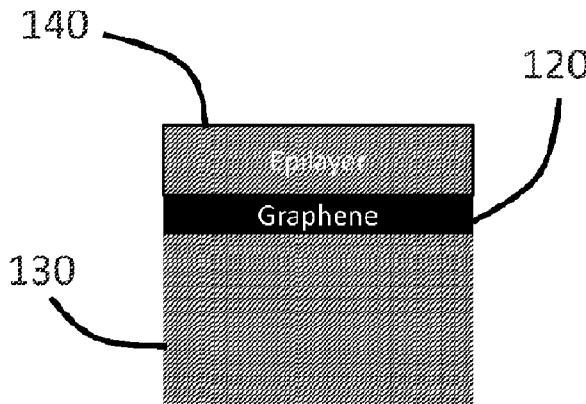
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(54) Title: SYSTEMS AND METHODS FOR GRAPHENE BASED LAYER TRANSFER



**FIG. 1D**

(57) **Abstract:** A graphene-based layer transfer (GBLT) technique is disclosed. In this approach, a device layer including a III-V semiconductor, Si, Ge, III-N semiconductor, SiC, SiGe, or II-VI semiconductor is fabricated on a graphene layer, which in turn is disposed on a substrate. The graphene layer or the substrate can be lattice-matched with the device layer to reduce defect in the device layer. The fabricated device layer is then removed from the substrate via, for example, a stressor attached to the device layer. In GBLT, the graphene layer serves as a reusable and universal platform for growing device layers and also serves a release layer that allows fast, precise, and repeatable release at the graphene surface.



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## Systems and Methods for Graphene Based Layer Transfer

### CROSS-REFERENCES TO RELATED APPLICATIONS

**[0001]** This application claims the priority benefit under 35 U.S.C. § 119(e) of U.S. Application No. 62/215,223, filed September 8, 2015, entitled “GRAPHENE-BASED LAYER TRANSFER PROCESS FOR ADVANCED COST-EFFICIENT ELECTRONICS/PHOTONICS,” which is hereby incorporated herein by reference in its entirety.

**[0002]** This application also claims the priority benefit under 35 U.S.C. § 119(e) of U.S. Application No. 62/335,784, filed May 13, 2016, entitled “DISLOCATION-FREE III-V INTEGRATION ON A SI WAFER,” which is hereby incorporated herein by reference in its entirety.

**[0003]** This application claims the priority benefit under 35 U.S.C. § 119(e) of U.S. Application No. 62/361,717, filed July 13, 2016, entitled “COST-EFFECTIVE LAYER-TRANSFER TECHNIQUE FOR ALL ELECTRONIC/PHOTONIC/MAGNETIC MATERIALS,” which is hereby incorporated herein by reference in its entirety.

### BACKGROUND

**[0004]** In advanced electronic and photonic technologies, devices are usually fabricated from functional semiconductors, such as III-N semiconductors, III-V semiconductors, II-VI semiconductors, and Ge. The lattice constants of these functional semiconductors typically do not match the lattice constants of silicon substrates. As understood in the art, lattice constant mismatch between a substrate and an epitaxial layer on the substrate can introduce strain into the epitaxial layer, thereby preventing epitaxial growth of thicker layers without defects. Therefore, non-silicon substrates are usually employed as seeds for epitaxial growth of most functional semiconductors. However, non-Si substrates with lattice constants matching those of functional materials can be costly and therefore limit the development of non-Si electronic/photonic devices.

**[0005]** One method to address the high cost of non-silicon substrates is the “layer-transfer” technique, in which functional device layers are grown on lattice-matched substrates and then removed and transferred to other substrates. The remaining lattice-matched substrates can then

be reused to fabricate another device layer, thereby reducing the cost. To significantly reduce manufacturing costs, it can be desirable for a layer-transfer method to have the following properties: 1) substrate reusability; 2) a minimal substrate refurbishment step after the layer release; 3) a fast release rate; and 4) precise control of release thickness.

**[0006]** Conventional methods to remove and transfer a device layer from a lattice-matched substrate include chemical lift-off (also referred to as epitaxial lift-off or ELO), optical lift-off (also referred to as laser lift-off or LLO, and mechanical lift-off (also referred to as controlled spalling). Unfortunately, none of these methods has the four desired properties at the same time.

**[0007]** The chemical lift-off technique can be used for lifting off devices layers made of III-V semiconductors from GaAs wafers. A sacrificial layer of AlAs is usually epitaxially inserted between the device layer and the substrate. Chemical lift-off technique selectively etches the sacrificial layer in a wet-chemical solution to release the device layers.

**[0008]** Despite its continuous development over the last three decades, chemical lift-off still has several disadvantages. For example, the release rate is slow owing to slow penetration of chemical etchant through the sacrificial layer (e.g., typically a few days to release a single 8-inch wafer). Second, etching residues tend to become surface contamination after release. Third, chemical lift-off has limited reusability owing to the chemical mechanical planarization (CMP) performed after release to recover the roughened substrate surface into an epi-ready surface. Fourth, it can be challenging to handle released epilayers in the chemical solution.

**[0009]** The optical lift-off technique usually uses a high-power laser to irradiate the back of the lattice-matched substrate (e.g., a transparent sapphire or SiC substrate) and selectively heat the device-substrate interface, causing decomposition of the interface and release of the device layer (e.g., III-N film). This technique can reduce the cost of manufacturing III-N-based light emitting diodes (LEDs) and address the problem of heat accumulation from the device by transferring released III-Ns to a substrate that has high thermal conductivity.

**[0010]** However, optical lift-off has its own limitations. First, because the molten III-N/substrate interface can make the substrate rough, a reconditioning step is usually carried out before reuse, thereby reducing the reusability to less than five times. Second, local pressurization at the interface caused by high-power thermal irradiation can induce cracks or dislocations. Third, the laser scanning speed can be too slow to permit high-throughput.

**[0011]** Controlled spalling can have a higher throughput than optical lift-off. In this technique, high-stress films (also referred to as “stressors”) are deposited on the epitaxial film, inducing fracture below the epilayers and resulting in the separation of active materials from the substrate. When sufficient tensile stress is applied to the interface, a  $K_{II}$  shear mode can initiate a crack and a  $K_I$  opening mode can allow the propagation of the crack parallel to the interface between the epilayer and the substrate. By controlling the internal stress and thickness of the stressor, strain energy sufficient to reach the critical  $K_I$  can be provided, leading to fracture of the film/substrate interface. Because the exfoliation occurs via crack propagation, the spalling process can cause rapid release of films.

**[0012]** However, controlled spalling is not mature enough to be used for commercial manufacturing for at least the following reasons. First, because crack propagation generally occurs through cleavage planes that are not always aligned normal to the surface, the surface may need polishing for reuse. Second, a thick stressor is usually used to provide enough energy to separate strong covalent bonds, particularly when working with high Young’s modulus materials like III-N semiconductors. Third, the internal stress of the stressor may only be controlled in a narrow range, which constrains the achievable thickness of the resulting spalled film. For example, because the maximum internal stress in a typical Ni stressor is about 1 GPa, the critical Ni thickness under 1 GPa tensile stress to initiate spalling of a GaAs film is about 1.5  $\mu\text{m}$ , which can induce spalling of the GaAs film itself if the GaAs is about 10  $\mu\text{m}$  thick. Therefore, when using a Ni stressor it can be challenging to make a GaAs film less than 10  $\mu\text{m}$  thick, but typically most devices use films that are much thinner.

## SUMMARY

**[0013]** Embodiments of the present invention include apparatus, systems, and methods for nanofabrication. In one example, a method of manufacturing a semiconductor device includes forming a graphene layer on a first substrate and transferring the graphene layer from the first substrate to a second substrate. The method also includes forming a single-crystalline film on the graphene layer.

**[0014]** In another example, a method of semiconductor processing includes forming a graphene monolayer on a silicon carbide substrate and transferring the graphene monolayer from the silicon carbide substrate to a semiconductor substrate. The method also includes forming a

plurality of holes in the graphene monolayer and forming a first single-crystalline layer of semiconductor material on the graphene monolayer. The semiconductor substrate acts as a seed for the first single-crystalline layer of semiconductor material. The method also includes removing the first single-crystalline layer of semiconductor material from the graphene monolayer and forming a second single-crystalline layer of semiconductor material on the graphene monolayer. The semiconductor substrate acts as a seed for the second single-crystalline layer of semiconductor material. The method further includes removing the second single-crystalline layer of semiconductor material from the graphene monolayer.

**[0015]** In yet another example, a method of semiconductor processing includes forming a graphene layer on a first substrate and transferring the graphene layer from the first substrate to a second substrate. The method also includes depositing a semiconductor layer on the graphene layer and depositing a stressor layer on the semiconductor layer. The stressor layer causes propagation of a crack between the semiconductor layer and the graphene layer. The method further includes disposing a flexible tape on the stressor layer and pulling the semiconductor layer and the stressor layer off the graphene layer with the flexible tape.

**[0016]** It should be appreciated that all combinations of the foregoing concepts and additional concepts discussed in greater detail below (provided such concepts are not mutually inconsistent) are contemplated as being part of the inventive subject matter disclosed herein. In particular, all combinations of claimed subject matter appearing at the end of this disclosure are contemplated as being part of the inventive subject matter disclosed herein. It should also be appreciated that terminology explicitly employed herein that also may appear in any disclosure incorporated by reference should be accorded a meaning most consistent with the particular concepts disclosed herein.

#### BRIEF DESCRIPTION OF THE DRAWINGS

**[0017]** The skilled artisan will understand that the drawings primarily are for illustrative purposes and are not intended to limit the scope of the inventive subject matter described herein. The drawings are not necessarily to scale; in some instances, various aspects of the inventive subject matter disclosed herein may be shown exaggerated or enlarged in the drawings to facilitate an understanding of different features. In the drawings, like reference characters generally refer to like features (e.g., functionally similar and/or structurally similar elements).

[0018] FIGS. 1A-1D illustrate a method of fabricating a semiconductor device using a graphene-based layer transfer process.

[0019] FIG. 2 is a graph showing materials that can be used to fabricate devices using the graphene-based technique illustrated in FIGS. 1A-1D, as well as the lattice constant and lattice mismatch of these materials.

[0020] FIGS. 3A-3F illustrate a method of graphene-based layer fabrication and transfer using a stressor layer and tape.

[0021] FIG. 4A-4B show the effects of graphene layer thickness and the underlying substrates on the growth of device layers on the graphene layer.

[0022] FIGS. 5A-5E illustrate a method of graphene-based layer transfer using a thin graphene layer.

[0023] FIG. 6A shows high-resolution X-ray diffraction (HRXRD) scans of GaN grown on graphene disposed on SiO<sub>2</sub> substrate.

[0024] FIG. 6B shows HRXRD scans of GaN grown on graphene disposed on SiC substrate.

[0025] FIGS. 7A-7C illustrate three configurations of graphene-based fabrication techniques using graphene layers of different thicknesses.

[0026] FIGS. 8A-8H illustrate a method of graphene-based layer fabrication and transfer using porous graphene, corresponding to the configuration shown in FIG. 7C.

[0027] FIGS. 9A and 9B are scanning electron microscope (SEM) images of Ge and GaAs epilayers, respectively, grown on damaged graphene.

[0028] FIGS. 10A and 10B are SEM images of the Ge and GaAs epilayers shown in FIGS. 9A and 9B, respectively, after release from the substrate.

[0029] FIGS. 11A-11H illustrate a method of fabricating light emitting diodes using a graphene-based layer fabrication and transfer technique.

[0030] FIGS. 12A-12G illustrate a method of fabricating GaAs solar cells using a graphene-based layer fabrication and transfer technique.

[0031] FIGS. 13A-13E illustrate a method of fabrication multi-junction solar cells using a graphene-based layer fabrication and transfer technique.

[0032] FIGS. 14A-14C illustrate a method of fabrication transistors using a graphene-based layer fabrication and transfer technique.

**[0033]** FIGS. 15A-15F illustrate a method of hetero-integration using a graphene-based layer fabrication and transfer technique.

**[0034]** FIGS. 16A-16F illustrate a method of preparing a platform for fabricating III-V devices using a graphene-based layer fabrication and transfer technique.

## DETAILED DESCRIPTION

### **[0035] Graphene-Based Layer Growth**

**[0036]** As described above, it can be desirable for a layer-transfer process to have substrate reusability, minimal needs for post-release treatment, a fast release rate, precise control of release interfaces, and universality for a wide range of device materials. Conventional layer-transfer processes may exhibit some of the desired properties. For example, layer release is much faster for mechanical lift-off than for chemical or optical lift-off, whereas the release location can be better controlled in chemical and optical lift-off. However, conventional layer-transfer methods suffer from rough surface formation after layer release, thereby limiting substrate reusability. In fact, the process cost to refurbish the substrate surface in conventional layer-transfer methods typically exceeds the substrate cost, so practical applications in manufacturing can be challenging. In addition, each conventional method usually works for a limited number of specific materials (e.g., chemical lift-off for III-V materials, whose lattice is close to that of GaAs, and optical lift-off for materials that can be grown on transparent substrates). Therefore, it is also challenging to make universal use of these methods.

**[0037]** To address the shortcomings in conventional layer-transfer methods, systems and methods described herein employ a graphene-based layer transfer (GBLT) approach to fabricate devices. In this approach, functional devices are fabricated on a graphene layer, which in turn is disposed on a substrate that is lattice-matched to the functional device layers. In one example, the graphene layer is deposited directly on the lattice-matched substrate. In another example, the graphene layer is transferred to the lattice-matched substrate from another substrate. The fabricated functional devices can then be removed from the lattice-matched substrate via, for example, a stressor attached to the functional devices.

**[0038]** In this GBLT approach, graphene serves as a reusable and universal platform for growing device layers and also serves a release layer that allows fast, precise, and repeatable release at the graphene surface. Compared to conventional methods, GBLT has several

advantages. First, because graphene is a crystalline film, it is a suitable substrate for growing epitaxial over-layers. Second, graphene's weak interaction with other materials can substantially relax the lattice mismatching rule for epitaxial growth, potentially permitting the growth of most semiconducting films with low defect densities. Third, the epilayer (e.g., functional devices) grown on a graphene substrate can be easily and precisely released from the substrate owing to graphene's weak van der Waals interactions, which permits rapid mechanical release of epilayers without post-release reconditioning of the released surface. Fourth, graphene's mechanical robustness can maximize its reusability for multiple growth/release cycles.

**[0039]** Implementation of GBLT for general material systems can have a significant impact on both the scientific community and industry because GBLT has the potential to fabricate devices without the expensive millimeter-thick, single-crystalline wafers used in current semiconductor processing. Moreover, the entire functional device can be transferred from the graphene layer, for additional flexible functions.

**[0040]** FIGS. 1A-1D illustrate a method 100 of fabricating a device layer using graphene as a platform. As shown in FIG. 1A, a graphene layer 120 is fabricated on a first substrate 110, such as a Si substrate, SiC substrate, or copper foil. The fabricated graphene layer 120 is then removed from the first substrate 110 as shown in FIG. 1B. The removed graphene layer 120 is then disposed on a second substrate 130, such as a Ge substrate, as shown in FIG. 1C. FIG. 1D shows that an epilayer 140 (e.g., a single crystalline film to have high electrical and optical device performance) is then fabricated on the graphene layer 120. The epilayer 140 is also referred to as a device layer or a functional layer in this application.

**[0041]** The graphene layer 120 can be fabricated on the first substrate 110 via various methods. In one example, the graphene layer 120 can include an epitaxial graphene with a single-crystalline orientation and the substrate 110 can include a (0001) 4H-SiC wafer with a silicon surface. The fabrication of the graphene layer 120 can include multistep annealing steps. A first annealing step can be performed in H<sub>2</sub> gas for surface etching and vicinalization, and a second annealing step can be performed in Ar for graphitization at high temperature (e.g., about 1,575 °C).

**[0042]** In another example, the graphene layer 120 can be grown on the first substrate 110 via a chemical vapor deposition (CVD) process. The substrate 110 can include a nickel substrate or a copper substrate. Alternatively, the substrate 100 can include an insulating substrate of SiO<sub>2</sub>,

HfO<sub>2</sub>, Al<sub>2</sub>O<sub>3</sub>, Si<sub>3</sub>N<sub>4</sub>, and practically any other high temperature compatible planar material by CVD.

[0043] In yet another example, the first substrate 110 can be any substrate that can hold the graphene layer 120 and the fabrication can include a mechanical exfoliation process. In this example, the first substrate 110 can function as a temporary holder for the graphene layer 120.

[0044] Various methods can also be used to transfer the graphene layer 120 from the first substrate 110 to the second substrate. In one example, a carrier film can be attached to the graphene layer 120. The carrier film can include a thick film of Poly(methyl methacrylate) (PMMA) or a thermal release tape and the attachment can be achieved via a spin-coating process. After the combination of the carrier film and the graphene layer 120 is disposed on the second substrate 130, the carrier film can be dissolved (e.g., in acetone) for further fabrication of the epilayer 140 on the graphene layer 120.

[0045] In another example, a stamp layer including an elastomeric material such as polydimethylsiloxane (PDMS) can be attached to the graphene layer 120 and the first substrate can be etched away, leaving the combination of the stamp layer and the graphene layer 120. After the stamp layer and the graphene layer 120 are placed on the second substrate 130, the stamp layer can be removed by mechanical detachment, producing a clean surface of the graphene layer 120 for further processing.

[0046] In yet another example, a self-release transfer method can be used to transfer the graphene layer 120 to the second substrate 130. In this method, a self-release layer is first spun-cast over the graphene layer 120. An elastomeric stamp is then placed in conformal contact with the self-release layer. The first substrate 110 can be etched away to leave the combination of the stamp layer, the self-release layer, and the graphene layer. After this combination is placed on the second substrate 130, the stamp layer can be removed mechanically and the self-release layer can be dissolved under mild conditions in a suitable solvent. The release layer can include polystyrene (PS), poly(isobutylene) (PIB) and Teflon AF (poly[4,5-difluoro-2,2-bis(trifluoromethyl)-1,3-dioxole-co-tetrafluoroethylene]).

[0047] The epilayer 140 can include a III-V semiconductor, Si, Ge, III-N semiconductor, SiC, SiGe, and II-VI semiconductors, among others. In one example, the lattice of the second substrate 130 is matched to the epilayer 140, in which case the second substrate 130 functions as the seed for the growth of the epilayer 140 if the graphene layer 120 is porous or thin enough

(e.g., if the graphene layer 120 is one layer thick). Sandwiching the graphene layer 120 between the second substrate 130 and the epilayer 140 can facilitate quick and damage-free release and transfer of the epilayer 140.

**[0048]** In another example, the graphene layer 120 can be thick enough (e.g., several layers thick) to function as a seed to grow the epilayer 140, in which case the epilayer 140 can be latticed-matched to the graphene layer 120. This example also allows repeated use of the second substrate 130. In yet another example, the second substrate 130 together with the graphene layer 120 can function as the seed to grow the epilayer 140.

**[0049]** Using graphene as the seed to fabricate the epilayer 140 can also increase the tolerance over mismatch of lattice constant between the epilayer material and graphene.

Without being bound by any particular theory or mode of operation, surfaces of two-dimensional (2D) materials (e.g., graphene) or quasi-2D layered crystals typically have no dangling bonds and interact with material above them via weak van der Waals like forces. Due to the weak interaction, an epilayer can grow from the beginning with its own lattice constant forming an interface with a small amount of defects. This kind of growth can be referred to as Van Der Waals Epitaxy (VDWE). The lattice matching condition can be drastically relaxed for VDWE, allowing a large variety of different heterostructures even for highly lattice mismatched systems.

**[0050]** In practice, the lattice mismatch can be about 0% to about 70% (e.g., about 0%, about 10%, about 20%, about 30%, about 40%, about 50%, about 60%, and about 70%, including any values and sub ranges in between).

**[0051]** In one example, the epilayer 140 includes a 2D material system. In another example, the epilayer 140 includes a 3D material system. The flexibility to fabricate both 2D and 3D material systems allows fabrication of a wide range of optical, opto-electronic, and photonic devices known in the art.

**[0052]** FIG. 2 is a graph showing materials that can be deposited on the graphene layer 120 to form the epilayer 140. FIG. 2 also shows the lattice constants of these materials and the mismatch of these lattice constants with respect to graphene. These materials include SiC, AlN, GaN, InN, GaP, AlP, Silicon, AlAs, Ge, GaAs, and InP. These materials listed on FIG. 2 are for illustrative purposes only. In practice, other materials with similar lattice mismatches with respect to graphene can also be used to form the epilayer 140.

**[0053]** The fabrication of the epilayer 140 can be carried out using semiconductor fabrication technique known in the art. For example, low-pressure Metal-Organic Chemical Vapor Deposition (MOCVD) can be used to grow the epilayer 140 (e.g., a GaN film) on the graphene layer 120, which in turn is disposed on the second substrate 130 (e.g., a SiC substrate). In this example, the graphene layer 120 and the second substrate 130 can be baked (e.g., under H<sub>2</sub> for >15 min at >1,100 °C) to clean the surface. Then the deposition of the epilayer 140 including GaN can be performed at, for example, 200 mbar. Trimethylgallium, ammonia, and hydrogen can be used as the Ga source, nitrogen source, and carrier gas, respectively. A modified two-step growth can be employed to obtain flat GaN epitaxial films on the epitaxial graphene 120. The first step can be carried out at a growth temperature of 1,100 °C for few minutes where guided nucleation at terrace edges can be promoted. The second growth step can be carried out at an elevated temperature of 1,250 °C to promote the lateral growth. Vertical GaN growth rate in this case can be around 20 nm per min.

**[0054] Graphene-Based Layer Transfer**

**[0055]** FIGS. 3A-3F illustrate a method 300 of graphene-based layer transfer. FIG. 3A shows that a graphene layer 320 is formed or disposed on a donor wafer 310, which may be a single-crystalline wafer. For example, the graphene layer 320 can include epitaxial graphene grown on the donor wafer 310 as known in the art. Alternatively, the graphene layer 320 can be exfoliated and transferred to the donor wafer 310 from another wafer (not shown). In yet another example, any of the graphene transfer techniques described above with reference with FIGS. 1A-1D can be used here to prepare the graphene layer 320 disposed on the donor wafer 320.

**[0056]** FIG. 3B shows that an epilayer 330 is epitaxially grown on the graphene layer 320. The epilayer 330 can include an electronic layer, a photonic layer, or any other functional device layer. Methods to fabricate the epilayer 330 can include any methods and techniques described above with respect to FIGS. 1A-1D.

**[0057]** FIG. 3C shows that a stressor 340 is disposed on the epilayer 330. For example, the stressor 330 can include a high-stress metal film such as a Ni film. In this example, the Ni stressor can be deposited in an evaporator at a vacuum level of  $1\times10^{-5}$  Torr.

**[0058]** FIG. 3D shows that a tape layer 350 is disposed on the stressor 340 for handling the stressor 340. Using the tape 350 and the stressor 340 can mechanically exfoliate the epilayer 330 from the graphene layer 320 at a fast release rate by applying high strain energy to the interface

between the epilayer 330 and the graphene layer 320. The release rate can be fast at least due to the weak van der Waals bonding between graphene and other materials such as the epilayer 330.

**[0059]** In FIG. 3E, the released epilayer 330, together with the stressor 340 and the tape layer 350 are disposed on a host wafer 360. In FIG. 3F, the tape 340 and the stressor 340 are removed, leaving the epilayer 330 for further processing such as forming more sophisticated devices or depositing additional materials on the epilayer 330. In one example, the tape layer 350 and the stressor 340 can be etched away by a  $\text{FeCl}_3$ -based solution.

**[0060]** In the method 300, after the release of the epilayer 330 shown in FIG. 3D, the remaining donor wafer 310 and the graphene layer 320 can be reused for next cycle of epilayer fabrication. Alternatively, the graphene layer 320 can also be released. In this case, a new graphene layer can be disposed on the donor wafer 310 before next cycle of epilayer fabrication. In either case, the graphene layer 320 protects the donor wafer 310 from damage, thereby allowing multiple uses and reducing cost.

**[0061]** In contrast, conventional processes usually include chemical-mechanical planarization (CMP) after release to recondition the wafer surface. CMP can consume relatively thick materials, and repeated CMPs increase the chance of breaking a wafer. GBLT can increase or maximize reusability because it creates an atomically smooth release surface. In GBLT, layer release can occur precisely at the interface between the epilayer 330 and the graphene layer 320 because graphene's weak van der Waals force does not permit strong bonding to adjacent materials. This allows the graphene layer 320 to be reused for multiple growth/exfoliation cycles without the need for a polishing step and without damaging the graphene, due to its mechanical robustness. In addition, GBLT can ensure a fast release rate and universal application for different materials. Because the epilayer 330 is mechanically released from the weak graphene surface, the layer release rate in GBLT can be high. Whereas conventional layer-transfer methods are limited to specific materials, GBLT can be universally applied because VDWE can overcome extremely high lattice mismatch and most semiconductor films can be epitaxially grown on graphene.

**[0062]** Furthermore, by having highly strained freestanding epilayer 330 after release as shown in FIG. 3D, the devices made of the epilayer 330 can have higher electron or hole mobility. An optoelectronic device made of the epilayer 330 can also have an enhanced optical response.

**[0063]** For mechanical release of the epilayer 330 from the graphene layer 320, it can be desirable for the material of the stressor 340 to provide enough strain energy to the epilayer/graphene interfaces to promote damage-free exfoliation/transfer. One concern for the mechanical release process can be the bending of epilayer 330 during exfoliation and self-exfoliation during deposition of the stressor 340. If the radius of curvature is reduced during exfoliation, strain energy can increase in the epilayer 330. When the strain energy reaches a critical point, cracks can form. Also, if strain energy in the stressor exceeds the epilayer/graphene interface energy, the epilayer 330 may be delaminated during stressor deposition. To address this concern, the transfer of epilayers on graphene can be performed by a feedback loop control.

**[0064] Effects of Substrate Field On the Epilayer**

**[0065]** In the methods illustrated in FIGS. 1A-1D and FIGS. 3A-3F, device layers are fabricated on a graphene layer. Since graphene typically is on the order of one atom thick (e.g., on the order of 3 Å), any covalently-bonded substrate surface immediately below the graphene may affect the epitaxial growth of the device layer by, for example, altering the crystalline orientation of the device layer. Therefore, it can be beneficial to understand the effect of the underlying substrate on the growth of the device layer so as to, for example, reduce defect density on the device layer as well as to control the properties such as crystalline orientation of the device layer.

**[0066]** FIGS. 4A-4B show schematics of graphene-based fabrication systems to illustrate the effect of underlying substrates on the growth of device layers. FIG. 4A shows a system 401 including a substrate 411 and a graphene layer 421 disposed on the substrate 411. A device layer 431 is fabricated on the graphene layer 421. The substrate 411 has a potential field 441 (e.g., via van De Waals force or other atomic or molecular forces) indicated by arrows in FIG. 4A. In this case, the graphene layer 421 includes only a single monolayer of graphene (i.e., the graphene layer 421 is one atom thick) and the potential field 441 reaches beyond the graphene layer 421 and can interact with the device layer 431. As a result, the potential field 441, which depends on the material properties (such as crystalline orientation) of the substrate 411, can affect the growth of the device layer 431. At the same time, the graphene layer 421 also has its own potential field (not shown in FIG. 4A), which may similarly influence the growth of the device layer 431. The net result can be that the device layer 431 includes films 431a and 431b having two different

orientations such as (100) and (111) orientations. Alternatively, the substrate force can be strong enough to overcome graphene field, in which case single-crystalline films that resembles substrates can be grown.

**[0067]** FIG. 4B shows a system 402 including a substrate 412 and a graphene layer 422 disposed on the substrate 412. A device layer 432 is fabricated on the graphene layer 422. The substrate 412 has a potential field 442 indicated by arrows in FIG. 4B. In contrast to the graphene layer 421 in FIG. 4A, the graphene layer 422 in FIG. 4B includes multiple stacks of monolayer graphene (i.e., the graphene layer 422 is more than one atom thick). Accordingly, the potential field 442 may interact only with the graphene layer 422 and may not reach the device layer 432. In other words, the VDWE of the device layer 432 occurs outside the potential field 442 of the substrate 412. In this case, the potential field of the graphene layer 422 affects the growth of the device layer 432.

**[0068]** FIGS. 4A-4B illustrate that the effect of the substrates (e.g., 411 and 412) on the growth of the device layers (e.g., 431 and 432) depend on the distance between them. In other words, the thickness of the graphene layers (e.g., 421 and 422) sandwiched between the substrates and the device layers determines the interaction strength. After a critical distance, the underlying substrates may not have any effect on the epitaxial growth of the device layers. This critical distance can be verified using high-resolution X-ray diffraction (HRXRD) to monitor the crystalline orientation of the epilayer as a function of graphene thicknesses, because the epilayer can resemble the graphene lattice beyond the critical distance.

**[0069]** FIGS. 5A-5E illustrate a method 500 of graphene-based layer transfer using thin graphene layers. In FIG. 5A, a donor wafer 510a is provided to grow a graphene layer 520 (shown in FIG. 5B). FIG. 5B shows that the graphene layer 520 is then transferred to a second wafer 510b, which can include III-N semiconductors, II-IV semiconductors, III-V semiconductors, and IV semiconductors.

**[0070]** In FIG. 5C, a film 530 is grown epitaxially above the graphene layer 520. Since the graphene layer 520 is sufficiently thin in this case, the growth of the film 530 is seeded by the second wafer 510b underneath the graphene layer 520. In FIG. 5D, a stressor 540 is deposited on the film 530 to facilitate subsequent layer transfer. The stressor 540 can include high stress metal materials such as nickel. In FIG. 5E, a tape layer 550 is disposed on the stressor 540 so as to handle the stressor 540 for releasing the film 530 from the graphene layer 520 and the second

wafer 510b. In the method 500, the graphene layer 520 is thin enough and the graphene seeding effect can disappear while substrate seeding effect is strong. In this manner, one can make any releasable films via the method 500.

**[0071]** FIGS. 6A-6B show variations of crystallographic orientation of epilayers grown on graphene using different underlying substrates. FIG. 6A shows  $\omega - 2\theta$  scans in HRXRD of GaN on graphene/SiO<sub>2</sub> (graphene on SiO<sub>2</sub> substrate). FIG. 6B shows  $\omega - 2\theta$  scans of GaN on graphene/SiC (graphene on SiC substrate).

**[0072]** To eliminate the epitaxial relation between the epitaxial graphene and the SiC substrate, the epitaxial graphene as used in FIG. 6A can be exfoliated from the SiC and then transferred to amorphous SiO<sub>2</sub>-coated Si substrates. Then GaN can be grown on the substrate. The HRXRD  $\omega - 2\theta$  scan reveals that the GaN film grown on epitaxial graphene on top of SiO<sub>2</sub> is (0002)-textured polycrystalline, while the GaN film grown on epitaxial graphene on top of SiC has a single (0002) orientation (see FIG. 6A and FIG. 6B). This implies that the substrate right below the graphene layer plays a role in determining epitaxial orientation. Accordingly, the material (or the crystalline orientation) of the substrate can be employed to control the epitaxial orientation of the device layer.

**[0073] Control of Seeding Locations in Graphene-Based Layer Fabrication and Transfer**

**[0074]** In practical applications of graphene-based layer fabrication and transfer, it can be beneficial for the epitaxial registry to be tunable to either the graphene or the substrate so as to obtain high-quality single-crystalline films on graphene. With this control of the seeding location, direct epitaxy on the graphene or remote epitaxy seeded from the substrate can be achieved. In direct epitaxy on the graphene, graphene plays a role as a seed as well as a release layer. In remote epitaxy seeded from the substrate, graphene becomes a release layer only, while the substrate works as a seed.

**[0075]** FIGS. 7A-7C show schematics of three different types of graphene-based layer fabrication systems using graphene layers of different thicknesses. In applications, users can choose to use one of these systems based on the desired interaction strength between the device layer and the underlying substrate, or alternatively depending on the desired interaction strength between the device layer and the graphene. These three options can provide great flexibility to accommodate different fabrication tasks.

**[0076]** FIG. 7A shows a system 701 (also referred to as Type I system) including a substrate 711 and a graphene layer 721 grown on the substrate 711. An epilayer 731 is then grown on the graphene layer 721. In the type I system 701, both the graphene layer 721 and the substrate 711 interact with the epilayer 731, as indicated by the arrows in FIG. 7A.

**[0077]** In one example, the epitaxial graphene 721 (e.g., a monolayer graphene) can be grown on a SiC substrate for use in a type I system. In this example, because the crystallographic orientations of graphene and SiC are aligned, they can both offer a hexagonal seed for <0001> wurtzite structures. This substrate can be employed for growing single-crystalline wurtzite III-N (or SiC) films since the lattice mismatch between III-N semiconductors and graphene is small. This epitaxial graphene/SiC substrate can also be used to grow (111) cubic III-V, Si, and Ge films because both graphene and SiC become seeds for the (111) orientation.

**[0078]** In another example, the substrate 711 includes germanium (Ge) to epitaxially grow the graphene layer 721. The lattice mismatch between Ge and other cubic materials is typically smaller than the lattice mismatch between SiC and the cubic materials. In this example, the graphene layer 721 can be grown on the Ge substrate 711 via MOCVD techniques. In yet another example, graphene can be directly grown on other semiconductor wafers such as GaAs, InP, and GaN.

**[0079]** FIG. 7B shows a system 702 (also referred to as Type II system) including a substrate 712 and a graphene layer 722 grown on the substrate 712. An epilayer 732 is then grown on the graphene layer 722. In the type II system 702, the thickness of the graphene layer 722 is substantially equal to or larger than the critical distance of interaction between the substrate 712 and the epilayer 732. Therefore, the epilayer 732 only interacts with the epitaxial graphene 722, which provides pure VDWE. This Type II system can be suitable to grow III-N semiconductor films or SiC single-crystalline films because its lattice mismatch to graphene is not substantially high. Copper foils can be used to fabricate poly-crystalline graphene of large sizes (e.g., greater than 8", greater than 12", or more).

**[0080]** FIG. 7C shows a system 703 (also referred to as Type III system) including a substrate 713 and a graphene layer 723 grown on the substrate 713. An epilayer 733 is then grown on the graphene layer 723. In the type III system 703, the graphene layer 723 works only as a release layer and epitaxial growth is seeded only from the substrate 713. Substrate materials with the same or a similar lattice to the epilayer 733 can be used. The graphene layer 723 does not

participate in determining the crystalline orientation of the epilayer 733. Accordingly, the graphene layer 723 can include either single-crystalline graphene or polycrystalline graphene.

**[0081]** The Type III system assigns registry of the epilayer 733 to the substrate. One advantage of this configuration is that high-quality epilayers can be grown on lattice-matching substrates just like in homoepitaxy, while the epilayers can be released from the graphene surface. To accomplish this, it can be desirable for the graphene layer 723 to be substantially transparent to the epilayer 733 during growth. This can be achieved by amorphizing or damaging the graphene via ions (e.g., via dry etching). The damages in the graphene layer 723 can allow direct interaction of the epilayer 733 and the substrate 713 through the graphene layer 723 such that the graphene layer 723 does not guide the crystalline orientation of the epilayer 733.

**[0082]** In one example, the substrate has polarity such as III-V substrates, III-N substrates, II-V substrates, and/or Ionic bonded substrate (e.g., Oxide, perovskite), pristine graphene can be transferred onto the wafer and epilayer can have the same crystallinity as that of the wafer and the grown film can be ready to be exfoliated. In another example, the substrate can have no polarity (e.g., group IV), damaging graphene can help promote substrate/epilayer interaction.

**[0083]** FIGS. 8A-8H illustrate a method 800 of graphene-based layer fabrication and transfer using graphene with periodic holes, which is referred to as porous graphene hereafter. The method 800 can be implemented with the Type III system, in which the graphene functions as a release layer and the substrate seeds the epitaxial growth of one or more functional layers.

**[0084]** In FIG. 8A, a graphene layer 820 is disposed on a substrate 810. The graphene layer 820 can be grown on the substrate 810 via, for example, chemical vapor deposition. Alternatively, the graphene layer 820 can be transferred to the substrate 810. A porous film 830 (e.g., oxide, nitride, or photoresist film) is then disposed on the graphene layer 820 as shown in FIG. 8B. The porous film 830 has a high density of pinholes (e.g., about one hole per square micron). Alternatively, the porous film 830 can include any film with holes to allow subsequent processing shown in FIGS. 8C-8H.

**[0085]** In FIG. 8C, dry etching using Ar plasma or O<sub>2</sub> plasma is carried out to open up the pinholes in the porous film 830. This etching creates a plurality of holes 835 in the porous film 830, allowing the ions in the etching plasma to transmit through the porous film 830 and arrive at the graphene layer 820. The etching plasma then etches the portion of the graphene layer 820

directly underneath the pinholes 835 in the porous film 830. Ions in the etching plasma can damage the graphene layer 820 by creating a plurality of holes 825 in the graphene layer 820, which now becomes a porous graphene layer 820. In one example, the etching of the porous film 830 and the etching of the graphene layer 820 can be achieved with the same etching plasma. In another example, the etching of the porous film 830 and the etching of the graphene layer 820 can be achieved with different etching plasmas.

**[0086]** In FIG. 8E, the porous film 830 is removed, leaving the now-porous graphene layer 820 exposed to further processing. In one example, the porous film 830 includes photoresist material and can be removed by acetone. In another example, the porous film 830 includes oxide or nitride and can be removed by hydrogen fluoride (HF). FIG. 8E also shows that an epilayer 840 is grown on the porous graphene layer 820. The growth starts from the area where the holes 825 were created. The holes 825 allow direction interaction of the substrate 810 with the epilayer 840, thereby allowing the substrate 810 to guide the crystalline orientation of the epilayer 840. The growth of the epilayer 840 then extends to cover the entire graphene layer 820, forming a planar epilayer 840.

**[0087]** In FIG. 8G, the formed epilayer 840 is released from the graphene layer 820 and the substrate 810. The released epilayer 840 is transferred to a target substrate 850, as shown in FIG. 8H, for further processing, such as forming a functional device. The graphene layer 820 and the substrate 810, after the release of the epilayer 840 shown in FIG. 8G, is then reused to fabricate another epilayer, and the cycle can be repeated multiple times.

**[0088]** FIGS. 9A and 9B are scanning electron microscopy (SEM) images of the Ge and GaAs films, respectively, grown on damaged graphene. Although pits appear on the surface due to limited nucleation on the graphene and incomplete impingement of the growth fronts, planar (100) crystals completely seeded from the substrate are observed.

**[0089]** FIGS. 10A and 10B are SEM images of the Ge and GaAs films shown in FIG. 9A and 9B, respectively, after being exfoliated using a Ni stressor. The smooth exfoliated surface implies precise release of the layer from the graphene, and this is confirmed by observing the trace of graphene-like wrinkles during wet transfer.

**[0090]** This porous graphene approach as illustrated in FIGS. 8A-8H and experimentally investigated in FIGS. 9A-9B and FIGS. 10A-10B can be applied to several other material systems. In one example, InP films can be fabricated on damaged graphene disposed on InP

wafers. In another example, Si films can be grown on damaged graphene disposed on Si wafers. In yet another example, GaN films can be grown on damaged graphene disposed on GaN wafers. The epitaxial registry of the epilayer can be tuned to the substrate to secure successful epitaxial growth through the graphene onto the substrate.

**[0091] Fabrication of Functional Flexible Devices and Hetero-integration**

**[0092]** The graphene-based layer fabrication and transfer technique can be used to fabricate various functional devices based on the epilayers grown on graphene. In one example, III-N high electron mobility transistors (HEMTs) can be fabricated from III-N epilayers. The transistors can then be transferred to a polycrystalline diamond substrate for heat dissipation. GaN power devices can also be constructed from these films. In another example, flexible GaAs solar cells can be fabricated from III-V epilayers. Optoelectronic devices integrated with Si integrated circuits can also be constructed from III-V epilayers. In yet another example, Ge-based LEDs and photodetectors can be fabricated by growing IV epilayers on graphene, exfoliating them, stretching the freestanding Ge to tensile-strained Ge, and transferring them to Si integrated circuits. In yet another example, Ge can be grown on 12" Si wafer and then used as a seed to grow single-crystalline graphene. Then III-V optoelectronic materials can be grown on graphene on Ge/Si wafers without any dislocations.

**[0093]** FIGS. 11A-11H illustrate a method 1100 of fabricating light emitting diodes (LEDs) using graphene-based layer transfer techniques described above. In FIG. 11A, a graphene layer 1120 is grown on a substrate 1110 (e.g., a 6" SiC substrate). Then the graphene layer 1120 is released from the substrate 1110, as shown in FIG. 11B, and transferred to a target substrate 1130, as shown in FIG. 11C. The target substrate 1130 can be less expensive than, for example, the SiC wafer used in FIG. 11A.

**[0094]** In FIG. 11D, an LED stack 1140 (e.g., a visible LED stack) is fabricated on the graphene layer 1120. In this example, the LED stack 1140 includes three periods of III-nitride multi-quantum wells (InGaN well and GaN barrier) sandwiched between p-GaN and n-GaN layers. As readily appreciated by those of skill in the art, other types of LED stacks can also be grown on the graphene layer 1120.

**[0095]** The fabricated LED stack 1140 can then be processed in at least two ways. In one way, as illustrated in FIG. 11E, an electrode 1150 can be deposited on the LED stack 1140 to form an electrical contact. For example, thin Ni/Au (5 nm/5 nm) can be deposited on the LED

stack 1140 and then annealed at 500 °C for 10 min. This yields an LED that includes the substrate 1130.

**[0096]** Alternatively, as illustrated in FIG. 11F, the LED stack 1140 may be removed from the substrate 1130. To remove the LED stack 1140 from the substrate 1130, a stressor layer 1160 is disposed on the LED stack 1140 to release the LED stack 1140 from the target substrate 1130 and the graphene 1120. Then, the combination of stressor layer 1160 and the LED stack 1140 is flipped and placed on a second target substrate 1135, as shown in FIG. 11G. The stressor layer 1160 is in contact with the second target substrate 1135 and the LED stack 1140 is exposed for further processing. For example, FIG. 11G shows that LED mesas 1145 are etched from the LED stack 1140. In FIG. 11F, additional electrical contacts 1170 are integrated with the LED mesas 1145 and the stressor layer 1160.

**[0097]** In one example, the graphene layer 1120 can seed the growth of the LED stack 1140 and the target substrate 1130 may not have any effect on the growth of the LED stack 1140. In another example, type III seeding (e.g., illustrated in FIG. 7C) can be used. In this case, the graphene layer 1120 can be thin and the target substrate 1130 can seed the growth of the LED stack 1140. The target substrate 1130 can include GaN substrates.

**[0098]** FIGS. 12A-12G illustrate a method 1200 of fabricating GaAs solar cells using graphene-based layer transfer technique. In FIG. 12A, a graphene layer 1220 (e.g. a single-crystalline graphene layer) is fabricated on a substrate 1210 (e.g., a 6" SiC wafer). Then the graphene layer 1220 is transferred to a target substrate 1230 as seen in FIG. 12B. FIG. 12C shows that a GaAs solar cell 1240 is fabricated on the graphene layer 1220 via, for example, epitaxial growth techniques known in the art. FIG. 12D shows that a stressor layer 1250 is then deposited on the solar cell 1240 to facilitate subsequent device transfer. A tape layer 1260 is disposed on the stressor 1250 to help handle the device transfer as seen in FIG. 12E.

**[0099]** After release from the target substrate 1230, the solar cell 1240 becomes free standing and can be processed in two ways. In one way, as illustrated in FIG. 12F, the solar cell 1240 can be placed on metal 1240 for subsequent module fabrication. The solar cell 1240 can be placed on the metal 1240 via direct bonding or any other techniques known in the art. Alternatively, as illustrated in FIG. 12G, the free standing solar cell 1240, together with the stressor layer 1250 and the tape layer 1260, form a lightweight and flexible solar cell assembly in their own. This

flexible solar cell assembly can be easily integrated into other systems, including power electronic devices.

**[0100]** In one example, the graphene layer 1220 can seed the growth of the solar cell 1240 and the target substrate 1230 may not have any effect on the growth of the solar cell 1240. In another example, type III seeding (e.g., illustrated in FIG. 7C) can be used. In this case, the graphene layer 1220 can be thin and the target substrate 1230 can seed the growth of the solar cell 1240. The target substrate 1230 can include GaAs substrates.

**[0101]** FIGS. 13A-13E illustrate a method 1300 of fabricating multi-junction solar cells using graphene-based layer transfer technique. The method 1300 starts by disposing a graphene layer 1320 on a glass substrate 1310 having a transparent conductive oxide (TCO) surface, as shown in FIG. 13A. The graphene layer 1320 can be transferred to the glass substrate 1310 via any method described in this application or any other method known in the art.

**[0102]** FIG. 13B shows that three material layers are deposited on the graphene layer 1320, including an InGaP layer 1330, a GaAs layer 1340 on the InGaP layer 1330, and a second graphene layer 1350 on the GaAs layer 1340. FIG. 13C shows that an InGaAs layer 1360 is deposited on the second graphene layer 1350. The second graphene layer 1350 can help lattice-matching during the fabrication of the InGaAs layer 1360. Metal contacts 1370 are then placed on the InGaAs layer 1360 for electrical conduction, as shown in FIG. 13D. Then in FIG. 13E, the stack of InGaP layer 1330, the GaAs layer 1340, the second graphene layer 1350, and the InGaAs layer 1360 are etched into two solar cell mesas 1380, each of which is underneath a respective metal contact 1370.

**[0103]** FIGS. 14A-14C illustrate a method 1400 of fabricating transistors. In FIG. 14A, a graphene layer 1420 is disposed on a substrate 1410 such as a SiC wafer. An InGaAs layer 1430 is deposited on the graphene layer 1420. Then the InGaAs layer 1430 is transferred to a silicon wafer 1440 with an oxide layer 1450 disposed on the surface of the silicon wafer 1440, as shown in FIG. 14B. An  $\text{Al}_2\text{O}_3$  layer 1470 is then deposited on the InGaAs layer 1430 as the top gate dielectric. A gate 1480 is fabricated on the  $\text{Al}_2\text{O}_3$  layer 1470 to form a transistor, as shown in FIG. 14C.

**[0104]** In one example, the graphene layer 1420 can seed the growth of the InGaAs layer 1430 and the silicon wafer 1440 may not have any effect on the growth of the InGaAs layer 1430. In another example, type III seeding (e.g., illustrated in FIG. 7C) can be used. In this case, the

graphene layer 1420 can be thin and the silicon wafer 1440 be replaced by an InP substrate so as to seed the growth of the InGaAs layer 1430.

**[0105]** FIGS. 15A-15F illustrate a method 1500 of forming heterostructure using graphene-based layer transfer technique. In FIG. 15A, a graphene layer 1520 (e.g., a monolayer graphene) is disposed on a substrate 1510 such as a SiC wafer. An h-BN layer 1530 (i.e., hexagonal form boron nitride) is then epitaxially grown on the graphene layer 1520. FIG. 15B shows that a stressor layer 1540 (e.g., a nickel film) is coated on the h-BN layer 1530 and a tape layer 1550 is disposed on the stressor layer 1540. As described before, the tape layer 1550 and the stressor layer 1540 can transfer the h-BN layer 1530 to a second substrate including a silicon wafer 1560 with an oxide layer 1565 (e.g., silicon oxide) on the top, as illustrated in FIG. 15C. FIG. 15C also shows that the stressor layer 1540 and the tape layer 1550 are etched away, leaving the h-BN layer 1530 for further processing.

**[0106]** In FIG. 15D, a MoS<sub>2</sub> layer 1570 is deposited on the h-BN layer 1530, and a second h-BN layer 1580 is deposited on the MoS<sub>2</sub> layer 1570 so as to form h-BN/MoS<sub>2</sub> heterostructure. FIG. 15F shows that an HfO<sub>3</sub> layer 1590 is deposited on the second h-BN layer 1580 as top gate dielectric and a top gate 1595 is deposited on the HfO<sub>3</sub> layer 1590 for electrical conduction.

**[0107]** FIGS. 16A-16F illustrate a method 1600 of preparing a platform for fabricating III-V devices using graphene-based layer fabrication and transfer technique. FIG. 16A shows a 12" silicon wafer 1610. A relaxed Ge film 1620 is then disposed on the wafer 1610 via, for example, epitaxial growth, as shown in FIG. 12B. The Ge film 1620 then functions as seed to grow a graphene layer 1630 epitaxially, as seen in FIG. 16C. The graphene layer 1630 can include single crystalline graphene.

**[0108]** In FIG. 16D, the graphene layer 1630 is patterned via, for example, lithography techniques known in the art. The patterning results in gaps 1635 in the graphene layer 1630. In other words, the graphene layer 1630 can be patterned into isolated and smaller pieces of graphene layers. In FIG. 16E, device layers 1640 are fabricated on the graphene layer 1620. The device layers 1640 can include, for example, III-V materials or structures such as metal-oxide-semiconductor field-effect transistor (MOSFET), lasers, or any other structure known in the art. The devices layers 1640 then function as platforms to form additional devices 1650, as shown in FIG. 1610.

## **[0109] Conclusion**

**[0110]** While various inventive embodiments have been described and illustrated herein, those of ordinary skill in the art will readily envision a variety of other means and/or structures for performing the function and/or obtaining the results and/or one or more of the advantages described herein, and each of such variations and/or modifications is deemed to be within the scope of the inventive embodiments described herein. More generally, those skilled in the art will readily appreciate that all parameters, dimensions, materials, and configurations described herein are meant to be exemplary and that the actual parameters, dimensions, materials, and/or configurations will depend upon the specific application or applications for which the inventive teachings is/are used. Those skilled in the art will recognize, or be able to ascertain using no more than routine experimentation, many equivalents to the specific inventive embodiments described herein. It is, therefore, to be understood that the foregoing embodiments are presented by way of example only and that, within the scope of the appended claims and equivalents thereto, inventive embodiments may be practiced otherwise than as specifically described and claimed. Inventive embodiments of the present disclosure are directed to each individual feature, system, article, material, kit, and/or method described herein. In addition, any combination of two or more such features, systems, articles, materials, kits, and/or methods, if such features, systems, articles, materials, kits, and/or methods are not mutually inconsistent, is included within the inventive scope of the present disclosure.

**[0111]** The above-described embodiments can be implemented in any of numerous ways. For example, embodiments of designing and making the technology disclosed herein may be implemented using hardware, software or a combination thereof. When implemented in software, the software code can be executed on any suitable processor or collection of processors, whether provided in a single computer or distributed among multiple computers.

**[0112]** Further, it should be appreciated that a computer may be embodied in any of a number of forms, such as a rack-mounted computer, a desktop computer, a laptop computer, or a tablet computer. Additionally, a computer may be embedded in a device not generally regarded as a computer but with suitable processing capabilities, including a Personal Digital Assistant (PDA), a smart phone or any other suitable portable or fixed electronic device.

**[0113]** Also, a computer may have one or more input and output devices. These devices can be used, among other things, to present a user interface. Examples of output devices that can be used to provide a user interface include printers or display screens for visual presentation of

output and speakers or other sound generating devices for audible presentation of output.

Examples of input devices that can be used for a user interface include keyboards, and pointing devices, such as mice, touch pads, and digitizing tablets. As another example, a computer may receive input information through speech recognition or in other audible format.

**[0114]** Such computers may be interconnected by one or more networks in any suitable form, including a local area network or a wide area network, such as an enterprise network, and intelligent network (IN) or the Internet. Such networks may be based on any suitable technology and may operate according to any suitable protocol and may include wireless networks, wired networks or fiber optic networks.

**[0115]** The various methods or processes (outlined herein may be coded as software that is executable on one or more processors that employ any one of a variety of operating systems or platforms. Additionally, such software may be written using any of a number of suitable programming languages and/or programming or scripting tools, and also may be compiled as executable machine language code or intermediate code that is executed on a framework or virtual machine.

**[0116]** In this respect, various inventive concepts may be embodied as a computer readable storage medium (or multiple computer readable storage media) (e.g., a computer memory, one or more floppy discs, compact discs, optical discs, magnetic tapes, flash memories, circuit configurations in Field Programmable Gate Arrays or other semiconductor devices, or other non-transitory medium or tangible computer storage medium) encoded with one or more programs that, when executed on one or more computers or other processors, perform methods that implement the various embodiments of the invention discussed above. The computer readable medium or media can be transportable, such that the program or programs stored thereon can be loaded onto one or more different computers or other processors to implement various aspects of the present invention as discussed above.

**[0117]** The terms “program” or “software” are used herein in a generic sense to refer to any type of computer code or set of computer-executable instructions that can be employed to program a computer or other processor to implement various aspects of embodiments as discussed above. Additionally, it should be appreciated that according to one aspect, one or more computer programs that when executed perform methods of the present invention need not reside on a single computer or processor, but may be distributed in a modular fashion amongst a

number of different computers or processors to implement various aspects of the present invention.

**[0118]** Computer-executable instructions may be in many forms, such as program modules, executed by one or more computers or other devices. Generally, program modules include routines, programs, objects, components, data structures, etc. that perform particular tasks or implement particular abstract data types. Typically the functionality of the program modules may be combined or distributed as desired in various embodiments.

**[0119]** Also, data structures may be stored in computer-readable media in any suitable form. For simplicity of illustration, data structures may be shown to have fields that are related through location in the data structure. Such relationships may likewise be achieved by assigning storage for the fields with locations in a computer-readable medium that convey relationship between the fields. However, any suitable mechanism may be used to establish a relationship between information in fields of a data structure, including through the use of pointers, tags or other mechanisms that establish relationship between data elements.

**[0120]** Also, various inventive concepts may be embodied as one or more methods, of which an example has been provided. The acts performed as part of the method may be ordered in any suitable way. Accordingly, embodiments may be constructed in which acts are performed in an order different than illustrated, which may include performing some acts simultaneously, even though shown as sequential acts in illustrative embodiments.

**[0121]** All definitions, as defined and used herein, should be understood to control over dictionary definitions, definitions in documents incorporated by reference, and/or ordinary meanings of the defined terms.

**[0122]** The indefinite articles “a” and “an,” as used herein in the specification and in the claims, unless clearly indicated to the contrary, should be understood to mean “at least one.”

**[0123]** The phrase “and/or,” as used herein in the specification and in the claims, should be understood to mean “either or both” of the elements so conjoined, i.e., elements that are conjunctively present in some cases and disjunctively present in other cases. Multiple elements listed with “and/or” should be construed in the same fashion, i.e., “one or more” of the elements so conjoined. Other elements may optionally be present other than the elements specifically identified by the “and/or” clause, whether related or unrelated to those elements specifically identified. Thus, as a non-limiting example, a reference to “A and/or B”, when used in

conjunction with open-ended language such as “comprising” can refer, in one embodiment, to A only (optionally including elements other than B); in another embodiment, to B only (optionally including elements other than A); in yet another embodiment, to both A and B (optionally including other elements); etc.

**[0124]** As used herein in the specification and in the claims, “or” should be understood to have the same meaning as “and/or” as defined above. For example, when separating items in a list, “or” or “and/or” shall be interpreted as being inclusive, i.e., the inclusion of at least one, but also including more than one, of a number or list of elements, and, optionally, additional unlisted items. Only terms clearly indicated to the contrary, such as “only one of” or “exactly one of,” or, when used in the claims, “consisting of,” will refer to the inclusion of exactly one element of a number or list of elements. In general, the term “or” as used herein shall only be interpreted as indicating exclusive alternatives (i.e., “one or the other but not both”) when preceded by terms of exclusivity, such as “either,” “one of,” “only one of,” or “exactly one of.” “Consisting essentially of,” when used in the claims, shall have its ordinary meaning as used in the field of patent law.

**[0125]** As used herein in the specification and in the claims, the phrase “at least one,” in reference to a list of one or more elements, should be understood to mean at least one element selected from any one or more of the elements in the list of elements, but not necessarily including at least one of each and every element specifically listed within the list of elements and not excluding any combinations of elements in the list of elements. This definition also allows that elements may optionally be present other than the elements specifically identified within the list of elements to which the phrase “at least one” refers, whether related or unrelated to those elements specifically identified. Thus, as a non-limiting example, “at least one of A and B” (or, equivalently, “at least one of A or B,” or, equivalently “at least one of A and/or B”) can refer, in one embodiment, to at least one, optionally including more than one, A, with no B present (and optionally including elements other than B); in another embodiment, to at least one, optionally including more than one, B, with no A present (and optionally including elements other than A); in yet another embodiment, to at least one, optionally including more than one, A, and at least one, optionally including more than one, B (and optionally including other elements); etc.

**[0126]** In the claims, as well as in the specification above, all transitional phrases such as “comprising,” “including,” “carrying,” “having,” “containing,” “involving,” “holding,” “composed of,” and the like are to be understood to be open-ended, i.e., to mean including but not limited to. Only the transitional phrases “consisting of” and “consisting essentially of” shall be closed or semi-closed transitional phrases, respectively, as set forth in the United States Patent Office Manual of Patent Examining Procedures, Section 2111.03.

## CLAIMS

1. A method of manufacturing a semiconductor device, the method comprising:  
forming a graphene layer on a first substrate;  
transferring the graphene layer from the first substrate to a second substrate; and  
forming a single-crystalline film on the graphene layer.
2. The method of claim 1, wherein the first substrate comprises silicon carbide and the graphene layer comprises a single-crystalline graphene layer.
3. The method of claim 1, wherein the first substrate comprises a copper foil and the graphene layer comprises a poly-crystalline graphene layer.
4. The method of claim 1, wherein the first substrate comprises a silicon substrate and forming the graphene layer comprises:  
forming a germanium layer on the silicon substrate; and  
forming the graphene layer on the germanium layer.
5. The method of claim 1, wherein the graphene layer consists of a single layer of graphene and forming the single-crystalline film on the graphene layer comprises using the second substrate as a seed for the single-crystalline film and using the graphene layer as a release layer.
6. The method of claim 5, wherein the graphene layer comprises poly-crystalline graphene and the first substrate comprises a copper foil.
7. The method of claim 1, wherein the graphene layer comprises more than one layer of graphene and forming the single-crystalline film on the graphene layer comprises using the graphene layer as a seed for the single-crystalline film.
8. The method of claim 7, wherein the graphene layer comprises single-crystalline graphene.
9. The method of claim 1, wherein forming the single-crystalline film on the graphene layer comprises using a combination of the second substrate and the graphene layer as a seed for the single-crystalline film.

10. The method of claim 1, wherein forming the single-crystalline film comprises depositing material of the second substrate on the graphene layer.
11. The method of claim 1, further comprising:  
forming a plurality of holes in the graphene layer, and  
wherein forming the single-crystalline film comprises depositing material in the plurality of holes and on the graphene layer.
12. The method of claim 1, further comprising:  
removing the single-crystalline film from the graphene film.
13. The method of claim 12, wherein removing the single-crystalline film from the graphene film comprises exfoliating the single-crystalline film.
14. The method of claim 12, wherein removing the single-crystalline film from the graphene film comprises:  
forming a metal stressor on the single-crystalline film;  
disposing a flexible tape on the metal stressor; and  
pulling the single-crystalline film and the metal stressor off the graphene layer with the flexible tape.
15. The method of claim 12, further comprising:  
depositing the single-crystalline film on a third substrate.
16. The method of claim 12, further comprising:  
forming another single-crystalline film on the graphene layer.
17. The method of claim 1, further comprising:  
depositing material on the single-crystalline film.
18. The method of claim 1, further comprising:  
removing the single-crystalline film and the graphene layer from the second substrate.
19. A semiconductor device formed by the method of claim 1.

20. A method of semiconductor processing, the method comprising:

- forming a graphene monolayer on a silicon carbide substrate;
- transferring the graphene monolayer from the silicon carbide substrate to a semiconductor substrate;
- forming a plurality of holes in the graphene monolayer;
- forming a first single-crystalline layer of semiconductor material on the graphene monolayer, the semiconductor substrate acting as a seed for the first single-crystalline layer of semiconductor material;
- removing the first single-crystalline layer of semiconductor material from the graphene monolayer;
- forming a second single-crystalline layer of semiconductor material on the graphene monolayer, the semiconductor substrate acting as a seed for the second single-crystalline layer of semiconductor material; and
- removing the second single-crystalline layer of semiconductor material from the graphene monolayer.

21. The method of claim 20, wherein removing the first single-crystalline layer of semiconductor material from the graphene monolayer comprises exfoliating the first single-crystalline layer of semiconductor material.

22. The method of claim 20, further comprising:

- forming a plurality of holes in the graphene monolayer, and
- wherein forming the first single-crystalline layer of semiconductor material comprises depositing material in the plurality of holes.

23. A device formed by the method of claim 20.

24. A method of semiconductor processing, the method comprising:

- forming a graphene layer on a first substrate;
- transferring the graphene layer from the first substrate to a second substrate;
- depositing a semiconductor layer on the graphene layer;
- depositing a stressor layer on the semiconductor layer, the stressor layer causing propagation of a crack between the semiconductor layer and the graphene layer; and

disposing a flexible tape on the stressor layer; and  
pulling the semiconductor layer and the stressor layer off the graphene layer with the  
flexible tape.

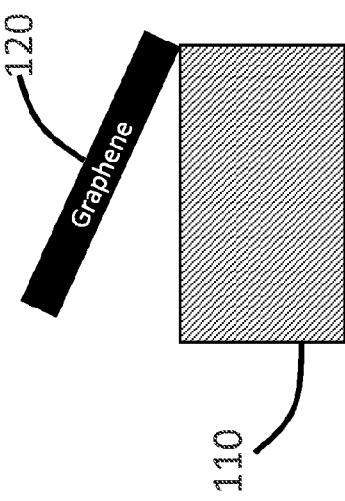


FIG. 1A

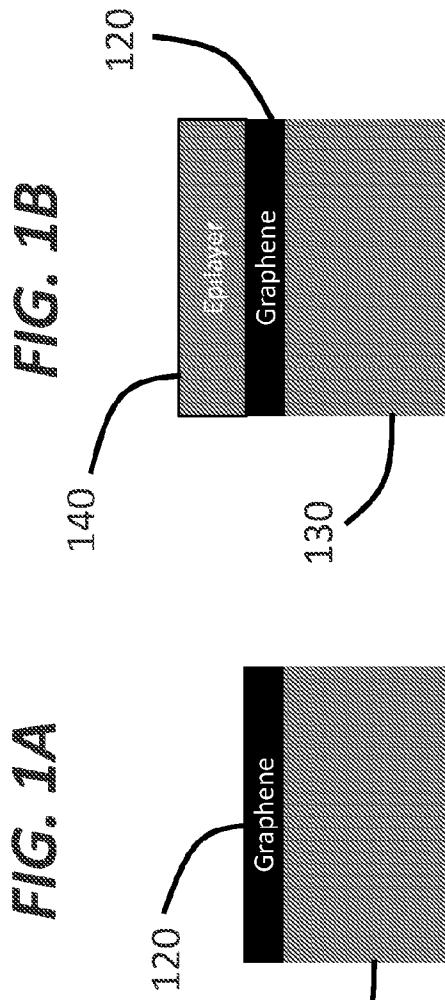
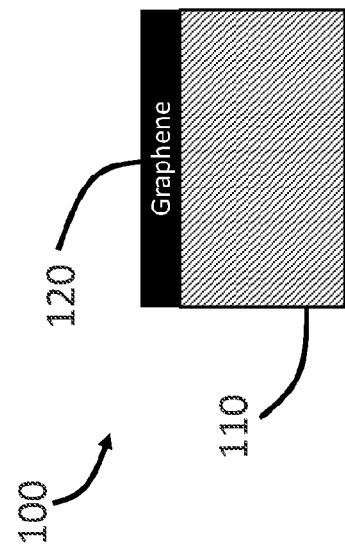


FIG. 1C

FIG. 1D

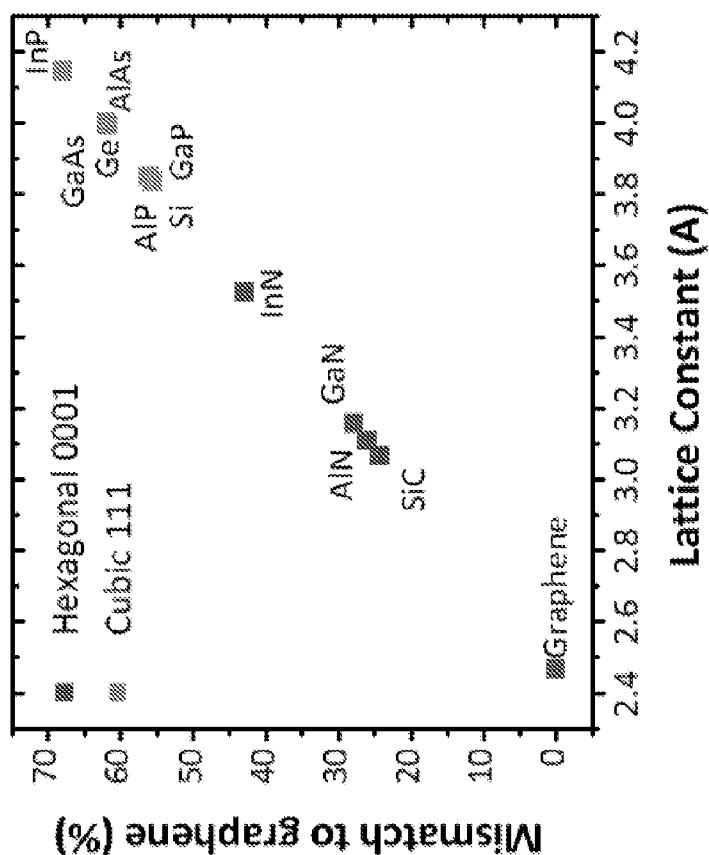


FIG. 2

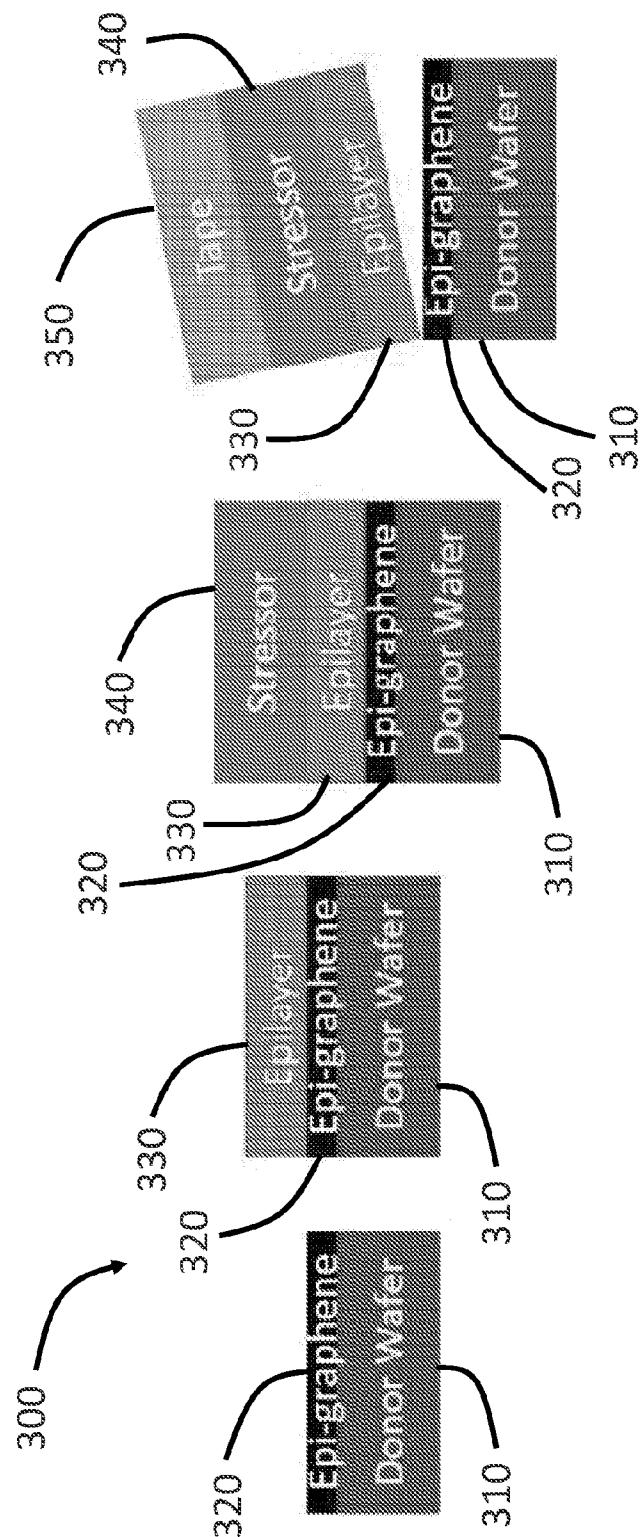


FIG. 3A

FIG. 3C

FIG. 3D

FIG. 3B

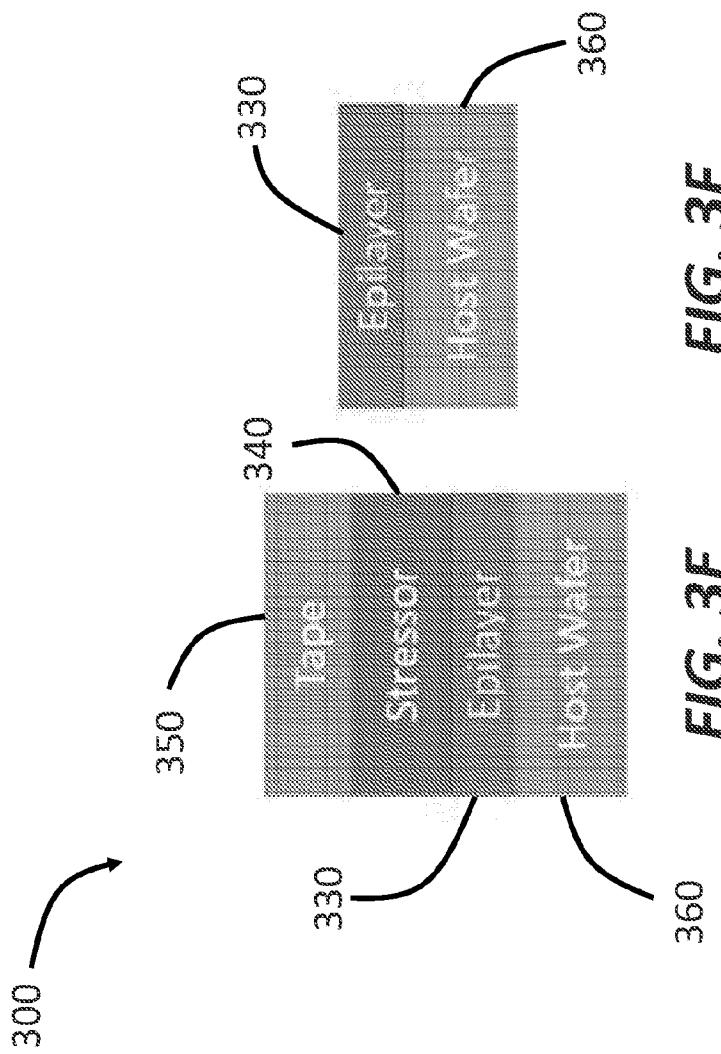


FIG. 3F

FIG. 3E

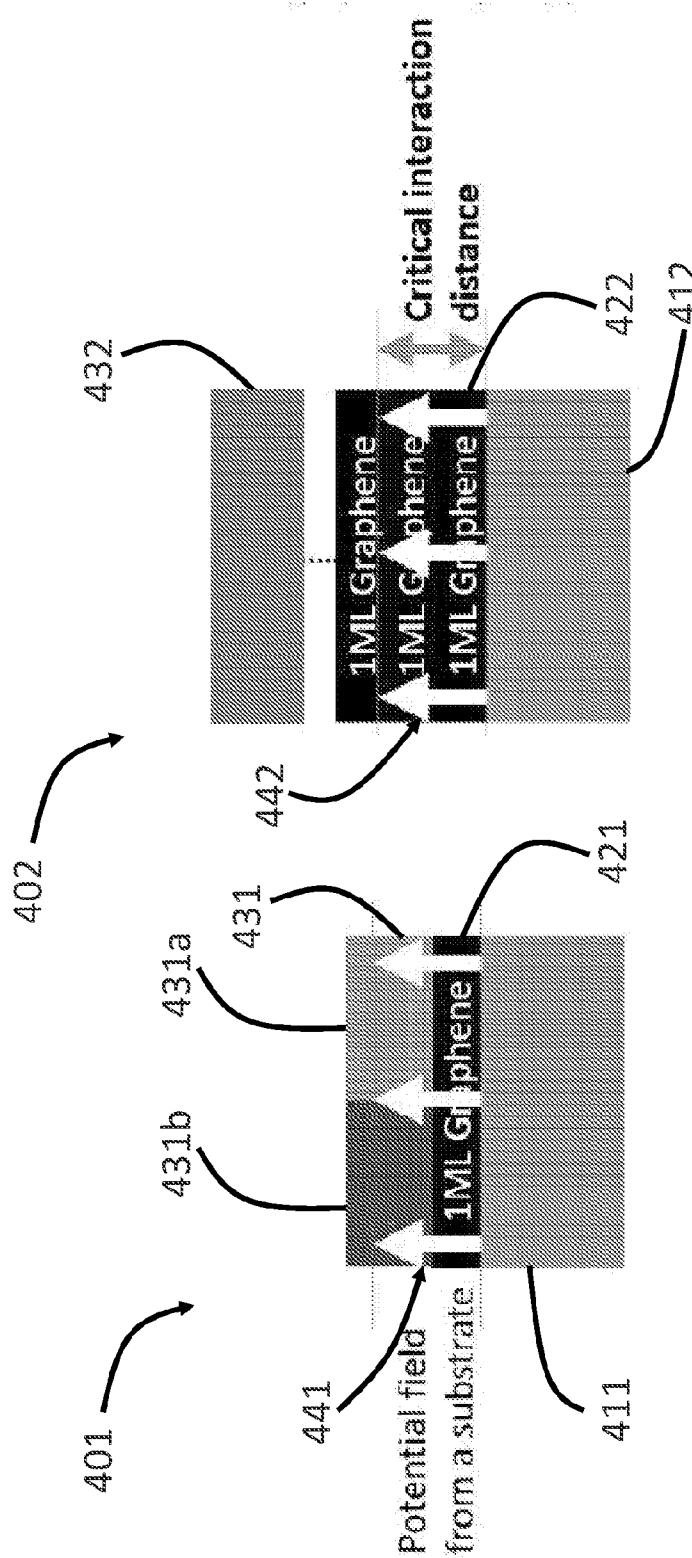


FIG. 4A  
FIG. 4B

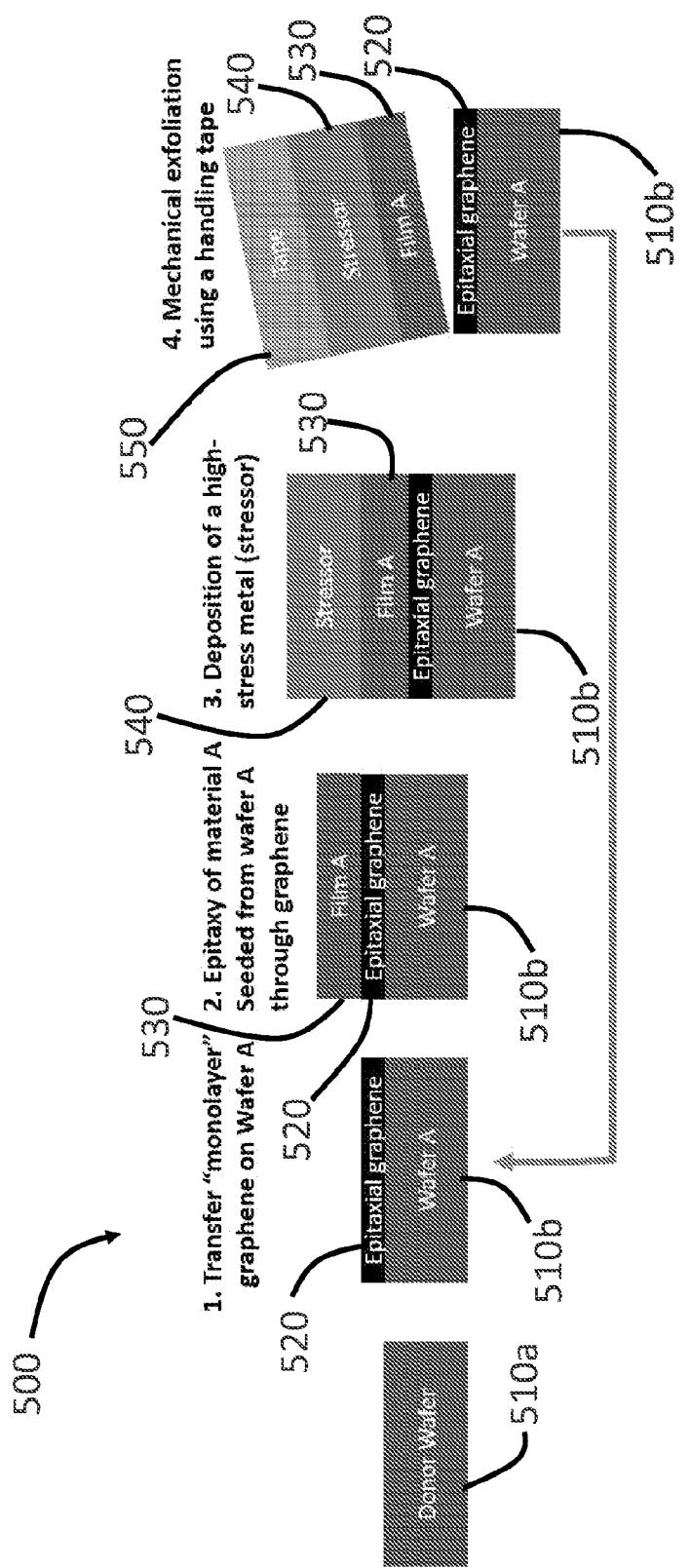
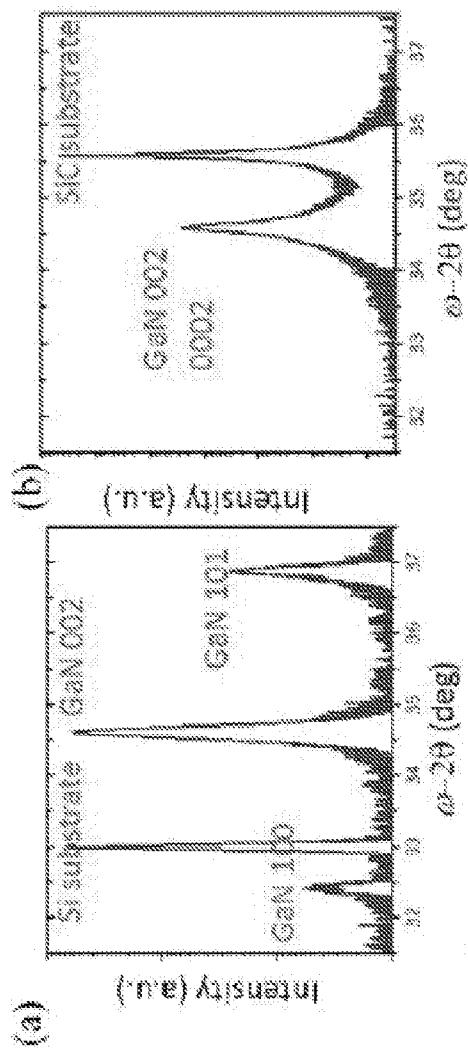


FIG. 5A FIG. 5B FIG. 5C

FIG. 5D

FIG. 5E



**FIG. 6A**  
**FIG. 6B**

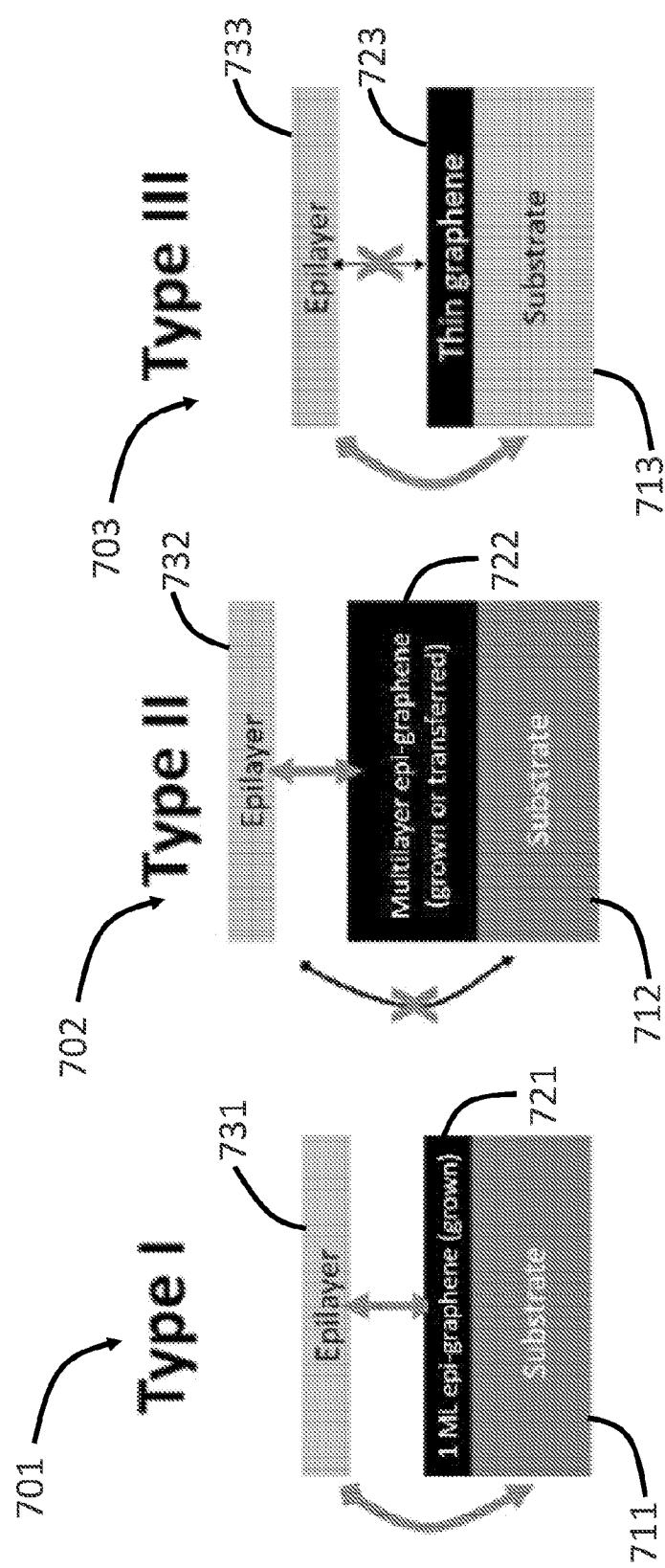


FIG. 7A

FIG. 7B

FIG. 7C

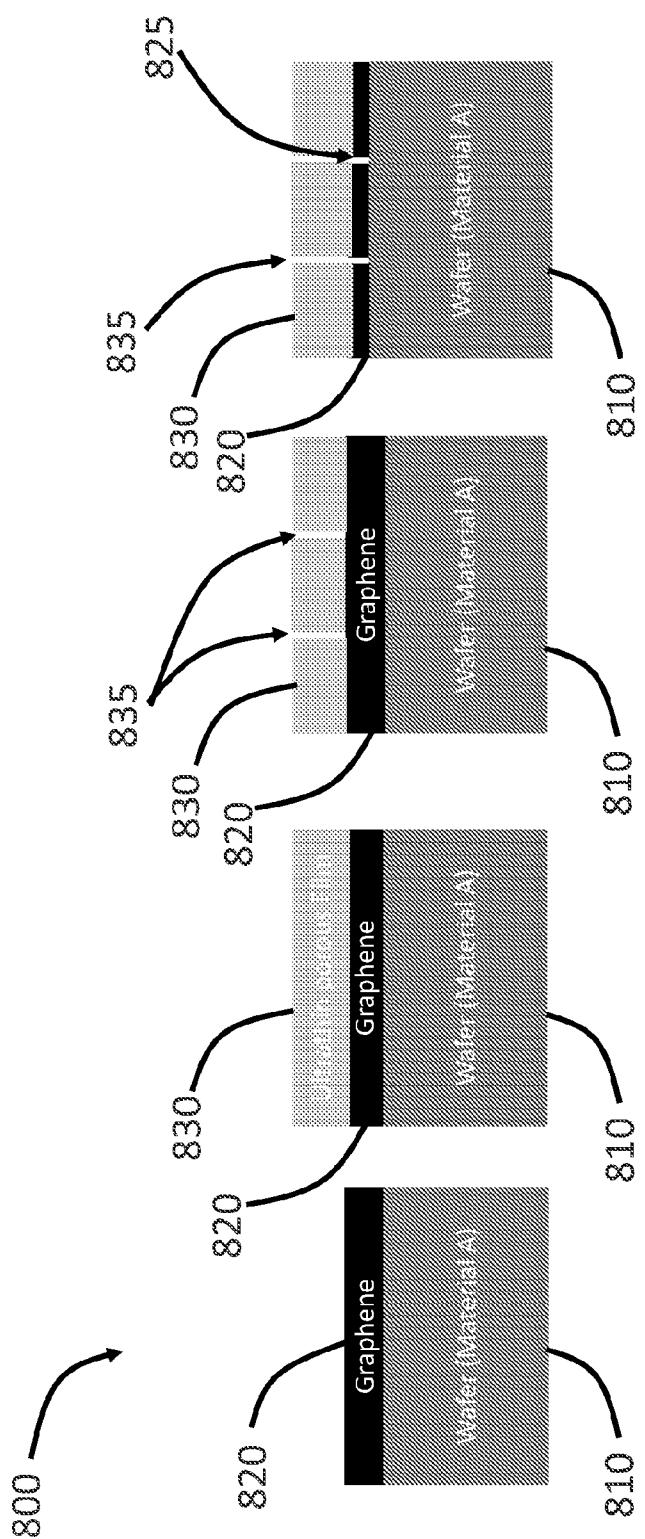
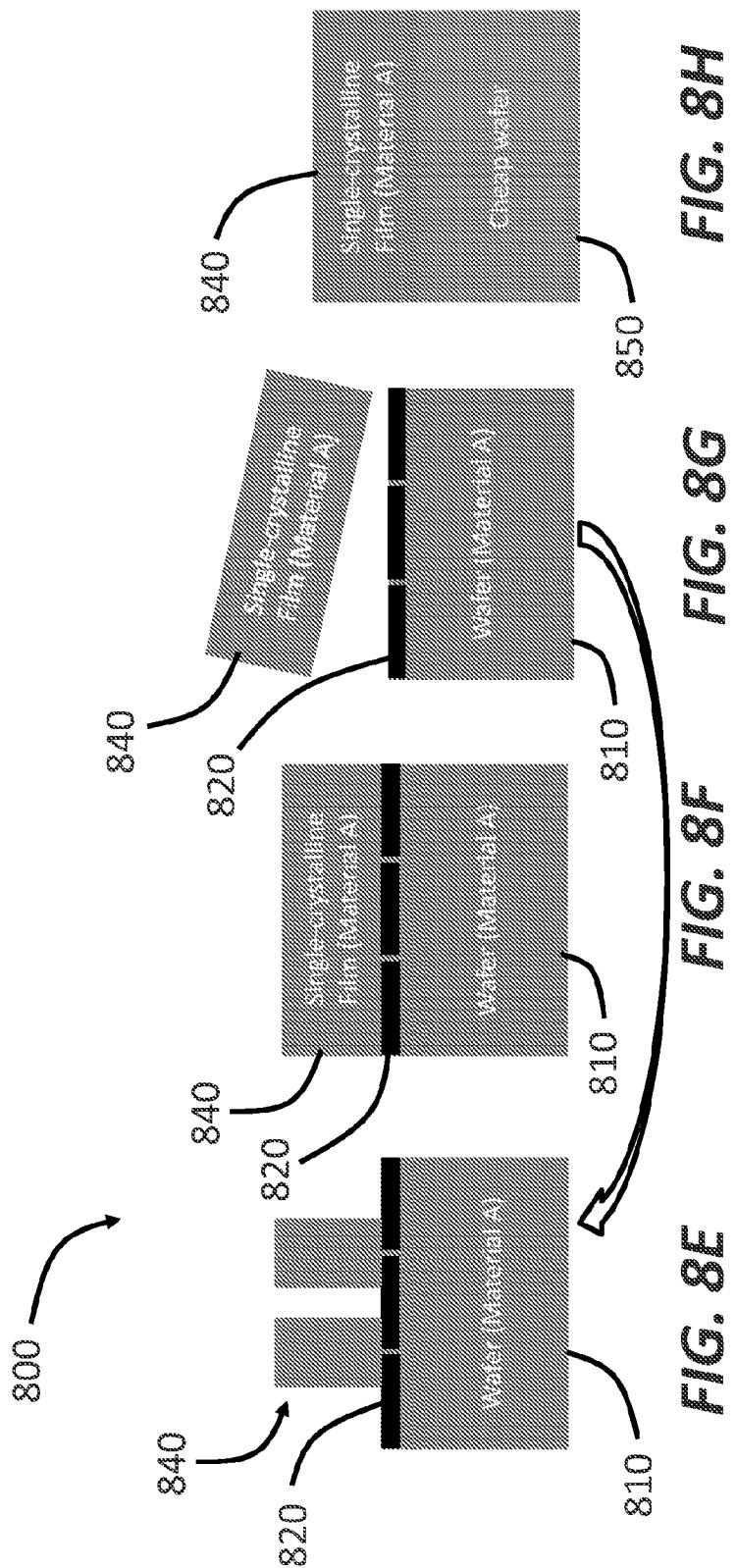


FIG. 8A

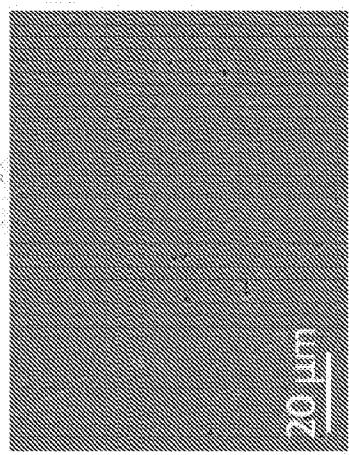
FIG. 8B

FIG. 8C

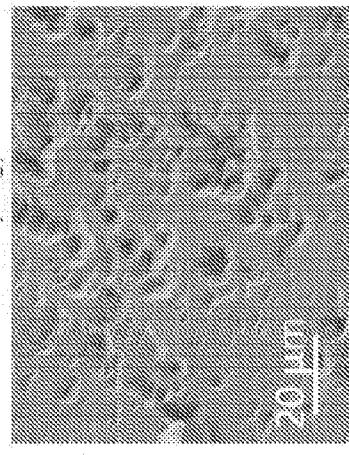
FIG. 8D



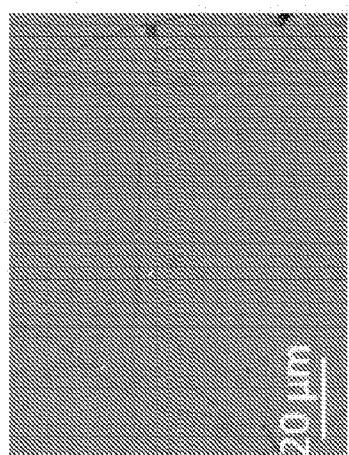
*FIG. 9A*



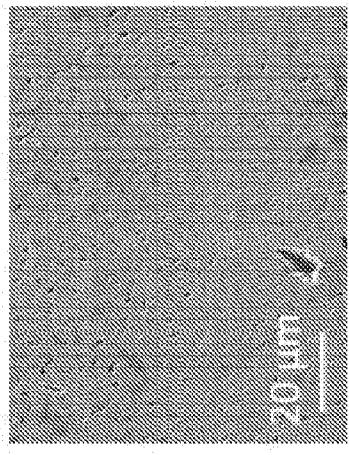
*FIG. 9B*

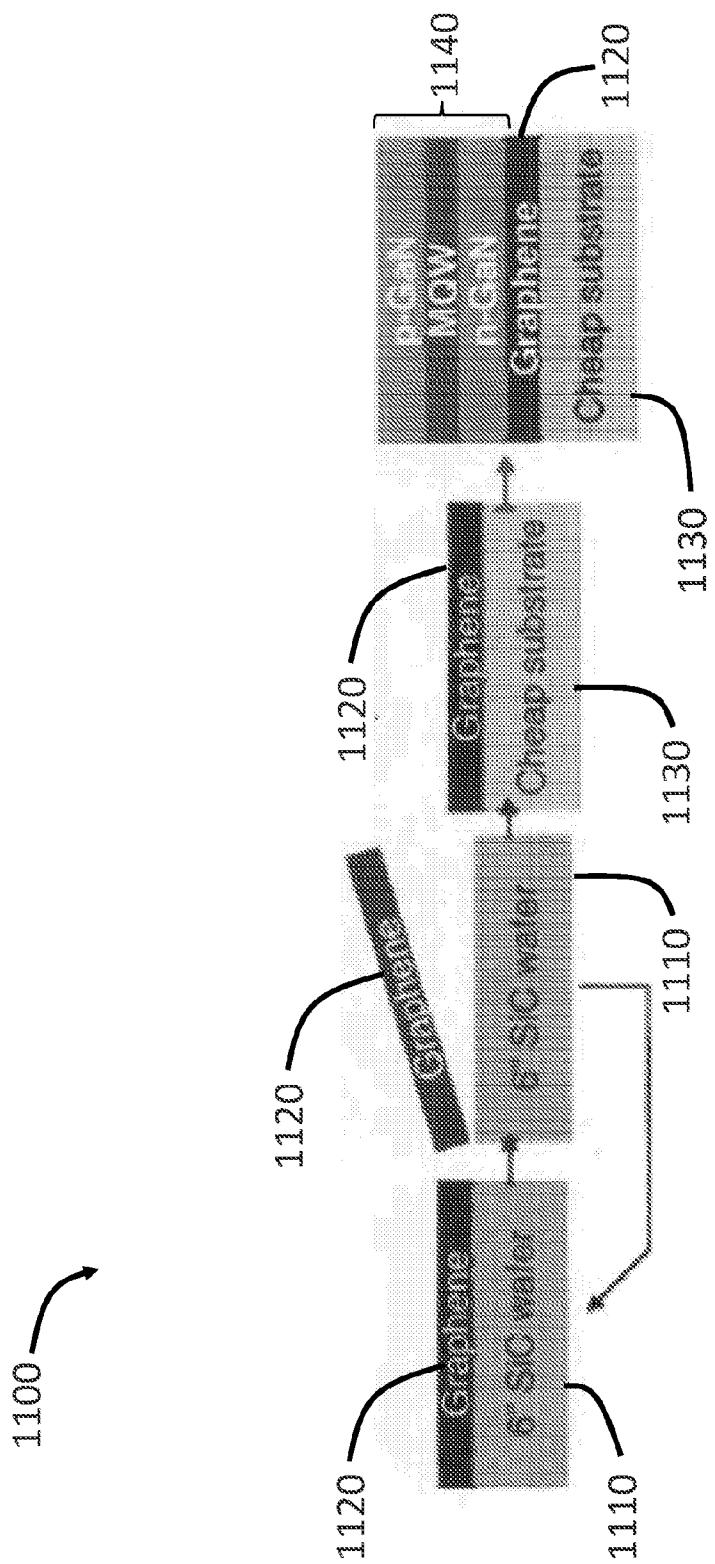


*FIG. 10A*

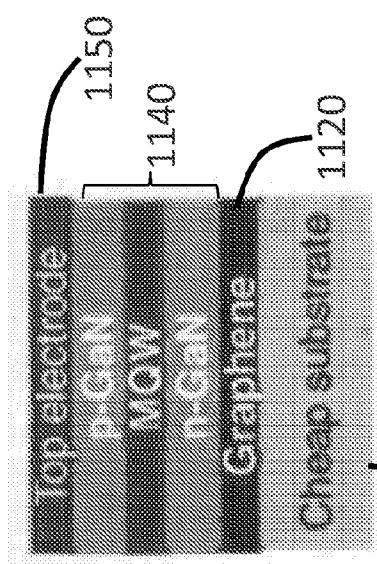


*FIG. 10B*

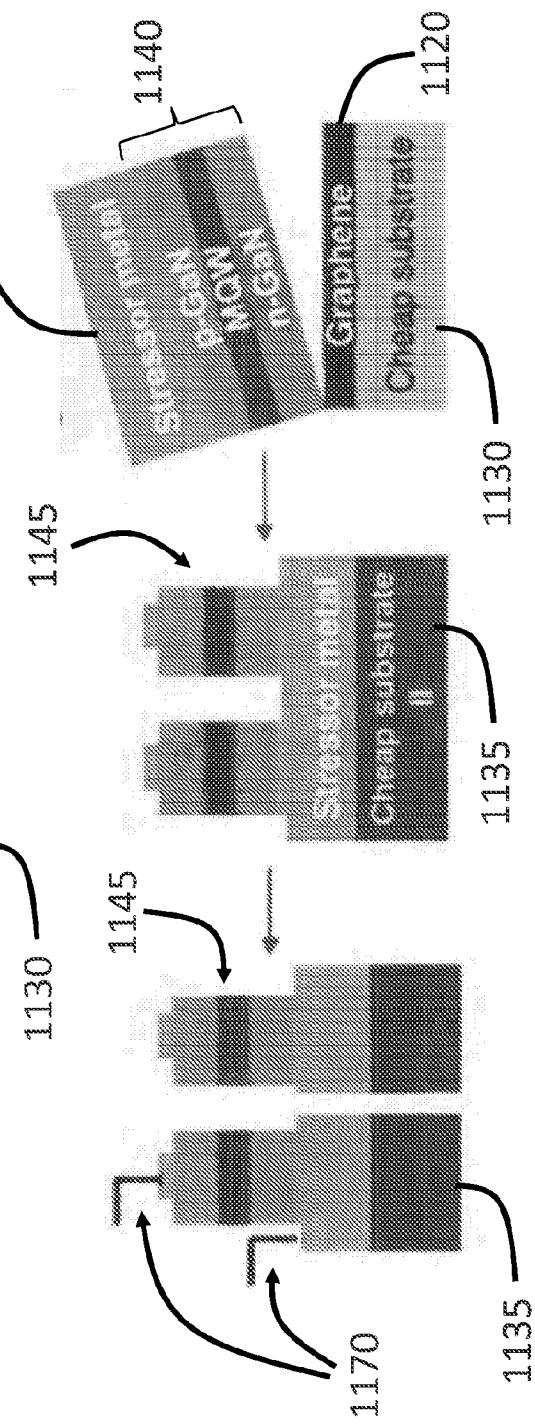




1100



**FIG. 11E**



**FIG. 11F**

**FIG. 11G**

**FIG. 11H**

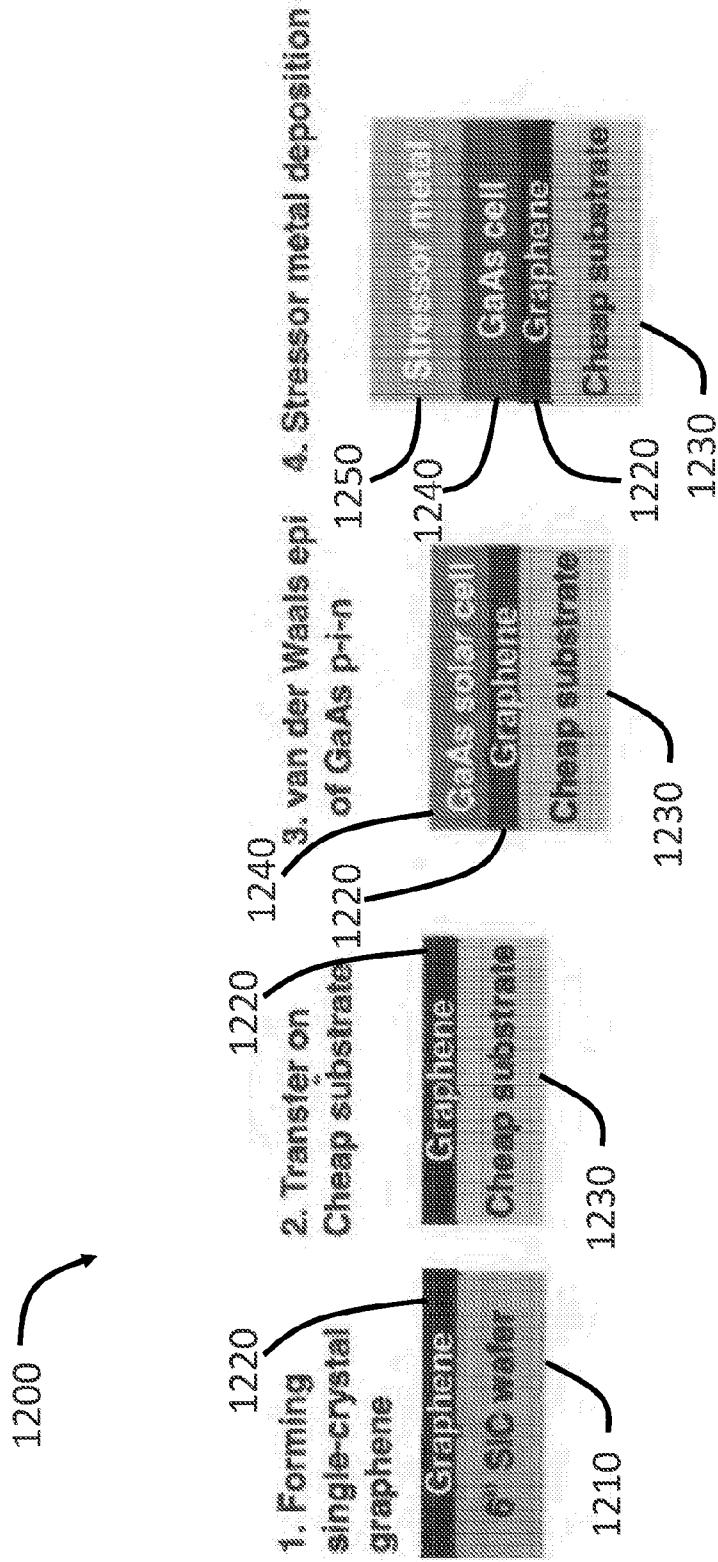
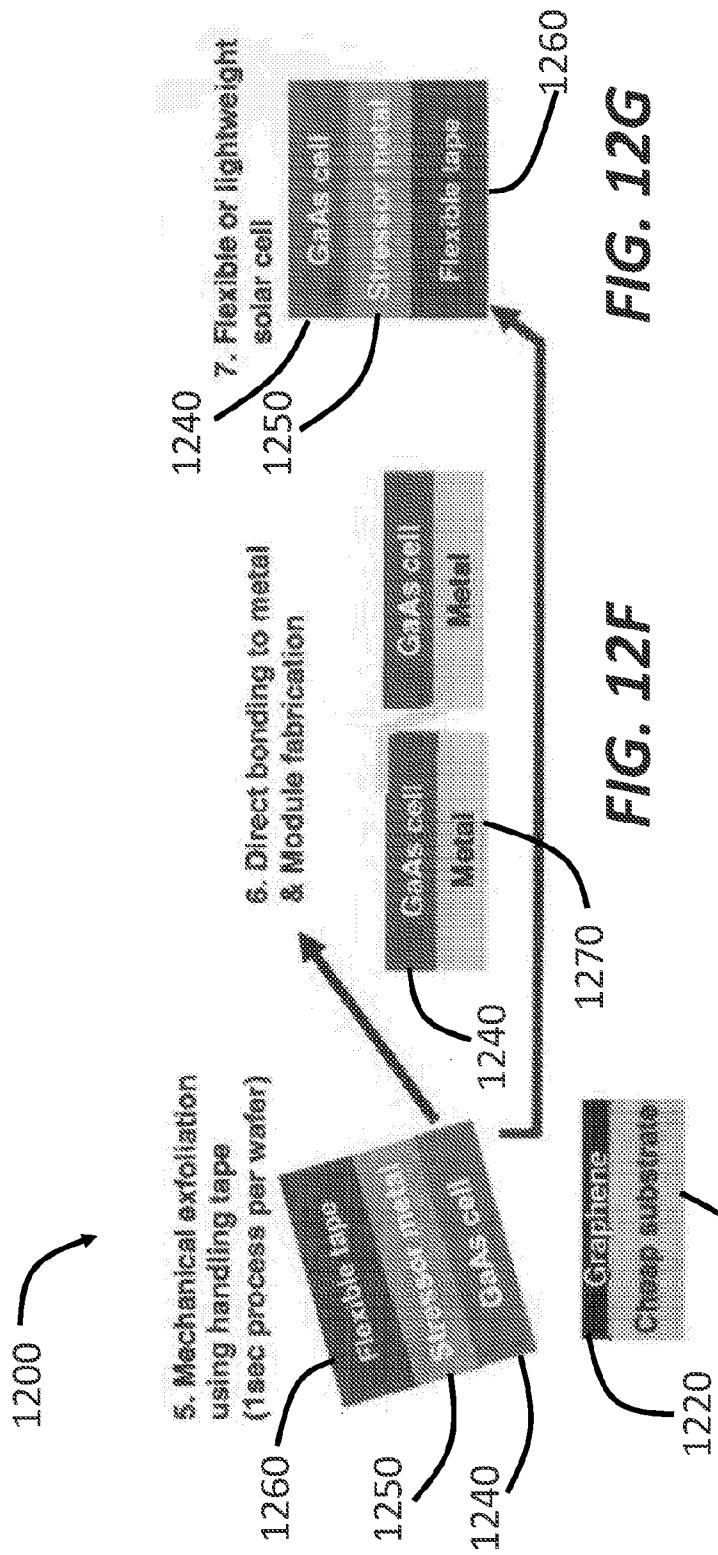
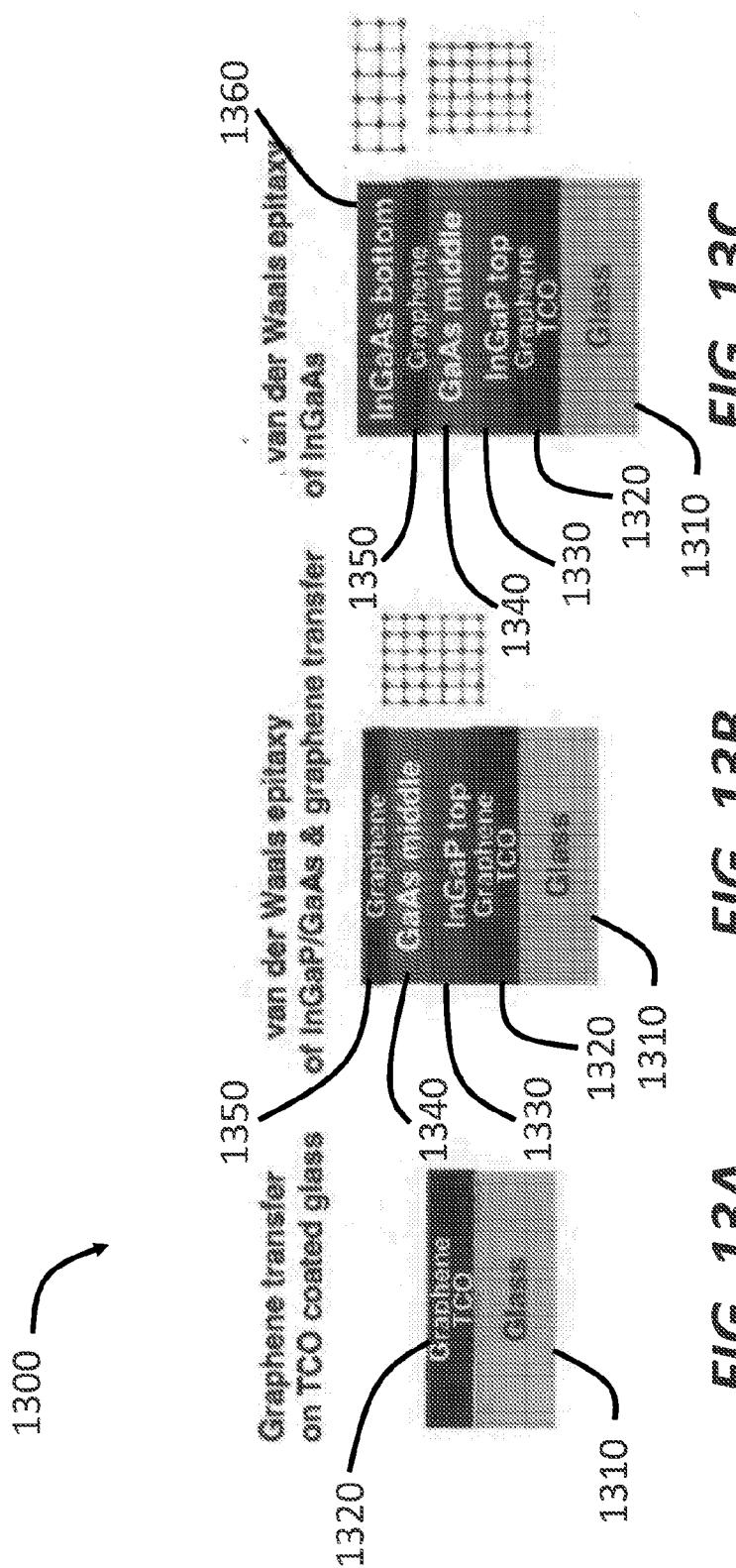


FIG. 12A FIG. 12B

FIG. 12C

FIG. 12D





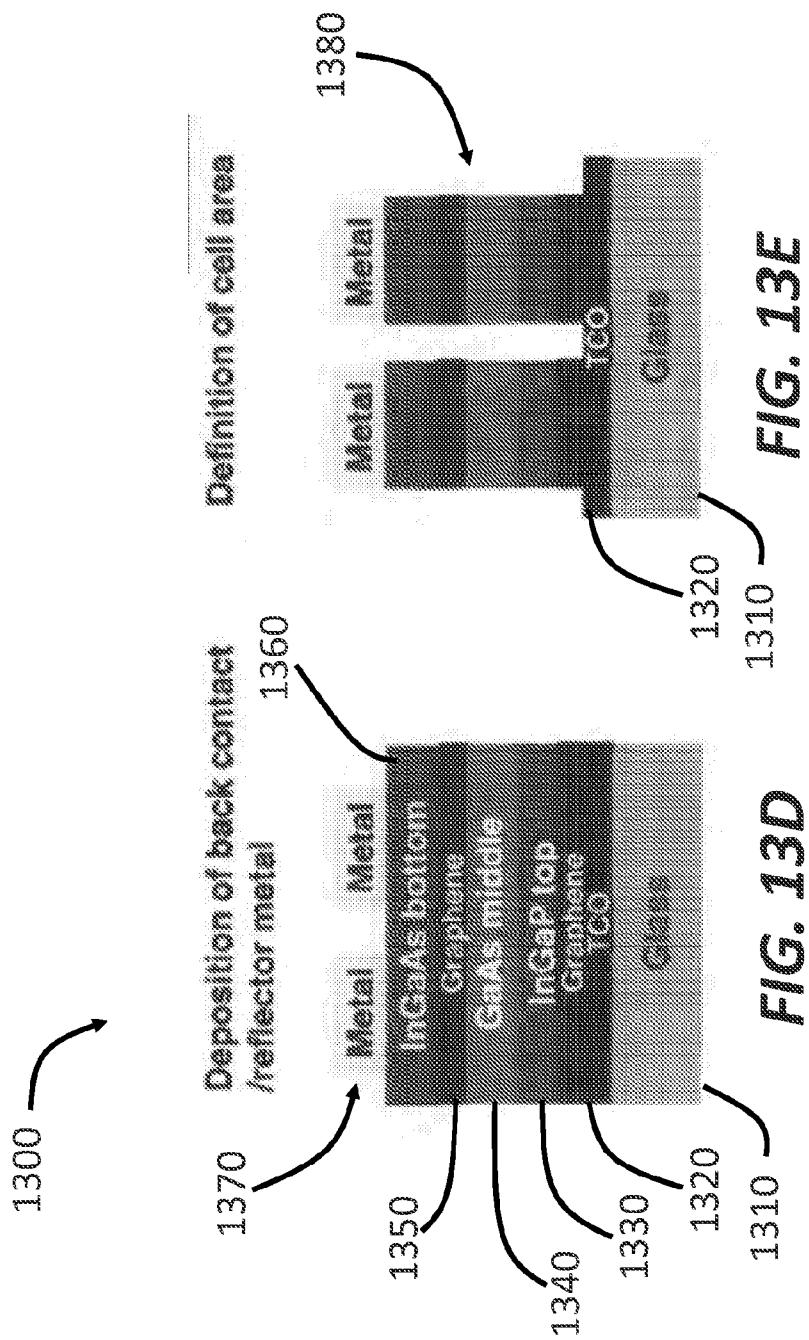
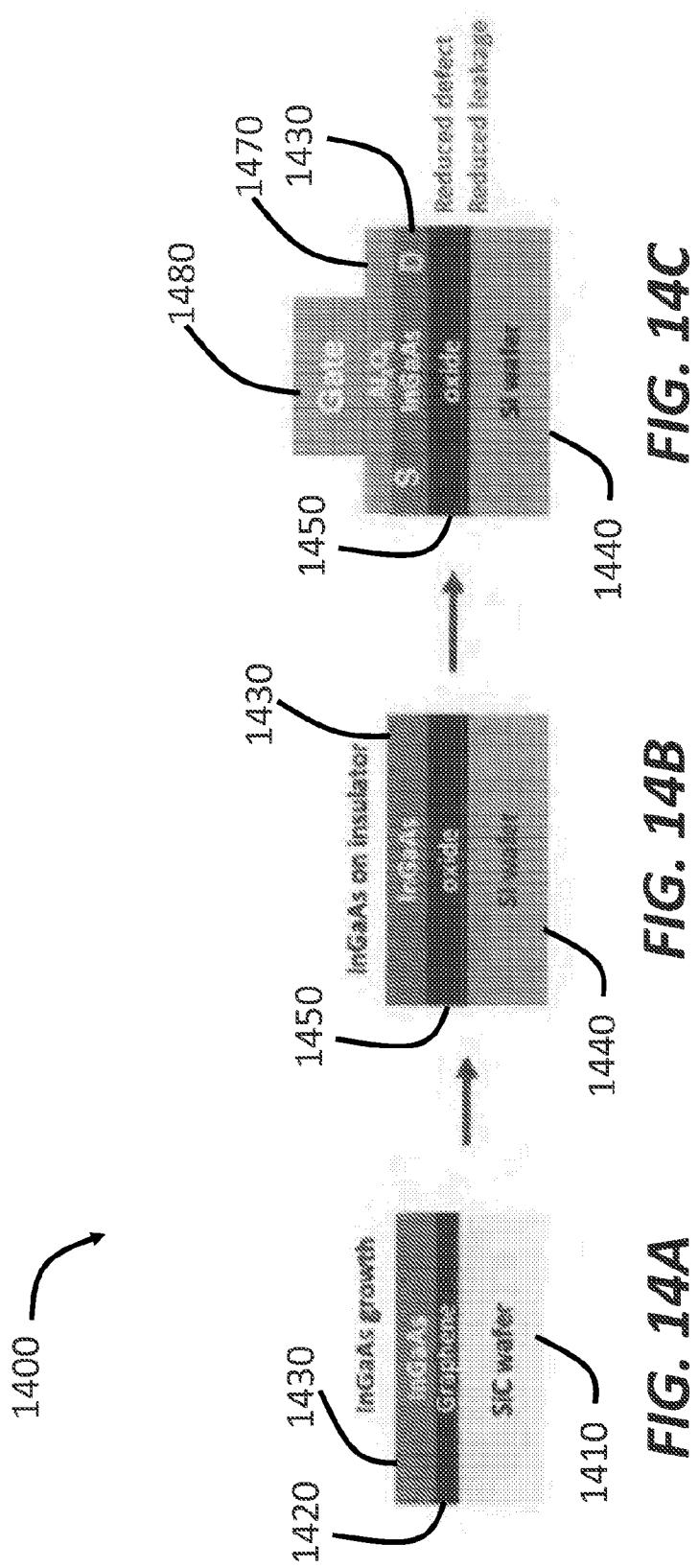
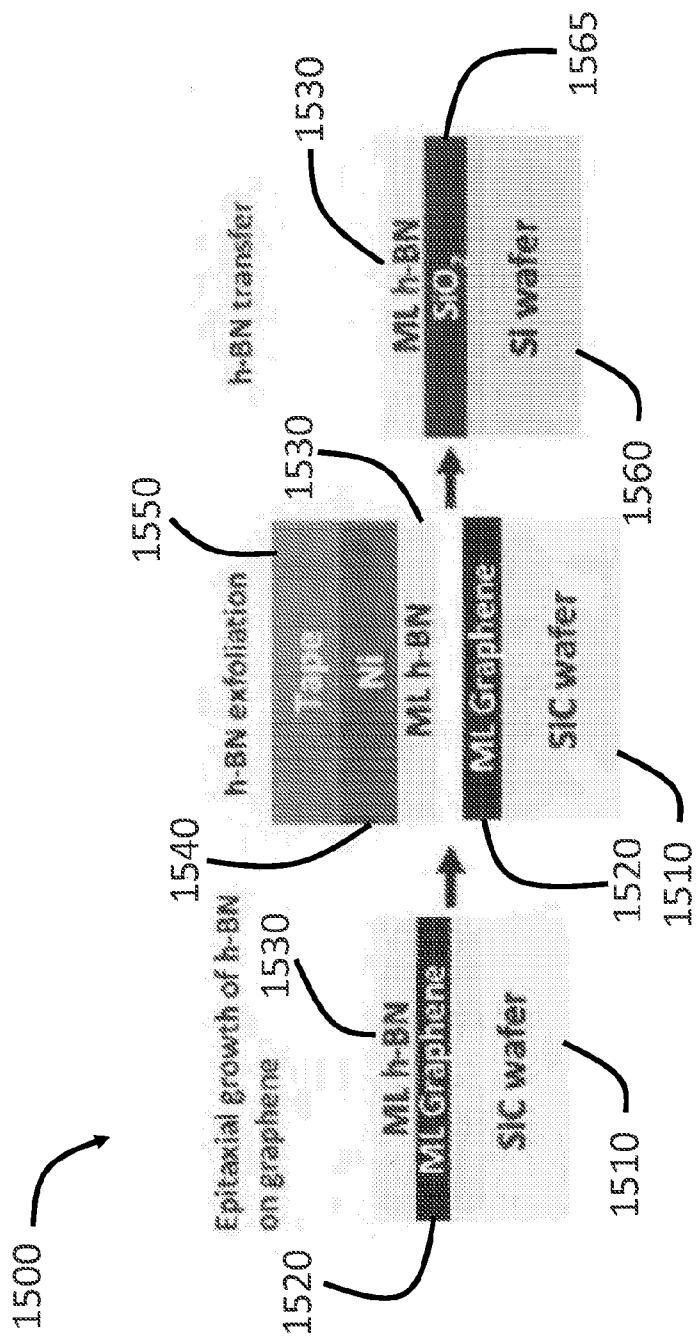


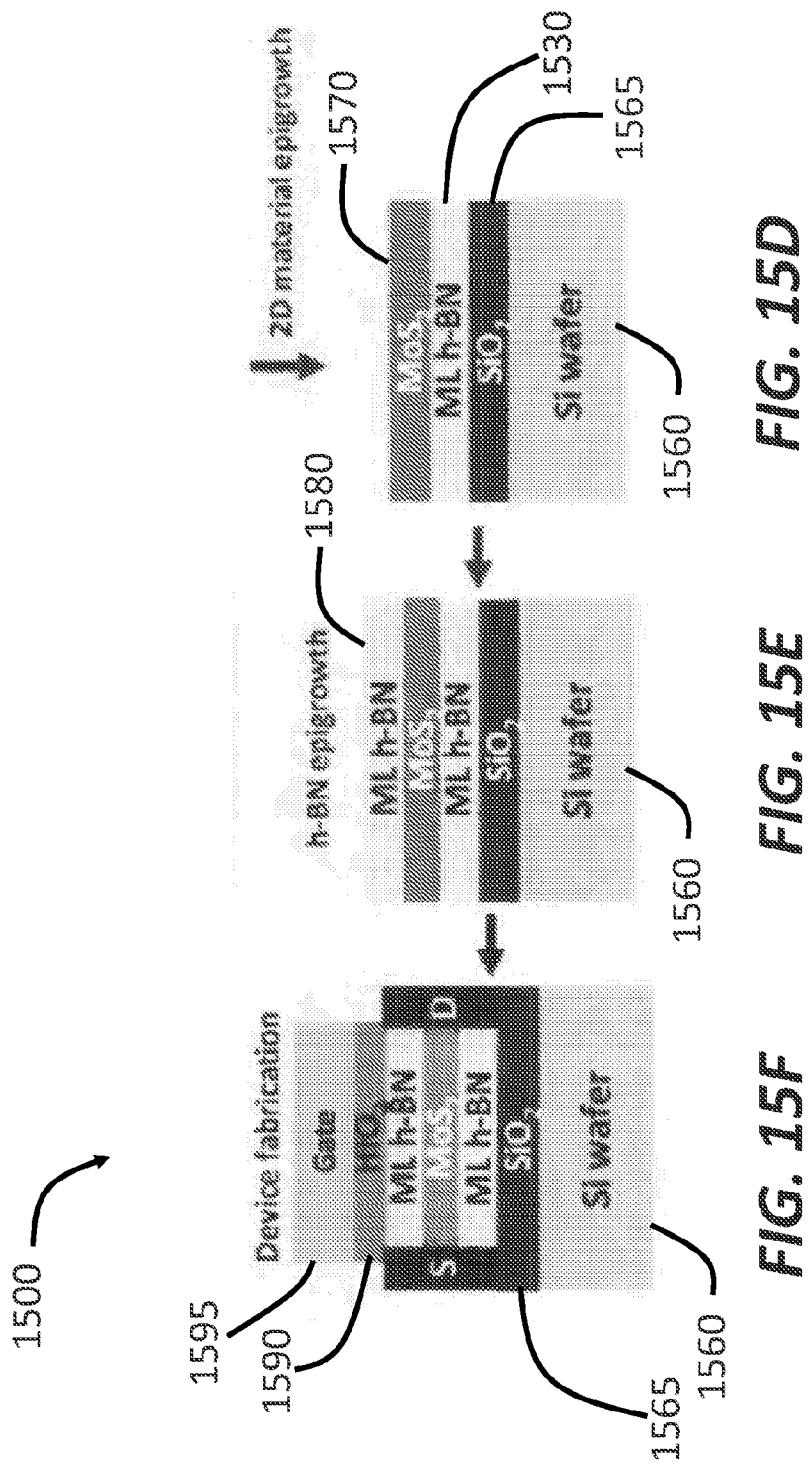
FIG. 13 D

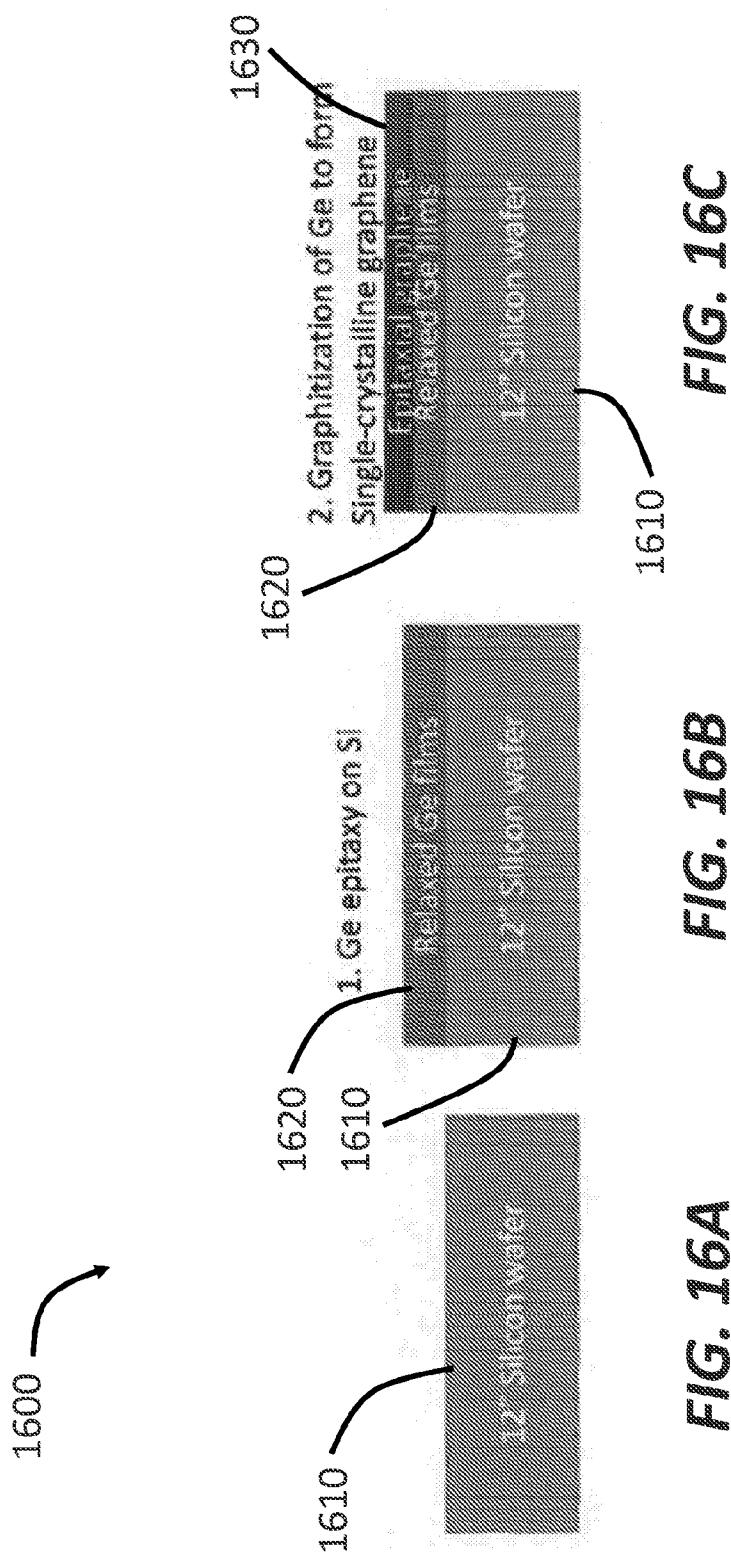
1310 FIG. 13E





**FIG. 15A**      **FIG. 15B**      **FIG. 15C**





*FIG. 16A*

*FIG. 16B*

*FIG. 16C*

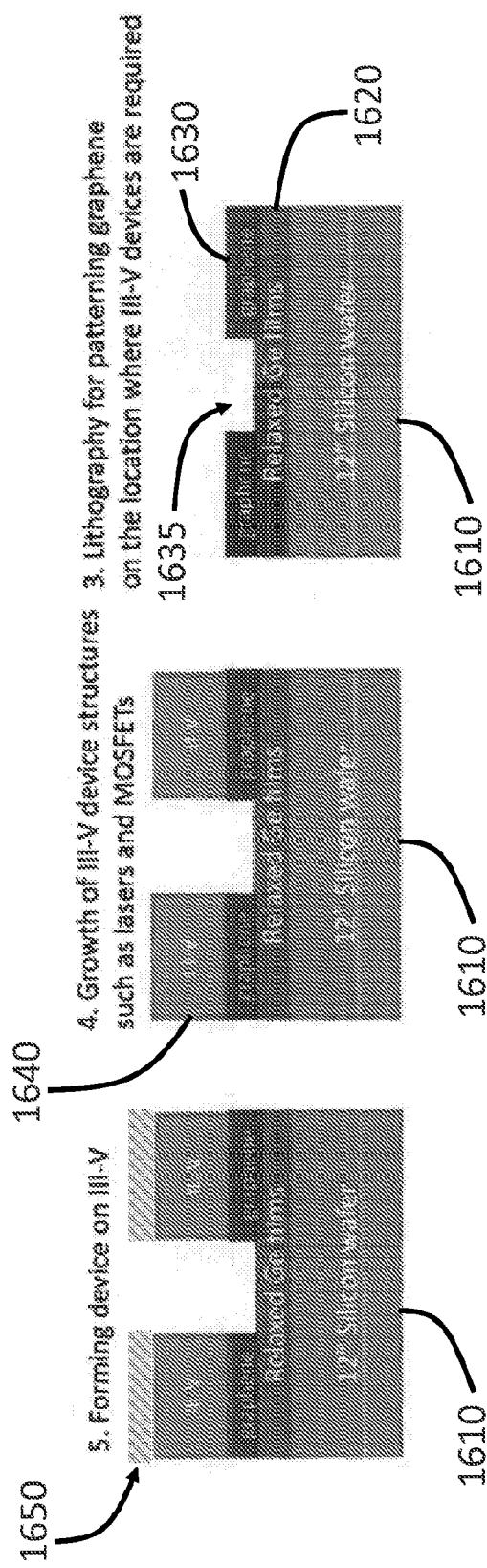


FIG. 16E

FIG. 16D

**INTERNATIONAL SEARCH REPORT**

International application No.

PCT/US16/50701

**A. CLASSIFICATION OF SUBJECT MATTER**

IPC(8) - H01L21/02, H01L 23/532, H01L 29/04 (2016.01)

CPC - H01L21/0242, H01L29/1606

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

IPC(8): H01L21/02, H01L 23/532, H01L 29/04 (2016.01)

CPC: H01L21/0242, H01L29/1606, H01L2221/68381

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSeer (US, EP, WO, JP, DE, GB, CN, FR, KR, ES, AU, IN, CA, INPADOC Data); EBSCO; Google; Google Scholar;  
KEYWORDS: silicon carbide, graphene, semiconductor, porous, single-crystalline, tape, epitaxial, exfoliation, transfer substrate

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2015/0084074 A1 (INTERNATIONAL BUSINESS MACHINES CORPORATION) March 26, 2015, figure 7, paragraphs [0003], [0007], [0035], [0038], [0040], [0042], [0046], [0048], [0053]-[0056], [0058], [0063], [0064]	19, 23
Y	US 2015/0228728 A1 (INTERNATIONAL BUSINESS MACHINES CORPORATION) August 13, 2015; paragraphs [0001], [0003], [0007], [0009]-[0011], [0040], [0046], [0047], [0061], [0063], [0064]	1-18, 20-22
Y	US 2011/0244662 A1 (LEE, E et al.); October 6, 2011; paragraph [0010], [0012], [0013]	4
Y	WO 2013/088948 A1 (KABUSHIKI KAISHA TOYOTA JIDOSHOEKI et al.) June 20, 2013; English translation, abstract; page 7, paragraph 2; page 8, paragraph 3	5,6,10,20-23
Y	US 2014/0220764 A1 (INTERNATIONAL BUSINESS MACHINES CORPORATION) August 7, 2014; paragraphs [0015], [0045], [0054]	7-9
Y	US 2013/0285016 A1 (WEI, L et al.) October 31, 2013; figures 1 & 11; paragraphs [0034], [0035], [0079], [0080]-[0082], [0088]	11, 20-23

Further documents are listed in the continuation of Box C.

See patent family annex.

* Special categories of cited documents:	
"A" document defining the general state of the art which is not considered to be of particular relevance	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"E" earlier application or patent but published on or after the international filing date	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"O" document referring to an oral disclosure, use, exhibition or other means	
"P" document published prior to the international filing date but later than the priority date claimed	"&" document member of the same patent family

Date of the actual completion of the international search

23 October 2016 (23.10.2016)

Date of mailing of the international search report

19 JAN 2017

Name and mailing address of the ISA/US

Mail Stop PCT, Attn: ISA/US, Commissioner for Patents  
P.O. Box 1450, Alexandria, Virginia 22313-1450  
Facsimile No. 571-273-8300

Authorized officer

Shane Thomas

PCT Helpdesk: 571-272-4300  
PCT OSP: 571-272-7774

**INTERNATIONAL SEARCH REPORT**

International application No.

PCT/US16/50701

**Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)**

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1.  Claims Nos.: because they relate to subject matter not required to be searched by this Authority, namely:
  
2.  Claims Nos.: because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
  
3.  Claims Nos.: because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

**Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)**

This International Searching Authority found multiple inventions in this international application, as follows:

See extra sheet.

1.  As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2.  As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.
3.  As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
  
4.  No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Group I: Claims 1-23

**Remark on Protest**

- The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- No protest accompanied the payment of additional search fees.

**INTERNATIONAL SEARCH REPORT**

International application No.

PCT/US16/50701

-\*\*\*-Continued from Box No. III Observations where unity of invention is lacking-\*\*\*-

This application contains the following inventions or groups of inventions which are not so linked as to form a single general inventive concept under PCT Rule 13.1. In order for all inventions to be examined, the appropriate additional examination fee must be paid.

Group I: Claims 1-23 are directed towards a method of manufacturing a semiconductor device comprising forming a single-crystalline film on a graphene layer.

Group II: Claims 24 are directed towards a method of semiconductor processor comprising disposing a flexible tape on a stressor layer.

The inventions listed as Groups I-II do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons:

The special technical features of Group I include at least forming a single-crystalline film on the graphene layer; forming a plurality of holes in the graphene monolayer; removing the first single-crystalline layer of semiconductor material from the graphene monolayer; forming a second single-crystalline layer of semiconductor material on the graphene monolayer, the semiconductor substrate acting as a seed for the second single-crystalline layer of semiconductor material; and removing the second single-crystalline layer of semiconductor material from the graphene monolayer, which are not present in Group II.

The special technical features of Group II include at least depositing a stressor layer on the semiconductor layer, the stressor layer causing propagation of a crack between the semiconductor layer and the graphene layer; and disposing a flexible tape on the stressor layer; and pulling the semiconductor layer and the stressor layer off the graphene layer with the flexible tape, which are not present in Group I.

The common technical features shared by Groups I-II are a method of semiconductor processing, the method comprising: forming a graphene layer on a first substrate; and transferring the graphene layer from the first substrate to a second substrate.

However, these common features are previously disclosed by US 2014/0001152 A1 to GRAPHENEAE, S.A. (hereinafter "Graphenea"). Graphenea discloses a method of semiconductor processing (method of manufacturing a graphene monolayer on insulating substrates from CVD graphene synthesis; Abstract), the method comprising: forming a graphene layer on a first substrate (a graphene layer deposited at the bottom of a metal foil; Abstract); and transferring the graphene layer from the first substrate to a second substrate (transferring the top graphene layer onto a substrate via a sacrificial protective layer; Abstract).

Since the common technical features are previously disclosed by the Graphenea reference, these common features are not special and so Groups I-II lack unity.