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Lane, Austin, TX 78729 (US). CHEN, Mary; 3606 Normandy Ridge Lane, Austin, TX 78759 (US).

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(74) Agent: APPERLEY, Elizabeth, A.; Advanced Micro Devices, Inc., 5204 East Ben White Boulevard, M/S 562, Austin, TX 78741 (US).

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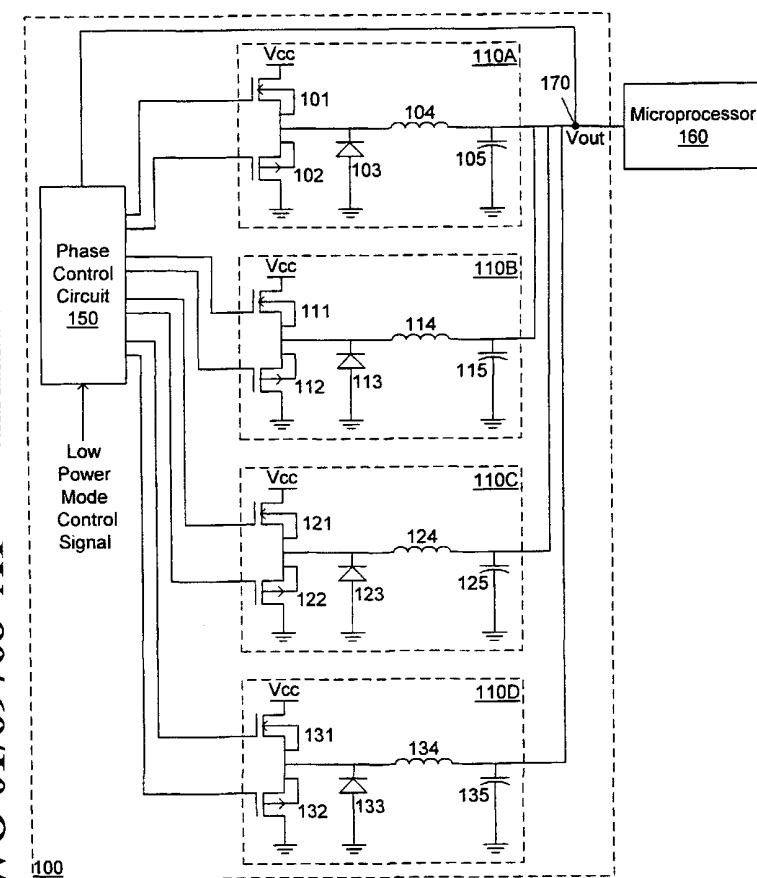
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(71) Applicant: ADVANCED MICRO DEVICES, INC.
[US/US]; One AMD Place, Mail Stop 68, Sunnyvale, CA 94088-3453 (US).

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(54) Title: IMPROVED EFFICIENCY OF A MULTIPHASE SWITCHING POWER SUPPLY DURING LOW POWER MODE



(57) Abstract: A multiphase power supply that minimizes losses during a low power mode. In a particular embodiment, a multiphase power supply may include a plurality of switching regulators coupled in parallel with respect to one another. The multiphase power supply further comprises a phase control circuit coupled to each of the switching regulators. The phase control circuit is configured to generate a plurality of control signals for controlling the switching of the switching regulators so that they are out of phase with respect to one another. During the low power mode of operation of the microprocessor, the phase control circuit is configured to selectively suspend operation of a subset of switching regulators by removing or disabling at least one of the plurality of control signals to each of the subset of switching regulators.

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TITLE: IMPROVED EFFICIENCY OF A MULTIPHASE SWITCHING POWER SUPPLY DURING LOW POWER MODE

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BACKGROUND OF THE INVENTION1. Technical Field

10 The present invention relates to the field of power supplies, and more particularly to multiphase switching power supplies.

2. Background Art

15 Power supplies are used in various types of devices. There are many specialized types of power supply circuits with various advantages and disadvantages. Microprocessors in computers may require a power supply circuit that regulates a high level of current while maintaining a high level of efficiency.

20 One such type of specialized power supply circuit is a switching regulator. Switching regulators typically provide an output with a lower voltage than the unregulated input while at the same time providing an output with a higher current than the current drawn from the unregulated supply. This is accomplished by a passive transistor that is constantly switching between the saturation mode and the nonconducting mode. Because the passive transistor is either in saturation or not conducting, there is very low power dissipation. A switching regulator therefore can regulate a high amount of current at a high efficiency rate.

25 A disadvantage with switching regulators is known as the "ripple effect." The ripple effect refers to ripples that are periodic variations in the output voltage that have to be smoothed out in order to generate a genuine DC current. The ripple effect problem may be reduced or eliminated by coupling multiple switching regulators in parallel and operating them such that they are out of phase with respect to one another. This configuration is known as a multiphase switching regulator. A multiphase switching regulator typically produces a high current output with high efficiency while at the same time reducing ripple. Consequently, a multiphase switching regulator is a popular choice for use in a power supply circuit where high levels of current and efficiency are desired.

30 Many microprocessors are configured to selectively operate in a low power mode of operation. During low power mode, the microprocessor may be configured to power down certain functional blocks (e.g. those that are inactive) and/or reduce the frequency of its internal clock(s). Powering down certain portions of the microprocessor and/or reducing clocking frequencies may advantageously reduce power consumption. When the microprocessor returns to a normal mode of operation, the microprocessor draws relatively higher amounts of current.

35 Unfortunately, when the microprocessor is operating in low power mode, a multiphase switching regulator becomes more inefficient as a percentage of the total current generated. This is because the transistors in the switching regulators continue to switch at the same frequency as during the normal mode of operation. Since the transistors are switching at the same frequency, the capacitive losses associated with the switching are the same during the low power and normal modes of operation. However, since less current is drawn during the low power mode of operation, the switching becomes more inefficient as a percentage of the total current generated. Therefore, an improved multiphase 40 power supply circuit is desired that will lower switching-related power losses during low power modes of operation.

DISCLOSURE OF INVENTION

The problems outlined above may in large part be solved by a power supply that lowers power losses during a low power mode of operation. In one embodiment, a multiphase power supply includes a plurality of switching regulators coupled in parallel with respect to one another. Each switching regulator may operate concurrently, and 5 each may be controlled out of phase with respect to one another. In a particular embodiment, each switching regulator may be a synchronous switching regulator. The multiphase power supply further includes a phase control circuit coupled to the plurality of switching regulators. The phase control circuit is configured to selectively suspend operation of at least one of the switching regulators during a low power mode of operation. The phase control circuit may further be configured to control the switching of the switching regulators so that they are out of phase with respect 10 to one another.

Various embodiments of the multiphase power supply may advantageously allow for relatively high current capabilities during a normal mode of operation, while minimizing losses during the low power mode of operation. By suspending operation of a subset of switching regulators during the low power mode of operation, capacitive switching losses associated with the transistors of the suspended switching regulators may be eliminated. 15 Therefore, overall efficiency of the power supply may be improved.

BRIEF DESCRIPTION OF DRAWINGS

A better understanding of the present invention can be obtained when the following detailed description of the preferred embodiment is considered in conjunction with the following drawings, in which:

20 Figure 1 illustrates a particular embodiment of a multiphase power supply;

Figure 2 is a timing diagram illustrating the duty cycles of selected transistors of Figure 1 during a normal mode of operation;

Figure 3 is a timing diagram illustrating reduced duty cycles of selected transistors of Figure 1 during a normal mode of operation;

25 Figure 4 is a timing diagram illustrating the duty cycles of selected transistors of Figure 1 during a low power mode of operation; and

Figure 5 illustrates another embodiment of a multiphase power supply.

While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof are shown by way of example in the drawings and will herein be described in detail. It should be 30 understood, however, that the drawings and detailed description thereto are not intended to limit the invention to the particular form disclosed, but on the contrary, the intention is to cover all modifications, equivalents and alternatives falling within the spirit and scope of the present invention as defined by the appended claims.

MODE(S) FOR CARRYING OUT THE INVENTION

35 Figure 1 illustrates a particular embodiment of a multiphase power supply 100. Multiphase power supply 100 comprises a plurality of synchronous switching regulators designated as 110A, 110B, 110C and 110D. Synchronous switching regulators 110A-D may, individually or collectively be referred to as switching regulator 110 or switching regulators 110, respectively. Switching regulators 110 are coupled to provide power to a microprocessor 160 at node 170. Multiphase power supply 100 further comprises a phase control circuit 150

coupled to each of switching regulators 110. It is important to note that different embodiments may comprise more or less than four switching regulators.

In the illustrated embodiment each switching regulator 110 includes a pair of transistors (e.g., transistors 101 and 102, transistors 111 and 112, etc.) coupled between a power supply terminal Vcc and ground. Each 5 switching regulator 110 further includes a diode (e.g., diodes 103, 113, etc.), an inductor (e.g. inductors 104, 114, etc.) and a capacitor (e.g., capacitors 105, 115, etc.). It is noted that other specific circuit arrangements may be employed to implement each switching regulator 110.

Phase control circuit 150 is configured to generate a plurality of control signals for controlling the states of the transistors in switching regulators 110 such that the switching regulators 110 operate out of phase with respect 10 to one another. In a particular embodiment, phase control circuit 150 may include a Semtech SC1144 integrated circuit. As will be described in further detail below, phase control circuit 150 also includes further circuitry to selectively suspend operation of a subset of switching regulators 110 during a low power mode of operation to thereby allow for improved efficiency.

Figures 2-4 illustrate aspects of the operation of multiphase power supply 100. Figures 2 and 3 are timing 15 diagrams illustrating exemplary duty cycles associated with transistors 101, 111, 121 and 131 during a normal mode of operation. Figure 4 is a timing diagram illustrating exemplary duty cycles associated with transistors 101, 111, 121 and 131 during a low power mode of operation.

Turning collectively to Figures 1 and 2, phase control circuit 150 activates (i.e. turns on) transistors 101, 111, 121 and 131, respectively, during different phases of operation. During a first phase of operation ("phase 1"), 20 transistor 101 is turned on while transistors 111, 121 and 131 are turned off. Since each switching regulator 110 is embodied as a synchronous regulator, when transistor 101 is turned on, transistor 102 is turned off (in response to a corresponding control signal from phase control circuit 150). Thus, during phase 1, current flows from Vcc through transistor 101 and inductor 104 to charge capacitor 105. Also during phase 1, transistors 111, 121 and 131 are turned off, and transistors 112, 122 and 132 are turned on.

25 During the next phase of operation ("phase 2"), phase control circuit 150 turns off transistor 101 and turns on transistor 102. When transistor 102 is turned on and transistor 101 is turned off, current may continue to temporarily flow through inductor 104 to charge capacitor 105 since current flow through inductor 104 cannot change instantaneously. Transistor 102 provides a return path for this current.

Also during phase 2, transistor 111 of switching regulator 110B is turned on and transistor 112 is turned off. 30 Consequently, similar to the previous discussion, capacitor 115 is charged by current flow from Vcc through transistor 111. Subsequent operations of switching regulators 510C and 510D during phases 3 and 4 are similar.

Phase control circuit 150 may be further configured to monitor the output voltage, Vout, at node 170 via a feedback control signal and adjust accordingly the duty cycle of transistors 101, 111, 121 and 131 to maintain a constant voltage level. Figure 3 illustrates an exemplary situation where the duty cycle of transistors 101, 111, 121 and 131 of Figure 1 is lessened due to, for example, reduced current draw by microprocessor 160. The duty cycle of transistors 101, 111, 121 and 131 would increase relative to the example of Figure 2 if there were a decreased output voltage at node 170, i.e., due to increased current draw by microprocessor 160.

As stated previously, microprocessor 160 is configured to operate in a low power mode of operation. During such mode of operation, microprocessor 160 requires less current. The low power mode of operation may be

controlled by, for example, a power management unit (not shown) which detects certain system inactivity, as desired. Phase control circuit 150 is configured to selectively suspend operation of a subset of switching regulators 110 (e.g. switching regulators 110B, 110C and 110D) upon assertion of a low power mode control signal which indicates that microprocessor 160 is currently operating in a low power mode. The low power mode control signal may be received 5 from the power management unit. As depicted in Figure 4, in this embodiment, phase control circuit 150 suspends operation of switching regulator circuits 110B, 110C and 110D during the low power mode by removing (or otherwise driving or disabling) the control signals provided to the associated switching transistors 111, 112, 121, 122, 131 and 132 such that the transistors are held in an off state. During this mode, switching regulator 110A operates in its normal manner as described previously.

10 Figure 5 illustrates another embodiment of a multiphase power supply 500. Multiphase power supply 500 of Figure 5 differs from multiphase power supply 100 of Figure 1 in that transistors 102, 112, 122 and 132 have been omitted. Thus, the switching regulators, e.g. 510A, 510B, 510C and 510D, of Figure 5 are not synchronous regulators. A respective diode i.e., diode 503, 513, 523 or 533, of each switching regulator 510 provides a return path for current to flow when the associated transistor, i.e., transistor 501, 511, 521 or 531, is turned off.

15 Various embodiments of the multiphase power supply may advantageously allow for relatively high current capabilities during a normal mode of operation, while minimizing losses during the low power mode of operation. By suspending operation of a subset of switching regulators during the low power mode of operation, capacitive switching losses associated with the transistors of the suspended switching regulators may be eliminated. Therefore, overall efficiency of the power supply may be improved.

20 It is noted that while in the above described embodiments, a total of four switching regulators are depicted in each of the power supplies, other embodiments are possible where other numbers of switching regulators may be provided. Similarly, while in the above described embodiments during the low power mode of operation all but one of the switching regulators is suspended from operation, other embodiments are possible where any number of switching regulators may be suspended.

25 Numerous variations and modifications will become apparent to those skilled in the art once the above disclosure is fully appreciated. It is intended that the following claims be interpreted to embrace all such variations and modifications.

INDUSTRIAL APPLICABILITY

30 This invention is applicable to power supplies.

WHAT IS CLAIMED IS:

1. A power supply comprising:
 - a first switching regulator circuit (110A);
 - 5 a second switching regulator circuit (110B);
 - a phase control circuit (150) coupled to said first switching regulator circuit and to said second switching regulator circuit; wherein said phase control circuit is configured to generate a plurality of switching control signals for controlling switching of said first and second switching regulator circuits; characterized in that said phase control circuit is configured to selectively suspend operation of said second
 - 10 switching regulator in response to receiving a signal indicative of a low power mode of operation.
2. A power supply comprising:
 - a first switching regulator circuit (110A);
 - a second switching regulator circuit (110B);
 - 15 a third switching regulator circuit (110C);
 - a fourth switching regulator circuit (110D);
 - a phase control circuit (150) coupled to said first switching regulator circuit, said second switching regulator circuit, said third switching regulator circuit and said fourth switching regulator circuit, wherein said phase control circuit is configured to generate a plurality of switching control signals for controlling
 - 20 switching of said first, second, third and fourth switching regulator circuits; characterized in that said phase control circuit is configured to selectively suspend operation of said second, third and fourth switching regulator circuits in response to receiving a signal indicative of a low power mode of operation.
- 25 3. The power supply as recited in either claim 1 or claim 2, wherein said phase control circuit (150) selectively suspends operation of said second switching regulator (110B) circuit during said low power mode of operation by disabling at least one of said plurality of control signals to said second switching regulator circuit.
4. The power supply as recited in any of the preceding claims, wherein each of said first and second switching
- 30 regulator circuits comprises a first transistor (101, 111) and a second transistor (102, 112), wherein said phase control circuit selectively activates and deactivates said first and second transistor with said control signals.
5. The power supply as recited in any of the preceding claims, wherein said phase control circuit (150) selectively activates and deactivates said first and second switching regulator circuits so that said first and second
- 35 switching regulator circuits are out of phase with respect to one another.
6. The power supply as recited in any of the preceding claims, wherein each of said first and second switching regulator circuits further comprises:

a capacitor (105, 115) coupled to receive charge from said first transistor in response to said first transistor being activated; and
an inductor (104, 114) coupled to said capacitor to provide current to said capacitor in response to said first transistor being deactivated.

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7. The power supply as recited in either claim 1 or claim 2, wherein each of said first and second switching regulator circuits (510A, 510B) comprises a first transistor (501, 511), wherein said phase control circuit selectively activates and deactivates said first transistor.

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8. The power supply as recited in claim 7, wherein said phase control circuit (150) selectively activates and deactivates said first and second switching regulator circuits (510A, 510B) so that said first and second switching regulator circuits are out of phase with respect to one another.

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9. The power supply as recited in claim 8, wherein each of said first and said second switching regulator circuits further comprises:

a capacitor coupled to receive charge from said first transistor in response to said first transistor being activated; and

an inductor coupled to said capacitor to provide current to said capacitor in response to said first transistor being deactivated.

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10. A computer system comprising:

a microprocessor;

a power supply as recited in any of claims 1-9 coupled to said microprocessor.

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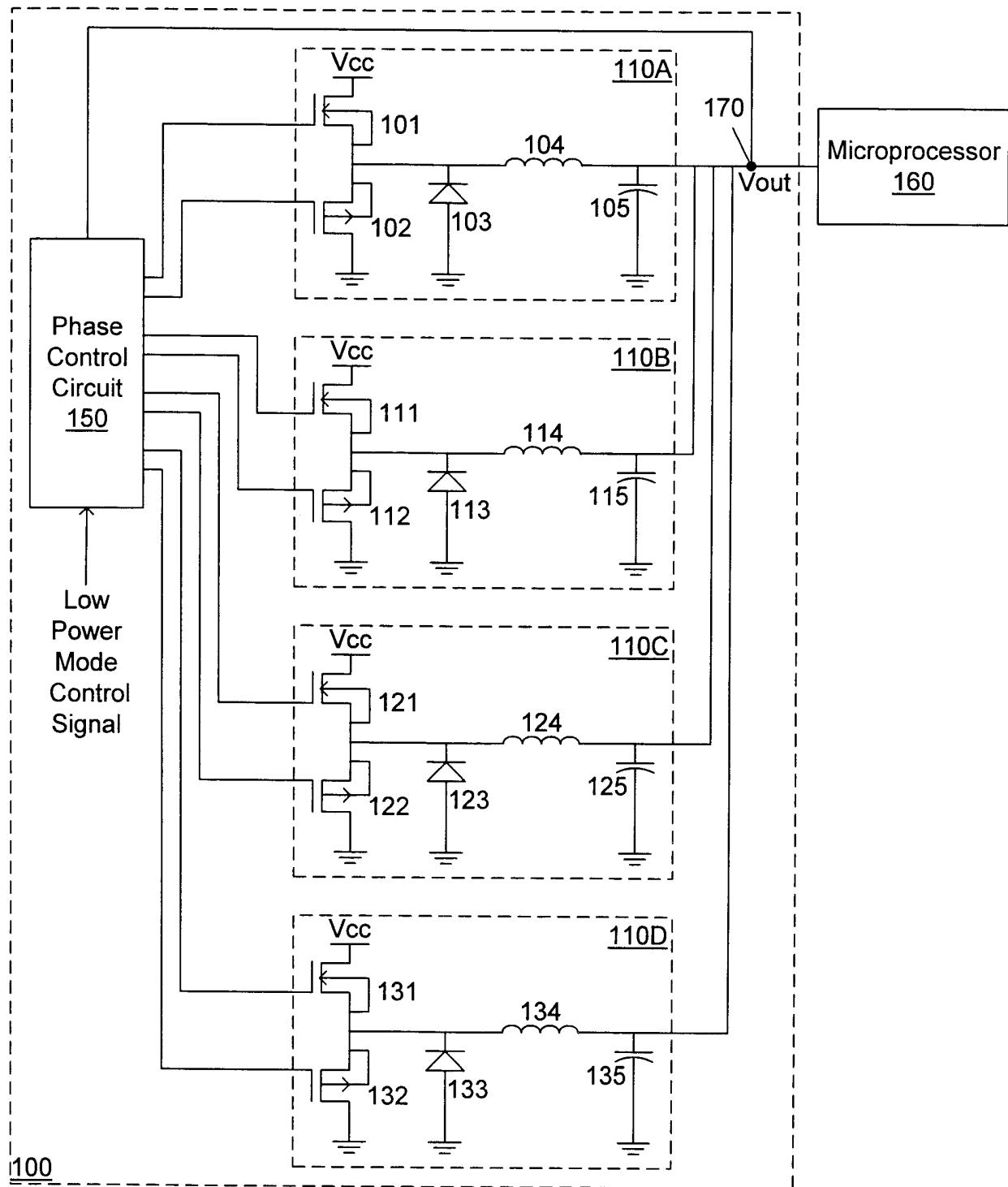


Fig. 1

2/5

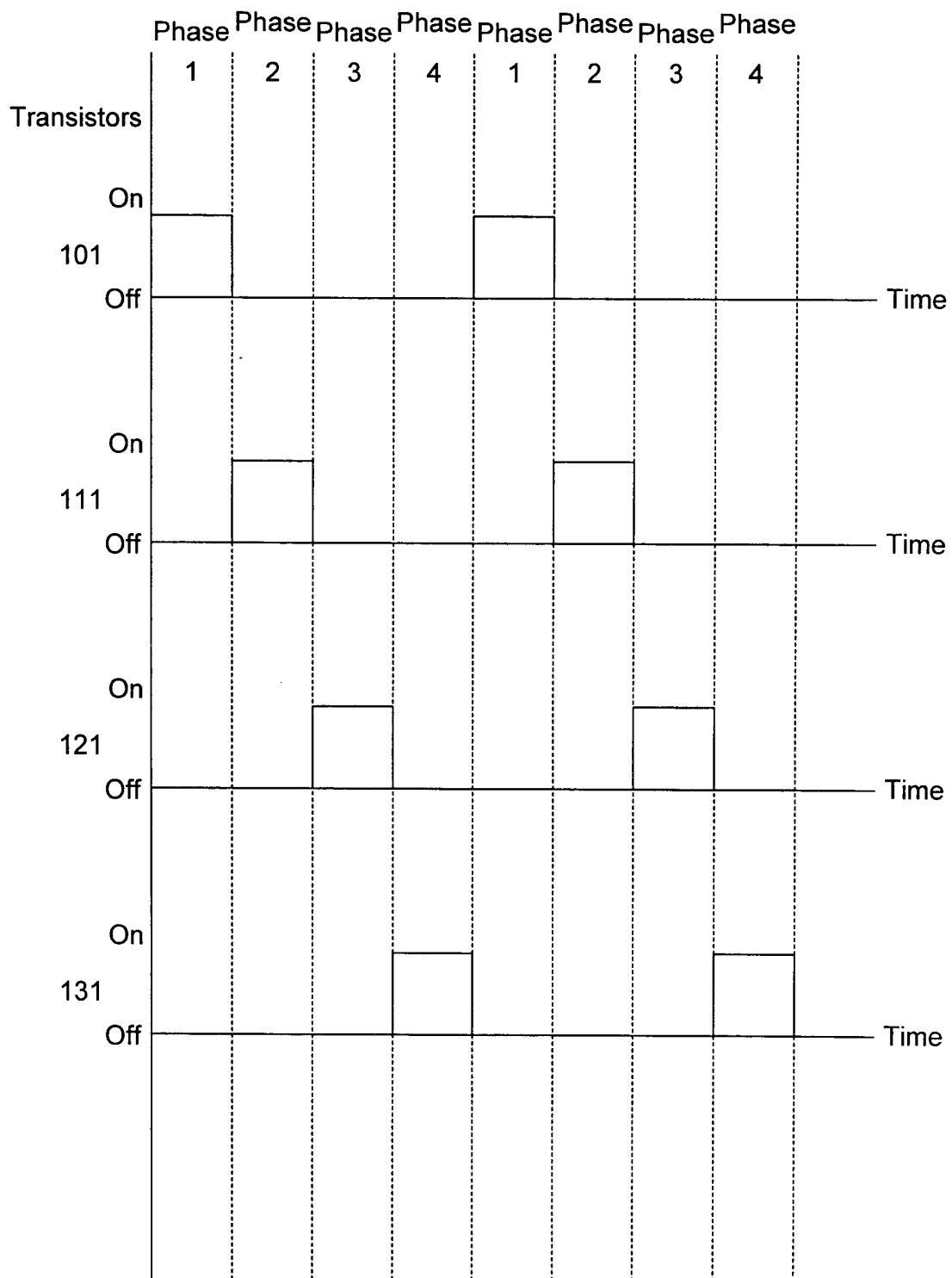


Fig. 2

3/5

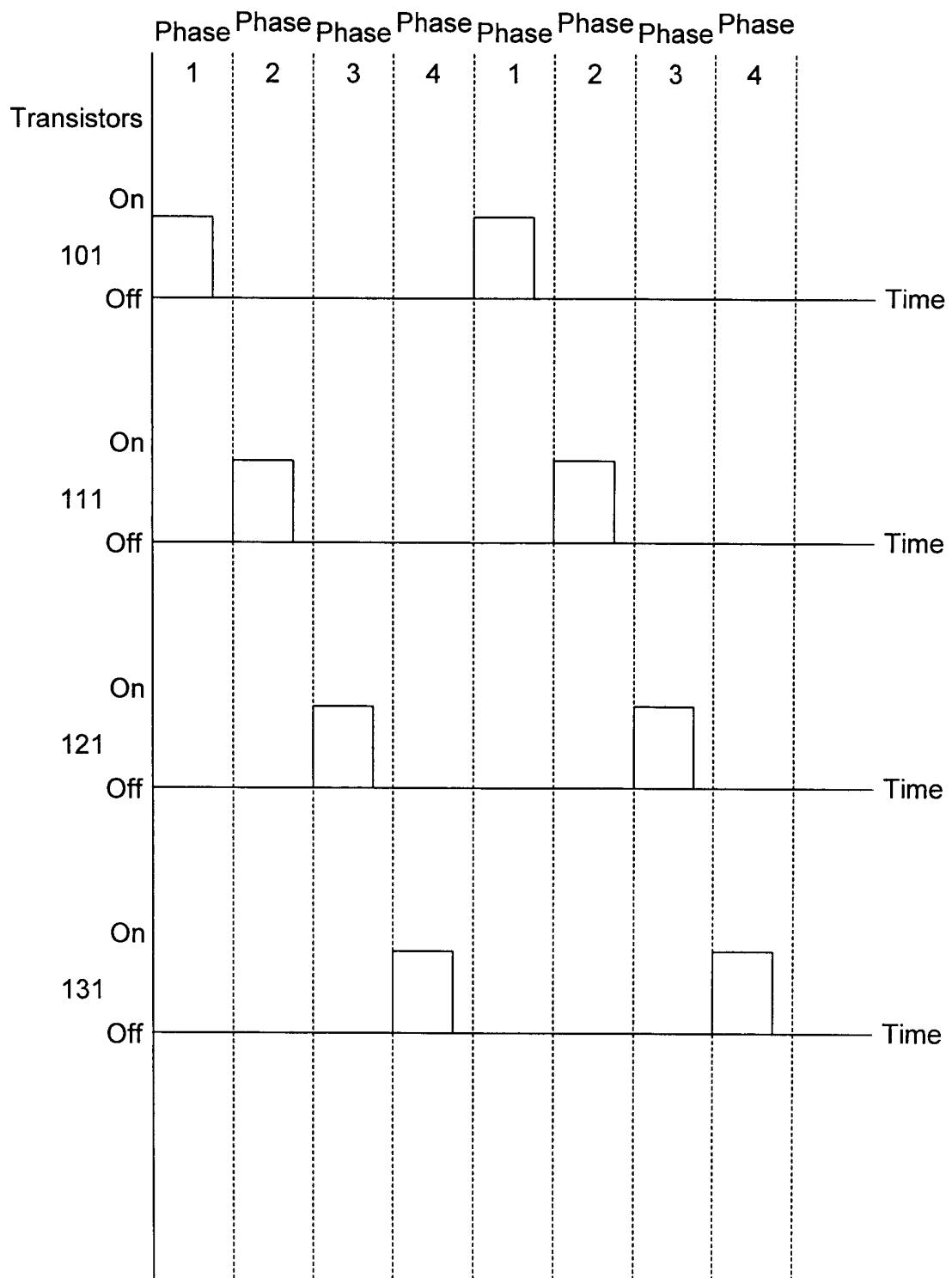


Fig. 3

4/5

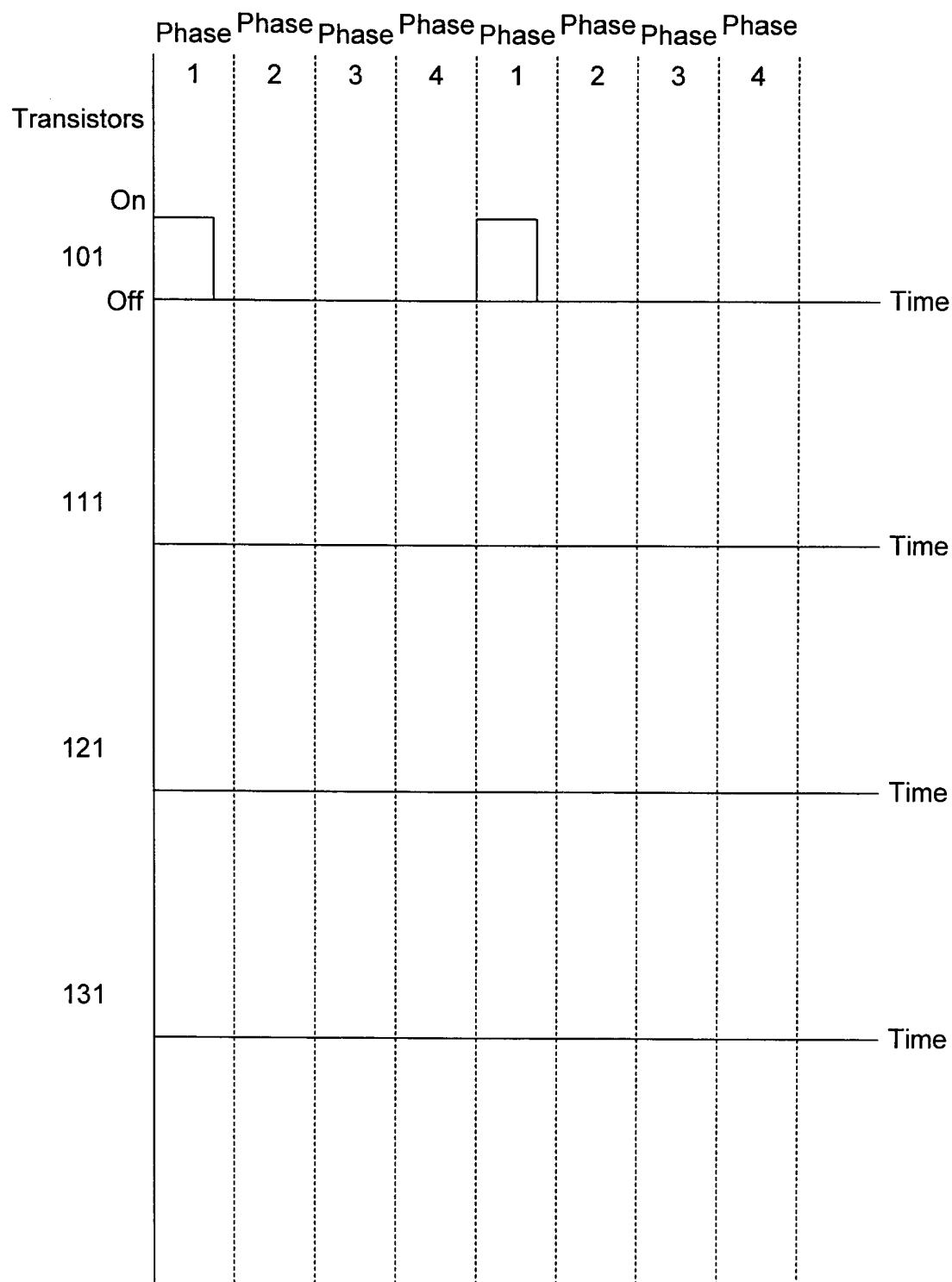


Fig. 4

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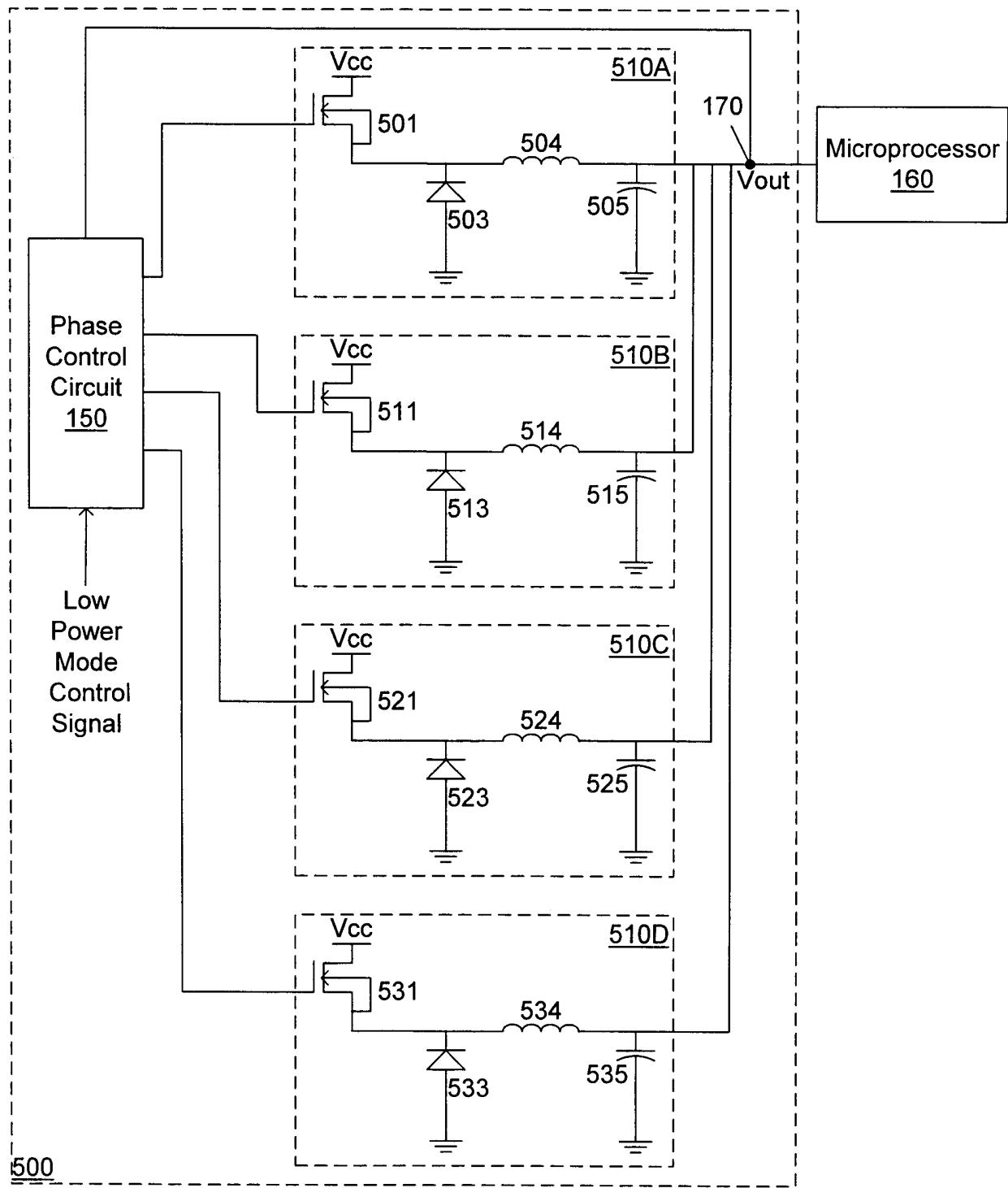


Fig. 5

INTERNATIONAL SEARCH REPORT

Int. Application No

PCT/US 00/31957

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H02M3/158

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 031 747 A (ILIC MILAN Z ET AL) 29 February 2000 (2000-02-29) column 5, line 65 -column 7, line 52; figures 3-6 -----	1-5,7,8, 10 6,9
Y	GUICHAO HUA ET AL: "SOFT-SWITCHING PWM TECHNIQUES AND THEIR APPLICATIONS" PROCEEDINGS OF THE EUROPEAN CONFERENCE ON POWER ELECTRONICS AND APPLICATIONS, GB, LONDON, IEE, vol. CONF. 5, 13 September 1993 (1993-09-13), pages 87-92, XP000427005 figures 1,2 ----- -/-	6,9

Further documents are listed in the continuation of box C.

Patent family members are listed in annex.

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Date of the actual completion of the international search

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Name and mailing address of the ISA
European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,
Fax: (+31-70) 340-3016

Authorized officer

Gentili, L

INTERNATIONAL SEARCH REPORT

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	<p>CHOI B: "COMPARATIVE STUDY ON PARALLELING SCHEMES OF CONVERTER MODULES FOR DISTRIBUTED POWER APPLICATIONS" IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, US, IEEE INC. NEW YORK, vol. 45, no. 2, 1 April 1998 (1998-04-01), pages 194-199, XP000740812 ISSN: 0278-0046 figure 3</p> <p>---</p>	1,2,6
A	<p>ZHOU X ET AL: "INVESTIGATION OF CANDIDATE VRM TOPOLOGIES FOR FUTURE MICROPROCESSORS" APEC 98, ANAHEIM, CA, FEBR. 15 - 19, 1998, NEW YORK, NY: IEEE, US, 15 February 1998 (1998-02-15), pages 145-150, XP000873661 ISBN: 0-7803-4341-7 figures 8,9</p> <p>-----</p>	1-10

INTERNATIONAL SEARCH REPORT**Information on patent family members****International Application No****PCT/US 00/31957**

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 6031747	A 29-02-2000	NONE	