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(71) Applicant (for all designated States except US): **DENSO CORPORATION** [JP/JP]; 1-1, Showa-cho, Kariya-shi, Aichi, 4488661 (JP).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **SATOU, Hayato** [JP/JP]; C/O DENSO CORPORATION, 1-1, Showa-cho,

Kariya-shi, Aichi, 4488661 (JP). **KIMURA, Tomonori** [JP/JP]; C/O DENSO CORPORATION, 1-1, Showa-cho, Kariya-shi, Aichi, 4488661 (JP). **AKAGI, Nozomu** [JP/JP]; C/O DENSO CORPORATION, 1-1, Showa-cho, Kariya-shi, Aichi, 4488661 (JP).

(74) Agent: **KIN, Junhi**; 6th Floor, Takisada Bldg., 2-13-19, Nishiki, Naka-ku, Nagoya-shi, Aichi, 4600003 (JP).

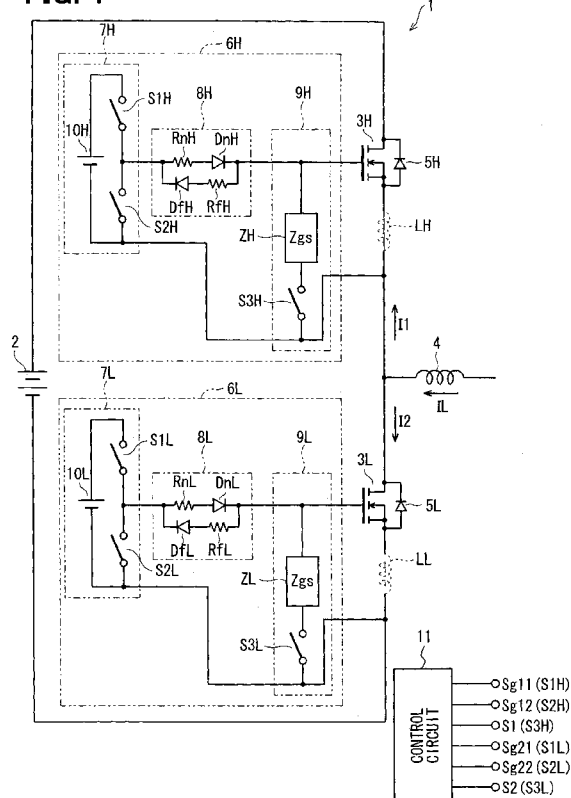
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(54) Title: POWER MOSFET DRIVER CIRCUIT AND ELEMENT VALUE DETERMINING METHOD THEREFOR

FIG. 1



(57) Abstract: When a driver circuit (1) drives a high-side and a low-side power MOSFETs (3H, 3L) at high speed, it prevents occurrence of self turn-on phenomenon caused by a voltage stemming from changes over time in a current flowing through a parasitic inductance (LH, LL). A control circuit (11) of the driver circuit turns on in one interval (T2) a high-side switch (S2H) and a low-side switch (S2L) with the others turned off, and in the following interval (T3) turns on another high-side switch (S1H) and another switch (S3H) with the others turned off. The gate-source impedance of the high-side MOSFET (3H) is thus switched to a predetermined impedance during the two intervals. This holds the gate-source voltage of the high-side MOSFET below its threshold voltage in the latter half of recovery.



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DESCRIPTION

**POWER MOSFET DRIVER CIRCUIT AND
ELEMENT VALUE DETERMINING METHOD THEREFOR**

CROSS REFERENCE TO RELATED APPLICATION

This application is based on and incorporates herein by reference Japanese patent applications No. 2011-123340 filed on June 1, 2011 and No. 2012-21805 filed on February 3, 2012.

TECHNICAL FIELD

The present disclosure relates to a power MOSFET driver circuit for driving voltage-driven power MOSFETs, which form a bridge circuit for driving inductive loads and to which freewheel diodes are coupled, and an element value determining method therefor.

BACKGROUND ART

Semiconductor switching devices are each turned on and off in response to control signals fed to the control terminals thereof. In such cases, the semiconductor switching device can be turned on erroneously because it cannot hold its off-state during a period where it should remain off, due to the presence of parasitic elements in its structure or in its peripheral circuits. This self turn-on phenomenon may incur switching loss, increased switching noise, and a circuit deterioration or destruction.

JP 2002-290224A (US 2002/0134999A1: patent document 1) discloses one example of a semiconductor device, which suppresses the self turn-on phenomenon. According to patent document 1, the gate and the source of a voltage-driven transistor are short-circuited to suppress the increase in the gate-source voltage thereof, which attributes to capacitance coupling generated when a voltage is applied between the drain and the source of the transistor.

The gate and the source of the voltage-driven transistor are short-circuited by turning on another transistor provided interposingly between

the gate and the source. When this arrangement keeps the gate-source voltage of the voltage-driven transistor below a threshold voltage thereof, the self turn-on phenomenon may be suppressed.

However, the self turn-on phenomenon may still occur when there is a parasitic inductance L_s on the source terminal where the drain and the source of the voltage-driven transistor are short-circuited. In this case, when a recovery current flowing through a diode in reverse parallel coupling with the voltage-driven transistor, the parasitic inductance L_s produces an induced electromotive force of a voltage $v = L_s \times di/dt$ (where L_s is the parasitic inductance value). When the voltage v exceeds the threshold value of the voltage-driven transistor, the self turn-on phenomenon takes place.

In particular, the technology proposed by patent document 1 cannot deal with cases where power MOSFETs such as SJ (super junction)-MOSFETs, in which the recovery current changes rapidly, are driven. When the SJ-MOSFET is driven, a large current change di/dt over time causes the above-described voltage v generated in the parasitic inductance to rise. The increased voltage v incurs the self turn-on phenomenon.

JP 2003-188699A (patent document 2) also discloses a transistor driver circuit.

SUMMARY

It is therefore an object to provide a driver circuit for driving a power MOSFET and an element value determining method for the same, the driver circuit being arranged to prevent occurrence of self turn-on phenomenon caused by a voltage attributable to changes over time in a current flowing through a parasitic inductance even when the power MOSFET is driven at high speed.

According to a first aspect, a power MOSFET driver circuit is provided for driving a voltage-driven first power MOSFET and a voltage-driven second power MOSFET in half-bridge coupling between a first power wire and a second power wire. The first and the second power MOSFETs have an inductive load coupled therebetween. The driver circuit comprises a first conduction switching circuit, a first charging/discharging circuit, a first impedance switching part, a second conduction switching circuit, a second charging/discharging

circuit, a second impedance switching part and a control section.

The first conduction switching circuit is configured to turn on and leave open a supply voltage relative to the potential of a low-potential reference terminal of the first power MOSFET as a reference potential. The first conduction switching circuit has a first on-switch and a first off-switch coupled in series between a supply terminal of the supply voltage and the low-potential reference terminal.

The first charging/discharging circuit is coupled between the first conduction switching circuit and a control terminal of the first power MOSFET. The first charging/discharging circuit adjusts a speed at which the control terminal of the first power MOSFET is electrically charged and discharged.

The first impedance switching part is coupled between the control terminal and the low-potential reference terminal of the first power MOSFET. The first impedance switching part switches the impedance between the control terminal and the low-potential reference terminal between a first impedance state and an open state. The first impedance state is a state in which the impedance is higher than an impedance of the first charging/discharging circuit. The open state is a state in which the impedance is higher than in the first impedance state.

The second conduction switching circuit is configured to turn on and leave open a supply voltage relative to the potential of a low-potential reference terminal of the second power MOSFET as a reference potential. The second conduction switching circuit has a second on-switch and a second off-switch coupled in series between a supply terminal of the supply voltage and the low-potential reference terminal.

The second charging/discharging circuit is coupled between the second conduction switching circuit and a control terminal of the second power MOSFET. The second charging/discharging circuit adjusts a speed at which the control terminal of the second power MOSFET is electrically charged and discharged.

The second impedance switching part is coupled between the control terminal and the low-potential reference terminal of the second power MOSFET. The second impedance switching part switches the impedance between the control terminal and the low-potential reference terminal between a second

impedance state to an open state. The second impedance state is a state in which the impedance is higher than an impedance of the second charging/discharging circuit. The open state is a state in which the impedance is higher than in the second impedance state.

5 The control section is configured to control the switching between states by the first and the second conduction switching circuits and the switching between states by the first and the second impedance switching parts. The control section is configured to perform switching control in such a manner that: in a first interval, a k-th on-switch is turned on and a k-th off-switch is turned off,
10 where a reference character "k" denotes one of integers 1 and 2; in a second interval, the k-th on-switch is turned off and thereafter the k-th off-switch is turned on; and in a third interval, the k-th off-switch is turned off and, at the same time, a k-th impedance switching part is switched to a predetermined k-th impedance state and an m-th on-switch is turned on, where reference character
15 "m" is the other of the integers 1 and 2.

 Further, an element value determining method is provided for determining element values of the k-th impedance switching part of the above-described power MOSFET driver circuit having the first power MOSFET and the second power MOSFET. The element value determining method adds
20 up an induced electromotive force generated in a parasitic inductance of a source of the k-th power MOSFET in response to a recovery current generated in a parasitic diode of the k-th power MOSFET, and a voltage generated by parasitic capacitance coupling of the k-th power MOSFET. The method then determines element values by which an added voltage remains below a threshold voltage of
25 the k-th power MOSFET, as the element values of the k-th impedance switching part. The method alternatively determines element values by which an added voltage becomes larger than a threshold voltage of the k-th power MOSFET and smaller than a voltage which is a sum of a threshold voltage determined based on a drain current characteristic of the k-th power MOSFET and a +10% margin
30 of the same, as the element values of the k-th impedance switching part.

 According to a second aspect, a power MOSFET driver circuit is provided for driving a voltage-driven a-th power MOSFET and a voltage-driven b-th power MOSFET in half-bridge coupling between a first power wire and a second power

wire, where reference character "a" denotes one of integers 1 and 2 and reference character "b" denotes the other of the integers 1 and 2. The a-th and the b-th power MOSFETs have an inductive load coupled therebetween. The power MOSFET driver circuit comprises an a-th conduction switching circuit, an a-th charging/discharging circuit, an a-th impedance switching part, a b-th conduction switching circuit, a b-th charging/discharging circuit, a b-th impedance switching part and a control section.

The a-th conduction switching circuit is configured to turn on and leave open a supply voltage relative to the potential of a low-potential reference terminal of the a-th power MOSFET as a reference potential. The a-th conduction switching circuit has an a-th on-switch and an a-th off-switch coupled in series between a supply terminal of the supply voltage and the low-potential reference terminal.

The a-th charging/discharging circuit is coupled between the a-th conduction switching circuit and a control terminal of the a-th power MOSFET. The a-th charging/discharging circuit adjusts a speed at which the control terminal of the a-th power MOSFET is electrically charged and discharged.

The a-th impedance switching part is coupled between the control terminal and the low-potential reference terminal of the a-th power MOSFET. The a-th impedance switching part switches the impedance between the control terminal and the low-potential reference terminal between a predetermined a-th impedance state and an open state. The a-th impedance state is a state in which the impedance is higher than an impedance of the a-th charging/discharging circuit. The open state is a state in which the impedance is higher than in the predetermined a-th impedance state.

The b-th conduction switching circuit is configured to power a control terminal of the b-th power MOSFET through a b-th on-switch to turn on the b-th power MOSFET.

The control section is configured to control the switching between states by the a-th and the b-th conduction switching circuits and the switching between states by the a-th impedance switching part. The control section is configured to perform switching control in such a manner that: in a first interval, the a-th on-switch is turned on and the a-th off-switch is turned off; in a second

interval, the a-th on-switch is turned off and thereafter the a-th off-switch is turned on; and in a third interval, the a-th off-switch is turned off and, at the same time, the a-th impedance switching part is switched to the predetermined a-th impedance state and the b-th on-switch is turned on.

5 Further, an element value determining method is provided for determining element values of the a-th impedance switching part of the above-described power MOSFET driver circuit having the a-th MOSFET and the b-th MOSFET. The element value determining method adds up an induced electromotive force generated in a parasitic inductance of the source of the a-th
10 power MOSFET in response to a recovery current generated in a parasitic diode of the a-th power MOSFET, and a voltage generated by parasitic capacitance coupling of the a-th power MOSFET. The method then determines element values by which an added voltage remains below a threshold voltage of the a-th power MOSFET, as the element values of the a-th impedance switching part.
15 The method alternatively determines element values by which an added voltage becomes larger than a threshold voltage of the a-th power MOSFET and smaller than a voltage which is a sum of a threshold voltage determined based on a drain current characteristic of the a-th power MOSFET and a +10% margin of the same, as the element values of the a-th impedance switching part.

20 BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, features and advantages will become more apparent from the following detailed description made with reference to the accompanying drawings, in which:

25 Fig. 1 is an electric circuit diagram of a high-side driver circuit and a low-side driver circuit as a first embodiment;

Figs. 2A through 2E are circuit diagrams showing impedance switching parts;

30 Figs. 3A and 3B are electric circuit diagrams showing typical control circuits;

Fig. 4 is a time chart showing on and off intervals of switches;

Fig. 5 is a table listing the on and off states of switches over different intervals;

Fig. 6 is a time chart showing relations between the on and off states of each switch and the voltage/current waveform of each node;

Fig. 7 is an electric circuit diagram showing changes in a current over an interval T4;

5 Fig. 8 is a flowchart showing a method for determining an element value of an impedance switching part;

Fig. 9 is a table listing typical parameter values to be collected in advance;

10 Fig. 10 is a circuit diagram showing an equivalent circuit for acquiring a voltage generated in a parasitic inductance in keeping with a recovery current;

Fig. 11 is a circuit diagram showing relations among the recovery current flowing through the parasitic inductance, a resistor and a parasitic capacitance; an induced electromotive force generated in the parasitic inductance; and a gate-source voltage of a transistor;

15 Fig. 12 is a time chart showing relations between currents and voltages at different components before and after a recovery current conducts;

Fig. 13 is a flowchart showing steps for acquiring a voltage that develops between the gate and the source of an MOSFET in keeping with a recovery current;

20 Fig. 14 is a circuit diagram showing an equivalent circuit that takes the parasitic capacitance in the periphery of an MOSFET into consideration;

Fig. 15 is a time chart showing relations between a recovery current and a response waveform of a drain-source voltage;

Fig. 16 is a circuit diagram showing a second embodiment;

25 Fig. 17 is a table corresponding to Fig. 5 with regard to the second embodiment;

Fig. 18 is a time chart corresponding to Fig. 6 with regard to the second embodiment;

30 Fig. 19 is a circuit diagram showing a third embodiment and corresponding to Fig. 7;

Fig. 20 is a time chart corresponding to Fig. 6 with regard to the third embodiment;

Fig. 21 is a circuit diagram showing changes in the current over the

interval T2 in Fig. 20;

Fig. 22 is an electric circuit diagram of a high-side driver circuit as a fourth embodiment;

Fig. 23 is a circuit diagram corresponding to Fig. 3B with regard to the fourth embodiment;

Fig. 24 is a time chart corresponding to Fig. 6 with regard to the fourth embodiment;

Fig. 25 is a time chart corresponding to Fig. 6 with regard to a fifth embodiment;

Figs. 26A and 26B are circuit diagrams each showing a typical switching speed control circuit as a sixth embodiment;

Fig. 27 is a table view corresponding to Fig. 9 with regard to a seventh embodiment;

Fig. 28 is a flowchart corresponding to Fig. 13 with regard to the seventh embodiment;

Fig. 29 is a graph showing a voltage region;

Figs. 30 is a time chart corresponding to Fig. 6 with regard to the seventh embodiment;

Fig. 31 is a waveform chart showing current changes upon application of an element value such as to make the applied voltage fall within a voltage region VR2;

Fig. 32 is a waveform chart showing current changes upon application of an element value such as to make the applied voltage fall within a voltage region VR1;

Fig. 33 is a waveform chart corresponding to Figs. 31 and 32 with regard to a comparative example;

Fig. 34 is a circuit diagram of an evaluation circuit for verifying surge voltage characteristics;

Fig. 35 is a waveform chart showing a transient response waveform of the drain-source voltage of a power MOSFET (part 1);

Fig. 36 is a waveform chart showing another transient response waveform of the drain-source voltage of the power MOSFET (part 2);

Fig. 37 is a waveform chart showing another transient response

waveform of the drain-source voltage of the power MOSFET (part 3);

Fig. 38 is a waveform chart showing another transient response waveform of the drain-source voltage of the power MOSFET (part 4); and

Fig. 39 is a graphic representation showing typical dependency of switching loss and surge voltage on impedance.

DESCRIPTION OF EMBODIMENTS

(First Embodiment)

The first embodiment of a power MOSFET driver circuits will now be described with reference to Figs. 1 through 15. The first embodiment is applied to a half bridge circuit.

A half bridge circuit 1 shown in Fig. 1 is a basic circuit of a power converter circuit. The circuit 1 has switching devices of an upper and a lower arms operating in complementary fashion to convert a DC voltage to an AC voltage. The half bridge circuit 1 is formed of two N-channel type SJ (super-junction)-MOSFETs (power MOSFETs) 3H and 3L (i.e., a first power MOSFET and a second power MOSFET) interposed in series coupling between a supply node (first power line) and a ground (second power line) of a DC power source 2 (e.g., 100 V). Driver circuits 6H and 6L for the power MOSFETs may be applied to the power converter circuit (converter or inverter).

One end of a stator coil 4 in an AC motor is coupled to the common node between the N-channel MOSFETs 3H and 3L as an inductive load, for example. A parasitic diode 5H is embedded between the drain and source of the high-side MOSFET 3H. A parasitic diode 5L is embedded between the drain and source of the low-side MOSFET 3L. These parasitic diodes 5H and 5L function as freewheel diodes.

The circuit for driving the high-side (upper-arm) MOSFET 3H is indicated as the driver circuit 6H and the circuit for driving the low-side (lower-arm) MOSFET 3L is indicated as the driver circuit 6L. Since the driver circuits 6H and 6L have the same circuit configuration, the description will be made with respect to only the high-side driver circuit 6H. The components forming the low-side driver circuit 6L will each be identified by an additional character L replacing the character H, and the electric circuit of the circuit 6L will

not be discussed further.

5 The driver circuit 6H includes a drive voltage generating circuit (first conduction switching circuit) 7H, a switching speed control circuit (first charging/discharging circuit) 8H, and an off-holding circuit (first impedance switching part) 9H. The drive voltage generating circuit 7H is structured to include a control terminal-equipped switch (first on-switch) S1H and another control terminal-equipped switch (first off-switch) S2H interposed in series coupling between the positive and the negative terminals of a DC power source 10H. Thus, the drive voltage generating circuit 7H switchingly outputs a power source voltage of the DC power source 10H and 0V, or leave the output in an open state. The switches S1H and S2H may each be formed of an NPN transistor, for example.

10 The switching speed control circuit 8H is formed of two series coupling circuits in parallel coupling with each other. One series coupling circuit is formed of a resistor RnH and a diode DnH. The other series connection circuit is formed of a resistor RfH and a diode DfH. When the switch S2H is turned off after the switch S1H is turned on, the gate of the MOSFET 3H is electrically charged through the resistor RnH and diode DnH, whereby the electric charge is accumulated in a gate input capacitance of the MOSFET 3H. The accumulation rate of the charges is dependent on the gate input capacitance of the MOSFET 3H and on the resistance value of the resistor RnH. When the switch S2H is turned on after the switch S1H is turned off, the accumulated charge in the gate input capacitance of the MOSFET 3H is discharged through the resistor RfH and the diode DfH. The discharge rate is dependent on the gate input capacitance of the MOSFET 3H and on the resistance value of the resistor RfH.

20 The off-holding circuit 9H is formed of a suitable impedance element ZH and a control terminal-equipped switch S3H interposed in series coupling between the gate and the source of the MOSFET 3H. Figs. 2A through 2E show typical configurations of the off-holding circuit 9H. The impedance element ZH of the off-holding circuit 9H should preferably have resistance or inductance. The higher the resistance value or the inductance value, the greater the effect of suppressing the increase in the gate-source voltage of the MOSFET 3H. Thus a resistor Rgs may be used as the impedance element ZH as shown in Fig. 2A, or

an on-resistor of a MOSFET M1 may be utilized as shown in Fig. 2B. Where the configuration of Fig. 2B is adopted, a single transistor can solely assume the function of the configuration of Fig. 2A in which the resistor Rgs and a switch SW are in series coupling with each other. In another example, an inductance Lgs may be used to replace the resistor Rgs as shown in Fig. 2C. In a further example, both the resistor Rgs and the inductance Lgs may be series-coupled with each other as shown in Fig. 2D. In a still further example, the inductance Lgs may be series-coupled to the MOSFET M1 as shown in Fig. 2E. This type of driver circuit 6H is also implemented on the low side as the driver circuit 6L.

A control circuit (control section) 11 feeds on/off control signals Sg11, Sg12 and S1 to the control terminals of the switches S1H, S2H and S3H, respectively, to turn on and off these switches S1H, S2H and S3H. The control circuit 11 also supplies on/off signals Sg21, Sg22 and S2 to the control terminals of switches S1L, S2L and S3L, respectively, to turn on and off these switches S1L, S2L and S3L.

The control circuit 11 is formed as shown in Fig. 3A. The control circuit 11 includes a comparison circuit 12 and a logic circuit 13. The comparison circuit 12 compares a triangular wave signal Stri with an output voltage command value (DC signal) Scom, and outputs PWM signals Ssd1 and Ssd2. The logic circuit 13 inputs the PWM signals Ssd1 and Ssd2 from the comparison circuit 12, and outputs the control signals Sg11, Sg12, S1, Sg21, Sg22 and S2.

The logic circuit 13 is formed as shown in Fig. 3B. The logic circuit 13 includes a NOR gate 14. The logic circuit 13 is wired to output the PWM signal Ssd1 as the on/off control signals Sg11 and S2 and to output the PWM signal Ssd2 as the on/off control signals Sg21 and S1. Also, the NOR gate 14 inputs the PWM signals Ssd1 and Ssd2, and outputs the on/off control signals Sg12 and Sg22.

The PWM signals Ssd1 and Ssd2 are output from the comparison circuit 12 in the waveforms shown in Fig. 4. The signals Ssd1 and Ssd2 repeat the following states at predetermined frequencies and duty ratios during intervals T1 through T4:

T1: Ssd1 is "H" (on) and Ssd2 is "L" (off);

T2: Ssd1 is "L" (off) and Ssd2 is "L" (off);

T3: Ssd1 is "L" (off) and Ssd2 is "H" (on); and

T4: Ssd1 is "L" (off) and Ssd2 is "L" (off).

With the states in each of these intervals T1 through T4 repeated, the logic circuit 13 outputs the on/off control signals Sg11, Sg12, S1, Sg21, Sg22 and S2 in suitable periodic fashion. Fig. 5 shows those on/off states of the high-side and low-side power MOSFETs which vary depending on the on/off control signals. Figs. 6A through 6L show such on/off states in time charts. In each of the intervals T1 through T4, the output of the logic circuit 13 repeats the following states:

T1: Sg11 and S2 are "H" (on) and the others are "L" (off);

T2: Sg12 and Sg22 are "H" (on) and the others are "L" (off);

T3: S1 and Sg21 are "H" (on) and the others are "L" (off); and

T4: Sg12 and Sg22 are "H" (on) and the others are "L" (off).

Where the above switching is repeated, the switches S1H and S2H are turned on and off almost simultaneously between the intervals T1 and T2, and the switches S1L and S2L are turned on and off almost simultaneously between the intervals T3 and T4. The circuit may be arranged to provide a suitable dead time in order to prevent short-circuiting between the DC power supplies 10H and 10L.

Described below with reference to Figs. 1, 6 and 7, among others, are the basic operations of the circuit in effect when the on/off control signals Sg11, Sg12, S1, Sg21, Sg22 and S2 are input to the switches S1H through S3H and S1L through S3L, respectively, in each of the intervals T1 through T4. It is assumed that a load current flows through the stator coil 4 in the direction shown in Fig. 1.

<Basic operation in interval T1>

In the interval T1, on the high side, the switch S1H is turned on while the other switches S2H and S3H are turned off. This causes the electric charge to be fed from the DC power source 10H to the gate of the MOSFET 3H, whereby the gate input capacitance of the MOSFET 3H is electrically charged. In the interval T1, as shown by (i) of Fig. 6, a gate-source voltage V_{gs1} of the MOSFET 3H exceeds a threshold gate-source voltage V_t thereof so that the MOSFET 3H is turned on.

In the meantime, on the low side, the switch S3L is turned on and the

switches S1L and S2L are turned off. This causes the off-holding circuit 9H to generate a predetermined impedance (e.g., tens of ohms) between the gate and the source of the MOSFET 3L. Thus as shown by (j), a gate-source voltage V_{gs2} of the MOSFET 3L becomes approximately zero, so that the MOSFET 3L remains in its off-state.

<Basic operation in interval T2>

In the interval T2, on the high side, the switch S2H is turned on after the switch S1H is turned off. This causes the electric charge accumulated in the gate of the MOSFET 3H to be discharged through the resistor R_{fH} of the switching speed control circuit 8H. Thus as shown by (i), the gate-source voltage V_{gs1} of the MOSFET 3H drops below the threshold voltage V_t , at which time the MOSFET 3H is turned off.

Meanwhile, on the low side, the switch S3L is turned off and the switch S2L is turned on. This causes the impedance of the switching speed control circuit 8H to be fixed between the gate and the source of the MOSFET 3L. Thus as shown by (j), the gate-source voltage V_{gs2} of the MOSFET 3L is held at approximately 0 V, so that the MOSFET 3L remains in its off-state. When the MOSFETs 3H and 3L are both turned off, the load current I_L flowing through the stator coil 4 flows in the forward direction of the diode 5H.

<Basic operation in interval T3>

In the interval T3, on the high side, the switch S2H is turned off and the switch S3H is turned on simultaneously. This causes the impedance element Z_H of the off-holding circuit 9H to be coupled between the gate and the source of the MOSFET 3H, allowing the off-holding circuit 9H to hold a predetermined impedance of the impedance element Z_H between the gate and the source of the MOSFET 3H. In this manner, the MOSFET 3H is held in the off-state as shown by (i).

Meanwhile, on the low side, the switch S1L is turned on after the switch S2L is turned off. This causes the gate input capacitance of the MOSFET 3L to be charged electrically through the resistor R_{nL} of the switching speed control circuit 8L. As shown by (j), the gate-source voltage V_{gs2} of the MOSFET 3L rises and exceeds the threshold voltage V_t thereof, at which time the MOSFET 3L is turned on.

<Basic operation in interval T4>

In the interval T4, on the high side, the switch S3H is turned off and the switch S2H is turned on simultaneously. This causes the impedance of the switching speed control circuit 8H to be coupled between the gate and the source of the MOSFET 3H. Meanwhile, on the low side, the switch S2L is turned off after the switch S1L is turned on. This causes the electric charge accumulated in the gate of the MOSFET 3L to be discharged through the resistor RfL of the switching speed control circuit 8L. The gate of the MOSFET 3L is then coupled to the impedance of the switching speed control circuit 8L.

The above-described basic operations are repeated during the intervals T1 through T4. While such periodical basic operations are being repeated, the load current I_L flows in the forward direction of the diode 5H in the interval T2. When the MOSFET 3L is turned on in the interval T3, a current I_2 rises rapidly as shown by (l). This phenomenon is brought about when, with the MOSFET 3L turned on, the carrier storage effect causes a reverse recovery current (recovery current) I_r to flow to the diode 5H thereby incurring sudden changes in currents I_1 and I_2 .

In particular, the currents I_1 and I_2 change rapidly when the reverse recovery current is damped down. The degree of current damping is particularly pronounced during an interval where the current I_1 rises as shown by (k), i.e., where the current I_2 drops to a settling current I_{st} shown by (l) in the latter half of the recovery.

There exists a parasitic inductance L_H in the source of the MOSFET 3H, and a parasitic inductance L_L in the source of the MOSFET 3L. Thus the inductances L_H and L_L each produce an induced electromotive force $-L di/dt$ reflecting the changes over time in the currents I_1 and I_2 .

When the induced electromotive force is generated in the parasitic inductance L_H in the latter half of the recovery, a voltage develops in that node of the parasitic inductance L_H which is located on the side of the stator coil 4 relative to the source of the MOSFET 3H. Consequently, the gate-source voltage V_{gs1} of the MOSFET 3H rises.

In the interval T3, the MOSFET 3H remains in its off state. This makes it necessary to arrange for the gate-source voltage V_{gs1} of the MOSFET 3H to be

kept below the threshold voltage V_t thereof.

In this embodiment, the off-holding circuit 9H is coupled between the gate and the source of the MOSFET 3H. Before entering the latter half of the recovery in which the induced electromotive force of the parasitic inductance LH rises in particular, the switch S3H is always turned on causing the off-holding circuit 9H to couple the impedance element ZH between the gate and the source of the MOSFET 3H.

Thus when the induced electromotive force develops in the parasitic inductance LH, the impedance element ZH of the off-holding circuit 9H operates to charge electrically the gate of the MOSFET 3H through the impedance element ZH in keeping with the induced electromotive force in the parasitic inductance LH. This suppresses the increase in the gate-source voltage V_{gs1} of the MOSFET 3H. In this manner, when the SJ-MOSFETs 3H and 3L are driven even at high speed, the self turn-on phenomenon can be prevented.

Fig. 7 schematically illustrates current changes in the interval T4 shown by (a) through (l) of Fig. 6. In the interval T4 by (a) through (l), on the low side, the switch S2L is turned on after the switch S1L is turned off. This causes the gate-source voltage V_{gs2} of the MOSFET 3L to drop as shown by (j). In the meantime, on the high side, a current increased by the amount reflecting the drop in the gate-source voltage V_{gs2} flows in the forward direction of the parasitic diode 5H, as shown by (k).

In such a case, the device may malfunction in response to the unexpected voltage rise. That is because an induced electromotive force VLL develops in the parasitic inductance LL in keeping with a current gradient reflecting the drop in the current I_2 caused by the MOSFET 3L getting turned off. In order to suppress the malfunction attributable to the induced electromotive force VLL, the current gradient of the current I_2 need only be made smaller. This can be accomplished by adjusting the resistance value of the resistor R_{fL} for controlling the turn-off speed. When the operations in the intervals T1 through T4 by (a) through (l) are repeated, the MOSFETs function normally.

When control is exercised as described above, an appropriate impedance is kept between the gate and the source of each of the MOSFETs 3H and 3L when it is turned off. This reduces the switching speed and suppresses

the rise in the gate-source voltage.

Particularly, in order to prevent the self turn-on phenomenon reliably, it is preferred to determine the circuit element values of the driver circuits 6H and 6L using a predetermined method. The element values are determined by the following method.

<Method for determining the impedance of the off-holding circuits>

It is useful especially to regard the impedance values of the impedance elements ZH and ZL in the off-holding circuits 9H and 9L as an important factor for preventing the self turn-on phenomenon. In view of circuit symmetry, the impedance is assumed to be the same for the impedance elements ZH and ZL. The method for determining the impedance value when the off-holding circuits 9H and 9L are each set to be a series circuit formed of the resistor Rgs and inductance Lgs will be described below.

The major causes of raising the gate-source voltage Vgs of each of the MOSFETs 3H and 3L are the induced electromotive force generated in the parasitic inductances LH and LL in keeping with the recovery current, and the coupling voltage of the parasitic capacitance. The effects of these causes on the voltage increases may be calculated individually. The impedance of the impedance elements ZH and ZL may then be determined in such a manner that the added voltages arising from the calculated effects remain below the predetermined threshold voltage Vt.

Specifically, the impedance of the impedance elements ZH and ZL is determined as shown in Fig. 8. First, necessary parameter values are collected in advance of the determination of the circuit impedance (S1). These parameters are design values determined through simulations and experiments based on the semiconductor configuration of the power MOSFETs 3H and 3L and on the manner in which the parasitic elements and the circuits involved are coupled. The parameters may be defined as shown in Fig. 9.

For example, as shown in Fig. 9, the parameters may be formed of the values Ls of parasitic inductances LL and LH, the gradient di/dt of the recovery current, the settling time ranging from the latter half of the recovery to an end, a gate-source parasitic capacitance value Cgs, a gate-drain parasitic capacitance value Cgd, and a drain-source voltage Vds.

Referring to Fig. 8, after the parameters are collected, the impedance for the off-holding circuits 9H and 9L is set provisionally (S2). As discussed above, although the induced electromotive force of the parasitic inductances LH and LL is generated in keeping with the recovery current, the impedance set provisionally in step S2 is used to calculate a gate-source voltage Vgsa (S3).

<Voltage Vgsa generated in the parasitic inductance>

Fig. 10 shows an equivalent circuit for determining the voltage Vgsa generated in the parasitic inductances LH and LL in keeping with the recovery current.

As shown in Fig 10, a parasitic capacitance Cgs exists between the gate and the source of the MOSFET 3H. The gate-source voltage Vgs of the MOSFET 3H is equal to the applied voltage of the parasitic capacitance Cgs. For this reason, as indicated by another equivalent circuit in Fig. 11, an induced electromotive force $-L_s \times di/dt$ generated in the parasitic inductance L_s in the reverse direction causes the capacitor Cgs to be charged through the inductance Lgs and the resistor Rgs accordingly. This in turn raises the gate-source voltage Vgs of the MOSFET 3H.

Fig. 11 illustrates relations among a recovery current i (I_r) flowing through the parasitic inductance L_s , the resistor Rgs, and the parasitic capacitance Cgs; the induced electromotive force $-L_s \times di/dt$ generated in the parasitic inductance L_s ; and the gate-source voltage Vgs of the transistor 3H. Fig. 12 shows current and voltage changes over time in the components involved before and after conduction of the recovery current.

In the interval T2 described above, the load current flows back to the diode 5H and the current i flows in the reverse direction of the diode 5H. Thereafter, when the MOSFET 3L is turned on in the interval T3, the reverse recovery current arising from the carrier storage effect flows to the diode 5H and causes the current i to increase rapidly (in an interval segment T31 of the interval T3 in Fig. 12). In the former half of the recovery indicated by the interval segment T31 of the interval T3 develops an induced electromotive force $-L_s \times di/dt$ corresponding to the gradient of the rising current in the parasitic inductance L_s . The gradient of the rising current in the former half of the recovery is less steep, along with a correspondingly smaller induced

electromotive force, than in the latter half of the recovery.

Thereafter, in the latter half of the recovery indicated by an interval segment T32 in the interval T3 develops an induced electromotive force corresponding to a steep gradient of the falling current. Thus the induced electromotive force tends to be large in keeping with the gradient of the falling current. When the recovery current i is assumed to decrease linearly, then a step voltage V_s may be assumed to develop in the parasitic inductance L_s only for a predetermined settling time t_f in the latter half of the recovery.

The gate-source voltage V_{gsa} of the MOSFET 3H rises in keeping with the step voltage V_s generated in the parasitic inductance L_s . For this reason, the element values involved are to be determined in such a manner that the maximum value of the voltage V_{gsa} in the latter half of the recovery is minimized.

The voltage V_{gs} is determined as shown in Fig. 13. Applying the step response equation of an RLC series circuit provides a secondary transfer function that is expressed by the following Laplace transform equation (1):

$$V_o = G(s) \cdot V_i = \frac{\omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} \cdot \frac{V_s}{s} \quad \dots (1)$$

where,

$$\omega_n = \frac{1}{\sqrt{L_{gs} C_{gs}}}, \quad \xi = \frac{R_{gs}}{2} \sqrt{\frac{C_{gs}}{L_{gs}}}$$

where, ω_n denotes an undamped natural angular frequency (natural frequency) and ξ represents a damping rate (braking rate).

Performing inverse Laplace transform on the equation (1) above divides it into three cases, $\xi=1$ (equation (2)), $\xi>1$ (equation (3)), and $0<\xi<1$ (equation (4)), as follows:

$$V_{gsa} = V_s \cdot \left\{ 1 - e^{-\omega_n t} (1 + \omega_n \cdot t) \right\} \quad \dots (2)$$

$$V_{gsa} = V_s \cdot \left\{ 1 - e^{-\xi\omega_n t} \left[\cosh \sqrt{(\xi^2 - 1)} \times \omega_n \cdot t + \frac{\xi}{\sqrt{(\xi^2 - 1)}} \sinh \sqrt{(\xi^2 - 1)} \times \omega_n \cdot t \right] \right\} \quad \dots (3)$$

$$V_{gsa} = V_s \cdot \left\{ 1 - e^{-\xi \omega_n t} \left[\cos \sqrt{(1 - \xi^2)} \times \omega_n \cdot t + \frac{\xi}{\sqrt{(1 - \xi^2)}} \sin \sqrt{(1 - \xi^2)} \times \omega_n \cdot t \right] \right\} \quad \dots (4)$$

As shown in Fig. 13, one of the cases above may be selected depending on the value of ζ , with a predetermined time t_f substituted in the corresponding equation (in steps S11 through S16). It should be noted that the voltage V_{gsa} in the equation (4) is a value that vibrates with the passage of time. Thus when the time $t_m = \pi / \omega_n (\sqrt{1 - \zeta^2})$ over which the voltage V_{gsa} is maximized is less than the predetermined settling time t_f (NO in step S15), then $t_m = \pi / \omega_n (\sqrt{1 - \zeta^2})$ is substituted in the equation (4) to acquire the voltage V_{gsa} . This makes it possible to determine the voltage V_{gsa} in step S3 in keeping with the parameter values collected in step S1 of Fig. 8.

After the voltage V_{gsa} is determined, a voltage V_{gsb} generated by the parasitic capacitance coupling is calculated (step S4).

<voltage V_{gsb} generated by the parasitic capacitance coupling>

Fig. 14 shows an equivalent circuit that takes the parasitic capacitance in the periphery of the MOSFETs into consideration. Fig. 15 illustrates relations between the recovery current i and a response waveform of the drain-source voltage V_{ds} . After the MOSFET 3H is turned off, its drain-source voltage V_{ds} increases. A maximum voltage value V_{gsb} of the gate-source voltage V_{gs} at this time may be obtained using the following equation (5):

$$V_{gsb} = \frac{C_{gd}}{C_{gs} + C_{gd}} \cdot V_{ds} \quad \dots (5)$$

This is possible because the voltage V_{gsb} occurs as a divided voltage derived from the gate-drain parasitic capacitance C_{gd} and gate-source capacitance C_{gs} .

In step S5 of Fig. 8, the added voltage V_{gs} adding up the effects above (= voltage V_{gsa} + voltage V_{gsb}) is obtained. The values of the resistor R_{gs} and the inductance L_{gs} are determined in such a manner that the added value V_{gs} remains below the threshold voltage V_t . When this condition is not met (NO in step S5), then step S2 is executed again and the subsequent processing is repeated starting from the provisional setting of the impedance for the off-holding circuits 9H and 9L. Preferably, an appropriate margin of the

threshold voltage V_t should be taken into account when the values of the resistor R_{gs} and the inductance L_{gs} are determined. Verification may then be made by substituting the acquired values of the resistor R_{gs} and inductance L_{gs} in the equation.

5 The appropriate element value can thus be determined because the element value for the off-holding circuits 9H and 9L is determined in accordance with the added voltage of the voltage V_{gsa} plus the voltage V_{gsb} . Given the symmetry of circuitry, the same method for determining the element value may be applied as described above to both the high-side MOSFET 3H and the
10 low-side MOSFET 3L.

As described above, the first embodiment operates as follows.

In the interval T1, on the high side, the switch S1H is turned on with the switch S2H turned off. Also, with the switch S3H turned off, the off-holding circuit 9H is left open. This causes the drive voltage generating circuit 7H to
15 feed the DC power source 10H between the gate and the source of the MOSFET 3H to turn it on.

On the low side also in the interval T1, the switches S1L and S2L are both turned off and the switch S3L is turned on to set the off-holding circuit 9L to the predetermined impedance. This establishes a predetermined fixed
20 impedance between the gate and the source of the MOSFET 3L.

In the interval T2, on the high side, the switch S2H is turned on after the switch S1H is turned off and the switch S3H is held off so as to leave the off-holding circuit 9H open. In this manner, the output voltage of the drive voltage generating circuit 7H is controlled to coincide with the source-side
25 voltage of the MOSFET 3H (i.e., voltage at its low-potential reference terminal). This causes the gate input capacitance of the MOSFET 3H to be discharged through the switching speed control circuit 8H.

On the low side also in the interval T2, the switch S2L is turned on with the switch S1L held off and the switch S3L is turned off to leave the off-holding circuit 9L left open. In this manner, the output voltage of the drive voltage generating circuit 7L is controlled to coincide with the source-side voltage of the
30 MOSFET 3L (voltage at its low-potential reference terminal).

In the interval T3, on the high side, the switch S2H is turned off with the

switch S1H held off while the switch S3H is turned on simultaneously to switch the off-holding circuit 9H from its open state to the predetermined impedance. This establishes the predetermined fixed impedance between the gate and the source of the MOSFET 3H.

5 On the low side also in the interval T3, the switch S1L is turned on after the switch S2L is turned off, and the off-holding circuit 9L is held open with the switch S3L kept off. This allows the output voltage of the drive voltage generating circuit 7L to become the output voltage of the DC power source 10L, to be applied between the gate and the source of the MOSFET 3L.

10 In the interval T4, on the high side, the switch S2H is turned on with the switch S1H held off and the switch S3H is turned off to leave the off-holding circuit 9H open. In this manner, the output voltage of the drive voltage generating circuit 7H is controlled to coincide with the source-side voltage of the MOSFET 3H (voltage at its low-potential reference terminal).

15 On the low side also in the interval T4, the switch S2L is turned on after the switch S1L is turned off and the switch S3L is held off to keep the off-holding circuit 9L open. In this manner, the output voltage of the drive voltage generating circuit 7L is controlled to coincide with the source-side voltage of the MOSFET 3L (voltage at its low-potential reference terminal). This causes the
20 gate input capacitance of the MOSFET 3L to be discharged through the switching speed control circuit 8L.

 When the control circuit 11 places the switches under driving control of the driver circuits 6H and 6L, the switches S2H and S2L are turned on and the other switches are turned off in the interval T2, and the switches S1L and S3H
25 are turned on and the other switches are turned off in the interval T3. With these settings, the gate-source impedance of the MOSFET on the high side can be switched to a predetermined impedance in the intervals T2 and T3. Even in the latter half of the recovery, the gate-source voltage V_{gs1} of the MOSFET on the high side can be held below the threshold voltage V_t thereof.

30 In particular, before the beginning of the interval T3 and prior to the elapse of a predetermined time over which the current I_2 exceeds a predetermined settling time for the first time (before the latter half of the recovery is finished), the gate-source impedance of the high-side MOSFET 3H is

fixed to a predetermined impedance.

This makes it possible to hold the gate-source voltage V_{gs} of the high-side MOSFET 3H and low-side MOSFET 3L below the threshold voltage V_t thereof. Thus the self turn-on phenomenon is prevented from taking place even when the power MOSFETs are driven at high speed.

Further, the induced electromotive force V_{gsa} generated in the parasitic impedance L_s by the flow of the recovery current and the voltage V_{gsb} generated by the parasitic capacitance coupling are added up. The element value of the impedance element Z_H for the off-holding circuits 9H and 9L is then determined in such a manner that the added voltage above remains below the threshold voltage of the MOSFETs 3H and 3L. This makes it possible to determine an appropriate element value of the off-holding circuits 9H and 9L in accordance with the parasitic capacitance and other factors.

(Second Th Embodiment)

The second embodiment of the driver circuit for MOSFET is shown in Figs. 16 to 18. The second embodiment primarily differs from the first embodiment in that the switches of the off-holding circuits operate at different switching timing. In the second embodiment, the same components as those of the first embodiment are given the same reference characters, and the description is simplified.

A logic circuit 15 replacing the logic circuit 13 in Fig. 3B is configured as shown in Fig. 16. The logic circuit 15 is formed of a NOR gate 16 and NOT gates 17 and 18. The PWM signals S_{sd1} and S_{sd2} are input from the comparison circuit 12 to the logic circuit 15. In turn, the logic circuit 15 outputs the control signals S_{g11} , S_{g12} , S_1 , S_{g21} , S_{g22} , and S_2 .

The logic circuit 15 outputs the PWM signal S_{sd1} as the on/off control signal S_{g11} and the PWM signal S_{sd2} as the on/off control signal S_{g21} . The NOR gate 16 inputs these PWM signals S_{sd1} and S_{sd2} and outputs the on/off control signals S_{g12} and S_{g22} . The NOT gate 17 inputs the PWM signal S_{sd1} and outputs the on/off control signal S_1 . The NOT gate 18 inputs the PWM signal S_{sd2} and outputs the on/off control signal S_2 .

The switches in the logic circuit 15 are turned on and off as indicated in Fig. 17. The switches S_{2L} and S_{3L} are both turned on in the interval T_2 as

indicated by reference character X1. Also, the switches S2H and S3H are both turned on in the interval T4 as indicated by reference character X2. The switch settings indicated by reference characters X1 and X2 may be either on or off. That is, both settings may be either on or off altogether. In such cases, the logic circuit 15 may be reconfigured as needed.

As shown in Fig. 18, the on/off control signal Sg12 from the switch S2H and the on/off control signal S1 from the switch S3H are both output as on-control signals in the interval T2. Thus in the interval T2, the off-holding circuit 9H is set to a predetermined impedance, and the output voltage of the drive voltage generating circuit 7H is controlled to coincide with the voltage at the source-side reference terminal of the MOSFET 3H.

In this case, the on/off control signals can be output at the timings shown in Figs. 18C through 18H. In the interval T2, turning on the switches S2H and S3H fixes the gate-source impedance of the MOSFET 3H to a low impedance. In the interval T3, turning off the switch S2H and turning on the switch S3H fixes the gate-source impedance of the MOSFET 3H to an impedance higher than that in the interval T2. That is, because the gate-source impedance of the MOSFET 3H occurs as a synthetic impedance of the resistor RfH and the impedance element ZH in the interval T2 but as the impedance of the impedance element ZH alone in the interval T3. Also, when the resistance value of the resistor RhH is set to be lower than that of the impedance element ZH, the gate-source impedance of the MOSFET 3H becomes lower than the synthetic impedance.

In such a case, the threshold voltage V_t will not be exceeded when the gate-source voltage V_{gs1} rises in the interval T3 in the latter half of the recovery. In this manner, as in the first embodiment, the second embodiment can hold the gate-source voltage V_{gs1} of the MOSFET 3H below the threshold voltage V_t thereof.

(Third Embodiment)

The third embodiment of the driver circuit for MOSFET is shown in Figs. 19 through 21. The third embodiment is different from the first embodiment in that the load current I_L is assumed to flow in reverse to the direction indicated in the first embodiment. In the third embodiment, the same components as those

of the first embodiment are given the same reference characters, and the description is simplified.

In the third embodiment, it is assumed that the load current I_L of the stator coil 4 flows rightward as illustrated in Fig. 19. Also, the source current I_1 of the high-side MOSFET 3H and the drain current I_2 of the MOSFET 3L are defined to flow in reverse to the directions indicated in the first embodiment.

The gate-source voltages V_{gs1} and V_{gs2} of the MOSFETs 3H and 3L change as shown in the time charts of Fig. 20. The source current I_1 of the MOSFET 3H and the drain current I_2 of the MOSFET 3L also change accordingly.

The changes in voltages and currents taking place this time in the third embodiment differ only in terms of the intervals in which they occur in the first embodiment and thus will not be described further. In a manner substantially similar to the first embodiment, the recovery current develops in the MOSFET 3L in the interval T_1 . In the latter half of the recovery, the gate-source voltage V_{gs2} of the MOSFET 3L increases. However, since the switch S_{2L} is turned on beforehand in the interval T_4 and then the switch S_{3L} is turned on in the interval T_1 , it is possible to control the gate-source impedance of the MOSFET 3L to coincide with the predetermined impedance and thereby to suppress the gate-source voltage V_{gs2} . Consequently, the gate-source voltage V_{gs2} of the MOSFET 3L can be held below the threshold voltage V_t thereof.

The current changes in the interval T_2 is shown in Fig. 21. In the interval T_2 on the high side, the switch S_{2H} is turned on after the switch S_{1H} is turned off, so that the gate-source voltage V_{gs1} of the MOSFET 3H decreases as shown by (i) in Fig. 20. In the meantime, on the low side, a current increased by the amount reflecting the drop in the voltage flows increasingly in the forward direction of the parasitic diode $5L$.

In such a case, the element may malfunction due to an unintended voltage rise. This can happen because the current I_1 drops due to the MOSFET 3H getting turned off, causing an induced electromotive force V_{LH} reflecting the current gradient to develop in the parasitic inductance L_H . To suppress the malfunction triggered by the induced electromotive force V_{LH} , the gradient of the current I_1 need only be made smaller. This is accomplished by suitably adjusting the resistance value of the resistor R_{fH} , which controls the turn-off

speed. Normal operations are then sustained when the operations in the intervals T1 through T4 in Fig. 20 are repeated.

In the third embodiment, the load current I_L is assumed to flow in reverse to the direction in the first embodiment. The gate-source voltage V_{gs2} of the MOSFET 3L generated in keeping with the recovery current can be held below the threshold voltage V_t of the MOSFET 3L.

(Fourth Embodiment)

The fourth embodiment of the driver circuit for MOSFET is shown in Figs. 22 to 24. The fourth embodiment primarily differs from the first embodiment in that, in the intervals where the switches S2H and S2L are turned on in the first embodiment, these switches are replaced with the switches S3H and S3L being turned on to hold the gate-source voltages V_{gs1} and V_{gs2} of the MOSFETs 3H and 3L below the threshold voltage V_t thereof. The load current is assumed to flow in the same direction as in the first or the second embodiment. In the fourth embodiment, the same components as those of the first embodiment are given the same reference characters, and the description is simplified.

A driver circuit on the high side includes, as shown in Fig. 22, a switching speed control circuit formed of a switch SWH and a resistor R_g in place of the switching speed control circuit 8H. The switch SWH and resistor R_g are serially coupled between the DC power source 2 and the gate of the MOSFET 3H. Although not shown in Fig. 22, there is also provided on the low side a similar switching speed control circuit formed of a switch SWL and a resistor R_g in place of the switching speed control circuit 8L. The switch SWL and resistor R_g are serially coupled between the DC power source 2 and the gate of the MOSFET 3L.

A logic circuit 19 replacing the logic circuit 13 is configured as shown in Fig. 23. The logic circuit 19 is formed of NOT gates 20 and 21. The PWM signals Ssd1 and Ssd2 are input from the comparison circuit 12 to the logic circuit 19. In turn, the logic circuit 19 outputs the control signals Sg11, S1, Sg21, and S2.

The logic circuit 19 outputs the PWM signal Ssd1 as the on/off control signal Sg11 and the PWM signal Ssd2 as the on/off control signal Sg21. The NOT gate 20 inputs the PWM signal Ssd1 and outputs the on/off control signal S1. The NOT gate 21 inputs the PWM signal Ssd2 and outputs the on/off control

signal S2.

The logic circuit 19 is configured as shown in Fig. 23. The switches involved are turned on and off as shown in Fig. 24. The switch S3H is turned on in the interval T2 as indicated by (e) in Fig. 24 before the switch SWL is turned on in the interval T3 as indicated by (f), whereby the predetermined impedance can be maintained between the gate and the source of the MOSFET 3H. Thus when the DC power source 2 on the low side feeds a voltage between the gate and the source of the MOSFET 3H to turn it on in the interval T3, the increase in the gate-source voltage V_{gs1} of the MOSFET 3L is suppressed. This keeps the gate-source voltage V_{gs1} of the MOSFET 3L below the threshold voltage V_t thereof. The fourth embodiment thus provides the same effects as those of the first embodiment, using a simpler circuit configuration.

(Fifth Embodiment)

The fifth embodiment of the driver circuit for MOSFET is shown in Fig. 25. The fifth embodiment primarily differs from the first embodiment in that, in the intervals where the switches S2H and S2L are turned on in the first embodiment, these switches are replaced with the switches S3H and S3L being turned on. Although the load current flows in the same direction as in the third embodiment, the fifth embodiment holds the gate-source voltage V_{gs2} of the MOSFET 3L below the threshold voltage V_t thereof, thereby preventing the self turn-on phenomenon.

(Sixth Embodiment)

The sixth embodiment of the driver circuit for MOSFET is shown in Figs. 26A and 26B. The switching speed control circuits 8H and 8L shown in Fig. 1 are modified to a switching speed control circuit shown in Fig. 26A or 26B.

In the case of the circuit configuration shown in Fig. 26A, when the circuit is turned on, the gate of the MOSFET 3H is electrically charged through the resistor R_{nH} . When the circuit is turned off, that gate is discharged through resistors R_{fH} and R_{nH} . Thus this circuit configuration may be advantageously adopted when the switching speed at turn-on time is to be higher than at turn-off time.

In the case of the circuit configuration shown in Fig. 26B, when the circuit is turned on, the gate of the MOSFET 3H is electrically charged through

the resistors R_{nH} and R_{nH} . When the circuit is turned off, that gate is discharged through the resistor R_{fH} . This circuit configuration may thus be adopted advantageously when the switching speed at turn-off time is to be higher than at turn-on time.

5 (Seventh Embodiment)

The seventh embodiment of the driver circuit for MOSFET is shown in Figs. 27 through 39. The seventh embodiment primarily differs from the first embodiment in that, a different method is adopted to determine the element value of the circuit. Although the calculating method shown in Fig. 8 remains the same, step S3 of the procedure is changed so that the voltages V_{gsa} and V_{gsb} are calculated differently. In the seventh embodiment, the same components as those of the first embodiment are given the same reference characters, and the description is simplified.

Fig. 27 corresponds to Fig. 9 described above in conjunction with the first embodiment. The predetermined time (settling time) t_f in Fig. 9 is replaced with a time t_{sr} in Fig. 27. This time t_{sr} refers to the time period from the time the latter half of the recovery is started until the injection (increase) of a channel current is started due to the formation of an inversion layer in the power MOSFET.

As described above in connection with the first embodiment, the parameter values are collected in step S1 of Fig. 8. In step S2, the impedance for the constant impedance holding circuit is provisionally set. In step S3, the voltage V_{gsa} generated in the parasitic inductance in keeping with the recovery current is calculated.

Where the secondary transfer function derived from the step response equation of the RLC series circuit is applied, the voltage V_{gsa} is determined as expressed by $\zeta=1$ (equation (2)), $\zeta>1$ (equation (3)), and $0<\zeta<1$ (equation (4)).

As shown in Fig. 28, different cases are assumed depending on the value of ζ , and the value of the time t_{sr} is substituted in the equations (2) through (6). As described above in connection with the first embodiment, the voltage V_{gsa} of the equation (4) is a voltage that vibrates over the passage of time. The time t_m over which the voltage V_{gsa} is maximized is expressed as $\pi/\omega_n(\sqrt{1-\zeta^2})$. When the time t_m falls within the time t_{sr} (NO in step S15),

then $t_m = \pi / \omega n(\sqrt{1 - \zeta^2})$ is substituted in the equation (4) to acquire the voltage V_{gsa} . In this manner, the maximized voltage V_{gsa} can be obtained in step S3 in accordance with the parameter values collected in step S1 of Fig. 8.

Next, in step S4, the voltage V_{gsb} arising from the parasitic capacitance coupling is calculated. The equivalent circuit shown in Fig. 14 is utilized here. On the assumption that C_{gd} stands for the gate-drain parasitic capacitance of the MOSFET 3H and C_{gs} for the gate-source parasitic capacitance thereof, the step response of the divided voltage is obtained. In this case, the voltage V_{gs} is acquired as expressed by the following equation (6):

$$V_{gs} = \frac{C_{gd}}{C_{gs} + C_{gd}} \cdot V_{ds} \cdot e^{-\frac{1}{R_{gs}(C_{gs} + C_{gd})} \cdot t} \quad \dots (6)$$

The voltage V_{gsb} in the equation (6) is a time-dependent function that decreases over time t and is maximized when the time t is 0. For this reason, when the maximum value of the function is determined as the voltage V_{gsb} , that value coincides with the value of the equation (5) discussed above in conjunction with the first embodiment. Thus in step S5 of Fig. 8, it may be appropriate to acquire the added voltage V_{gs} as a composite of the effects of the voltage V_{gsa} obtained using the processing of Fig. 28 and those of the above-described maximized voltage V_{gsb} .

On the other hand, when it is desired to accurately determine the voltage V_{gsb} that is dependent on the time t , the time t_{sr} of the latter half of the recovery may be substituted in the equation (6). This allows the voltage V_{gsb} to be acquired as expressed by the following equation (7):

$$V_{gsb} = \frac{C_{gd}}{C_{gs} + C_{gd}} \cdot V_{ds} \cdot e^{-\frac{1}{R_{gs}(C_{gs} + C_{gd})} \cdot t_{sr}} \quad \dots (7)$$

Then in step S5 of Fig. 8, the added voltage V_{gs} is determined as the composite of the voltage V_{gsb} dependent on the time t and the voltage V_{gsa} calculated in keeping with the processing of Fig. 28.

With the seventh embodiment, the determination in step S5 of Fig. 8 is replaced with the determination of whether the added voltage V_{gs} falls within a voltage region VR1 in which the added voltage is approximately equal to the

threshold voltage ($V_{td} \leq V_t \leq V_m$) or within a voltage region VR2 in which the added voltage is lower than the voltage V_{td} ($V_{gs} < V_{td}$). The definitions of the voltage regions VR1 and VR2 are illustrated in Fig. 29. The voltage region VR2 is a voltage region in which the gate-source voltage V_{gs} is regarded as approximately equal to the drain current $I_d \approx 0$ of the power MOSFET. Fig. 29 shows static characteristics of the drain current I_d and the gate-source voltage V_{gs} in a saturated region of a common MOSFET. In the circuit configuration of the seventh embodiment, a current with a characteristic different from the drain current characteristic shown in Fig. 29 may flow.

When the gate-source voltage V_{gs} is within the voltage region VR2, the drain current is difficult to flow due to a PN junction reverse bias generated between the drain and source of the power MOSFET. According to the characteristics shown in Fig. 29, the drain current I_d changes exponentially relative to the gate-source voltage V_{gs} in a sub-threshold region below the threshold voltage V_t .

In the seventh embodiment, it is determined whether the added voltage V_{gs} falls within a voltage region ($VR2 + VR1$) topped by a voltage value V_m obtained from adding up the threshold voltage V_t and a predetermined margin voltage. The threshold value is determined in such a manner that the determination condition above is met. The predetermined margin voltage may be about 10% of the threshold voltage V_t .

The voltage value V_m acquired by adding up the threshold voltage V_t and the margin voltage may be adjusted as needed because the voltage value varies depending on device characteristics and operating conditions (e.g., load current). Also, the threshold voltage V_t can vary significantly from one element manufacturer to another given their diverse technological levels. With the effects of the varying technological levels taken into consideration, the highest of the diverse threshold values may be adopted as the threshold voltage V_t . This threshold value V_t may then be supplemented with a margin voltage to provide the voltage value V_m that may be adopted as the uppermost voltage value.

When the element value is determined in such a manner that the added voltage V_{gs} falls within the voltage region VR1, time-dependent waveforms are obtained as shown in Fig. 30. The particularly noticeable waveforms here are

those indicated by (i), (k) and (l) in Fig. 30. The gate-source voltage V_{gs1} of the power MOSFET 3H is topped (see the part indicated by reference character Y in (i) of Fig. 30) by a voltage approximately equal to the threshold voltage V_t (within the voltage region VR1 according to the above-discussed definitions).

5 When the gate-source voltage V_{gs1} of the MOSFET 3H becomes approximately equal to the threshold voltage V_t and falls within the voltage region VR1, the channel current flowing through the MOSFET 3H increases so that a transient current change in the MOSFETs 3H and 3L in the latter half of the recovery becomes less pronounced (see the part ranging from a broken line to a
10 solid line as indicated by reference character Z in (k) and (l) in Fig. 30).

Simulations and experiments are carried out as described below to verify what is discussed above. Fig. 31 shows a current change in effect when the element value for which the condition of the added voltage V_{gs} falling within the voltage region VR2 is met is adopted. Fig. 32 shows a current change in
15 effect when the element value for which the condition of the added voltage V_{gs} falling within the voltage region VR1 is met is adopted. Fig. 33 shows a current change in effect when the circuit configuration of the prior art (patent document 1) is adopted.

Where the circuit configuration of patent document 1 is used as a
20 comparative example, the self turn-on phenomenon occurs as shown in Fig. 33. As a result of this, the drain current gradient di/dt in the latter half of the recovery becomes steeper and the ringing of the drain current becomes greater correspondingly. However, adoption of the element value for which the condition of the added voltage V_{gs} falling within the voltage region VR2 is met
25 suppresses the self turn-on phenomenon. This reduces the ringing of the drain current waveform as shown in Fig. 31.

Even when the element value for which the condition of the added voltage V_{gs} falling within the voltage region VR1 is met is adopted, the self turn-on phenomenon is suppressed. Thus as shown in Fig. 32, the ringing is
30 shown to be held smaller than in the current waveform of Fig. 33. Also, the current change gradient (dI_d/dt) in the latter half of the recovery is shown to be less steep (i.e., with a smaller absolute value) than in the current waveform of Fig. 31.

Further, valuation experiments are conducted to verify the surge voltage characteristic of the drain-source voltage V_{ds} of the MOSFET 3H, using a circuit in which an inductive load (corresponding to the stator coil 4) is coupled to the supply node of the DC power source 2 as shown in Fig. 34. As the test conditions, it is determined that the supply voltage of the DC power source 2 is 200V, the load current is 10A, and the inductive load 4 in Fig. 34 is 300 μ H, and that the value of the resistor R_d is varied from 0 Ω to 20 Ω to 50 Ω to 100 Ω .

While the impedance element Z_L (resistor R_d) coupled between the gate and the source of the power MOSFET 3H is being varied under the above-described conditions, the drain-source voltage V_{ds} of the power MOSFET 3H is observed. The resulting transient response waveforms are shown in Fig. 35 ($R_d=0\Omega$), in Fig. 36 ($R_d=20\Omega$), in Fig. 37 ($R_d=50\Omega$), and in Fig. 38 ($R_d=100\Omega$). The measurements of the switching loss W and of the surge voltage V_{srg} are summarized in Fig. 39 using relative levels.

As shown in Fig. 39 plotting the surge voltage measurements, the higher the value of the resistor R_d , the smaller the maximum value of the drain-source voltage V_{ds} becomes and so does the surge voltage V_{srg} [V]. It can be seen that the switching loss W [μ J] is the smallest when the adopted resistance value R_d of the impedance element Z_L is 20 [Ω] or thereabout.

It is shown in Fig. 39 that the lower the resistance value R_d , the smaller the switching loss W becomes but that an excessively low resistance value can raise the switching loss due to increased ringing. Under these circumstances, the element value may be determined by a trade-off of the necessary voltage characteristic against the switching loss involved.

The above-described evaluation results provide an example of resistance value dependency. For example, the value of the voltage V_{gsb} varies depending on the capacitance values C_{ds} and C_{gs} . It is noted based on this results that the resistance value R_d , to be determined by a trade-off of the various sizes (gate width and gate length) of the power MOSFETs 3H and 3L, varies in diverse fashion.

According to the seventh embodiment, the element value is adopted for which the added voltage V_{gs} falls within the voltage region VR_1 , which is larger than the threshold voltage V_{td} of the MOSFET and smaller than a voltage V_m .

This voltage V_m is determined as a sum of a threshold voltage V_t determined based on the drain current characteristic of Fig. 29 and a margin of 10% of the threshold voltage V_t . Thus the seventh embodiment makes ringing smaller than the comparable setup of the related art. The switching loss W can also be reduced.

Ringing is also reduced when the element value is adopted for which the added voltage V_{gs} falls within the voltage region $VR1$ in which the added voltage is approximately equal to the threshold voltage V_t . The surge voltage can also be lowered as well.

(Other embodiments)

It should be understood that the driver circuit for MOSFET is not limited to the above-described embodiments and that various modifications, variations and alternatives to be outlined below may be made so far as they are within the scope of the appended claims or the equivalents thereof.

For example, as discussed in conjunction with the first embodiment, it is possible to configure, in separate entities, the resistor R_{nH} conducting when the switching speed control circuit 8H is turned on, the resistor R_{fH} conducting when the switching speed control circuit 8H is turned off, the resistor R_{nL} conducting when the switching speed control circuit 8L is turned on, and the resistor R_{fL} conducting when the switching speed control circuit 8L is turned off. This configuration allows the turn-on and turn-off speeds to be controlled individually.

Where the current change in the latter half of the recovery at turn-on time is considerably larger than at turn-off time, the resistors R_{nH} and R_{fH} may be required to have a different resistance value each, and so may be the resistors R_{nL} and R_{fL} . In such a case, the resistance values of the resistors R_{nH} , R_{nL} , R_{fH} and R_{fL} may be controlled individually to facilitate adjusting to the required turn-on time and turn-off time. Consequently, it becomes easier to complete the switching within the required switching time and to reduce the switching loss at the same time.

It is possible to adopt the circuit configuration of the above-described embodiments only for the driver circuit 6H of the power MOSFET 3H on the high side while utilizing the circuit configuration of the prior art for the driver circuit 6L of the power MOSFET 3L on the low side. In such a case, as the prior art circuit

in place of the driver circuit 6L, a suitable configuration may be adopted to have the power MOSFET 6L turned on through an on-switch. This circuit configuration provides the same effects as those of the above-described embodiments.

5 Conversely, it is also possible to adopt the circuit configuration of the above-described embodiments only for the driver circuit 6L of the power MOSFET 3L on the low side while utilizing the circuit configuration of the prior art for the driver circuit 6H of the power MOSFET 3H on the high side. In this case, as the prior art circuit in place of the driver circuit 6H, an appropriate
10 configuration may be adopted to have the power MOSFET 6H turned on through an on-switch. This circuit configuration also provides the same effects as those of the above-described embodiments.

CLAIMS

1. A power MOSFET driver circuit for driving a voltage-driven first power MOSFET (3H) and a voltage-driven second power MOSFET (3L) in half-bridge coupling between a first power wire and a second power wire, the first and the second power MOSFETs having an inductive load (4) coupled therebetween, the driver circuit comprising:

a first conduction switching circuit (7H) configured to turn on and leave open a supply voltage relative to the potential of a low-potential reference terminal of the first power MOSFET as a reference potential, the first conduction switching circuit (7H) having a first on-switch (S1H) and a first off-switch (S2H) coupled in series between a supply terminal of the supply voltage and the low-potential reference terminal;

a first charging/discharging circuit (8H) coupled between the first conduction switching circuit and a control terminal of the first power MOSFET, the first charging/discharging circuit (8H) adjusting a speed at which the control terminal of the first power MOSFET is electrically charged and discharged;

a first impedance switching part (9H) coupled between the control terminal and the low-potential reference terminal of the first power MOSFET, the first impedance switching part (9H) switching the impedance between the control terminal and the low-potential reference terminal between a first impedance state and an open state, the first impedance state being a state in which the impedance is higher than an impedance of the first charging/discharging circuit, the open state being a state in which the impedance is higher than in the first impedance state;

a second conduction switching circuit (7L) configured to turn on and leave open a supply voltage relative to the potential of a low-potential reference terminal of the second power MOSFET as a reference potential, the second conduction switching circuit (7L) having a second on-switch (S1L) and a second off-switch (S2L) coupled in series between a supply terminal of the supply voltage and the low-potential reference terminal;

a second charging/discharging circuit (8L) coupled between the second conduction switching circuit and a control terminal of the second power MOSFET,

the second charging/discharging circuit (8L) adjusting a speed at which the control terminal of the second power MOSFET is electrically charged and discharged;

5 a second impedance switching part (9L) coupled between the control terminal and the low-potential reference terminal of the second power MOSFET, the second impedance switching part (9L) switching the impedance between the control terminal and the low-potential reference terminal between a second impedance state to an open state, the second impedance state being a state in which the impedance is higher than an impedance of the second
10 charging/discharging circuit, the open state being a state in which the impedance is higher than in the second impedance state, and

a control section (11) configured to control the switching between states by the first and the second conduction switching circuits and the switching between states by the first and the second impedance switching parts;

15 wherein the control section (11) is configured to perform switching control in such a manner that:

in a first interval (T1), a k-th on-switch (S1H or S1L) is turned on and a k-th off-switch (S2H or S2L) is turned off, where a reference character "k" denotes one of integers 1 and 2;

20 in a second interval (T2), the k-th on-switch is turned off and thereafter the k-th off-switch is turned on, and

in a third interval (T3), the k-th off-switch is turned off and, at the same time, a k-th impedance switching part (9H or 9L) is switched to a predetermined k-th impedance state and an m-th on-switch is turned on, where reference
25 character "m" is the other of the integers 1 and 2.

2. The power MOSFET driver circuit according to claim 1, wherein:
the control section (11) is configured to further control,

30 in the second interval (T2), the k-th impedance switching part to be held in the open state and the m-th off-switch is turned on after the k-th on-switch is turned off, and

in the third interval (T3), the k-th impedance switching part to be switched to the predetermined k-th impedance state from the open state.

3. The power MOSFET driver circuit according to claim 1, wherein:
the control section (11) is configured to control the k-th on-switch, the
k-th off-switch, the m-th on-switch and the m-th off-switch, in such a manner
that:

in the second interval (T2), the k-th impedance switching part is
switched from the open state to the predetermined k-th impedance state at the
same time as the k-th off-switch is turned on.

4. The power MOSFET driver circuit according to any one of claims 1
through 3, wherein:

the control section (11) is configured to perform the switching control in
such a manner that, before a current of the m-th power MOSFET is made to
exceed a predetermined settling current for the first time with the m-th
on-switch turned on to electrically charge the control terminal of the m-th power
MOSFET through the m-th charging/discharging circuit, the impedance of the
k-th impedance switching part is switched to the predetermined k-th impedance
state at the same time as the k-th off-switch is turned off.

5. An element value determining method for determining element
values of the k-th impedance switching part of the power MOSFET driver circuit
according to any one of claims 1 through 4, the element value determining
method comprising steps of:

adding up an induced electromotive force generated in a parasitic
inductance of a source of the k-th power MOSFET in response to a recovery
current generated in a parasitic diode of the k-th power MOSFET, and a voltage
generated by parasitic capacitance coupling of the k-th power MOSFET; and

determining element values by which an added voltage remains below a
threshold voltage of the k-th power MOSFET, as the element values of the k-th
impedance switching part.

6. An element value determining method for determining element
values of the k-th impedance switching part of the power MOSFET driver circuit

according to any one of claims 1 through 4, the element value determining method comprising steps of:

adding up an induced electromotive force generated in a parasitic inductance of the source of the k-th power MOSFET in response to a recovery current generated in a parasitic diode of the k-th power MOSFET, and a voltage generated by parasitic capacitance coupling of the k-th power MOSFET; and

determining element values by which an added voltage becomes larger than a threshold voltage of the k-th power MOSFET and smaller than a voltage which is a sum of a threshold voltage determined based on a drain current characteristic of the k-th power MOSFET and a +10% margin of the same, as the element values of the k-th impedance switching part.

7. A power MOSFET driver circuit for driving a voltage-driven a-th power MOSFET (3H or 3L) and a voltage-driven b-th power MOSFET (3L or 3H) in half-bridge coupling between a first power wire and a second power wire, where reference character "a" denotes one of integers 1 and 2 and reference character "b" denotes the other of the integers 1 and 2, the a-th and the b-th power MOSFETs having an inductive load (4) coupled therebetween, the driver circuit comprising:

an a-th conduction switching circuit (7H or 7L) configured to turn on and leave open a supply voltage relative to the potential of a low-potential reference terminal of the a-th power MOSFET as a reference potential, the a-th conduction switching circuit (7H or 7L) having an a-th on-switch (S1H or S1L) and an a-th off-switch (S2H or S2L) coupled in series between a supply terminal of the supply voltage and the low-potential reference terminal;

an a-th charging/discharging circuit (8H or 8L) coupled between the a-th conduction switching circuit and a control terminal of the a-th power MOSFET, the a-th charging/discharging circuit (8H or 8L) adjusting a speed at which the control terminal of the a-th power MOSFET is electrically charged and discharged;

an a-th impedance switching part (9H or 9L) coupled between the control terminal and the low-potential reference terminal of the a-th power MOSFET, the a-th impedance switching part (9H or 9L) switching the impedance

between the control terminal and the low-potential reference terminal between a predetermined a-th impedance state and an open state, the a-th impedance state being a state in which the impedance is higher than an impedance of the a-th charging/discharging circuit, the open state being a state in which the impedance is higher than in the predetermined a-th impedance state;

a b-th conduction switching circuit (7L or 7H) configured to power a control terminal of the b-th power MOSFET through a b-th on-switch (S1L or S1H) to turn on the b-th power MOSFET; and

a control section (11) configured to control the switching between states by the a-th and the b-th conduction switching circuits and the switching between states by the a-th impedance switching part,

wherein the control section (11) is configured to perform switching control in such a manner that:

in a first interval (T1), the a-th on-switch is turned on and the a-th off-switch is turned off;

in a second interval (T2), the a-th on-switch is turned off and thereafter the a-th off-switch is turned on, and

in a third interval (T3), the a-th off-switch is turned off and, at the same time, the a-th impedance switching part is switched to the predetermined a-th impedance state and the b-th on-switch is turned on.

8. The power MOSFET driver circuit according to claim 7, wherein:

the control section (11) is configured to further control, in the interval (T2), the a-th impedance switching part to be switched from the open state to the predetermined a-th impedance state.

9. An element value determining method for determining element values of the a-th impedance switching part of the power MOSFET driver circuit according to claim 7 or 8, the element value determining method comprising steps of:

adding up an induced electromotive force generated in a parasitic inductance of the source of the a-th power MOSFET in response to a recovery current generated in a parasitic diode of the a-th power MOSFET, and a voltage

generated by parasitic capacitance coupling of the a-th power MOSFET; and
determining element values by which an added voltage remains below a
threshold voltage of the a-th power MOSFET, as the element values of the a-th
impedance switching part.

5

10. An element value determining method for determining element
values of the a-th impedance switching part of the power MOSFET driver circuit
according to claim 7 or 8, the element value determining method comprising
steps of:

10

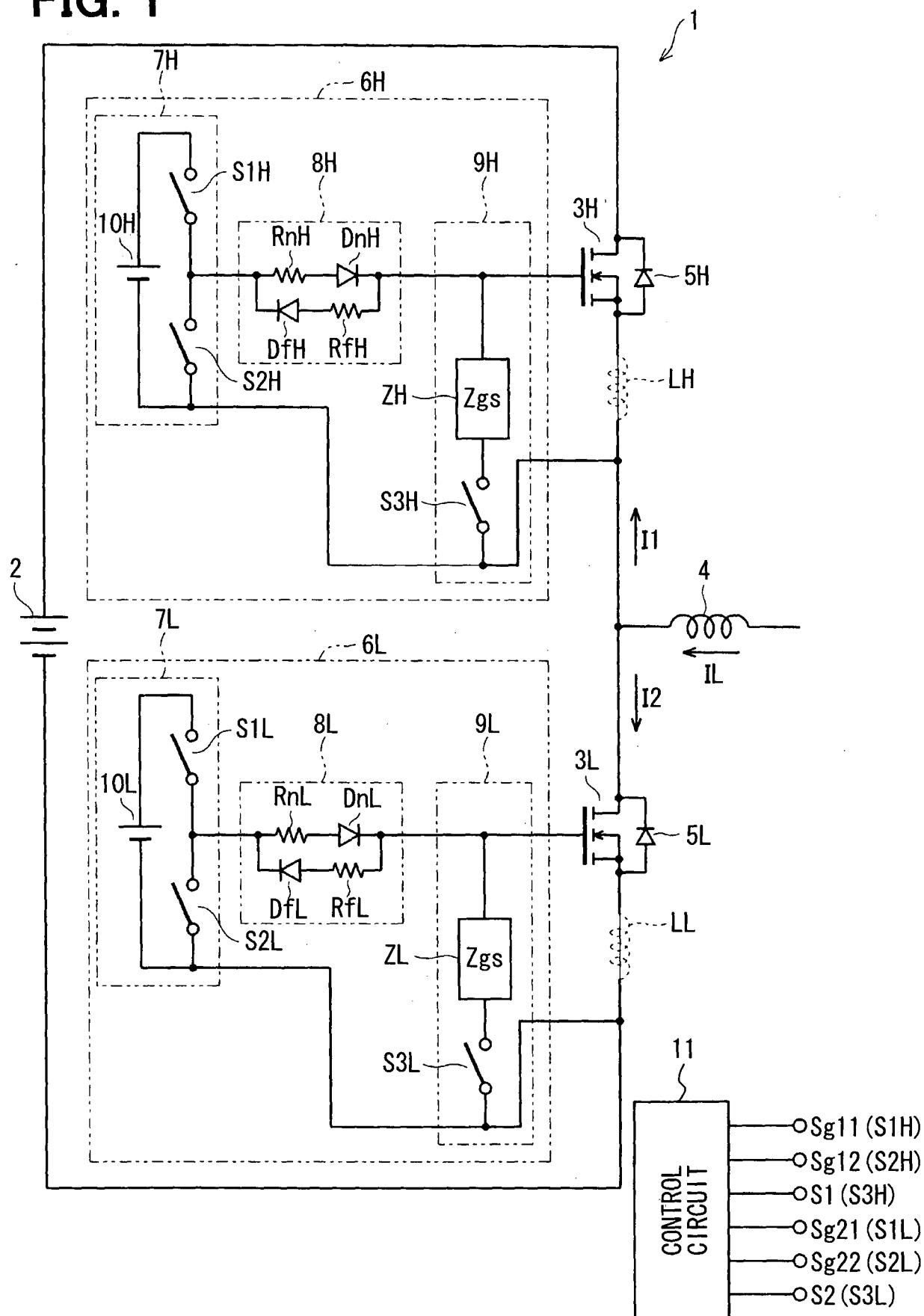
adding up an induced electromotive force generated in a parasitic
inductance of the source of the a-th power MOSFET in response to a recovery
current generated in a parasitic diode of the a-th power MOSFET, and a voltage
generated by parasitic capacitance coupling of the a-th power MOSFET; and

15

determining element values by which an added voltage becomes larger
than a threshold voltage of the a-th power MOSFET and smaller than a voltage
which is a sum of a threshold voltage determined based on a drain current
characteristic of the a-th power MOSFET and a +10% margin of the same, as the
element values of the a-th impedance switching part.

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FIG. 1



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FIG. 2A

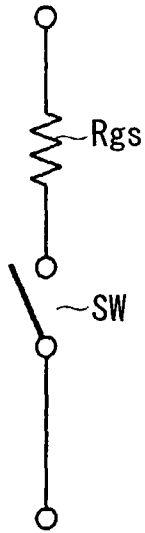


FIG. 2B

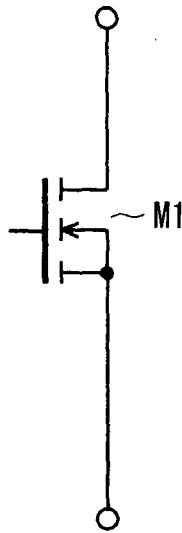


FIG. 2C

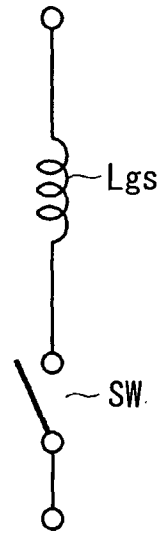


FIG. 2D

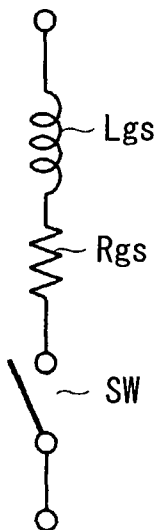
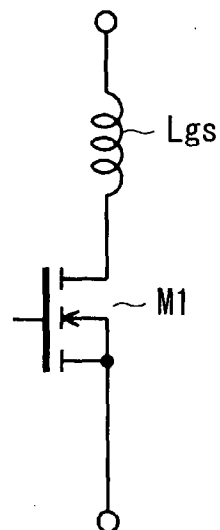


FIG. 2E



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FIG. 3A

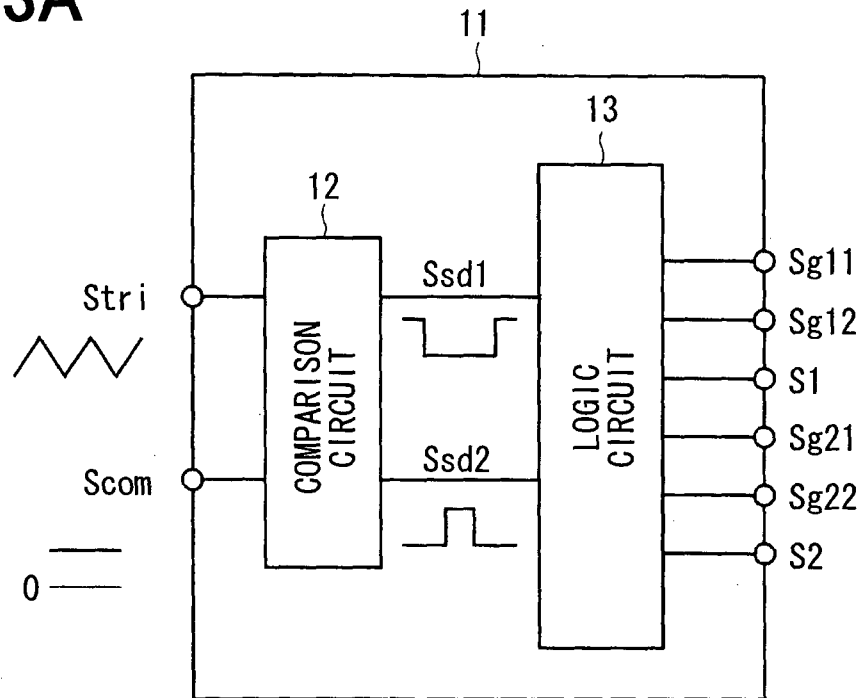


FIG. 3B

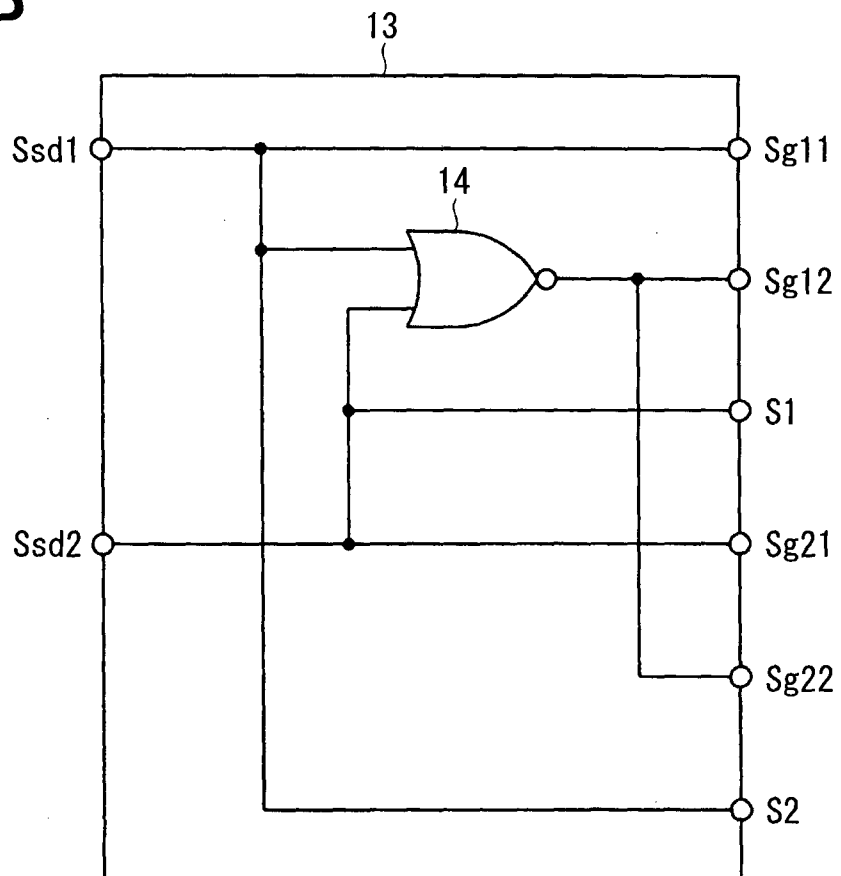


FIG. 4

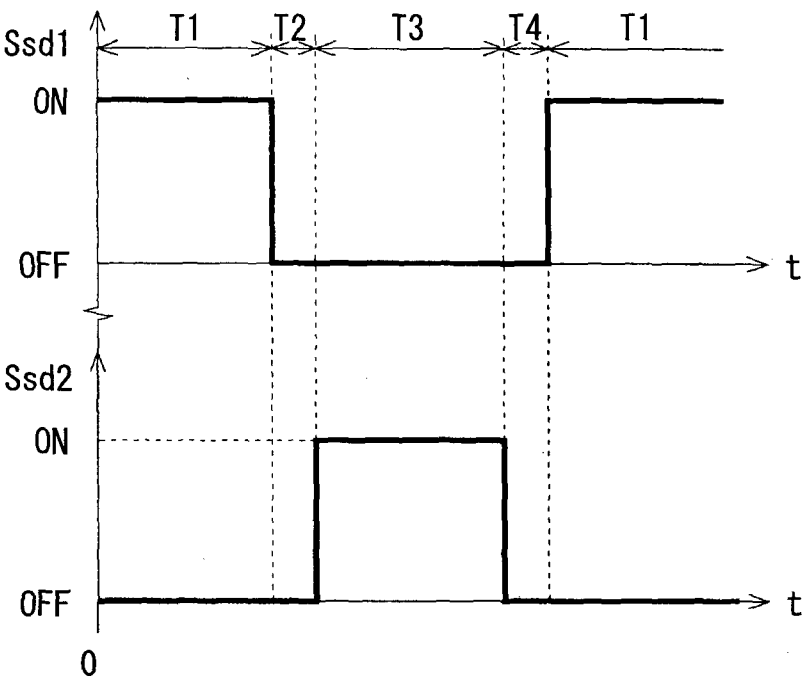
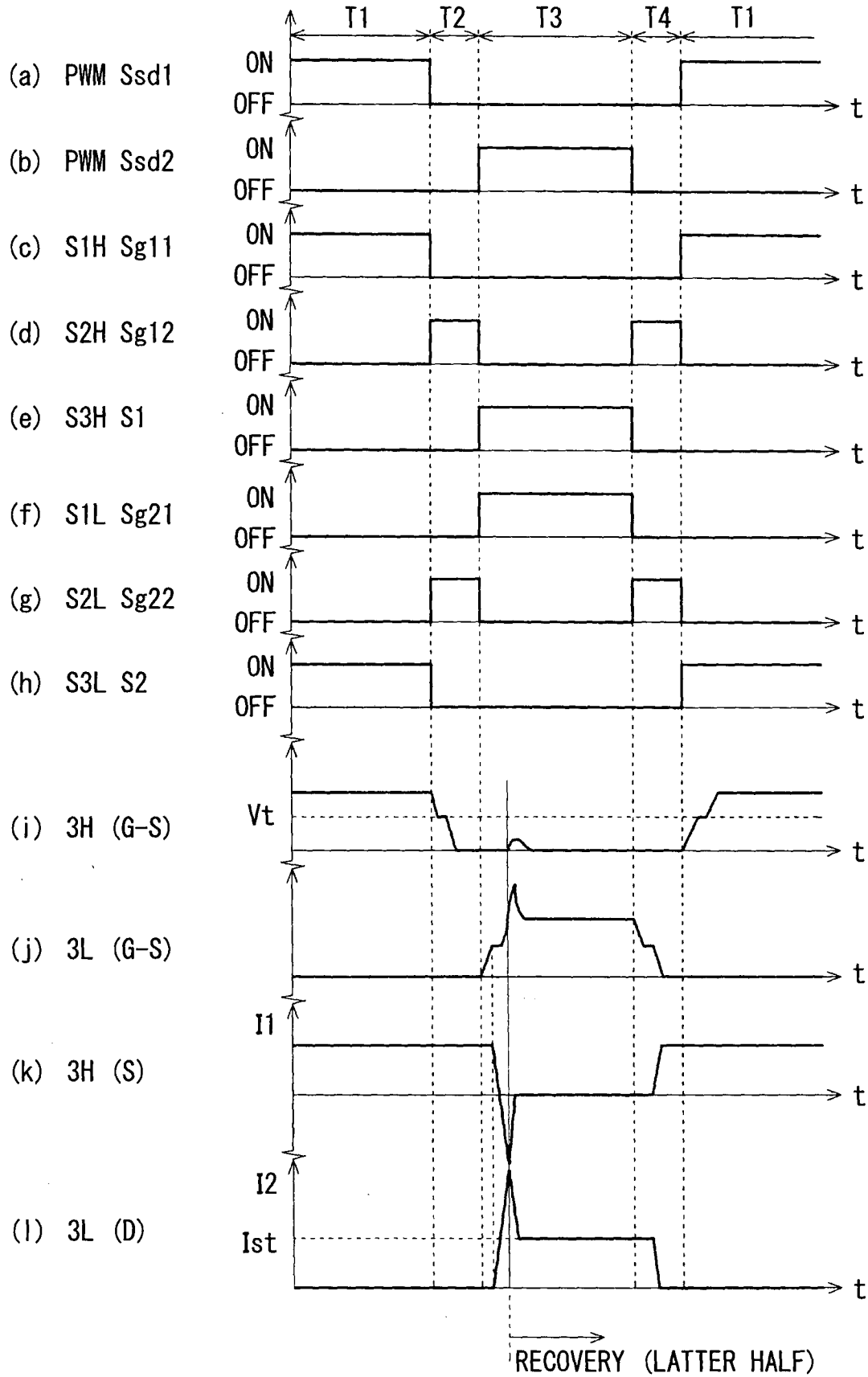


FIG. 5

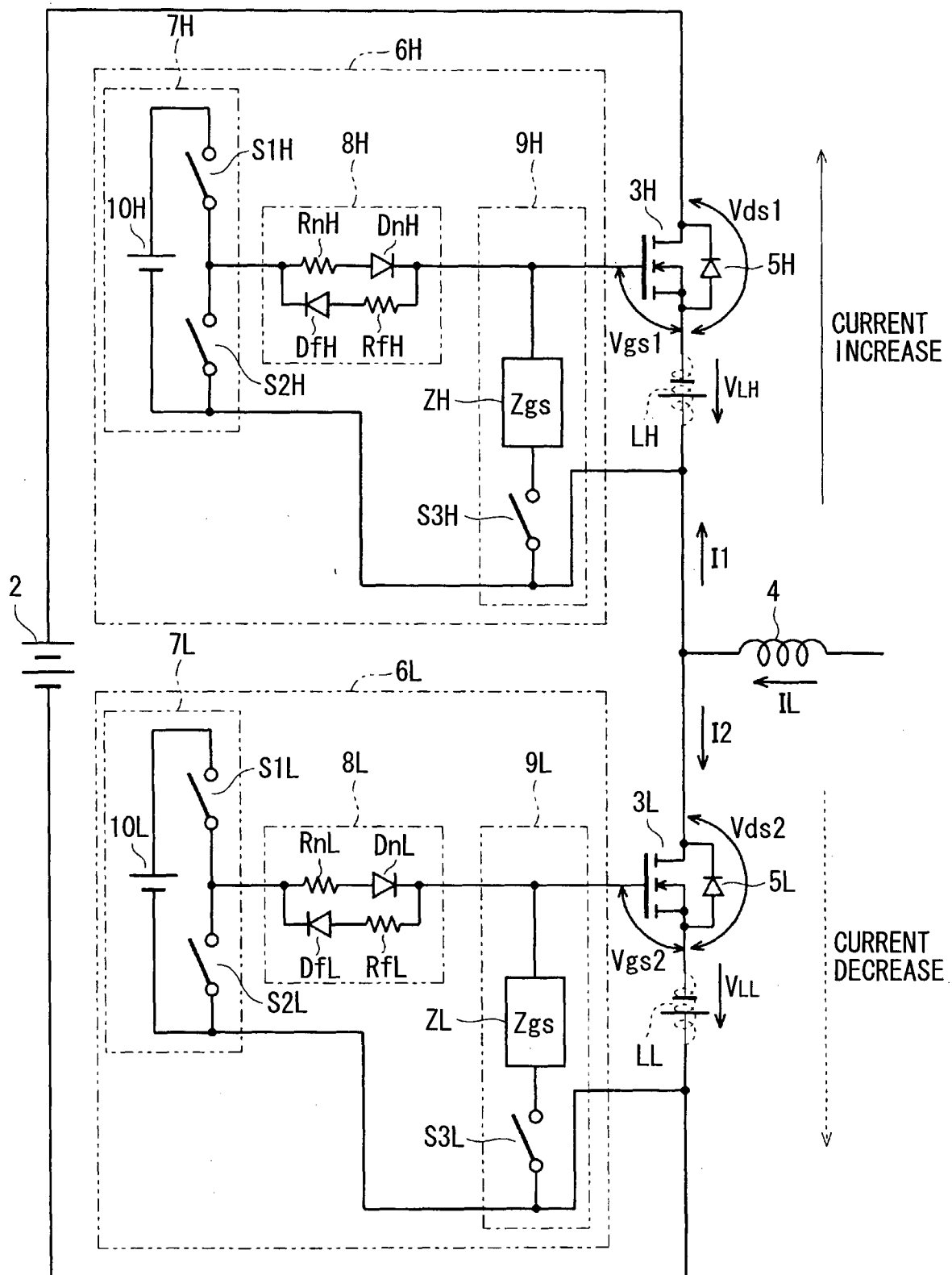
SWITCH	SIGNAL	T1	T2	T3	T4
		3H: TURN ON, REMAIN ON	3H: TURN OFF	3L: TURN ON, REMAIN ON	3L: TURN OFF
S1H	Sg11	ON	OFF	OFF	OFF
S2H	Sg12	OFF	ON	OFF	ON
S3H	S1	OFF	OFF	ON	OFF
S1L	Sg21	OFF	OFF	ON	OFF
S2L	Sg22	OFF	ON	OFF	ON
S3L	S2	ON	OFF	OFF	OFF

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FIG. 6

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FIG. 7



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FIG. 8

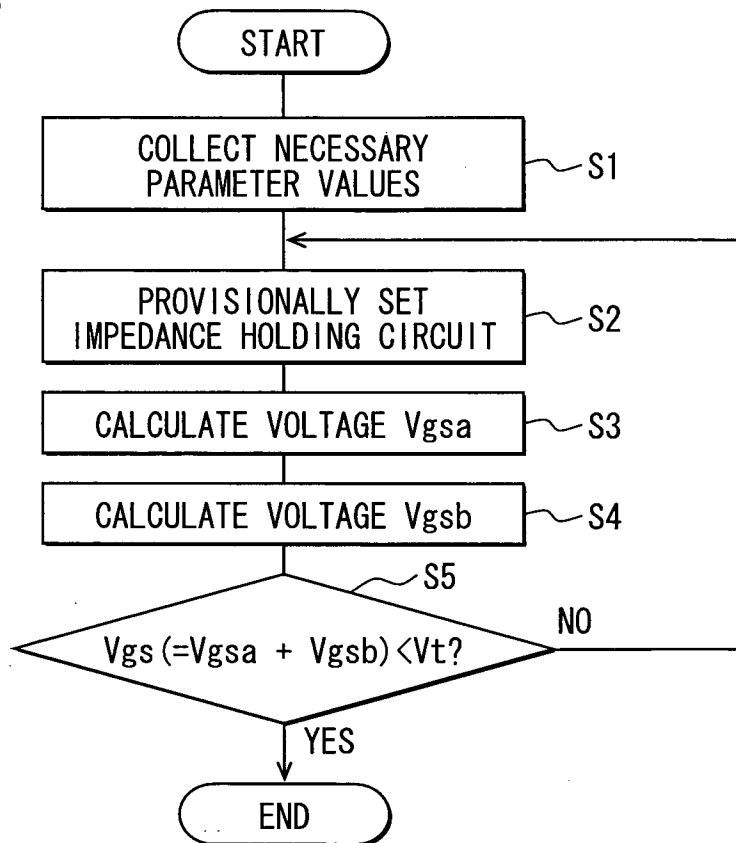


FIG. 9

SYMBOL	DEFINITION
L_s	SOURCE TERMINAL PARASITIC INDUCTANCE
di/dt	RECOVERY CURRENT GRADIENT
t_f	LATTER HALF RECOVERY TIME
C_{gs}	GATE-SOURCE PARASITIC CAPACITANCE
C_{gd}	GATE-DRAIN CAPACITANCE
V_{ds}	DRAIN-SOURCE VOLTAGE

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FIG. 10

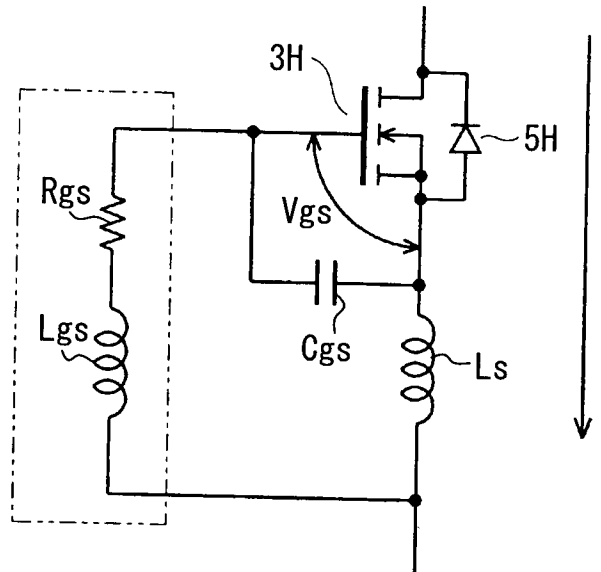


FIG. 11

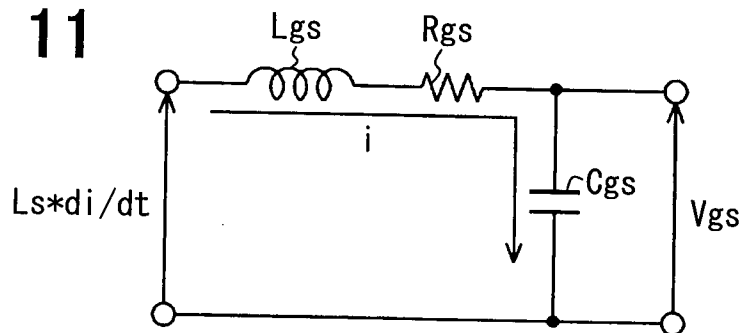
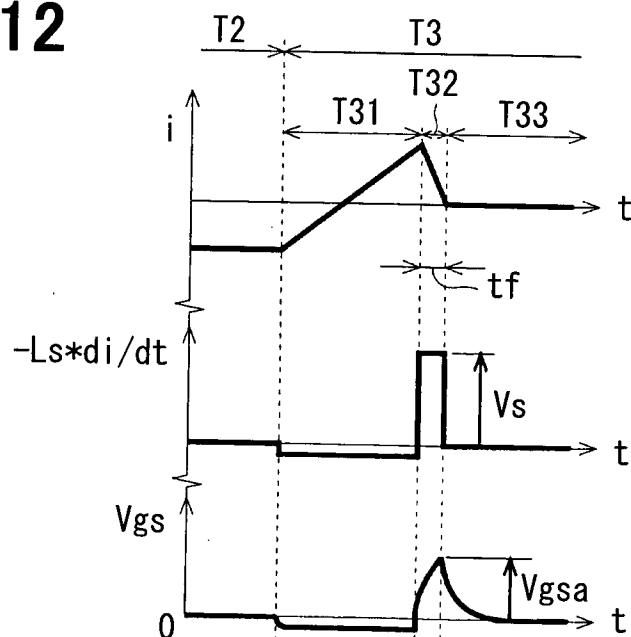


FIG. 12



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FIG. 13

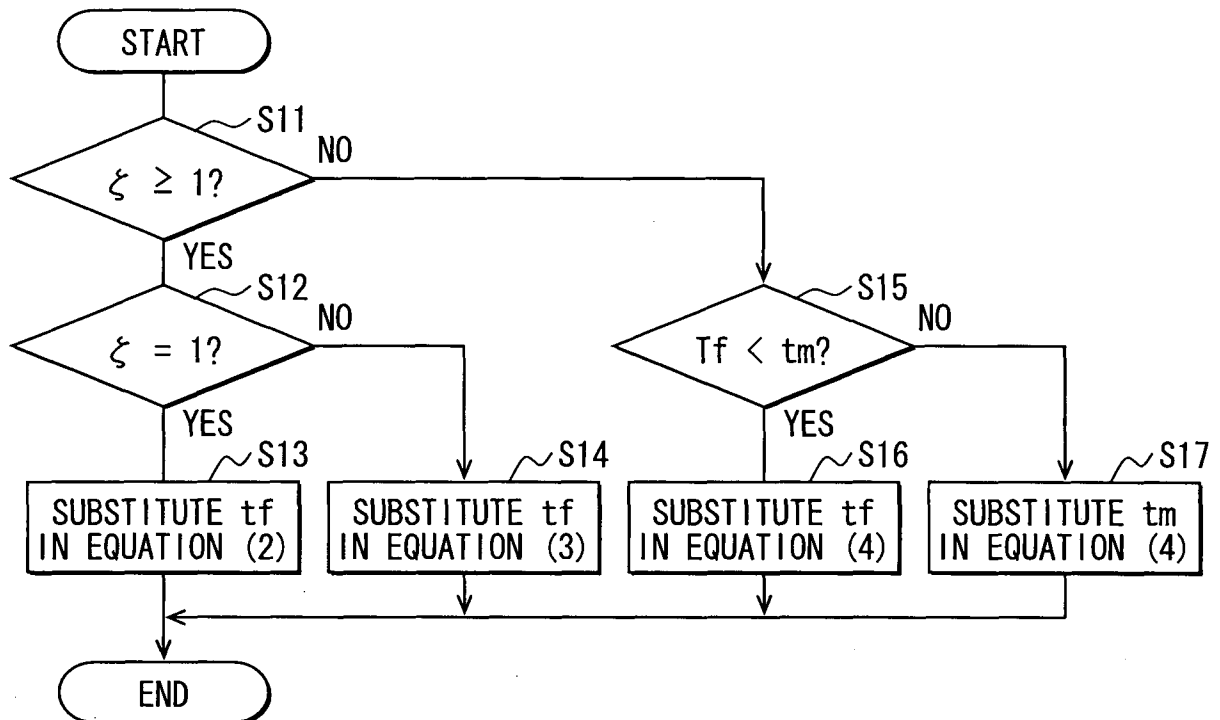
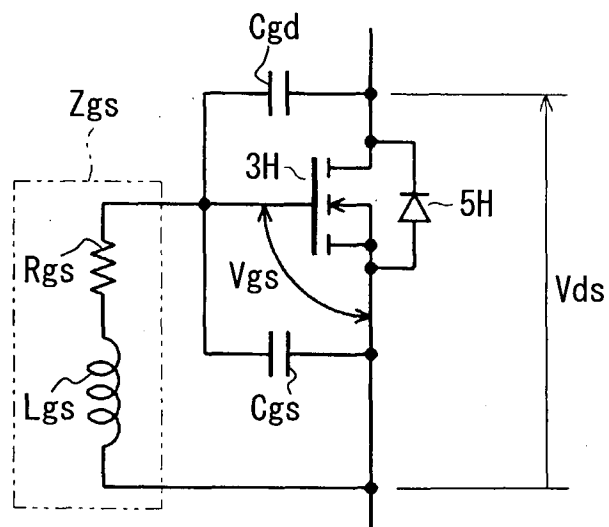


FIG. 14



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FIG. 15

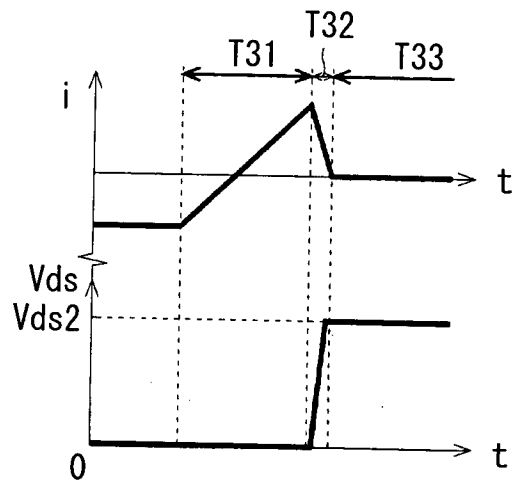
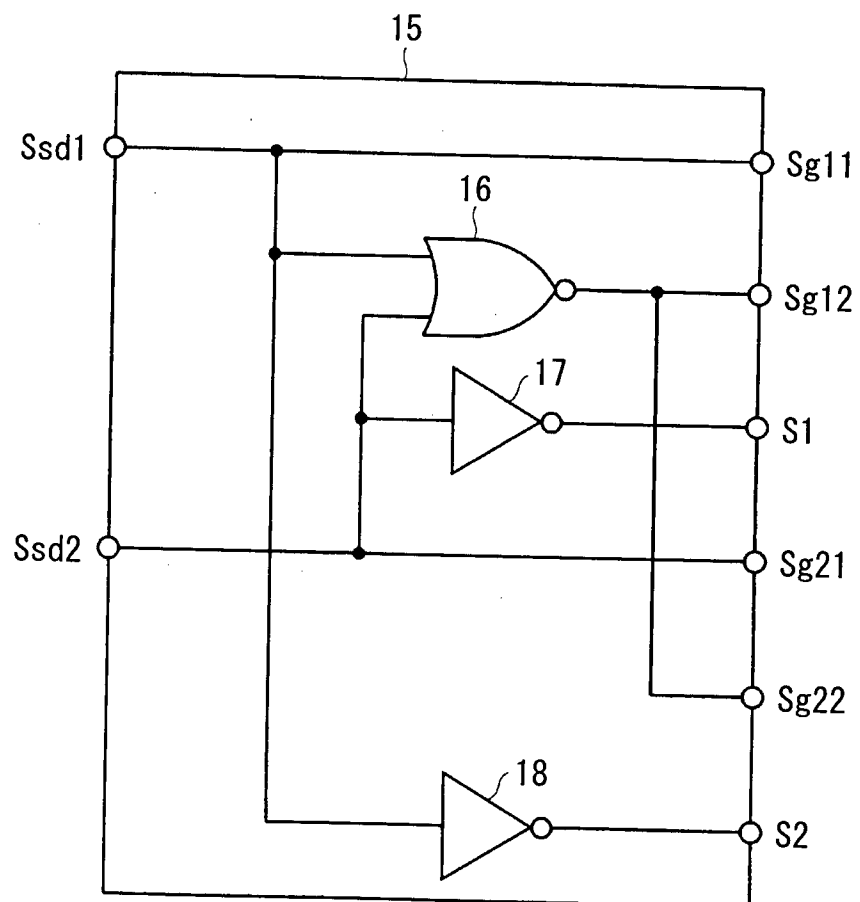


FIG. 16

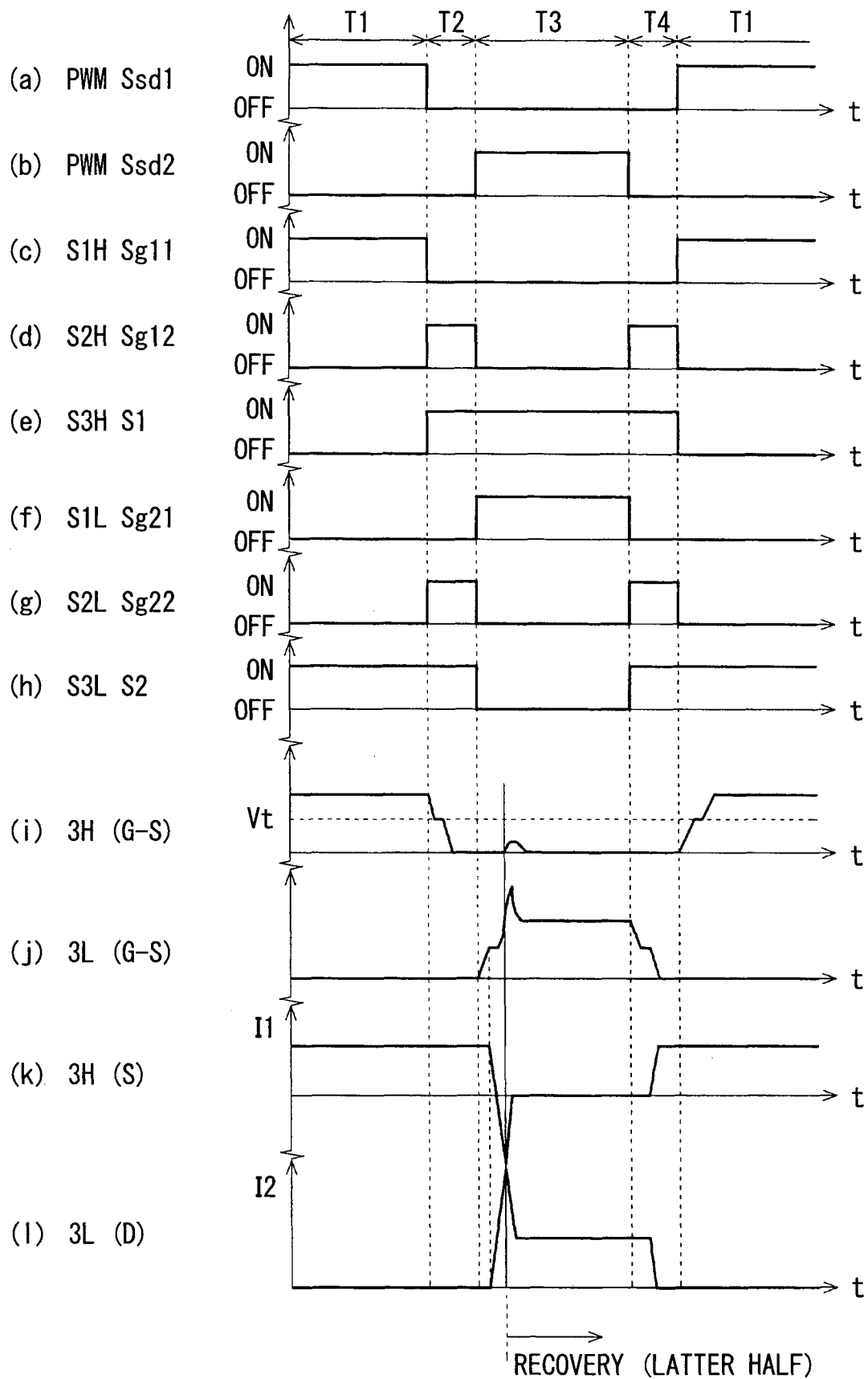


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FIG. 17

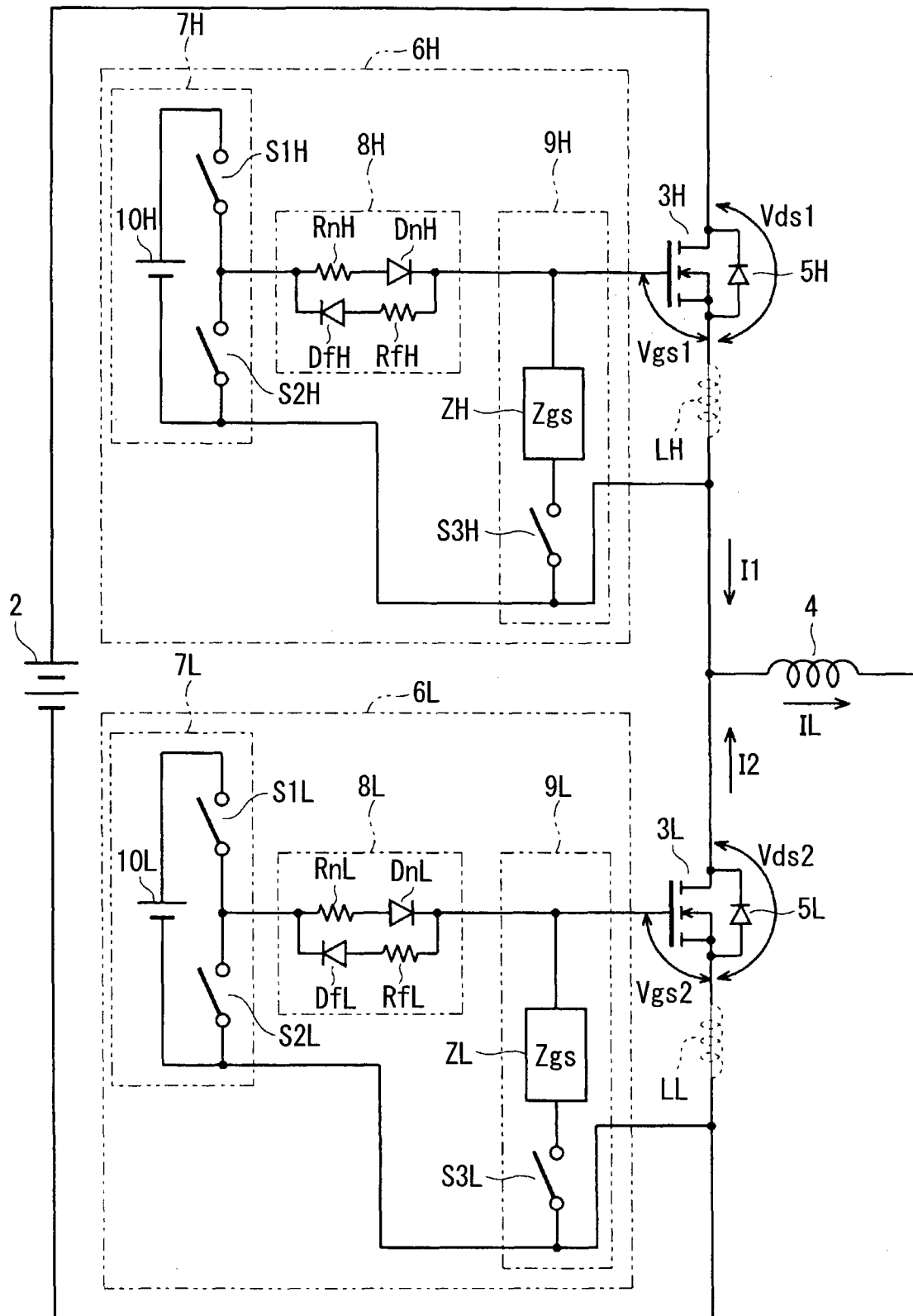
SWITCH	SIGNAL	T1	T2	T3	T4
		3H: TURN ON, REMAIN ON	3H: TURN OFF	3L: TURN ON, REMAIN ON	3L: TURN OFF
S1H	Sg11	ON	OFF	OFF	OFF
S2H	Sg12	OFF	ON	OFF	x2 (ON ON
S3H	S1	OFF	ON	ON	
S1L	Sg21	OFF	OFF	ON	OFF
S2L	Sg22	OFF	x1 (ON ON	OFF	ON
S3L	S2	ON		OFF	ON

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FIG. 18

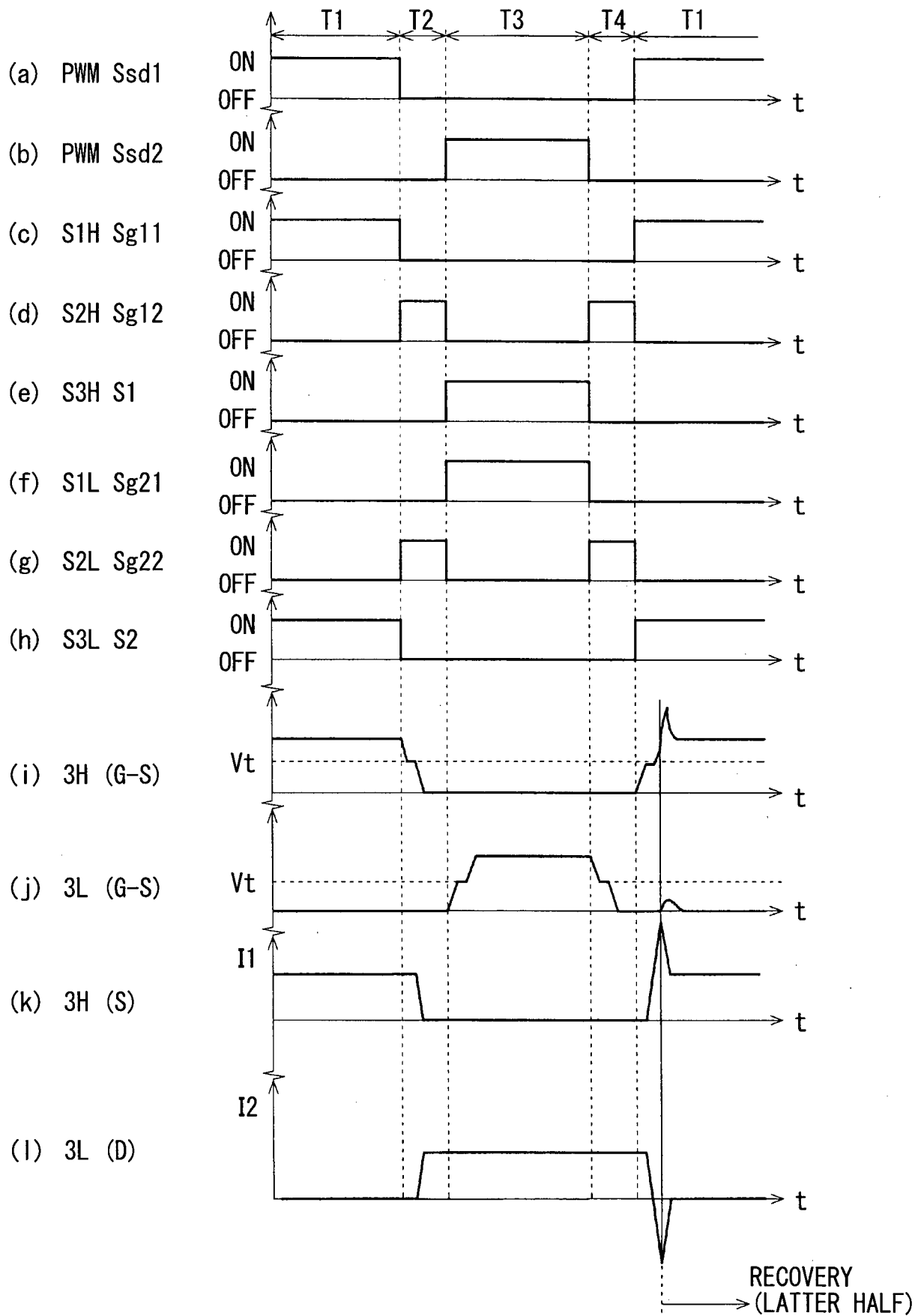
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FIG. 19



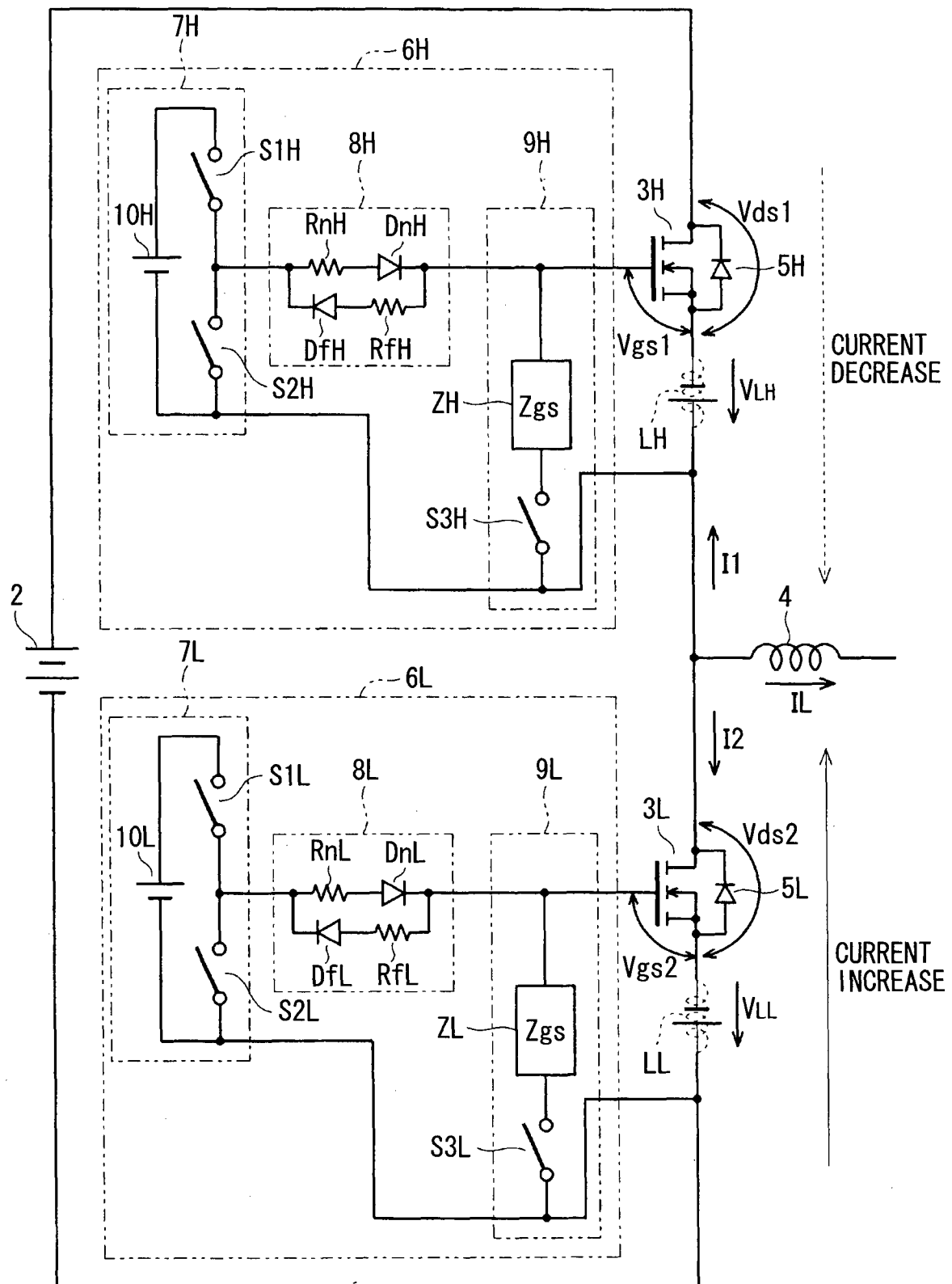
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FIG. 20



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FIG. 21



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FIG. 22

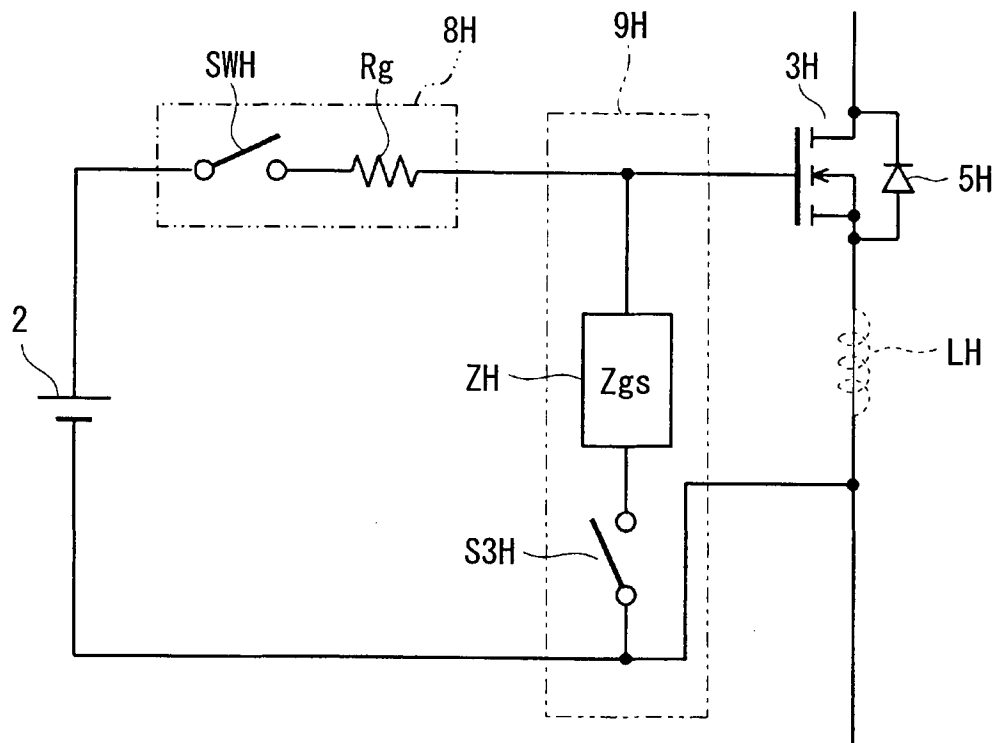
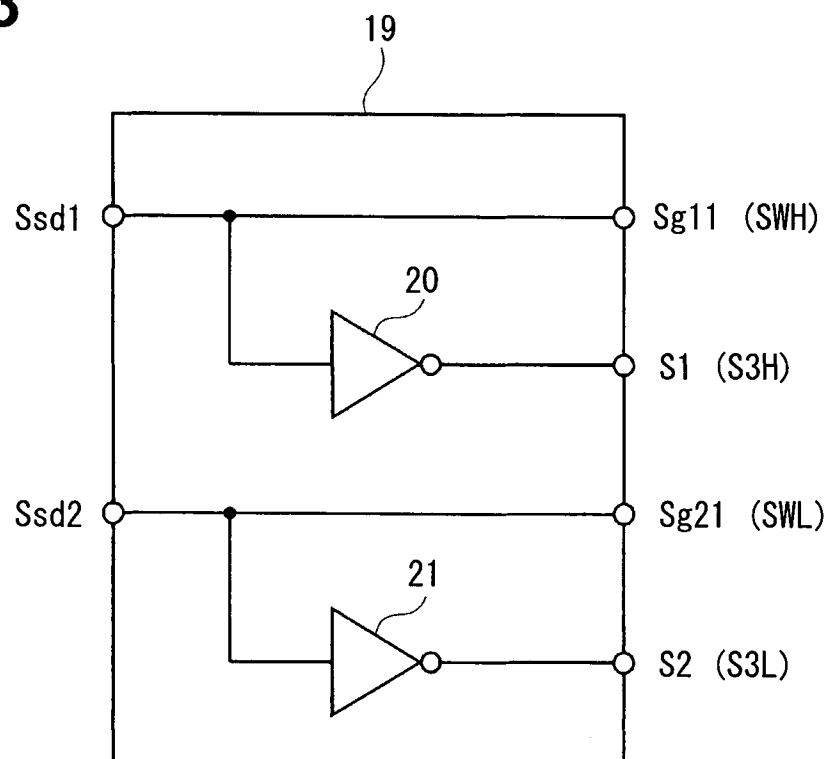
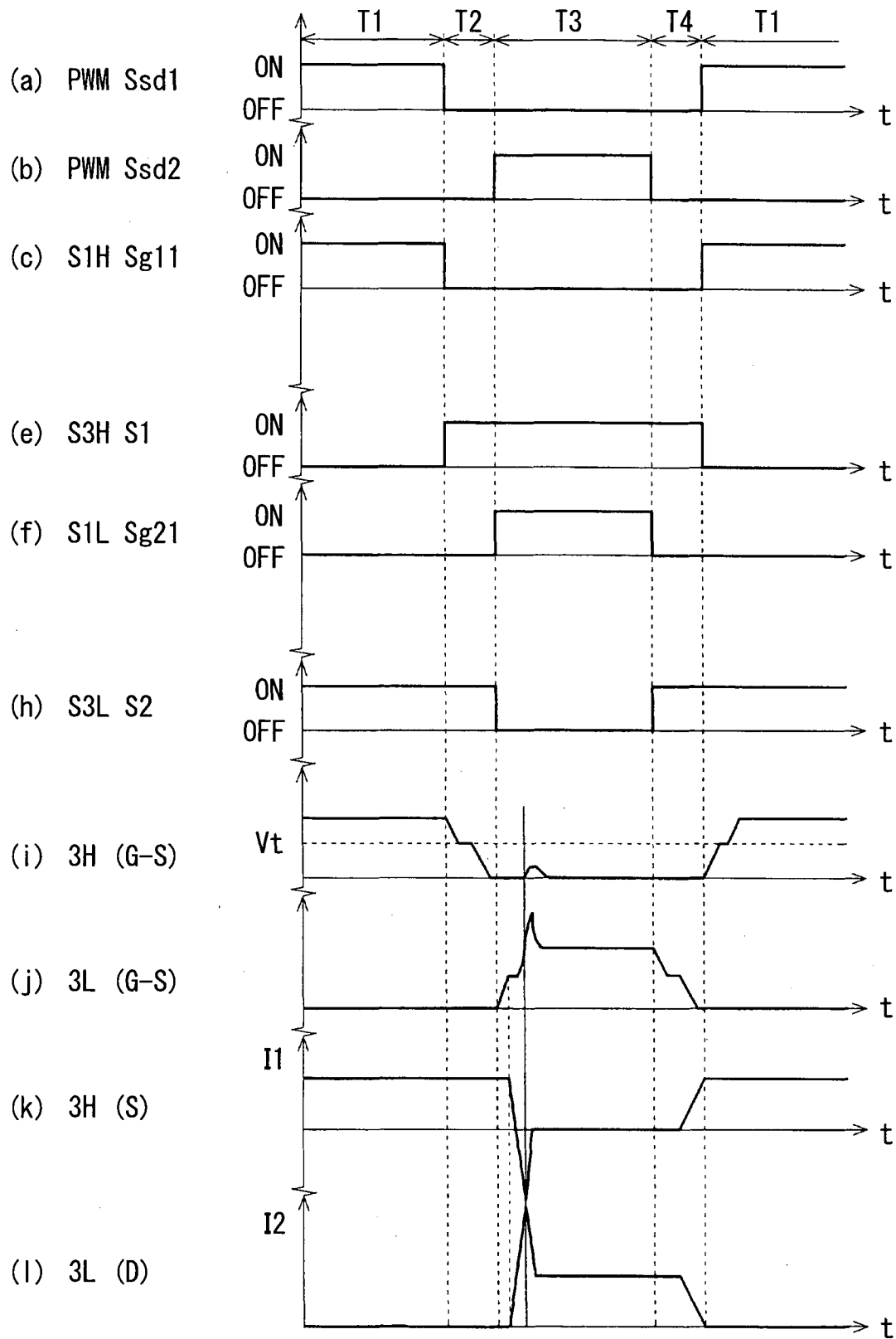


FIG. 23

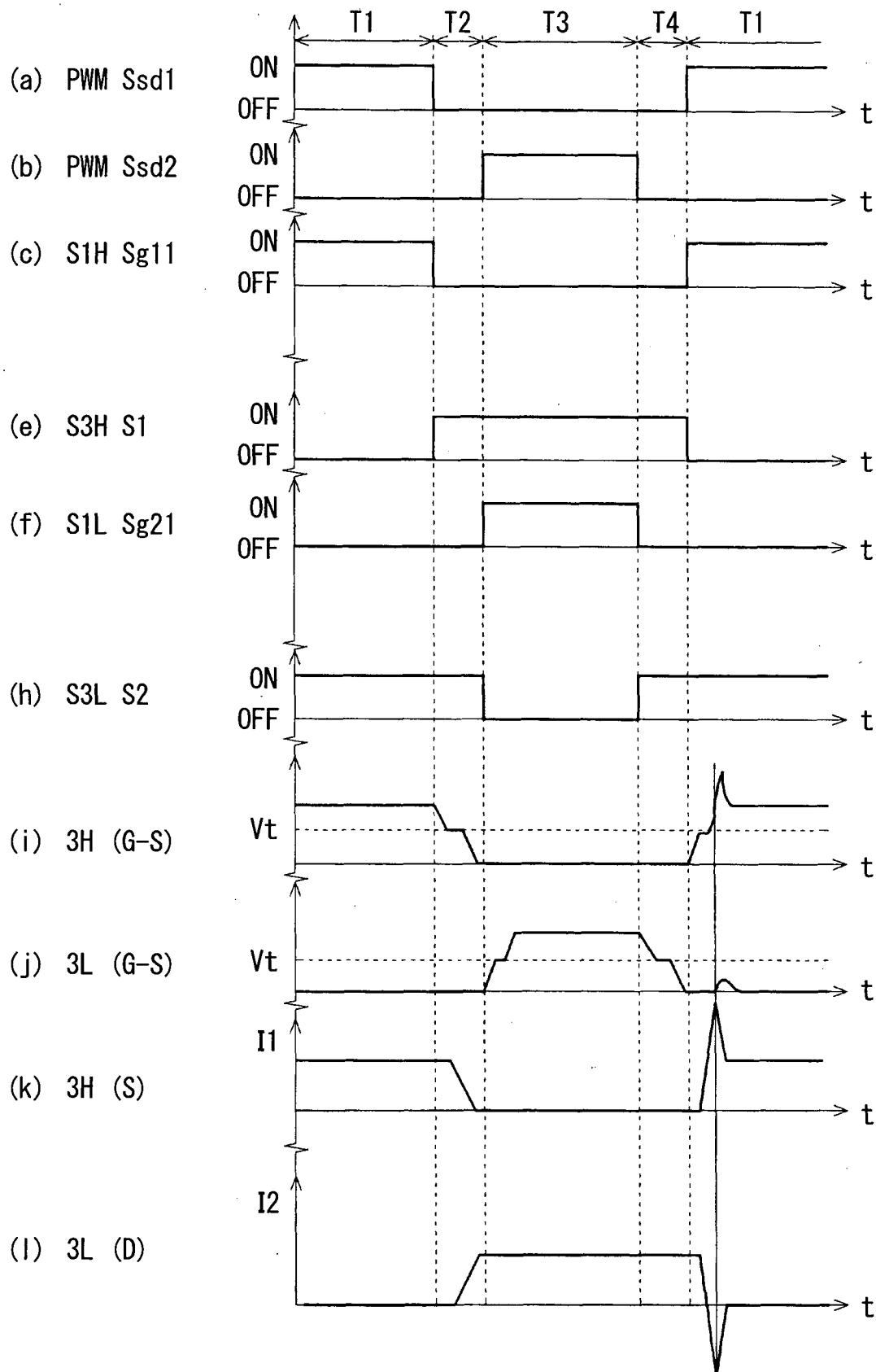


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FIG. 24



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FIG. 25

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FIG. 26A

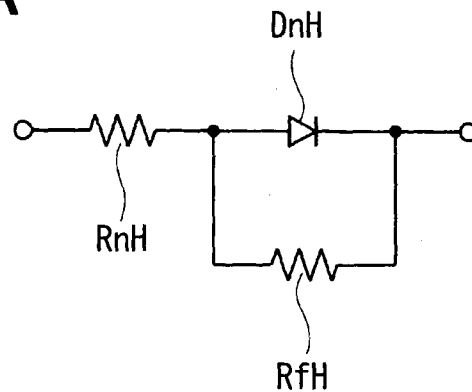


FIG. 26B

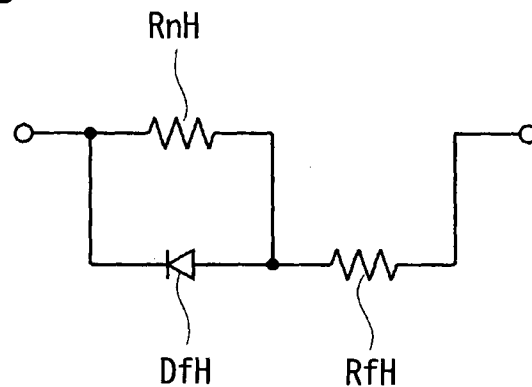


FIG. 27

SYMBOL	DEFINITION
L_s	SOURCE TERMINAL PARASITIC INDUCTANCE
di/dt	RECOVERY CURRENT GRADIENT
t_{sr}	TIME FROM RECOVERY LATTER HALF START TO CHANNEL CURRENT INJECTION
C_{gs}	GATE-SOURCE PARASITIC CAPACITANCE
C_{gd}	GATE-DRAIN CAPACITANCE
V_{ds}	DRAIN-SOURCE VOLTAGE

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FIG. 28

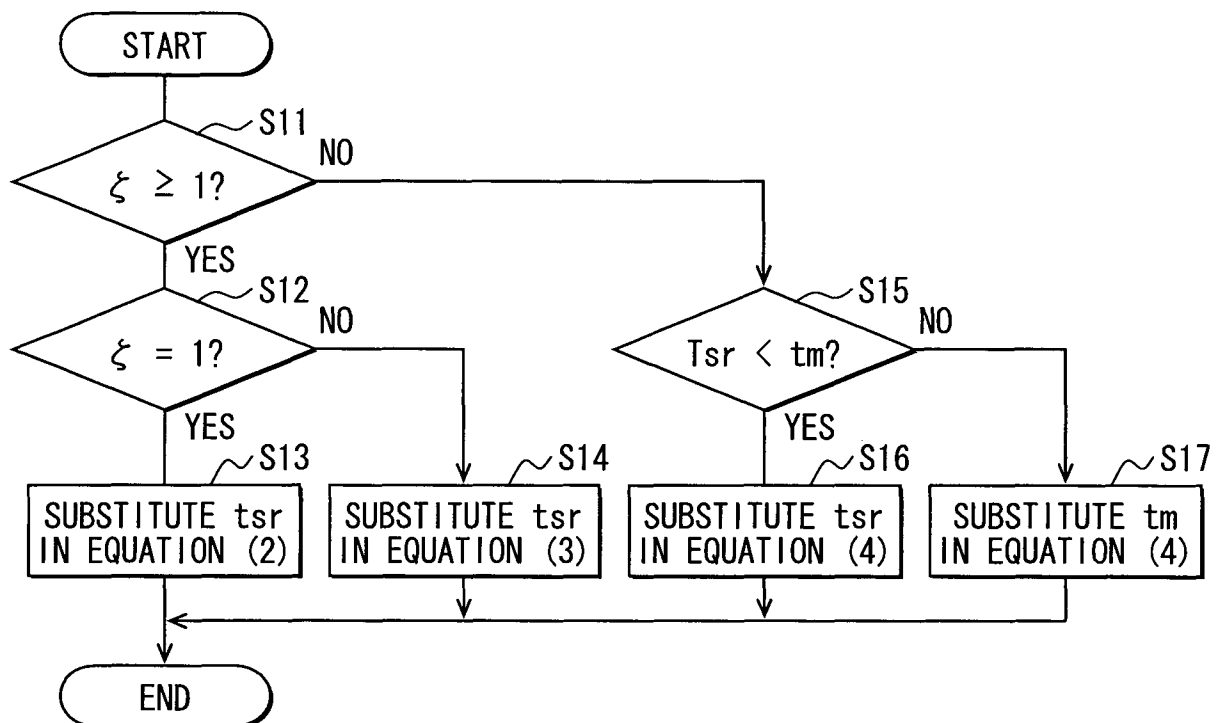
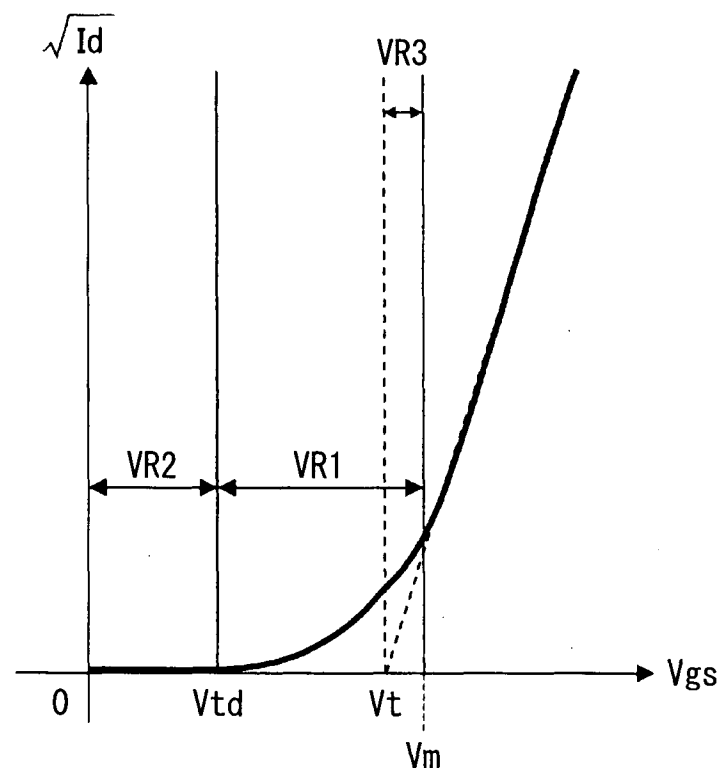
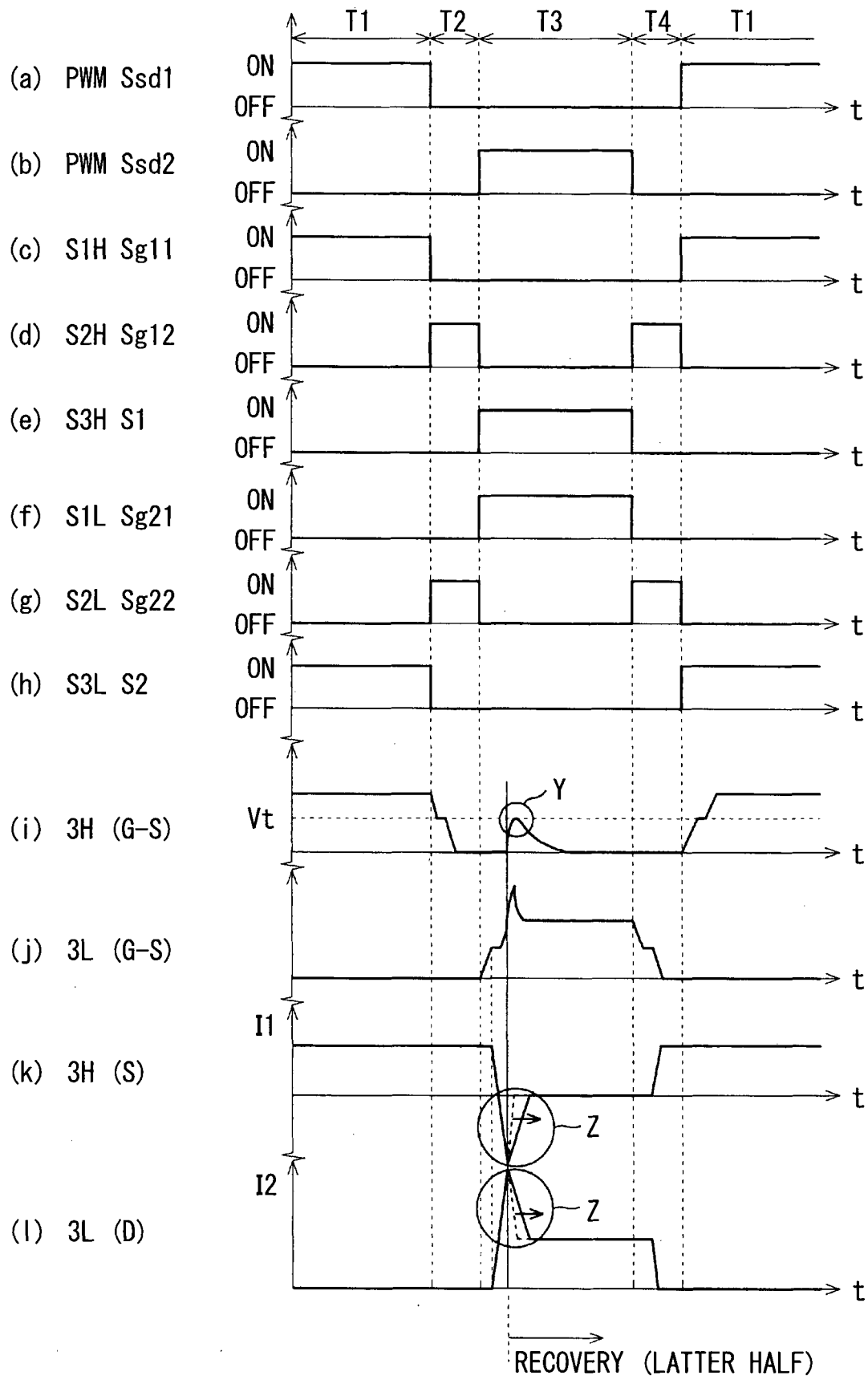


FIG. 29

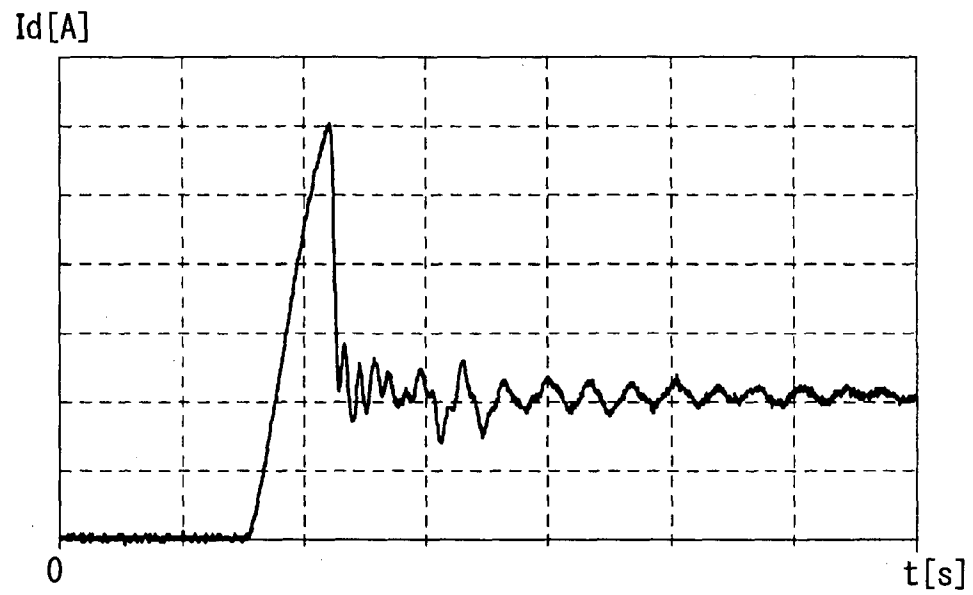
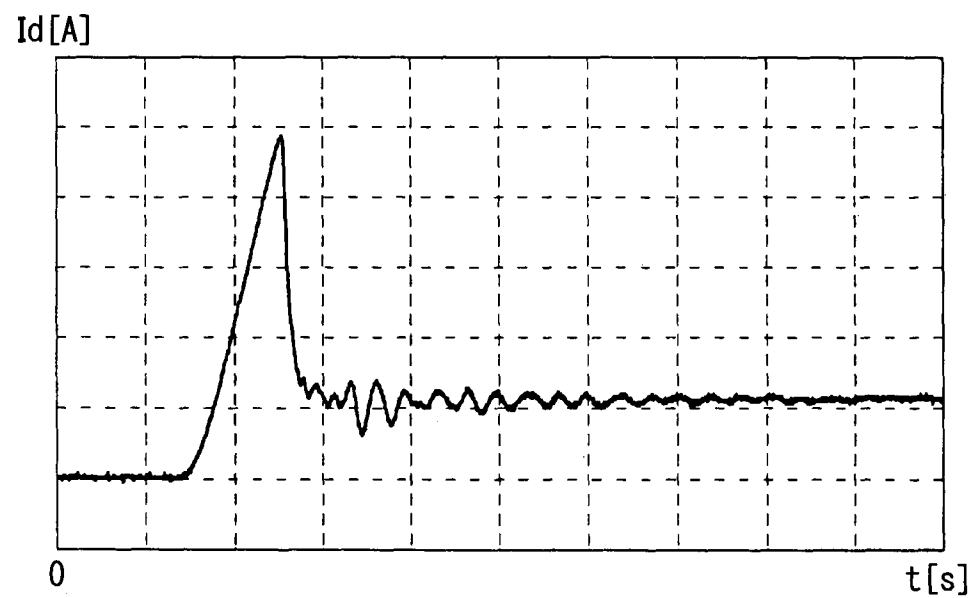


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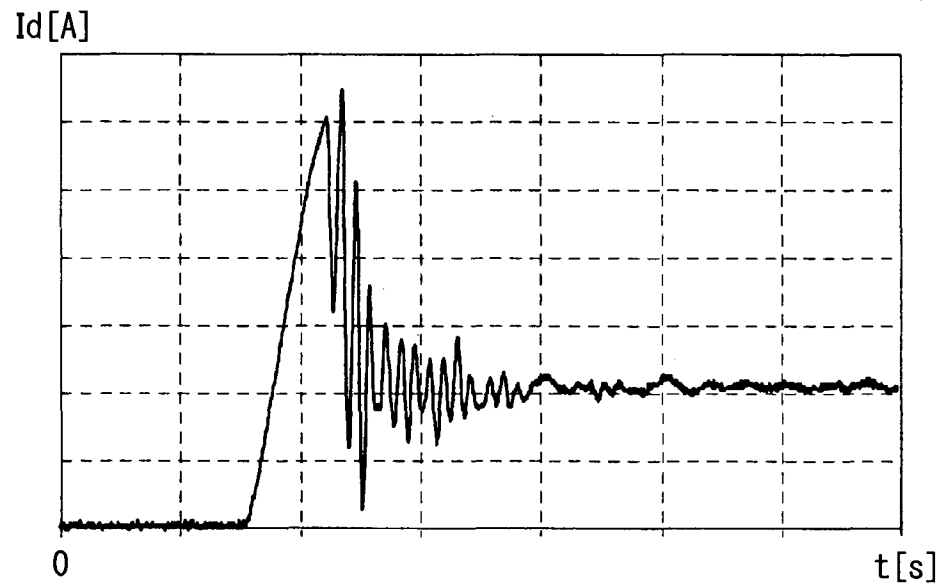
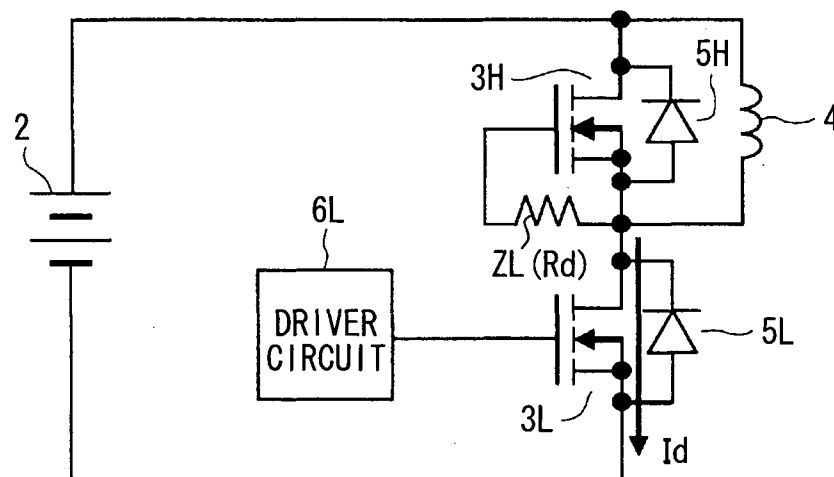
FIG. 30



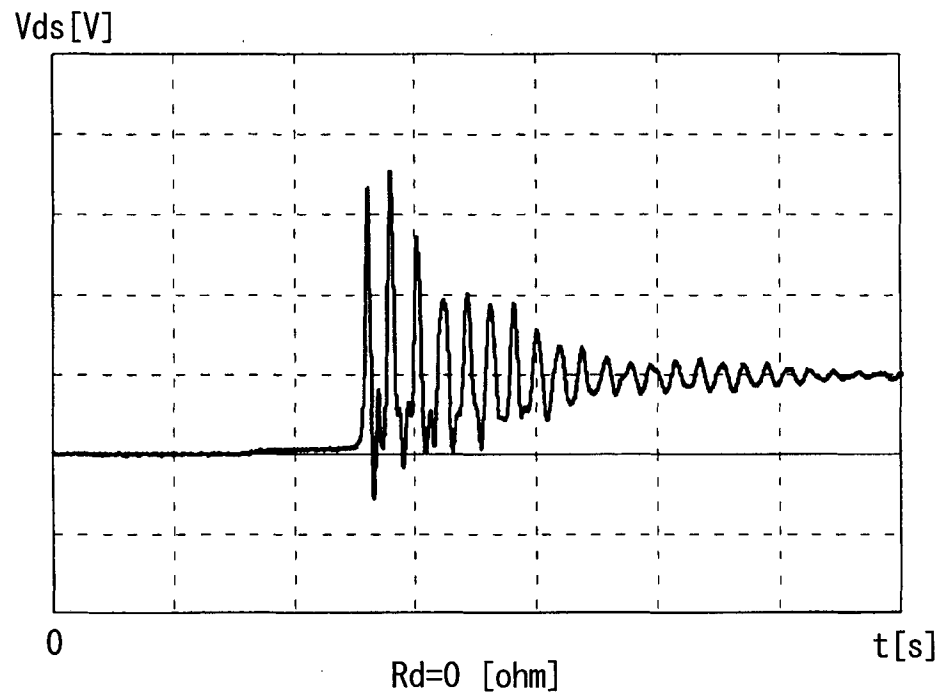
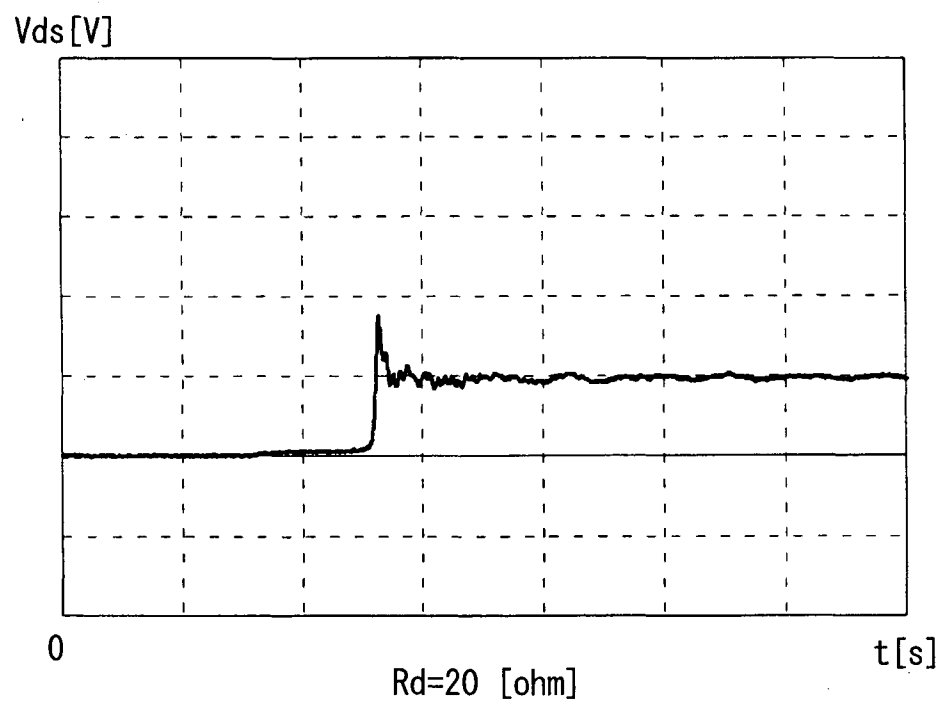
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FIG. 31**FIG. 32**

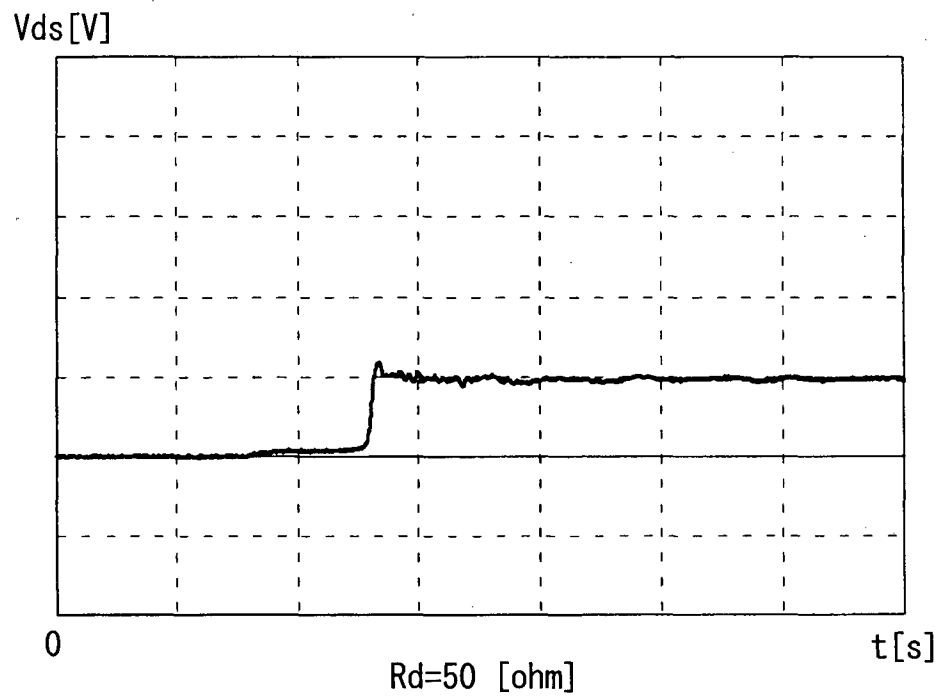
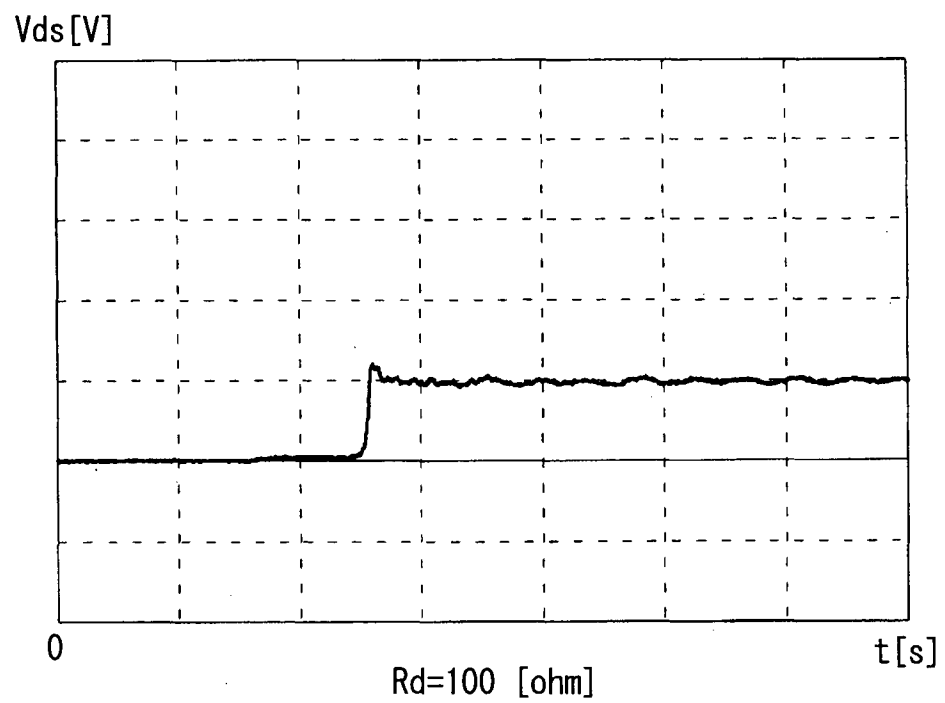
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FIG. 33 PRIOR ART**FIG. 34**

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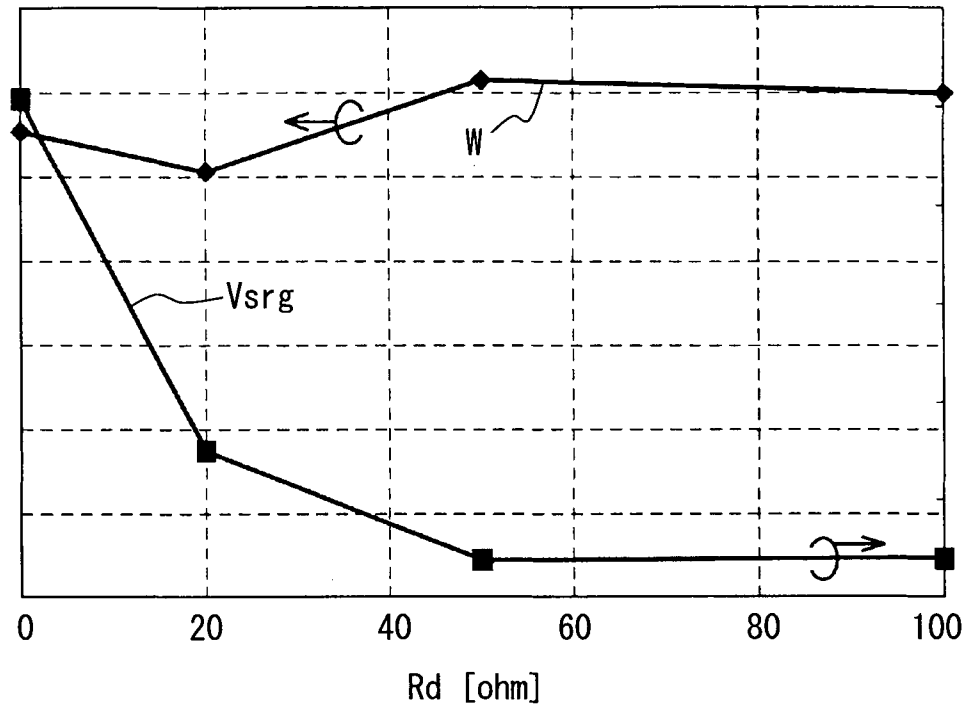
FIG. 35**FIG. 36**

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FIG. 37**FIG. 38**

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FIG. 39



INTERNATIONAL SEARCH REPORT

International application No
PCT/JP2012/064350

A. CLASSIFICATION OF SUBJECT MATTER INV. H03K17/0812 H03K17/16 H02M3/155 H02M7/217 ADD.		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) H03K H02M		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) EPO-Internal, WPI Data		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y A	EP 1 696 565 A1 (MITSUBISHI HEAVY IND LTD [JP]) 30 August 2006 (2006-08-30) figures 2-5 -----	1-5,7-9 6,10
Y A	WO 2007/138509 A2 (KONINKL PHILIPS ELECTRONICS NV [NL]; PHILIPS INTELLECTUAL PROPERTY [DE]) 6 December 2007 (2007-12-06) page 8, line 17 - line 30; figure 2A -----	1-5,7-9 6,10
☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.		
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Date of the actual completion of the international search 10 August 2012	Date of mailing of the international search report 21/08/2012	
Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Authorized officer Loiseau, Ludovic	

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/JP2012/064350

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