Title: DOHERTY POWER AMPLIFYING APPARATUS

Abstract: The present invention discloses a Doherty power amplifying apparatus wherein a high output RF Doherty power amplifier is constructed with a size smaller than the construction using conventional two single-ended package devices by using a single push-pull package device, and a gate-source voltage of a peaking amplifier and the length of a peaking compensation line are optimized to obtain the highest efficiency characteristic at a high output power so as to obtain a peaking point having the highest efficiency. A Doherty power amplifying apparatus in which a main amplifier and a peaking amplifier are connected to each other in parallel by means of a λ/4 impedance transformer, wherein the main amplifier and the peaking amplifier are constructed using a power amplification device of a single push-pull package type, a peaking compensation line is intervened between the main amplifier and the output terminal of the peaking amplifier, and the length of the peaking compensation line is controlled in order to obtain a peaking point for an optimized Doherty operation.
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— with international search report
— with amended claims

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.
Description

DOHERTY POWER AMPLIFYING APPARATUS

Technical Field

[1] The present invention relates to a Doherty power amplifying apparatus. More particularly, the present invention relates to a Doherty power amplifying apparatus wherein a field effect transistor (FET) device of a single push-pull package type is used as a main amplifier and a peaking amplifier, respectively, and an input/output impedance matching circuit, the length of a peaking compensation line for obtaining a peak efficiency point and a microstrip λ/4 impedance transformer are used to obtain an optimized Doherty operation.

Background Art

[2] Multi-channel high power RF amplifiers (MCPA), for repeater and base-station applications, have the continual challenge of improving the DC to RF power efficiency. Power amplifier efficiency, unlike linearity, is not a specified factor in the design of these applications. Modern digital communications standards, such as IS-95 and W-CDMA, can require a high peak-to-average power ratio (PAR) over a 10 dB back-off, this considerably deteriorates the available power amplifier efficiency.

[3] Output power levels and demands on efficiency and linearity of power amplifiers are significantly different for handset and base-station applications. The power amplifier is dependent on the available battery power in handset applications, where the demands on the required power and linearity are modest in comparison to base station applications. The power amplifier has higher output power and more stringent linearity requirements, in repeater and base-station applications, although their efficiency is significantly decreased. A low efficient MCPA necessitates the use of additional heat-sinking or external cooling due to the high RF power levels and inherent high temperatures. Large AC/DC and DC/DC power supplies also are required to feed electrical power to the RF power amplifier. The efficiency of the amplifier has a direct bearing on the size and cost of these components. It is therefore inevitably required to improve the efficiency of the power amplifier with the simplified manufacturing process.

[4] A Doherty power amplifier was developed by W.H. Doherty in the 1930's and was usually used in an amplitude modulation transmitter such as AM (amplitude modulation) as a traveling wave tube amplifier (TWTA) of low frequency (LF) and medium frequency (MF) bands. Thereafter, a solid-state Doherty power amplifier was
proposed but was usually used in low power applications of less than 1 Watt. For this reason, there are lots of difficulties in applying the solid-state Doherty power amplifier to a high output power amplifier for CDMA repeater and base station applications.

FIG. 1a is a block diagram of a conventional RF Doherty amplifier. The input signal is divided to a main amplifier 102 and a peaking amplifier 103 by means of a Wilkinson divider 101. The output signal of the main amplifier is passed through a microstrip \( \lambda/4 \) impedance transformer 105 and combined with the output signal of the peaking amplifier. Here, a \( \lambda/4 \) microstrip line 104 connected to the input terminal of the peaking amplifier 103 is inserted in order to synchronize their phases between the main amplifier 102 and the peaking amplifier 103. In FIG. 1a, '\( \lambda/4 \) @ \( Z_p \)' refers to \( \lambda/4 \) impedance transformation for impedance \( Z_p \) of the peaking amplifier 103 and '\( \lambda/4 \) @ \( Z_m \)' refers to \( \lambda/4 \) impedance transformation for impedance \( Z_m \) of the main amplifier 102. '\( \lambda/4 \) @ \( Z_o \)' to be described later refers to \( \lambda/4 \) impedance transformation for characteristic impedance \( Z_0 \).

FIG. 1b is a Smith chart illustrating the impedance relationship depending on the microstrip \( \lambda/4 \) impedance transformer 105 between the main amplifier 102 and the output of the peaking amplifier 103 in the conventional RF Doherty amplifier. As shown in FIG. 1b, if a low power signal is inserted, the low output impedance of the main amplifier 102 is transformed to a high output impedance of the peaking amplifier 103 by a \( \lambda/4 \) impedance transformer 105. It is assumed that the impedance \( Z_m \) has no reactive component. Therefore, the all signal power passing through the main amplifier 102 is represented in the load resistor 106.

FIG. 2 plots an efficiency characteristic of the conventional RF Doherty amplifier shown in FIG. 1 in comparison with Class-A and Class-B amplifiers over a nominal 6 dB back-off. If a main amplifier and a peaking amplifier are biased as a Class-B amplifier using the same device, it is available to achieve the highest peak efficiency point of 78.5 at the 6 dB back-off. Therefore, the efficiency of the Doherty amplifier is higher than that of the Class-A and Class-B amplifiers.

FIG. 3 shows the schematic diagram for the conventional RF Doherty amplifier using two single-ended RF LDMOS FETs for achieving high output power. Two FETs of a single-ended type are used as a main amplifier 210 and a peaking amplifier 220, respectively. Upon matching of the input and the output, microstrip \( \lambda/4 \) impedance transformers 204 and 207 are used to properly transform the output impedance of the peaking amplifier 220 depending on the input power.

In FIG. 3, reference numeral 201 indicates a Wilkinson power divider, 202 and 203
indicate input impedance matching circuits for the main amplifier 210 and the peaking amplifier 220, respectively, 205 and 206 indicate output impedance matching circuits for the main amplifier 210 and the peaking amplifier 220, respectively, 208 indicates a λ/4 power coupler and 209 indicates a load resistor.

[10] FIG. 4 is a block diagram illustrating a typical RF power amplifier using a conventional push-pull package device. Two FET devices having the same characteristic are constructed using one package 250, and thus perform a push-pull operation as in Class AB. Furthermore, for impedance matching, an input impedance matching circuit 235 and an output impedance matching circuit 236 are inserted between the input and output terminals of the single package 250. For a 180° push-pull operation, λ/2 microstrip lines 231 and 232 are inserted between the input and output terminals of the single package 250. Further, λ/4 impedance transformers 230 and 240 are used for coupling without loss at the input and output, respectively.

[11] As shown in FIG. 3, however, according to the method using the two single-ended transistors, a method for obtaining a peak efficiency point is not clearly proposed, which is an important characteristic of the Doherty operation. Also, in the methods for connecting a plurality of different transistors in parallel, the volume occupied by a device is increased due to the increased number of the transistors. Therefore, there are lots of problems in applying these methods to an actual manufacturing process.

[12] Incidentally, the power amplifier as shown in FIG. 4 for the feed-forward linearization has a disadvantage in that the whole efficiency is deteriorated since the main amplifier and the error amplifier operating in Class AB mode are used at the same time.

Disclosure of Invention

[13] Accordingly, the present invention has been made in view of the above problems, and it is an object of the present invention to provide a Doherty power amplifying apparatus wherein a high output RF Doherty power amplifier is constructed with a size smaller than that in the construction using conventional two single-ended package devices by using a single push-pull package device, and a gate-source voltage of a peaking amplifier and the length of a peaking compensation line are optimized to obtain the highest efficiency characteristic at a high output power so as to obtain a peaking point having the highest efficiency.

[14] To achieve the above objects, according to the present invention, there is provided a Doherty power amplifying apparatus in which a main amplifier and a peaking amplifier are connected to each other in parallel by means of a λ/4 impedance
transformer, wherein the main amplifier and the peaking amplifier are constructed using a power amplification device of a single push-pull package type, a peaking compensation line is intervened between the main amplifier and the output terminal of the peaking amplifier, and the length of the peaking compensation line is controlled in order to obtain a peaking point for an optimized Doherty operation.

[15] In the above, it is preferred that the Doherty power amplifying apparatus further includes a 90° hybrid coupler for dividing an input power to the input terminals of the main amplifier and the peaking amplifier, respectively, and delaying the phase of the peaking amplifier later than the phase of the main amplifier by 90°. It is preferable that the 90° hybrid coupler is of a surface mounted package type.

[16] Furthermore, if the two amplifying devices are coupled to each other in a balanced parallel shape, it is possible to obtain higher output power and efficiency.

Description of Drawings

[17] Further objects and advantages of the invention can be more fully understood from the following detailed description taken in conjunction with the accompanying drawings in which:

[18] FIG. 1a is a block diagram illustrating a conventional RF Doherty amplifier, and FIG. 1b is a Smith chart illustrating the impedance relationship depending on a λ/4 impedance transformer between a main amplifier and the output of a peaking amplifier in a conventional RF Doherty amplifier;

[19] FIG. 2 is a graph illustrating an example of ideal efficiency characteristics of the conventional RF Doherty amplifier shown in FIG. 1;

[20] FIG. 3 is a block diagram illustrating the construction of a conventional RF Doherty amplifier in which the Doherty amplifier shown in FIG. 1 is formed using a single-ended package device;

[21] FIG. 4 is a block diagram illustrating a typical RF power amplifier using a conventional push-pull package device;

[22] FIG. 5 is a block diagram illustrating the construction of a Doherty power amplifying apparatus according to a preferred embodiment of the present invention;

[23] FIG. 6 a Smith chart illustrating the impedance relationship depending on a λ/4 impedance transformer between a main amplifier and the output of a peaking amplifier and the length of a peaking compensation line in the Doherty power amplifying apparatus shown in FIG. 5;

[24] FIG. 7 is a graph illustrating simulation results for efficiency characteristics of the Doherty power amplifying apparatus shown in FIG. 5;
FIG. 8a is a graph illustrating simulation results for variation in efficiency characteristics depending on control in the length of the peaking compensation line shown in FIG. 5, and FIG. 8b is a graph illustrating simulation results for variation in efficiency characteristics depending on control in a gate-source voltage of the peaking amplifier shown in FIG. 5;

FIG. 9 is a graph illustrating measurement results for efficiency characteristics of the Doherty power amplifying apparatus shown in FIG. 5;

FIG. 10a is a graph illustrating measurement results for variation in efficiency characteristics depending on control in the length of the peaking compensation line shown in FIG. 5, and FIG. 10b is a graph illustrating simulation results for variation in efficiency characteristics depending on control in the gate-source voltage of the peaking amplifier shown in FIG. 5; and

FIG. 11 is a block diagram illustrating the construction of a balanced parallel Doherty power amplifying apparatus in which the Doherty power amplifying apparatus shown in FIG. 5 is coupled to each other in a balanced parallel shape in order to obtain a higher output power.

Best Mode

Preferred embodiments of a Doherty power-amplifying apparatus according to the present invention will now be described in detail with reference to the accompanying drawings.

FIG. 5 is a block diagram illustrating the construction of a Doherty power amplifying apparatus according to a preferred embodiment of the present invention. In the Doherty power amplifying apparatus according to the present invention, two single-ended devices 210 and 220 that occupy a great size in the Doherty power amplifier as shown in FIG. 3 are replaced with a push-pull package device, which is construed to serve as the conventional Class AB push-pull shown in FIG. 4. That is, a single device 310 of a push-pull package type is used as a main amplifier 310m and a peaking amplifier 310p. Input impedance matching circuits 303 are 304 are connected to the front ends of the main amplifier 310m and the peaking amplifier 310p, respectively. Meanwhile, in order to distribute an input signal \( \text{RF}^{\text{in}} \) to the main amplifier 310m and the peaking amplifier 310p, a 90° (quadrature) hybrid coupler 301 of, for example, a surface mounted package type is used as a power divider. This replaces the conventional Wilkinson power divider 201 and the microstrip line 204 for a 90° phase difference shown in FIG. 3. This reduces the size, lowers the loss and increases the isolation.
Next, in order to obtain an optimized power, output impedance matching circuits 305 and 306 are connected to the outputs of the main amplifier 310m and the peaking amplifier 310p, respectively, like the input terminals. For a Doherty operation, a $\lambda/4$ impedance transformer 309 for characteristic impedance ($Z_0$) is inserted between the main amplifier 310m and the peaking amplifier 310p. Furthermore, a peaking compensation line 307 is inserted between the rear ends of the output impedance matching circuits 305 and 306 in the main amplifier 310m and the peaking amplifier 310p. The length of the peaking compensation line 307 is then adjusted so as to obtain a maximum peaking point in a desired back-off output power. Also, by controlling a power signal being the input to the peaking amplifier 310p and a gate-source voltage ($V_{gs}$) applied through a RF choke coil 311, an operating point of the peaking amplifier 310p can be optimized so that a peaking point of the Doherty power amplifying apparatus can be suitably found. Unexplained reference numeral 302 indicates $Z_0$ for isolation, for example, a 50 ohm termination resistor.

FIG. 6 a Smith chart illustrating the impedance relationship depending on a $\lambda/4$ impedance transformer between a main amplifier and the output of a peaking amplifier and the length of a peaking compensation line in the Doherty power amplifying apparatus shown in FIG. 5. Impedance of the main amplifier 310m and the peaking amplifier 310p can be maintained to have the relationship as shown in FIG. 1b by means of the length of the peaking compensation line ($\lambda_{2m}$). A typical high output FET used in the present invention has low drain impedance. Thus, unless the impedance relationship between the main amplifier 310m and the output of the peaking amplifier 310p is not established by the impedance matching circuits 305 and 306 and the length of the peaking compensation line ($\lambda_{2m}$) 307, a peaking point of a complete Doherty operation cannot be obtained.

In FIG. 6, the output impedance ($Z_{m}$) of the main amplifier 310m is properly increased through the output impedance matching circuit 305 and the peaking compensation line 307 (point B). The signal passing through the main amplifier 301m controls the $\lambda/4$ impedance transformer 309 to make the peaking amplifier 310p have high impedance ($Z_{p}$) close to infinite impedance. Accordingly, the power of all the signals passing through the main amplifier 310 are represented in the load impedance ($Z_0$).

FIG. 7 is a graph illustrating simulation results for efficiency characteristics of the Doherty power amplifying apparatus in a state where the Doherty power amplifying apparatus shown in FIG. 5 is designed to operate at a frequency band of 2.140[GHz].
The main amplifier 310m is operated as a Class AB and the peaking amplifier 310p is operated as a Class C by controlling the gate-source voltage (Vgs). As can be seen from FIG. 7, efficiency characteristics of a Doherty A obtained by optimizing the gate-source voltage (Vgs) of the peaking amplifier 310p and the length of the peaking compensation line 307 are higher than those obtained by the conventional method (Doherty B) shown in FIG. 2 or the Class AB power amplifier.

FIG. 8a is a graph illustrating simulation results for variation in efficiency characteristics depending on control in the length of the peaking compensation line shown in FIG. 5, and FIG. 8b is a graph illustrating simulation results for variation in efficiency characteristics depending on control in the gate-source voltage of the peaking amplifier shown in FIG. 5. As can be seen from FIG. 8a, a peaking point of efficiency is obtained at a length (graph A) of an optimized peaking compensation line. As variation with the optimized length is severe, its efficiency characteristic is lowered like A → B → C → D and the peaking point disappears. Meanwhile, as can be seen from FIG. 8b, in case of the gate-source voltage (Vgs) of the peaking amplifier 310p that is optimized with the Class C bias, it is possible to find a peaking point of the highest efficiency like 'A'. As the bias point approaches 'E' being a Class B, its efficiency characteristic is lowered like A → B → C → D → E and a peaking point thus disappears.

FIG. 9 is a graph illustrating measurement results for efficiency characteristics of the embodiment shown in FIG. 5. FIG. 9 is a graph showing efficiency characteristics measured in a state where the Doherty power amplifying apparatus shown in FIG. 5 is designed to operate at a frequency band of 2.140 GHz. As can be seen from FIG. 9, a peaking point is obtained at a point where an output power is back-offed approximately -6[dB] and efficiency characteristics higher than a common Class AB are thus obtained.

FIG. 10a is a graph illustrating measurement results for variation in efficiency characteristics depending on control in the length of the peaking compensation line shown in FIG. 5, and FIG. 10b is a graph illustrating simulation results for variation in efficiency characteristics depending on control in the gate-source voltage of the peaking amplifier shown in FIG. 5.

As shown in FIG. 10a, in an optimized length, a peaking point having the highest efficiency like 'A' can be obtained. In the same manner as the simulation results in FIG. 8a, as there is variation in the optimized length, a peaking point disappears like 'A → B → C → D' and efficiency characteristics are lowered. Meanwhile, in case of the gate-source voltage (Vgs) of the peaking amplifier 310p optimized with a Class C bias,
a peaking point of the highest efficiency can be found like 'A'. In case where it is simulation data of FIG. 8b, however, as a bias point approaches 'E' being a Class B, efficiency is lowered like 'A → B → C → D → E' and a peaking point being a characteristic of the Doherty operation disappears.

FIG. 11 is a block diagram illustrating the construction of a balanced parallel Doherty power amplifying apparatus in which the Doherty power amplifying apparatus shown in FIG. 5 is coupled to each other in a balanced parallel shape in order to obtain a higher output power. FIG. 11 shows an example for application to a higher power such as a mobile communication repeater and a base station. The balanced parallel Doherty power amplifying apparatus of FIG. 11 is coupled to each of the input and output terminals of the power amplifying apparatus shown in FIG. 5 by using 90° hybrid couplers 401 and 402 of a surface mounted package type. The Doherty power amplifying apparatus of the present invention is not to be restricted by the embodiments but can be changed or modified without departing from the scope and spirit of the present invention.

Industrial Applicability

According to the present invention described above, there is provided a high output and high efficiency RF Doherty power amplifying apparatus using a single push-pull package type device, which can be used in a repeater or base station for mobile communication. Furthermore, the length of a peaking compensation line between a main amplifier and a peaking amplifier is controlled to find a maximum peaking point, thus optimizing a Doherty operation.

Accordingly, if a feed-forward power amplifier is constructed using the Doherty power amplifying apparatus of the present invention, the linearity having the same as a conventional feed-forward linear power amplifier of a Class AB that is used in a mobile communication repeater or base station can be obtained and an improved efficiency characteristic can be realized. Also, like an application to the feed-forward linear power amplifier, a digital pre-distortion power amplifier of efficiency better than the feed-forward linear power amplifier can be produced by integrating digital pre-distortion technologies. The digital pre-distortion power amplifier generates components of opposite phase and size to the power amplifier at the front end of a power amplifier of a Class AB as a digital signal, receives and then makes the signal linear. If the signal is made linear using a digital pre-distorter, it is possible to realize a power amplifier of higher efficiency and linearity.

Resultantly, since a conventional feed-forward linear power amplifier that is used
in a mobile communication repeater or a base station is replaced with a Doherty power amplifying apparatus of the present invention, efficiency is increased. A size problem, which is a disadvantage of the conventional high output Doherty power amplifier, can be addressed. This makes it possible to miniaturize the entire system.

Incidentally, since high efficiency is obtained at a high output, it is possible to reduce the amount of current consumed by an amplifier, and the number and cost of a cooling apparatus within the entire system, accordingly. As a result, the present invention has advantages that it can reduce the cost needed for an electrical use and the manufacturing cost in manufacturers and operators of a mobile communication repeater and a base station system. Eventually, reliability of the system is further improved and a communication service of a good quality can be provided to mobile communication subscribers.
Claims

1. A Doherty power amplifying apparatus in which a main amplifier and a peaking amplifier are connected to each other in parallel by means of a λ/4 impedance transformer,
   wherein the main amplifier and the peaking amplifier are constructed using a power amplification device of a single push-pull package type,
   a peaking compensation line is intervened between the main amplifier and the output terminal of the peaking amplifier, and
   the length of the peaking compensation line is controlled in order to obtain a peaking point for an optimized Doherty operation.

2. The Doherty power amplifying apparatus as claimed in claim 1, further comprising a 90° hybrid coupler for dividing an input power to the input terminals of the main amplifier and the peaking amplifier, respectively, and delaying the phase of the peaking amplifier later than the phase of the main amplifier by 90°.

3. The Doherty power amplifying apparatus as claimed in claim 2, wherein the 90° hybrid coupler is of a surface mounted package type.

4. The Doherty power amplifying apparatus as claimed in claim 3, wherein the Doherty power amplifying apparatus is used as a main amplifier of a feed-forward mode.

5. The Doherty power amplifying apparatus as claimed in claim 3, wherein the Doherty power amplifying apparatus is used in combination with a digital predistorter.

6. The Doherty power amplifying apparatus as claimed in any one of claims 1 to 5, wherein two Doherty power amplifying apparatuses are connected to each other in a balanced parallel shape.
What Is Claimed Is:

1. A Doherty power amplifying apparatus in which a main amplifier and a peaking amplifier are connected to each other in parallel by means of a \(\lambda/4\) impedance transformer,

wherein the main amplifier and the peaking amplifier are constructed using a power amplification device of a single push-pull package type,

a peaking compensation line is intervened between the main amplifier and the output terminal of the peaking amplifier, and

the length of the peaking compensation line is controlled in order to obtain a peaking point for an optimized Doherty operation.

2. The Doherty power amplifying apparatus as claimed in claim 1, further comprising a 90° hybrid coupler for dividing an input power to the input terminals of the main amplifier and the peaking amplifier, respectively, and delaying the phase of the peaking amplifier later than the phase of the main amplifier by 90°

3. The Doherty power amplifying apparatus as claimed in claim 2, wherein the 90° hybrid coupler is of a surface mounted package type.

4. The Doherty power amplifying apparatus as claimed in claim 3, wherein the Doherty power amplifying apparatus is used as a main amplifier of a feed-forward mode.

5. The Doherty power amplifying apparatus as claimed in claim 3, wherein the Doherty power amplifying apparatus is used in combination with a digital predistorter.
6. The Doherty power amplifying apparatus as claimed in any one of claims 1 to 5, wherein two Doherty power amplifying apparatuses are connected to each other in a balanced parallel shape.

7. (Added) The Doherty power amplifying apparatus as claimed in any one of claims 1 to 5, wherein the main and peaking amplifiers are either separate miniature microwave integrated circuits (MMIC) or one integrated MMIC.

8. (Added) The Doherty power amplifying apparatus as claimed in any one of claims 1 to 5, being applicable to L, S, C, X, Ku, K, Ka and EHF Band applications.
[FIG. 8]

a) 

Output Power [dBm]

PAE [%]

A
B
C
D

b) 

Output Power [dBm]

PAE [%]

A
B
C
D
E
INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER

IPC7 H03F 1/07

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7: H03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

KR: IPC as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKIPASS, PAJ, FPD, USAPP

C. DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
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<tr>
<th>Category</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No.</th>
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<tbody>
<tr>
<td>X</td>
<td>US 6617929 B2 (Postech Foundation) 9 Sep. 2003 See the abstract, Figs.3, 5A, 5B, 6A, 6B, column 1, line 55 - column 2, line 7, column 2, line 36 - column 4, line 13</td>
<td>1-6</td>
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<tr>
<td>A</td>
<td>WO 1999/52206 (ERICSSON, INC.) 14 Oct. 1999 See the abstract</td>
<td>1-6</td>
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