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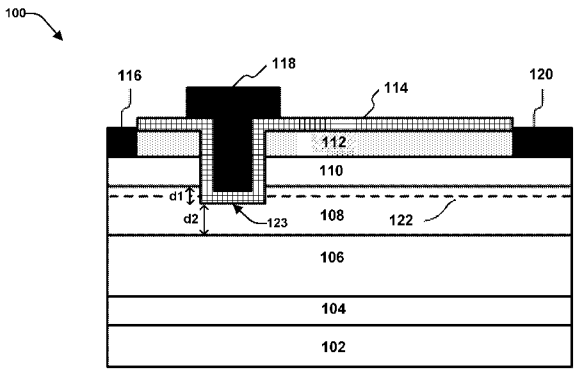

FIG. 1

(57) Abstract: Enhancement-mode (E-mode) double-channel (DC) HEMTs are provided. In one embodiment a semiconductor device is provided that includes a substrate and a heterostructure formed on the substrate. The heterostructure can include a lower channel layer, an upper channel layer, an insertion layer formed between the lower channel layer and the upper channel layer, and one or more barrier layers formed on the upper channel layer. The semiconductor device further includes a recess formed within the one or more barrier layers and at least a first portion of the upper channel layer, a gate structure formed within the recess. In various implementations, the gate structure has a gate dielectric layer formed on and adjacent to a wall of the recess and a gate electrode formed on and adjacent to the electrode dielectric layer.

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ENHANCEMENT-MODE DOUBLE-CHANNEL HIGH ELECTRON MOBILITY TRANSISTOR

RELATED APPLICATION

[0001] This patent cooperative treaty (PCT) international application claims priority to U.S. Provisional Patent Application No. 62/231,294, filed on July 1, 2015, and entitled "ENHANCEMENT-MODE GAN DOUBLE-CHANNNEL MOS-HEMT AND METHOD OF FABRICATION," the entirety of which is hereby incorporated by reference herein.

TECHNICAL FIELD

[0002] This disclosure relates generally to enhancement-mode high-electron-mobility transistors (HEMTs), and more particularly to enhancement-mode (E-mode) double-channel (DC) HEMTs based on group III-nitride (III-N) compound semiconductor materials.

BACKGROUND

[0003] Group III-nitride (III-N) compound semiconductor materials, such as GaN, possess the advantages of wide energy bandgap, high breakdown electrical field, and high thermal conductivity. In addition, a wide-bandgap heterostructure system, such as a system incorporating an aluminum gallium nitride (AlGaN)/GaN heterostructure, has a two-dimensional electron gas (2DEG) channel with a high sheet charge concentration and high electron mobility as enhanced by spontaneous and piezoelectric polarization effects. Due to these merits, HEMTs based on III-N semiconductor heterostructures such as AlGaN/GaN are considered as promising candidates for the next generation power devices. However, the traditional III-N HEMTs are depletion-mode devices with negative threshold voltage. The depletion-mode operation hinders quick adoption of these devices in applications.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Non-limiting and non-exhaustive embodiments of the subject disclosure are described with reference to the following figures, wherein like reference numerals refer to like parts throughout the various views unless otherwise specified.

[0005] FIG. 1 presents a conventional III-nitride enhancement-mode (E-mode) HEMT device with a fully recessed barrier layer under the gate.

[0006] FIG. 2 shows the resistance components of a conventional III-nitride E-mode HEMT device with a fully recessed barrier layer under the gate.

[0007] FIG. 3 presents another conventional III-nitride E-mode HEMT device with a partially recessed barrier layer under the gate.

[0008] FIG. 4 presents an example E-mode semiconductor device in accordance with one or more embodiments described herein.

[0009] FIG. 5 presents a circuit diagram of the equivalent resistance of an example E-mode semiconductor device in accordance with various aspects and embodiments described herein.

[0010] FIG. 6 provides a graph depicting the simulated conduction bands at the access region of an example E-mode semiconductor device in accordance with aspects and embodiments described herein.

[0011] FIG. 7 provides another graph depicting the simulated conduction bands at the recessed gate region of an example E-mode semiconductor device in accordance with aspects and embodiments described herein.

[0012] FIG. 8 presents graphs demonstrating the threshold voltage robustness of an example E-mode semiconductor device having with different gate structure recess depths in accordance with one or more embodiments described herein.

[0013] FIGs. 9-14 present an example fabrication process of an example E-mode semiconductor device in accordance with one or more embodiments described herein.

[0014] FIG. 15 presents another example E-mode semiconductor device in accordance with one or more additional embodiments described herein.

[0015] FIGs. 16-20 present an example fabrication process of another example E-mode semiconductor device in accordance with one or more additional embodiments described herein.

[0016] FIG. 21 presents another example E-mode semiconductor device in accordance with one or more additional embodiments described herein.

[0017] FIG. 22 presents another example E-mode semiconductor device configured in a rectifier mode in accordance with one or more additional embodiments described herein.

[0018] FIG. 23 provides graphs demonstrating the experimental transfer I_D-V_{GS} characteristics of an example DC-MOS-HEMT in accordance with one or more embodiments described herein.

[0019] FIG. 24 provides a graph demonstrating the experimental transfer I_D-V_{DS} characteristics of an example DC-MOS-HEMT in accordance with one or more embodiments described herein.

[0020] FIG. 25 provides a graph depicting the measured field-effect mobility of an example DC-MOS-HEMT in accordance with one or more embodiments described herein.

[0021] FIG. 26 provides a graph of the experimental off-state breakdown characteristics of an example DC-MOS-HEMT in accordance with one or more embodiments described herein.

[0022] FIG. 27 provides a graph of the experimental IV characteristics of a DC-MOS-HEMT configured as a field-effect rectifier in accordance with one or more embodiments described herein.

[0023] FIG. 28 presents a flow diagram of an example method for fabricating an E-mode semiconductor device in accordance with one or more embodiments described herein.

[0024] FIG. 29 presents a flow diagram of another example method for fabricating an E-mode semiconductor device in accordance with one or more embodiments described herein.

[0025] FIG. 30 presents a flow diagram of another example method for fabricating an E-mode semiconductor device in accordance with one or more embodiments described herein.

DETAILED DESCRIPTION

[0026] Various aspects or features of this disclosure are described with reference to the drawings, wherein like reference numerals are used to refer to like elements throughout. In this specification, numerous specific details are set forth in order to provide a thorough understanding of the subject disclosure. It should be understood, however, that the certain aspects of this disclosure may be practiced without these specific details, or with other methods, components, materials, *etc*. In other instances, well-known structures and devices are shown in block diagram form to facilitate describing the subject disclosure.

[0027] By way of introduction, the subject matter disclosed herein relates to enhancement-mode (E-mode) semiconductor devices, and more particularly to E-mode HEMTs including a double channel (DC). In various exemplary embodiments, the subject semiconductor devices are HEMTs including a III-N DC heterostructure and a metal-oxide-semiconductor (MOS) structure, also referred to herein as a DC-MOS-HEMT. Methods for fabricating such DC-MOS-HEMTs are also provided. It is contemplated and intended that the design of the various features of the subject E-mode semiconductor devices can be applied to other heterostructures. For clarity, various exemplary embodiments of the subject E-mode semiconductor devices are based on an AlGaN/GaN heterostructure. However, a person of ordinary person in the art can extend the various features of the subject E-mode semiconductor devices to other heterostructure variations and forms of design.

[0028] The subject E-mode semiconductor devices have a well-controlled threshold voltage and a low on-resistance. In one or more embodiments, the subject E-mode semiconductor devices feature an upper MOS-channel and a lower heterojunction channel under the control gate. Two heterojunction channels are formed in the the source-to-gate and gate-to-drain access regions, an upper channel and a lower channel, both of which exhibit high electron mobility and relatively high electron density. Carriers in the E-mode semiconductor device can flow from the upper channel to the lower channel or from the

lower channel to the upper channel with very low resistance. In accordance with one or more embodiments, the E-mode semiconductor device includes a group III-nitride heterostructure including a substrate, a nucleation layer, a buffer layer, a lower channel layer, an insertion layer, an upper channel layer, and one or more barrier layers. At least one of the one or more barrier layers has a bandgap larger than that of the underlying upper channel layer, and the insertion layer has a bandgap larger than the underlying lower channel layer. The heterostructure features two channels, one at the interface between the barrier and the upper channel layer, and the other one at the interface between the insertion layer and lower channel layer. The E-mode semiconductor device further includes a recessed gate structure provided within a recess formed within the one or more barrier layers and in some embodiments, at least a portion of the upper channel layer. A gate dielectric and a gate electrode are then formed in the gate recess. A source electrode and a drain electrode are formed at opposite sides of the gate electrode.

[0029] Due to the gate structure being formed within a recess that passes through the one or more barrier layers, the semiconductor devices operate as an E-mode device. Because the recess is terminated at or within the upper channel layer, the lower channel layer maintains a heterojunction channel with high electron mobility. In addition, the electrical connections between the access regions and the gate-controlled channel are not disrupted, resulting in a low connection resistance. Consequently, a low overall on-state resistance can be realized in subject E-mod semiconductor devices. The threshold voltage of the subject E-mode semiconductor devices is also insensitive to variations in recess depth of the recessed gate structure as long as recess is terminated at or within the upper channel layer.

[0030] In one or more embodiments, a semiconductor device is provided that includes a substrate and a heterostructure formed on the substrate. The heterostructure can include a lower channel layer, an upper channel layer, an insertion layer formed between the lower channel layer and the upper channel layer, and one or more barrier layers formed on the upper channel layer. The insertion layer has a first bandgap that is larger than a second bandgap of the lower channel layer. In addition, at least one of the one or more barrier layers has a first bandgap that is larger than a second bandgap of the upper channel layer. The semiconductor device further includes a recess formed within the one or more barrier layers and at least a first portion of the upper channel layer, a gate structure formed within the recess. In various implementations, the gate structure has a gate dielectric layer formed on and adjacent to a wall of the recess and a gate electrode formed on and adjacent to the electrode dielectric layer.

[0031] The semiconductor device further includes an upper channel formed within the upper channel layer near an interface between the upper channel layer and the

one or more barrier layers, and a lower channel formed within the lower channel layer near an interface between the lower channel layer and the insertion layer. The upper channel and the lower channel can be electrically connected thereby facilitating merged conduction of the upper channel and the lower channel. The semiconductor device can have a low on-state resistance (e.g., less than about 7.0 Ω·mm) based on the merged conduction of the upper channel and the lower channel. In another embodiment, the semiconductor device has a buffer layer formed between the upper channel layer and the insertion layer, and wherein the recess is formed through the upper channel layer and reaches the buffer layer without passing through the buffer layer. Further, in one or more implementations, a threshold voltage of the semiconductor device does not vary based on a depth of the recess within the at least the first portion of the upper channel layer.

[0032] In another embodiment, a semiconductor device is provided that includes a buffer layer, a lower channel layer formed on and adjacent to the buffer layer, an upper channel layer formed on and adjacent to the lower channel layer and one or more barrier layer formed on and adjacent to the upper channel layer. The upper channel layer has a first bandgap that is larger than a second bandgap of the lower channel layer. In addition, at least one of the one or more barrier layers has a first bandgap that is larger than a second bandgap of the upper channel layer. The semiconductor device further includes a recess formed within the one or more barrier layers and at least a first portion of the upper channel layer, and a gate structure formed within the recess. In one or more implementations, the gate structure includes a gate dielectric layer formed on and adjacent to a wall of the recess and a gate electrode formed on and adjacent to the electrode dielectric layer.

[0033] The semiconductor device can further include an upper channel formed within the upper channel layer near an interface between the upper channel layer and the one or more barrier layers, and a lower channel formed within the lower channel layer near an interface between the lower channel layer and the upper channel layer. The upper channel and the lower channel can be electrically connected thereby causing merged conduction of the upper channel and the lower channel. In some implementations, an on-state resistance of the semiconductor device is less than about 7.0 Ω·mm based on the merged conduction of the upper channel and the lower channel.

[0034] Still in yet another embodiment, a method is provided that includes forming a heterostructure including a buffer layer, a lower channel layer on and adjacent to the buffer layer, an insertion layer on and adjacent to the lower channel layer, an upper channel layer on the insertion layer, and a barrier layer on the upper channel layer. The method further includes forming a source electrode and a drain electrode on and adjacent

to the barrier layer of the heterostructure, forming a passivation layer on and adjacent to the barrier layer and between the source electrode and the drain electrode, and forming a recess through the passivation layer, the barrier layer and a first portion of the upper channel layer, wherein a second portion of the upper channel layer remains below the recess. In one or more implementations, the method further includes forming a gate dielectric layer on and adjacent to a wall of the recess and the passivation layer, and forming a gate electrode within the recess and adjacent to the gate dielectric layer structure formed within the recess.

[0035] In various embodiments, the method further includes forming an upper channel within the upper channel layer near an interface between the upper channel layer and the one or more barrier layers, forming a lower channel within the lower channel layer near an interface between the lower channel layer and the insertion layer, and electrically connecting the upper channel and the lower channel resulting in merged conduction of the upper channel and the lower channel. The method further includes, applying the positive voltage to the gate electrode, achieving an on-state resistance of less than about 7.0 Ω·mm based the merged conduction of the upper channel and the lower channel.

[0036] With reference now to the drawing, FIG. 1 presents a conventional III-nitride enhancement-mode (E-mode) HEMT device 100 in accordance with various aspects and embodiments described herein. Device 100 has a heterostructure that includes a substrate 102, a nucleation layer 104 formed on and adjacent to the substrate 102, a buffer layer 106 formed on and adjacent to the nucleation layer 104, a channel layer 108 formed on and adjacent to the buffer layer 106, and a barrier layer 110 formed on and adjacent to the channel layer 108. Device 100 also includes a passivation layer 112 formed on and adjacent to the barrier layer 110. Device 100 further includes a recessed gate structure formed with a recess that passes completely through the passivation layer 112 and the barrier layer 110 and into the channel layer 108. The recessed gate structure includes a gate dielectric layer 114 formed on and adjacent to a wall of the recess (e.g., lining the recess) and a gate electrode 118 formed within and above the recess on and adjacent to the gate dielectric layer 114. The gate dielectric layer 114 further covers portions of the passivation layer 112. A source electrode 116 and drain electrode 120 are respectively provided on the heterostructure on either sides of the gate electrode 118. Device 100 further includes a channel 122 located within the channel layer 108 at or near the interface between the channel layer 108 and the barrier layer 110.

[0037] Device 100 includes a fully recessed barrier layer 110 under the gate electrode 118. In particular, the bottom or foot region 123 of the recessed gate structure (e.g., including the gate dielectric layer 114 and the gate electrode 118), extends through the

entire thickness of the barrier layer 110. For example, as shown in FIG. 1, the foot region 123 of the recessed gate structure extends into a portion of the channel layer 108. Device 100 (and devices having a similar structure) can operate as an E-mode device as a result of recessing the gate structure into the barrier layer 110. The gate dielectric layer 114 serves to suppress gate leakage current at the foot region 123. However, because device 100 does not include any portion of the barrier layer 110 below the foot region 123, the electrons or carriers at the gate foot region 123 flow at the interface between the gate dielectric layer 114 and the underlying channel layer 108. The interface between the gate dielectric layer 114 and the underlying channel layer 108 is a metal-insulator-semiconductor channel (abbreviated as MIS-channel). Typically, carriers flowing through a MIS-channel exhibit reduced mobility compared to carriers at the interface of a heterojunction. Reduced carrier mobility leads to undesirable effects such as high conduction loss and lower power conversion efficiency. Further, with device 100, the depth d1 of the recessed gate structure substantially affects the conduction path between the channel 122 and the access regions (not shown) respectively located on either sides of the gate electrode 114 near the source electrode 116 and the drain electrode 120. In particular, the depth d1 of the gate foot region 123 below the upper surface of the channel 108. For example, if there is any over-recess of depth d1 by even a few nanometers, the conduction path between the access regions (not shown) and the channel 122 will be disrupted.

[0038] FIG. 2 shows the resistance components of conventional III-nitride E-mode HEMT device 100 with a fully recessed barrier layer under the gate. Repetitive description of like elements employed in respective embodiments is omitted for sake of brevity. Line 200 represents the flow of carriers through the device 100 when in an on-state. The respective rectangles along line 200 represent regions where carrier flow is hindered. For example, as shown in FIG. 2 due to the fully recessed barrier layer 110 of device 100, device 100 exhibits a large carrier resistance at an area 204 under the recessed gate structure at the foot region 123, and at the two corner areas 202 and 206 at the two edges of the gate region. A large on-resistance leads to higher conduction loss and lower power conversion efficiency. Thus although device 100 provides the advantages of being an E-mode III-nitride device, device 100 has a relatively high conduction loss and low power conversion efficiency.

[0039] FIG. 3 presents another conventional III-nitride E-mode HEMT device 300 in accordance with various aspects and embodiments described herein. Device 300 includes same or similar features as device 100 with the modification of having a partially recessed barrier layer 110. Repetitive description of like elements employed in respective embodiments is omitted for sake of brevity.

[0040] As shown in FIG. 3, the foot region 123 of the recessed gate structure (e.g.,

including the gate dielectric layer 114 and the gate electrode 118) of device 300 extends through only a portion of the thickness of the barrier layer 110. For example, a portion 302 of the barrier layer 110 remains between the foot region 123 of the recessed gate structure and the channel layer 108. With this configuration, carriers can flow below the foot region 123 of the recessed gate structure at the interface between the remaining portion 302 of the barrier layer 110 and the underlying channel region 108. Carriers at this heterojunction interface exhibits higher mobility relative to carriers in the MIS-channel of device 100 (e.g., the interface between the gate dielectric layer 114 and the upper channel layer 108). However, the thickness of portion 302 of the barrier layer below the foot region 123 of the recessed gate structure is difficult to control. The threshold voltage of device 300 is highly sensitive to the thickness of the portion 302 of the barrier layer below the foot region 123 of the recessed gate structure. As a result, the threshold voltage of device 300 is difficult to control. Therefore, although device 300 has reduced on-state resistance relative to device 100, device 300 suffers from a hindered ability to control the uniformity and repeatability of the threshold voltage for the partially recessed gate structure, since the threshold voltage is highly sensitive to the recess depth.

[0041] FIG. 4 presents an example E-mode semiconductor device 400 in accordance with one or more embodiments described herein. In various implementations, semiconductor device 400 is a DC-MOS-HEMT. Similar to devices 100 and 300, device 400 includes a recessed gate structure, resulting in operation of device 400 as an E-mode device. However, device 400 includes several notable differences relative to devices 100 and 300, as explained in detail below. These differences result in device 400 having a well-controlled threshold voltage and a low on-state resistance relative to devices 100, 300 and other similar E-mode HEMTs.

[0042] Device 400 has a heterostructure that includes a substrate 402, a nucleation layer 404 formed on and adjacent to the substrate 402, and a buffer layer 406 formed on and adjacent to the nucleation layer 404. The substrate can include but is not limited to, silicon, sapphire, diamond, silicon carbide (SiC), aluminum nitride (AlN), gallium nitride (GaN), and other suitable materials. The nucleation layer 404 can include but is not limited to, AlN, GaN, indium nitride (InN), or their alloys. The buffer 406 can include but is not limited to, AlN, GaN, InN, or their alloys. The heterostructure further includes a lower channel layer 408b, an insertion layer 409, an upper channel layer 408a, and a barrier layer 410. In some implementations, the barrier layer 410 can include a stack of two or more layers (not shown).

[0043] The materials of the lower channel layer 408b, the insertion layer 409, the upper channel layer 408a, and the barrier layer 410 can vary so long as the bandgap of the insertion layer 409 is larger than the bandgap of the lower channel layer 408b, and the

bandgap of the barrier layer 410 (or at least one layer of the barrier layer 410 when the barrier layer 410 is composed of two or more layers) is larger than the bandgap of the upper channel layer 408a. In various embodiments, the materials of the lower channel layer 408b, the insertion layer 409, the upper channel layer 408a, and the barrier layer 410 respectively include group III-nitrides. For example, in one or more embodiments, the lower channel layer 408b can include but is not limited, to GaN, AlN, InN, or their alloys. In an exemplary embodiment, the lower channel layer 408b includes GaN. The insertion layer 409 can also include but is not limited to, GaN, AlN, InN, or their alloys. In an exemplary embodiment, the insertion layer 409 includes AlN. The upper channel layer 408a can also include but is not limited to, GaN, AlN, InN, or their alloys. In an exemplary embodiment, the upper channel layer 408a includes GaN. The barrier layer 410 can also include GaN, AlN, InN, or their alloys. In one implementation, the barrier layer 410 includes AlGaN. In some implementations, the barrier layer 410 includes a stack of two or more layers formed with different materials selected from GaN, AlN, InN, or their alloys. For example, in another implementation, the barrier layer 410 includes a layer of AlN and a layer of GaN. In another example, the barrier layer can include an AlN layer formed on and adjacent to the upper channel layer 408a, an AlGaN layer formed on and adjacent to the AlN layer, and a GaN layer formed on and adjacent to the AlGaN layer.

[0044] In one or more embodiments, device 400 also includes a passivation layer 412 (or layers) formed on and adjacent to the barrier layer 410. The passivation layer 412 is adopted to relieve the current collapse phenomenon in III-nitride HEMTs. The passivation can include but is not limited to, one or more insulating, or semi-conducting layers, such as silicon nitride (SiN_x), silicon dioxide (SiO_2), di-aluminium trioxide (Al_2O_3), AlN, GaN, Si, or diamond. Device 400 further includes a recessed gate structure formed with a recess that passes completely through the passivation layer 412 and the barrier layer 410 and into the upper channel layer 408a. The recessed gate structure includes a gate dielectric layer 414 formed on and adjacent to a wall of the recess (e.g., lining the recess) and a gate electrode 418 formed within and above the recess on and adjacent to the gate dielectric layer 414. The gate dielectric layer 414 further covers portions of the passivation layer 412. The gate dielectric layer 414 serves to insulate the gate electrode 418 and prevent gate current leakage. The gate dielectric layer 414 can include but is not limited to one or more of Al_2O_3, AlN, SiN_x, gallium trioxide (Ga_2O_3), SiO_2, hafnium dioxide (HfO_2), or any other dielectrics commonly practiced in semiconductor technology. The gate electrode 418 covers at least the recessed gate region so that the recessed gate region is modulated by the gate voltage. In the embodiment shown, the gate electrode 418 also covers portions of the heterostrucure on either sides of the recess. The gate electrode 418 can include any suitable metal. For

example, the gate electrode can include but is not limited to one or more of one or more of, titanium (Ti), Al, nickel (Ni), gold (Au), tungsten (W), vanadium (V), and tantalum (Ta).

[0045] A source electrode 416 and a drain electrode 420 are respectively provided on (or within, not shown) the heterostructure on either sides of the gate electrode 418. For example, in the embodiment shown, the source electrode 416 and the drain electrode 420 are respectively provided on and adjacent to the barrier layer 410 on either sides of the gate electrode 418. The passivation layer 412 is further provided on the barrier layer 410 between the source electrode 416 and the drain electrode 420. In another embodiment, the source electrode 416 and the drain electrode 420 can be provided on either sides of the gate electrode 418 and within portions of the passivation layer 412 and/or the barrier layer 410 (not shown). In various implementations, the source electrode 416 and the drain electrode 420 are Ohmic contacts formed with a metal, including but not limited to one or more of, Ti, Al, Ni, Au, W, V, and Ta. In an aspect, a thermal annealing process is applied to device 400 during the fabrication process to cause the source electrode 416 and the drain electrode 420 to become Ohmic.

[0046] Because the bandgap of the insertion layer 409 is larger than the bandgap of the lower channel layer 408b, and the bandgap of the barrier layer 410 (or at least one layer of the barrier layer) is larger than the bandgap of the upper channel layer 408a, device 400 includes two channels, an upper channel 422a and a lower channel 422b. In the embodiment shown, the upper channel 422a is formed within the upper channel layer 408a at the heterojunction interface between the upper channel layer 408a and the barrier layer 410. The lower channel 422b is formed within the lower channel layer 408b at the heterojunction interface between the insertion layer 409 and the lower channel layer 408b. In various implementations, the upper channel 422a and the lower channel 422b are electrically connected thereby facilitating movement of electrons or carriers between the upper channel 422a and the lower channel 422b when a positive gate voltage is applied to gate electrode 418 to turn the device 400 on. When carriers move between the upper channel 422a and the lower channel 422b, they have to cross the upper channel layer 408a and/or the insertion layer 409. The thickness of upper channel layer 408a thus determines the 2DEG distribution. Accordingly, the thicknesses of the insertion layer 409 and the upper channel layer 408a can be selected so as to facilitate movement of carriers between the respective channels (e.g., so as that the two channels in the access region are effectively connected to the channel under the gate). For example, a thickness of the insertion layer 409 and the upper channel layer 408a is selected to facilitate movement of electrons from the lower channel 422b to the upper channel 422a, and vice versa. In an exemplary embodiment, the thickness of the insertion layer 409 is thin enough so that at a zero gate-to-source voltage, both the upper channel 422a

and the lower channel 422b are pinched off.

[0047] In one or more embodiments, the insertion layer 409 has a thickness from about 0.1 nanometer (nm) to about 10 nm. In another embodiment, the insertion layer 409 has a thickness from about 0.5 nm to about 5.0 nm. Still in yet another embodiment, the insertion layer 409 has a thickness of about 1.5 nm. Further, the upper channel layer 408a can have a thickness from about 1.0 nm to about 20 nm. In another embodiment, the upper channel layer 408a has a thickness form about 2.0 nm to about 15 nm. Still in another embodiment, the upper channel layer 408a has a thickness of about 4.0 nm to about 10.0 nm. In one exemplary embodiment, the upper channel layer 408a has a thickness of about 6.0 nm. In various embodiments, a combined thickness of the upper channel layer 408a and the insertion layer 409 is from about 1.0 nm to about 30.0 nm. In other embodiments, a combined thickness of the upper channel layer 408a and the insertion layer 409 is from about 10.0 nm to about 20.0 nm.

[0048] As shown in FIG. 4, similar to device 100, the recessed gate structure is formed in a recess that passes completely through the thickness of the barrier layer 410 thereby making device 400 an E-mode device. Also similar to device 100, in device 400 the recess of the recessed gate structure extends into a portion of the upper channel layer 408a. As a result, the upper channel 422a at the gate foot region 423 is located between gate dielectric layer 410 and the upper channel layer 408a, which is referred to as a metal insulator semiconductor (MIS) channel. As discussed above with respect to FIGs. 1 and 3, the electron mobility of an MIS channel (e.g., upper channel 422a) is lower than a channel located at a heterojunction interface. However, in addition to the upper channel 422a, device 422b also includes lower channel 422b which is formed at the heterojunction interface between the lower channel layer 408b and the insertion layer 409. Further, the lower channel 422b is located away from the gate foot region 423 of the recessed gate structure. As a result, high electron mobility is maintained in the lower channel 422b and the resistance originated from the gate foot region 423 is greatly reduced.

[0049] When a positive gate voltage is applied to the gate electrode 418, because the upper channel 422a and the lower channel 422b are electrically connected, electrons flow between the two channels, resulting in a merged conductance of the two channels. Device 400 thus exhibits a reduced on-state resistance relative to devices 100 and 300 as a result of merged conduction of the upper channel 422a and the lower channel 422b. The resistance originated from the access region is determined by the 2DEG density and electron mobility in the access region, independent of the characteristics of the recessed gate structure region. The thickness of upper channel layer 408a determines the 2DEG distribution. Therefore, the resistance originated from the access region maintains low. In one or more implementations,

with the combined low resistance of the access region and the gate region, the total on-state resistance (R_{on}) of device 400 is less than about 7.0 Ω·mm (e.g., about 6.9 Ω·mm) which is significantly less than that of device 100 (e.g., which is about 20.0 Ω·mm).

[0050] FIG. 5 presents a circuit diagram 500 of the equivalent resistance of example E-mode semiconductor device 400 in accordance with various aspects and embodiments described herein. As shown in diagram 500, the total on-resistance (R_{on}) of semiconductor device 400 is a combination of the contact resistances R_C, resistance at source-side access region R_S, resistance at drain-side access region R_D, and the resistance at the gated region R_G. Each resistance along the channel (i.e. R_S, R_D, R_G) is equivalent to a parallel of an upper channel resistance and a lower channel resistance (i.e. $R_S = R_{S\text{-up}} // R_{S\text{-low}}$, $R_S = R_{G\text{-up}} // R_{G\text{-low}}$, $R_S = R_{D\text{-up}} // R_{D\text{-low}}$).

[0051] FIG. 6 provides a graph 600 depicting the simulated conduction bands at the access region of an example E-mode semiconductor device (e.g., device 400) in accordance with aspects and embodiments described herein. FIG. 7 provides another graph depicting the simulated conduction bands at the recessed region of the example E-mode semiconductor device in accordance with aspects and embodiments described herein. The graphs of FIGs. 6 and 7 are generated based on the subject E-mode semiconductor device 400 having a gate dielectric layer 414 including Al_2O_3, a barrier layer 410 including an upper layer of GaN, a middle layer of AlGaN and lower layer of AlN, an upper channel layer 408a including GaN, an insertion layer 409 including AlN, and a lower channel layer 408b including GaN. The conduction band depicted in graph 600 is simulated for the access region of device 400 when voltages of all electrodes are zero. Owing to the polarization effect in the insertion layer, a channel is formed at the interface between the insertion layer and the upper channel layer, in addition to the original upper channel at the interface between the barrier and the upper channel layer. The conduction band depicted in graph 700 is simulated for the recessed gate region for device 400, with voltage of the gate electrode increasing from 0 V to 6 V. With the polarization effect in the insertion layer, the lower channel is turned on first, and the upper channel is turned on later with a larger gate voltage.

[0052] With reference back to FIGs. 1 and 4, as previously described, device 300 suffers from a hindered ability to control the uniformity and repeatability of the threshold voltage for the partially recessed gate structure since the threshold voltage is highly sensitive to the recess depth. However, in addition to providing low on-state resistance, device 400 is substantially insensitive to variations in recess depth of the recessed gate structure as long as recess is terminated at or within the upper channel layer 408a. In particular, the threshold voltage of device 400 does not vary (or substantially vary) based on a depth of the recess within the at least the first portion of the upper channel layer. In particular, the depth (d1) of

the gate foot region 423 below the upper surface of the upper channel 408a, or the depth (d2) between the gate foot region 423 and the lower surface of the upper channel 408a is not critical in device 400 to ensure the conduction paths of channel 422a or channel 422b between the access regions (not shown) are not disrupted. For example, in one or more implementations, the threshold voltage of device 400 varies less than 10% when the depth (d1) of the gate foot region 423 below the upper surface of the upper channel 408a increases or decreases by 150%.

[0053] For example, FIG. 8 presents graphs 801-806 demonstrating the threshold voltage robustness of example E-mode semiconductor device 400 with different gate structure recess depths in accordance with one or more embodiments described herein. The graphs of FIG. 8 generated based on the subject E-mode semiconductor device 400 having a gate dielectric layer 414 including Al_2O_3, a barrier layer 410 including an upper layer of GaN, a middle layer of AlGaN and lower layer of AlN, an upper channel layer 408a including GaN, an insertion layer 409 including AlN, and a lower channel layer 408b including GaN. Graphs 801, 803 and 805 respectively depict simulated conduction bands of the device 400 when d2 (e.g., the thickness of the upper channel layer 408a below the foot region 423 of the recessed gate structure) is 6.0 nm, 4.0 nm and 2.0 nm respectively. Graphs 802, 804 and 806 depict the simulated threshold voltage V_{th} when d2 is 6.0 nm, 4.0 nm and 2.0 nm respectively. As shown in graph 806, the threshold voltage (V_{th}) of device 400 is about 0.3 V when d2 is 6.0 nm, about 0.25 V when d2 is 4.0 nm, and about 0.22 V when d2 is 2 nm. Thus the threshold voltage of device 400 does not vary or significantly vary (e.g., varies less than 10%) based on the depth of the recessed gate structure so long as the depth of the recessed gate structure remains within the thickness of the upper channel layer 408a.

[0054] FIGs. 9-14 present an example fabrication process of an example E-mode semiconductor device 400 in accordance with one or more embodiments described herein. Repetitive description of like elements employed in respective embodiments is omitted for sake of brevity.

[0055] FIG. 9 presents an initial heterostructure 900 from which device 400 can be created. The heterostructure 900 includes a substrate 402, a nucleation layer 404 formed on and adjacent to the substrate 402, a buffer layer 406 formed on and adjacent to the nucleation layer 404, a lower channel layer 408a formed on and adjacent to the buffer layer 406, an insertion layer 409 formed on and adjacent to the lower channel layer 408b, an upper channel layer 408a formed on and adjacent to the insertion layer 409 and a barrier layer 410 (or layers) formed on and adjacent to the upper channel layer 408a. The heterostructure 900 can be prepared or grown using various semiconductor fabrication techniques, including but not limited to metal-organic chemical vapour deposition (MOCVD), molecular beam epitaxy

(MBE), hydride vapour phase epitaxy (HVPE), and other suitable techniques. In various embodiments, the heterostructure 900 is composed of various layers including III-nitrides. For example, in one embodiment, the lower channel layer 408b includes GaN, the insertion layer 409 includes AlN, the upper channel layer 408a includes GaN, and the barrier layer 410 includes AlGaN. In addition, the insertion layer 409 has a larger bandgap relative to the bandgap of the lower channel layer 408b and the barrier layer 410 has a larger bandgap relative to the upper channel layer 408b. As a result, the heterostructure 900 includes an upper channel 422a at the interface between the barrier layer 410 and the upper channel layer 408a, and a lower channel 422b at the interface between the insertion layer 409 and the lower channel layer 408b.

[0056] In FIG. 10, Ohmic contacts are formed on the heterostructure 900 for the source electrode 416 and the drain electrode 420. The metal employed to form the source electrode 416 and the drain electrode 420 can include but is not limited to one or more of, Ti, Al, Ni, Au, W, V, or Ta. In one or more implementations, a thermal annealing process is employed to cause the source electrode 416 and the drain electrode 420 to be Ohmic contacts.

[0057] After the source electrode 416 and the drain electrode 420 are formed, a passivation layer 412 is formed on the heterostructure between the source electrode 416 and the drain electrode 420, as shown in FIG. 11. The passivation layer 412 can include one or a combination of insulating, or semi-conducting layers, such as SiNx, SiO2, Al2O3, AlN, GaN, Si, or diamond. A recess 1202 is then formed through the passivation layer 412, the barrier layer 410, and a portion of the upper channel layer 408a using a suitable etching technique, as shown in FIG. 12. The etching of the passivation layer 412 can include a wet etch or dry etch depending on the material employed for the passivation layer 412. The method for etching the barrier layer 410 and the portion of upper channel layer 408a is not limited. For example, suitable methods for etching the barrier layer 410 and/or the upper channel layer 408a can include but are not limited to, plasma dry etching, digital etching, or a combination of them.

[0058] As previously described, the depth of the recess 1202 can vary so long as the recess does not pass through the upper channel layer 408a and into the insertion layer 409. In one or more embodiments, the depth d2 of the recess 1202 is between about 0.1 nm and about 19.0 nm. In another embodiment, the depth d2 of the recess 1202 is between about 1.0 nm and about 10.0 nm. Still in another embodiment, the depth d2 of the recess 1202 is between about 2.0 nm and about 6.0 nm. The depth d1 of the recess 1202 can also vary based on the thickness of the upper channel layer 408a which is preferably between about 0.1 nm to about 20.0 nm. For example, in one implementation the depth d1 of the recess is about 90% of the thickness of the upper channel layer 408a. In another implementation the depth d1 of the recess is about 75% of the thickness of the upper channel layer 408a. In another

implementation the depth d1 of the recess is about 50% of the thickness of the upper channel layer 408a. In another implementation the depth d1 of the recess is about 25% of the thickness of the upper channel layer 408a. In yet another implementation the depth d1 of the recess is about 10% of the thickness of the upper channel layer 408a.

[0059] After formation of the recess 1202, the gate dielectric layer 414 is deposited as shown in FIG. 13. The gate dielectric layer 414 can include various suitable dielectric materials, including but not limited to one or more of, Al_2O_3, AlN, SiN_x, Ga_2O_3, SiO_2, or HfO_2, the gate dielectric layer 414 can be deposited using various techniques, including but not limited to, MOCVD, plasma-enhanced chemical vapor deposition (PECVD), atomic layer deposition (ALD), low-pressure chemical vapor deposition (LPCVD), thermal oxidation, sputtering, evaporation, or spin-coating. In FIG. 14, the gate electrode 418 is then formed over the gate dielectric layer 414 within the recess, resulting in the formation of E-mode semiconductor device 400.

[0060] FIG. 15 presents another example E-mode semiconductor device 1500 in accordance with one or more additional embodiments described herein. In various implementations, semiconductor device 1500 is a DC-MOS-HEMT. Semiconductor device 1500 includes same or similar feature as semiconductor device 400 with the difference noted below. Repetitive description of like elements employed in respective embodiments is omitted herein for sake of brevity.

[0061] The structure of device 1500 differs from that of device 400 with respect to the depth of the recessed gate structure (e.g., including the gate electrode 418 and the gate dielectric layer 414) and the addition of a buffer layer 1502 between the insertion layer 409 and the upper channel layer 408a. The structure of device 1500 also does not include a passivation layer 412. According to this embodiment, the gate dielectric layer 418 can be formed directly on the barrier layer 410. As shown in FIG. 15, the recessed gate structure of device 1500 extends through the entire thickness of the upper channel layer 408a. In particular, the gate foot region 423 is located at the interface between the upper channel layer 408 and the buffer layer 1502. In one or more embodiments, the upper buffer layer 1502 includes at least one of GaN, AlN, InN, or their alloys. In an exemplary embodiment, the upper buffer layer 1502 includes GaN. In addition, in one or more implementations, the upper buffer layer 1502 and the upper channel layer 408a respectively include the same material (e.g., GaN).

[0062] With device 1500, when the electrons move between the upper channel 422a and the lower channel 422b, they have to cross the upper channel layer 408a, the buffer layer 1502 and the insertion layer 409. Thus the thicknesses of the upper channel layer 408a, the buffer layer 1502 and the insertion layer 409are designed not to isolate the two channels (e.g.,

so as to facilitate movement of electrons between the two channels with low resistance). In one or more embodiments, the upper channel layer 408a can have a thickness from about 1.0 nm to about 20 nm. In another embodiment, the upper channel layer 408a has a thickness form about 5.0 nm to about 15 nm. Still in another embodiment, the upper channel layer 408a has a thickness of about 10.0 nm. Similarly, in one or more embodiments, the buffer layer 1502 can have a thickness from about 1.0 nm to about 20 nm. In another embodiment, the buffer layer 1502 has a thickness form about 5.0 nm to about 15 nm. Still in another embodiment, the buffer layer 1502 has a thickness of about 10.0 nm. Further, in one or more embodiments, the insertion layer 409 has a thickness from about 0.1 nanometer (nm) to about 10 nm. In another embodiment, the insertion layer 409 has a thickness from about 0.5 nm to about 5.0 nm. Still in yet another embodiment, the insertion layer 409 has a thickness of about 1.5 nm. Furthermore, in various embodiments, a combined thickness of the upper channel layer 408a, the buffer layer 1502 and the insertion layer is from about 1.0 nm to about 30.0 nm. In other embodiments, a combined thickness of the upper channel layer, 408a, the buffer layer 1502 and the insertion layer is from about 10.0 nm to about 20.0 nm.

[0063] Device 1500 provides the same or similar advantages as device 400. In particular, due to the gate structure being formed within a recess that passes through the one or more barrier layers, the semiconductor device 1500 operate as an E-mode device. Because the recess is terminated within the upper channel layer 408a, the lower channel layer 408b maintains a heterojunction channel (e.g., lower channel 422b) with high electron mobility. Because the upper channel 422a and the lower channel 422b are electrically connected, electrons flow between the two channels, resulting in a merged conductance of the two channels. As a result, device 1500 thus exhibits a reduced on-state resistance relative to devices 100. For example, in one or more implementations, with the combined low resistance of the access region and the gate region, the total on-state resistance of device 1500 is less than about 7.0 Ω·mm while that of device 100 is about 20.0 Ω·mm. In addition, device 400 is substantially insensitive to variations in recess depth of the recessed gate structure as long as recess is terminated at or within the upper channel layer 408a. In particular, the threshold voltage of device 1500 does not vary (or substantially vary) based on the depth of the recess spanning the entire width of the upper channel layer 408a. Accordingly, the threshold voltage of device 1500 can be easily controlled.

[0064] FIGs. 16-20 present an example fabrication process of example E-mode semiconductor device 1500 in accordance with one or more additional embodiments described herein. Repetitive description of like elements employed in respective embodiments is omitted for sake of brevity.

[0065] FIG. 16 presents an initial heterostructure 1600 from which device 1500 can

be created. The heterostructure 1560 includes a substrate 402, a nucleation layer 404 formed on and adjacent to the substrate 402, a buffer layer 406 formed on and adjacent to the nucleation layer 404, a lower channel layer 408a formed on and adjacent to the buffer layer 406, an insertion layer 409 formed on and adjacent to the lower channel layer 408b, and a second buffer layer 1502 formed on and adjacent to the insertion layer 409. The heterostructure 1600 can be prepared or grown using various semiconductor fabrication techniques, including but not limited to metal-organic chemical vapour deposition (MOCVD), molecular beam epitaxy (MBE), hydride vapour phase epitaxy (HVPE), and other suitable techniques. In various embodiments, the heterostructure 1600 is composed of various layers including III-nitrides.

[0066] As shown in FIG. 17, the fabrication process of device 1500 involves the formation of a regrowth mask 1702 (referred to herein as "mask") on a portion of the second buffer layer 1502 where the recessed gate structure will later be formed. Various materials could be used as the mask, for example SiO_2, Al_2O_3, SiN, or another suitable material. After the mask 1702 is formed on the second buffer layer 1502, as shown in FIG. 18, the upper channel layer 408a and the barrier layer 410 are then formed or grown on the second buffer layer 1502 around the mask. The upper channel 422a is further established within the upper channel layer 408a at the heterojunction interface between the upper channel layer 408a and the barrier layer 410, and a lower channel 422b is established within the lower channel layer 408b at the heterojunction interface between the lower channel layer 408b and the insertion layer 409. The mask 1702 is then removed (e.g., by wet etch or dry etch) and a recess 1902 is formed within the barrier layer 410 and the upper channel layer 408, as shown in FIG. 19. The gate recess 1902 is terminated within the upper channel layer 408a.

[0067] After formation of the recess 1202, as shown in FIG. 20, the gate dielectric layer 414 is deposited onto the one or more barrier layers 410 and the source electrode 416, the gate electrode 418 and the drain electrode 420 are formed, resulting in device 1500. The gate dielectric layer 414 can include various suitable dielectric materials, including but not limited to one or more of, Al_2O_3, AlN, SiN_x, Ga_2O_3, SiO_2, or HfO_2, the gate dielectric layer 414 can be deposited using various techniques, including but not limited to, MOCVD, plasma-enhanced chemical vapor deposition (PECVD), atomic layer deposition (ALD), low-pressure chemical vapor deposition (LPCVD), thermal oxidation, sputtering, evaporation, or spin-coating. The gate electrode 418 can cover at least the recessed gate region, so that the recessed region is modulated by the gate voltage. As with device 400, with an increasing gate voltage, the lower channel 422b of device 1500 is turned on first due to the polarization effect of the insertion layer 409. Because the lower channel 422b remains a heterojunction channel, the electron mobility in the lower channel is high, thus compensating for the lower

electron mobility of the upper channel 422a which is a MIS-channel formed between the upper channel layer 408a and the gate dielectric layer 418.

[0068] FIG. 21 presents another example E-mode semiconductor device 2100 in accordance with one or more additional embodiments described herein. In various implementations, semiconductor device 2000 is a DC-MOS-HEMT. Semiconductor device 2000 includes same or similar feature as semiconductor devices with the difference noted below. Repetitive description of like elements employed in respective embodiments is omitted herein for sake of brevity.

[0069] The structure of device 2100 differs from that of device 400 with respect to the removal of the insertion layer 409. Although the insertion layer 409 is removed, device 2100 still includes the upper channel layer 408a and the lower channel layer 408b as well as the upper channel 422a and the lower channel 422b. According to this embodiment, the upper channel layer 408a, the lower channel layer 408b, and the barrier layer 410 have different bandgaps. In particular, the upper channel layer 408a can have a larger bandgap than the lower channel layer 408b and the barrier layer 410 can have a larger bandgap than the upper channel layer. For example, in one embodiment, the lower channel layer 408b can include InGaN, the upper channel layer 408a can include GaN, and the barrier layer 410 can include stack of three layers, including an AlN layer formed on and adjacent to the upper channel layer 408a, an AlGaN layer formed on and adjacent to the AlN layer, and a GaN layer formed on and adjacent to the AlGaN layer.

[0070] Similar to devices 400 and 1500, the upper channel 422a of device 2100 is provided at the interface between the upper channel layer 408a and the barrier layer 410. However, unlike devices 400 and 1500, the lower channel 422b is provided at the interface between the lower channel layer 408a and the upper channel layer 408b, which is a heterojunction. When the electrons move between the two channels in response to application of a positive voltage to the gate electrode 418, they have to cross only the upper channel layer 408a. The thicknesses of the upper channel layer 408a and the conduction band off-set between the upper channel layer 408a and the lower channel layer 408b are designed so as to not to isolate the two channels (e.g. that is, the electrons can move from the upper channel 422a to the lower channel 422b with very small resistance, and vice versus). For example, in one or more embodiments, the thickness of the upper channel layer 408a can is from about 1.0 nm to about 30 nm. In another embodiment, the upper channel layer 408a has a thickness form about 1.0 nm to about 20 nm. In another embodiment, the upper channel layer 408a has a thickness form about 5.0 nm to about 15 nm. Still in another embodiment, the upper channel layer 408a has a thickness of about 10.0 nm. The gate recess is terminated within the upper channel layer 408a. The depth of the gate recess (e.g., d1 or d2) can vary so

long as the gate recess does not extend into the lower channel layer 408b. With an increasing gate voltage, the lower channel 422b is turned on first due to the polarization effect of the upper channel layer 408a. As the lower channel remains a heterojunction channel, the electron mobility in the lower channel is high.

[0071] FIG. 22 presents another example E-mode semiconductor device 2200 configured in a rectifier mode in accordance with one or more additional embodiments described herein. In various implementations, semiconductor device 2200 is a DC-MOS-HEMT, configured as a field-effect rectifier. Semiconductor device 2200 includes same or similar feature as semiconductor device 400 with the difference noted below. Repetitive description of like elements employed in respective embodiments is omitted herein for sake of brevity.

[0072] Semiconductor device 2200 differs from semiconductor device 400 in that its gate electrode 418 is shorted to the source electrode 416. The combination of the gate electrode 418 and the source electrode 416 serves as the anode 2202 of the semiconductor device 2200. With this configuration, the drain electrode 420 serves as the cathode of the semiconductor device 2200. The resulting semiconductor device 2200 thus has a two-terminal configuration and exhibits rectifying characteristics based on the two-terminal configuration (e.g., the resulting semiconductor device 2200 operates as a rectifier). When operating as a rectifier and being configured with the subject DC-MOS-HEMT structure, the semiconductor device 2200 features a low channel resistance, which is beneficial in reducing the on-state voltage of the rectifier. For a DC-MOS-HEMT configured as a rectifier (e.g., semiconductor device 2200), the distance between electrode 416 and electrode 418 can be shortened and is preferably as short as possible. It is noted that although semiconductor device 2200 includes substantially the same heterostructure as device 400, it is feasible to configure the semiconductor devices 1500 and 2100 into rectifiers using a similar technique (e.g., by shorting the gate electrode 418 to the source electrode 116).

[0073] FIG. 23 provides graphs 2301 and 2302 demonstrating the experimental transfer I_D-V_{GS} characteristics of an example DC-MOS-HEMT (e.g., device 400) in accordance with one or more embodiments described herein. As shown in graph 2301, the threshold voltage V_{th} is 0.5 V for the DC-MOS-HEMT at a drain current criterion of 10.0μA/mm. As shown in graph 2302, two g_m peaks are present, indicating the strongest gate modulation of the lower channel and upper channel, respectively. For example, the device has a source-to-gate distance L_{GS}, gate length L_G, and gate-to-drain distance L_{GD} of 2 μm, 1.5 μm and 15 μm, respectively.

[0074] FIG. 24 provides a graph 2400 demonstrating the experimental transfer I_D-V_{DS} characteristics of an example DC-MOS-HEMT (e.g., device 400 in accordance with one or

more embodiments described herein. The gate-to-source voltage V_{GS} is changed from 0 V to 10 V, with a step of 2 V. As shown in graph 2400, a very low on-resistance (e.g., about 6.9 Ω·mm) is obtained for the subject DC-MOS-HEMT device (e.g., device 400) with gate-to-drain distance of 15 μm.

[0075] FIG. 25 provides a graph 2500 depicting the measured field-effect mobility of an example DC-MOS-HEMT (e.g., device 400) in accordance with one or more embodiments described herein. As shown in graph 2500, the maximum field-effect mobility of the lower channel in the DC-MOS-HEMT is around 1800 $cm^2/(V·s)$, which is close to the maximum field effect mobility of the lower channel in the double-channel HEMT (DC-HEMT) with no gate recess. Therefore, the gate recess process causes very little degradation of the mobility in the lower channel of the DC-MOS-HEMT. The subject DC-MOS-HEMT has a gate length of 44 μm.

[0076] FIG. 26 provides a graph 2600 of the experimental off-state breakdown characteristics of an example DC-MOS-HEMT (e.g., device 400) in accordance with one or more embodiments described herein. As shown in graph 2500, a breakdown of over 700 V is achieved at a drain current criterion of 1μA/mm. The subject DC-MOS-HEMT has a gate-to-drain distance of 15 μm.

[0077] FIG. 27 provides a graph 2700 of the experimental IV characteristics of a DC-MOS-HEMT configured as a field-effect rectifier (e.g., semiconductor device 2200) in accordance with one or more embodiments described herein. As shown in graph 2700, rectifying characteristics is achieved. In the forwards state, the rectifier begins to conduct at a low voltage, and in reverse state, the rectifier blocks a high voltage. The subject rectifier configured from a DC-MOS-HEMT has an anode-to-cathode distance of 15 μm.

[0078] FIGs. 28-30 illustrate methods in accordance with certain aspects of this disclosure. While, for purposes of simplicity of explanation, the methods are shown and described as a series of acts, it is to be understood and appreciated that this disclosure is not limited by the order of acts, as some acts may occur in different orders and/or concurrently with other acts from that shown and described herein. For example, those skilled in the art will understand and appreciate that methods can alternatively be represented as a series of interrelated states or events, such as in a state diagram. Moreover, not all illustrated acts may be required to implement methods in accordance with certain aspects of this disclosure. Additionally, it is to be further appreciated that the method disclosed hereinafter and throughout this disclosure is capable of being stored on an article of manufacture to facilitate transporting and transferring such methods to computers.

[0079] Turning now to FIG. 28, presented is a flow diagram of an example method 2800 for fabricating an E-mode semiconductor device in accordance with one or more

embodiments described herein. In various embodiments, method 2800 can be employed to fabricate a DC-MOS-HEMT, such as E-mode semiconductor device 400. Repetitive description of like elements employed in respective embodiments is omitted for sake of brevity.

[0080] At 2802, a heterostructure is formed (e.g., heterostructure 900) using a suitable semiconductor fabrication technique, such as but not limited to, MOCVD, MBE, HVPE, and other suitable techniques. The heterostructure can include a buffer layer (e.g., buffer layer 406), a lower channel layer (e.g., lower channel layer 408b) on and adjacent to the buffer layer, an insertion layer (e.g., insertion layer 409) on and adjacent to the lower channel layer, an upper channel layer (e.g., upper channel layer 408a) on the insertion layer, and a barrier layer (e.g., barrier layer 410) on the upper channel layer. In various embodiments, the heterostructure 900 is composed of various layers including III-nitrides. For example, in one embodiment, the lower channel layer 408b includes GaN, the insertion layer 409 includes AlN, the upper channel layer 408a includes GaN, and the barrier layer 410 includes AlGaN. In addition, the insertion layer 409 has a larger bandgap relative to the bandgap of the lower channel layer 408b and the barrier layer 410 has a larger bandgap relative to the upper channel layer 408b. At 2804, a source electrode (e.g., source electrode 416) and a drain electrode (e.g., drain electrode 420) are formed on and adjacent to the barrier layer of the heterostructure. At 2806, a passivation layer (e.g., passivation layer 412) is formed on and adjacent to the barrier layer and between the source electrode and the drain electrode, and at 2808, a recess (e.g., gate recess 1202) is formed through the passivation layer, the barrier layer and a first portion of the upper channel layer, wherein a second portion of the upper channel layer remains below the recess.

[0081] FIG. 29 presents a flow diagram of another example method 2900 for fabricating an E-mode semiconductor device in accordance with one or more embodiments described herein. In various embodiments, method 2900 can be employed to fabricate a DC-MOS-HEMT, such as E-mode semiconductor device 400. Repetitive description of like elements employed in respective embodiments is omitted for sake of brevity.

[0082] At 2902, a heterostructure is formed (e.g., heterostructure 900) using a suitable semiconductor fabrication technique, such as but not limited to, MOCVD, MBE, HVPE, and other suitable techniques. The heterostructure can include a buffer layer (e.g., buffer layer 406), a lower channel layer (e.g., lower channel layer 408b) on and adjacent to the buffer layer, an insertion layer (e.g., insertion layer 409) on and adjacent to the lower channel layer, an upper channel layer (e.g., upper channel layer 408a) on the insertion layer, and a barrier layer (e.g., barrier layer 410) on the upper channel layer. In various embodiments, the heterostructure 900 is composed of various layers including III-nitrides. For example, in one

embodiment, the lower channel layer 408b includes GaN, the insertion layer 409 includes AlN, the upper channel layer 408a includes GaN, and the barrier layer 410 includes AlGaN. In addition, the insertion layer 409 has a larger bandgap relative to the bandgap of the lower channel layer 408b and the barrier layer 410 has a larger bandgap relative to the upper channel layer 408b. At 2904, a source electrode (e.g., source electrode 416) and a drain electrode (e.g., drain electrode 420) are formed on and adjacent to the barrier layer of the heterostructure. At 2906, a passivation layer (e.g., passivation layer 412) is formed on and adjacent to the barrier layer and between the source electrode and the drain electrode, and at 2908, a recess (e.g., gate recess 1202) is formed through the passivation layer, the barrier layer and a first portion of the upper channel layer, wherein a second portion of the upper channel layer remains below the recess.

[0083] At 2910, a gate dielectric layer (e.g., gate dielectric layer 414) is formed on and adjacent to a wall of the recess and the passivation layer. At 2912, a gate electrode (e.g., gate electrode 418) is formed within the recess and adjacent to the gate dielectric layer formed within the recess. At 2914, an upper channel (e.g., upper channel 422a) is formed within the upper channel layer near an interface between the upper channel layer and the one or more barrier layers, and at 2916, a lower channel (e.g., lower channel 422b) is formed within the lower channel layer near an interface between the lower channel layer and the insertion layer. In various embodiments, the method can further include electrically connecting the upper channel and the lower channel resulting in merged conduction of the upper channel and the lower channel when a positive voltage is applied to gate electrode. In some implementations, when a positive voltage is applied to the gate electrode, on-state resistance of less than about 7.0 Ω·mm is achieved based on the merged conduction of the upper channel and the lower channel.

[0084] FIG. 30 presents a flow diagram of another example method 3000 for fabricating an E-mode semiconductor device in accordance with one or more embodiments described herein. In various embodiments, method 3000 can be employed to fabricate a DC-MOS-HEMT, such as E-mode semiconductor device 1500. Repetitive description of like elements employed in respective embodiments is omitted for sake of brevity.

[0085] At 3002, a heterostructure (e.g., heterostructure 1600) is formed using a suitable semiconductor fabrication technique, such as but not limited to, MOCVD, MBE, HVPE, and other suitable techniques. The heterostructure can include a first buffer layer (e.g., buffer layer 406), a lower channel layer (e.g., lower channel layer 408b) on and adjacent to the first buffer layer, an insertion layer (e.g., insertion layer 409) on and adjacent to the lower channel layer, and a second buffer layer (e.g., buffer layer 1502) on and adjacent to the insertion layer. In various embodiments, the heterostructure 1600 is composed of

various layers including III-nitrides. At 3004, a mask structure (e.g., mask 1702) is formed on the second buffer layer. At 3006, an upper channel layer (e.g., upper channel layer 408a) is formed on and adjacent to the second buffer layer and around the mask structure. At 3008, a barrier layer (e.g., barrier layer 410) is formed on and adjacent to the upper channel layer and around the mask structure. At 3010, the mask structure is removed and a gate recess (e.g., recess 1902) is established through the upper channel layer and the barrier layer. Then at 3012, a gate structure (e.g., including gate dielectric layer 414 and gate electrode 418) is formed within the gate recess.

[0086] What has been described above includes examples of various embodiments of the subject invention. It is, of course, not possible to describe every conceivable combination of components or methods for purposes of describing the subject invention, but one of ordinary skill in the art may recognize that many further combinations and permutations of the subject invention are possible. Accordingly, the subject invention is intended to embrace all such alterations, modifications and variations that fall within the spirit and scope of the appended claims. Furthermore, to the extent that the term "includes" and "involves" are used in either the detailed description or the claims, such terms are intended to be inclusive in a manner similar to the term "comprising" as "comprising" is interpreted when employed as a transitional word in a claim.

[0087] Reference throughout this specification to "one embodiment," or "an embodiment," means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment. Thus, the appearances of the phrase "in one embodiment," or "in an embodiment," in various places throughout this specification are not necessarily all referring to the same embodiment. Furthermore, the particular features, structures, or characteristics may be combined in any suitable manner in one or more embodiments.

[0088] The word "exemplary" and/or "demonstrative" is used herein to mean serving as an example, instance, or illustration. For the avoidance of doubt, the subject matter disclosed herein is not limited by such examples. In addition, any aspect or design described herein as "exemplary" and/or "demonstrative" is not necessarily to be construed as preferred or advantageous over other aspects or designs, nor is it meant to preclude equivalent exemplary structures and techniques known to those of ordinary skill in the art. Furthermore, to the extent that the terms "includes," "has," "contains," and other similar words are used in either the detailed description or the claims, such terms are intended to be inclusive - in a manner similar to the term "comprising" as an open transition word - without precluding any additional or other elements.

CLAIMS

What is claimed is:

1. A semiconductor device comprising:

a substrate;

a heterostructure formed on the substrate, comprising:

a lower channel layer,

an upper channel layer,

an insertion layer formed between the lower channel layer and the upper channel layer, and

one or more barrier layers formed on the upper channel layer;

a recess formed within the one or more barrier layers and at least a first portion of the upper channel layer; and

a gate structure formed within the recess.

2. The semiconductor device of claim 1, wherein the gate structure comprises a gate dielectric layer formed on and adjacent to a wall of the recess and a gate electrode formed on and adjacent to the electrode dielectric layer.

3. The semiconductor device of claim 2, further comprising:

an upper channel formed within the upper channel layer near an interface between the upper channel layer and the one or more barrier layers; and

a lower channel formed within the lower channel layer near an interface between the lower channel layer and the insertion layer,

wherein the upper channel and the lower channel are electrically connected thereby facilitating merged conduction of the upper channel and the lower channel.

4. The semiconductor of claim 3, wherein the resistance of the access region of the semiconductor device is reduced based partly on the merged conduction of the upper channel and lower channel.

5. The semiconductor device of claim 1, wherein a threshold voltage of the semiconductor device is insensitive to the depth of the recess within the at least the first portion of the upper channel layer.

6. The semiconductor device of claim 1, wherein the insertion layer has a first bandgap that is larger than a second bandgap of the lower channel layer.

7. The semiconductor device of claim 1, wherein at least one of the one or more barrier layers has a first bandgap that is larger than a second bandgap of the upper channel layer.

8. The semiconductor device of claim 1, wherein the insertion layer has a thickness from about 0.1 nm to about 10 nm.

9. The semiconductor device of claim 1, wherein the upper channel layer has a thickness from about 1.0 nm to about 20 nm.

10. The semiconductor device of claim 1, wherein a combined thickness of the upper channel layer and the insertion layer is from about 1.0 nm to 30.0 nm.

11. The semiconductor device of claim 1, wherein the gate structure comprises a gate dielectric layer formed on and adjacent to a wall of the recess and a gate electrode formed on and adjacent to the electrode dielectric layer.

12. The semiconductor device of claim 2, further comprising a passivation layer formed on and adjacent to the one or more barrier layers.

13. The semiconductor device of claim 2, further comprising a source electrode and a drain electrode respectively formed on opposite sides of the gate electrode on the one or more barrier layers.

14. The semiconductor device of claim 13, wherein the gate electrode and the source electrode combine to form an anode, and wherein the drain electrode serves as a cathode, thereby resulting in the semiconductor device having a two-terminal configuration.

15. The semiconductor device of claim 14, wherein the semiconductor device exhibits rectifying characteristics based on the two-terminal configuration.

16. The semiconductor device of claim 1, further comprising:

a buffer layer formed between the upper channel layer and the insertion layer, and wherein the recess is formed through the upper channel layer and reaches the buffer layer without passing through the buffer layer.

17. The semiconductor device of claim 1, wherein the lower channel layer, the upper channel layer, and the insertion layer and the one or more barrier layers respectively comprise at least one of: GaN, AlN, InN, an alloy of GaN, an alloy of AlN, or an alloy of InN.

18. The semiconductor device of claim 1, wherein the lower channel layer and the upper channel layer respectively comprise GaN on an alloy or GaN, and the insertion layer comprises AlN or an alloy of AlN.

19. The semiconductor device of claim 1, wherein the semiconductor device operates in enhancement-mode.

20. A semiconductor device comprising:

a buffer layer;

a lower channel layer formed on and adjacent to the buffer layer;

an upper channel layer formed on and adjacent to the lower channel layer;

one or more barrier layer formed on and adjacent to the upper channel layer;

a recess formed within the one or more barrier layers and at least a first portion of the upper channel layer; and

a gate structure formed within the recess.

21. The semiconductor device of claim 20, wherein the gate structure comprises a gate dielectric layer formed on and adjacent to a wall of the recess and a gate electrode formed on and adjacent to the electrode dielectric layer.

22. The semiconductor device of claim 21, further comprising:

an upper channel formed within the upper channel layer near an interface between the upper channel layer and the one or more barrier layers; and

a lower channel formed within the lower channel layer near an interface between the lower channel layer and the insertion layer,

wherein the upper channel and the lower channel are electrically connected thereby causing merged conduction of the upper channel and the lower channel.

23. The semiconductor of claim 22, wherein the resistance of the access region of the semiconductor device is reduced based partly on the merged conduction of the upper channel and lower channel.

24. The semiconductor device of claim 20, wherein a threshold voltage of the semiconductor device is insensitive to the depth of the recess within the at least the first portion of the upper channel layer.

25. The semiconductor device of claim 20, wherein the insertion layer has a first bandgap that is larger than a second bandgap of the lower channel layer.

26. The semiconductor device of claim 20, wherein at least one of the one or more barrier layers has a first bandgap that is larger than a second bandgap of the upper channel layer.

27. The semiconductor device of claim 20, wherein the insertion layer has a thickness from about 0.1 nm to about 10 nm.

28. The semiconductor device of claim 20, wherein the upper channel layer has a thickness from about 1.0 nm to about 20 nm.

29. The semiconductor device of claim 20, wherein a combined thickness of the upper channel layer and the insertion layer is from about 1.0 nm to 30.0 nm.

30. The semiconductor device of claim 20, wherein the lower channel layer and the upper channel layer respectively comprise GaN on an alloy or GaN, and the insertion layer comprises AlN or an alloy of AlN.

31. A method, comprising:

forming a heterostructure comprising:

a buffer layer,

a lower channel layer on and adjacent to the buffer layer,

an insertion layer on and adjacent to the lower channel layer,

an upper channel layer on the insertion layer, and

a barrier layer on the upper channel layer;

forming a source electrode and a drain electrode on and adjacent to the barrier layer of the heterostructure;

forming a passivation layer on and adjacent to the barrier layer and between the source electrode and the drain electrode; and

forming a recess through the passivation layer, the barrier layer and a first portion of the upper channel layer, wherein a second portion of the upper channel layer remains below the recess.

32. The method of claim 31, further comprising:

forming a gate dielectric layer on and adjacent to a wall of the recess and the passivation layer; and

forming a gate electrode within the recess and adjacent to the gate dielectric layer formed within the recess.

33. The method of claim 32, further comprising:

forming an upper channel within the upper channel layer near an interface between the upper channel layer and the one or more barrier layers;

forming a lower channel within the lower channel layer near an interface between the lower channel layer and the insertion layer; and

electrically connecting the upper channel and the lower channel resulting in merged conduction of the upper channel and the lower channel.

34. The method of claim 33, further comprising:

applying the positive voltage to the gate electrode; and

achieving a low resistance of the access region of the semiconductor device based partly on the merged conduction of the upper channel and lower channel.

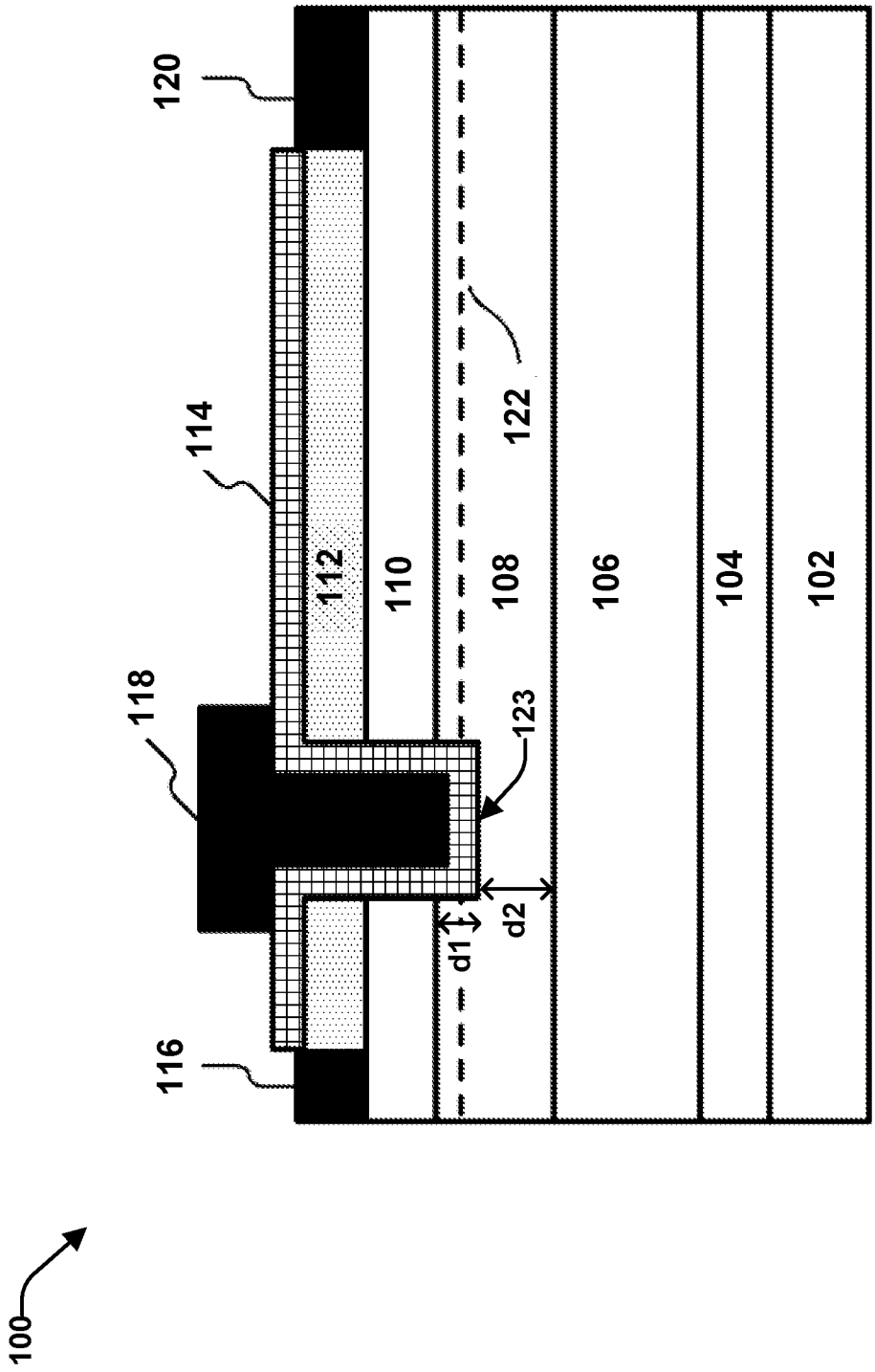


FIG. 1
(PRIOR ART)

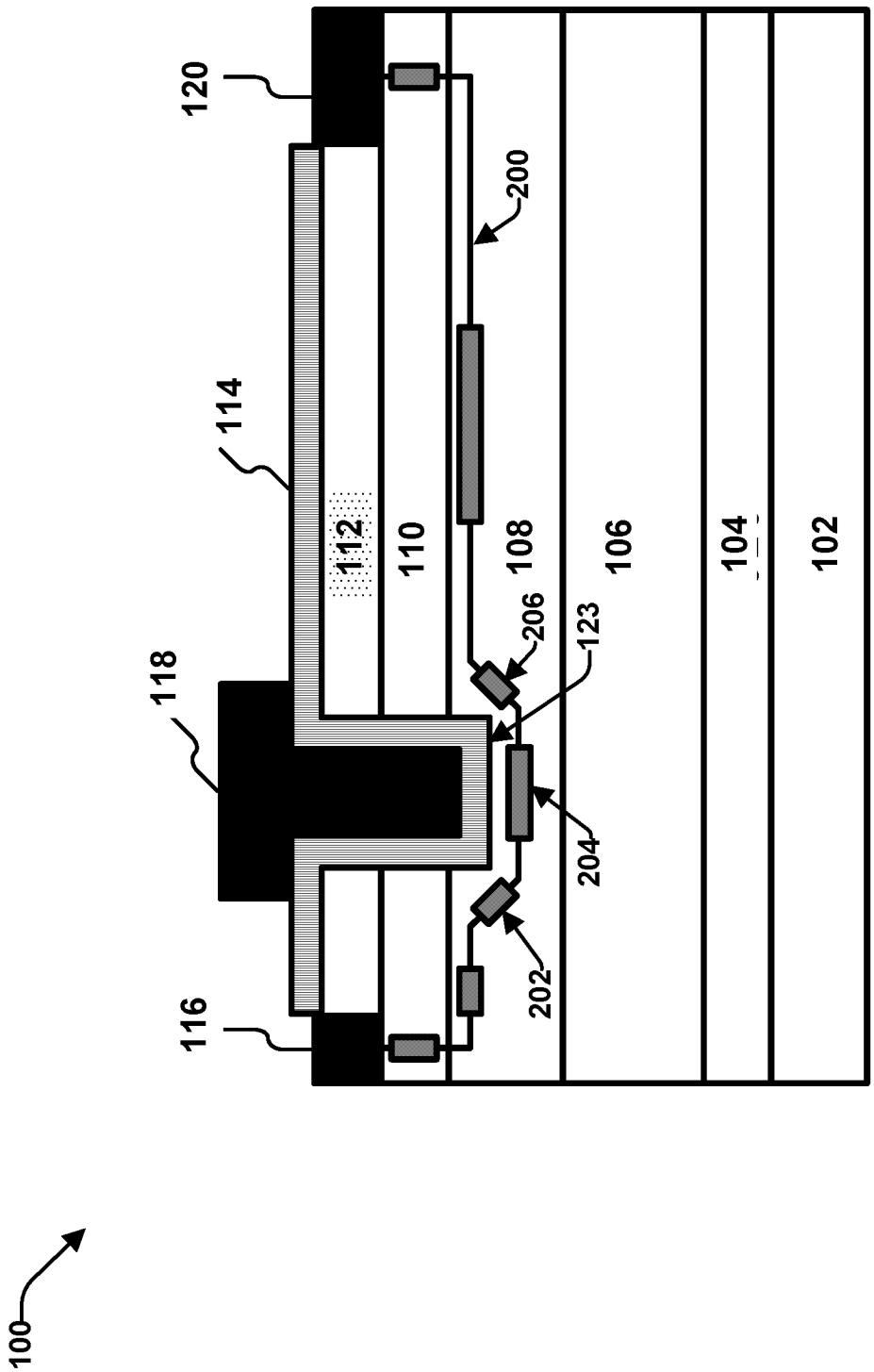


FIG. 2
(PRIOR ART)

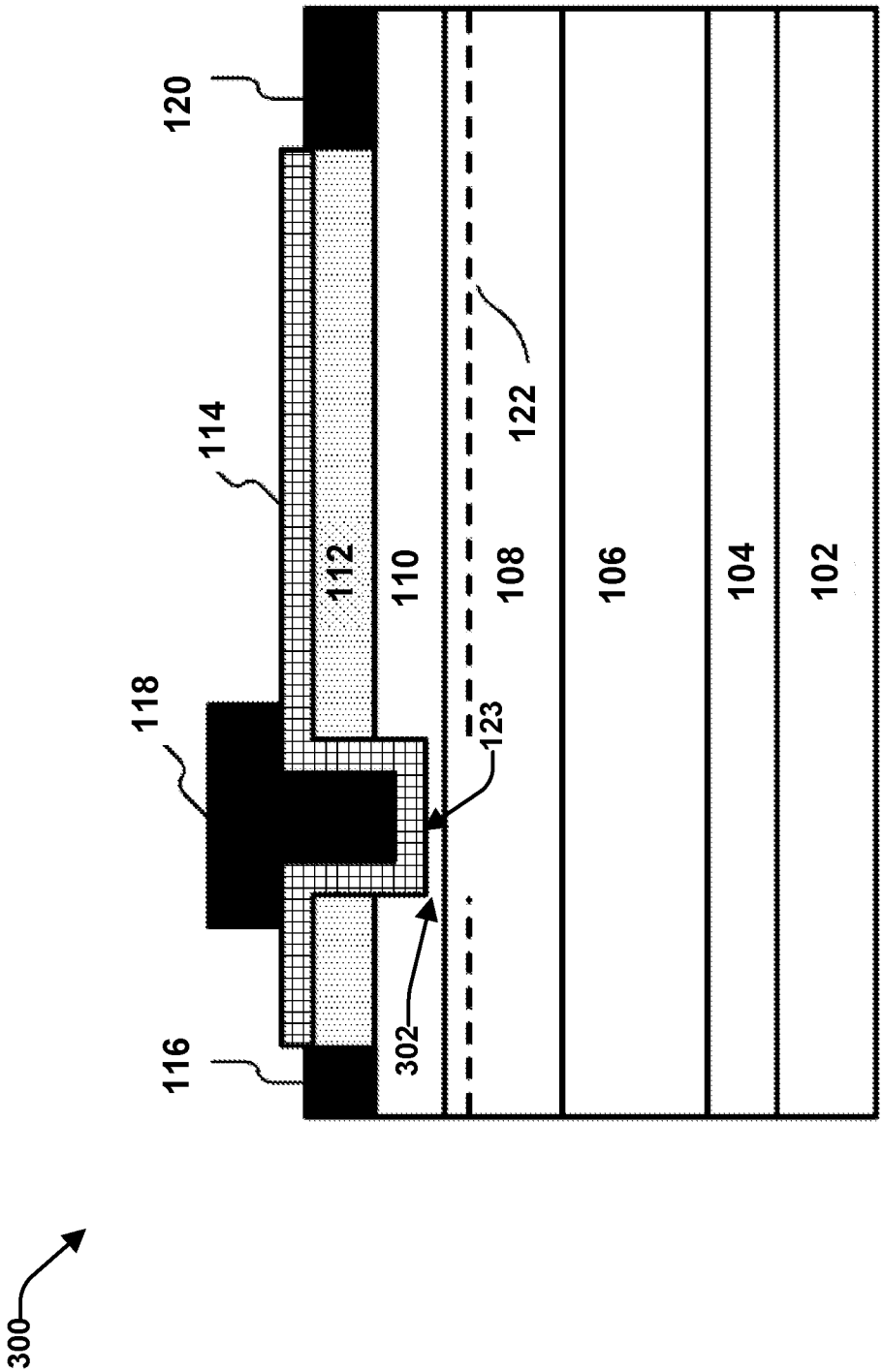


FIG. 3
(PRIOR ART)

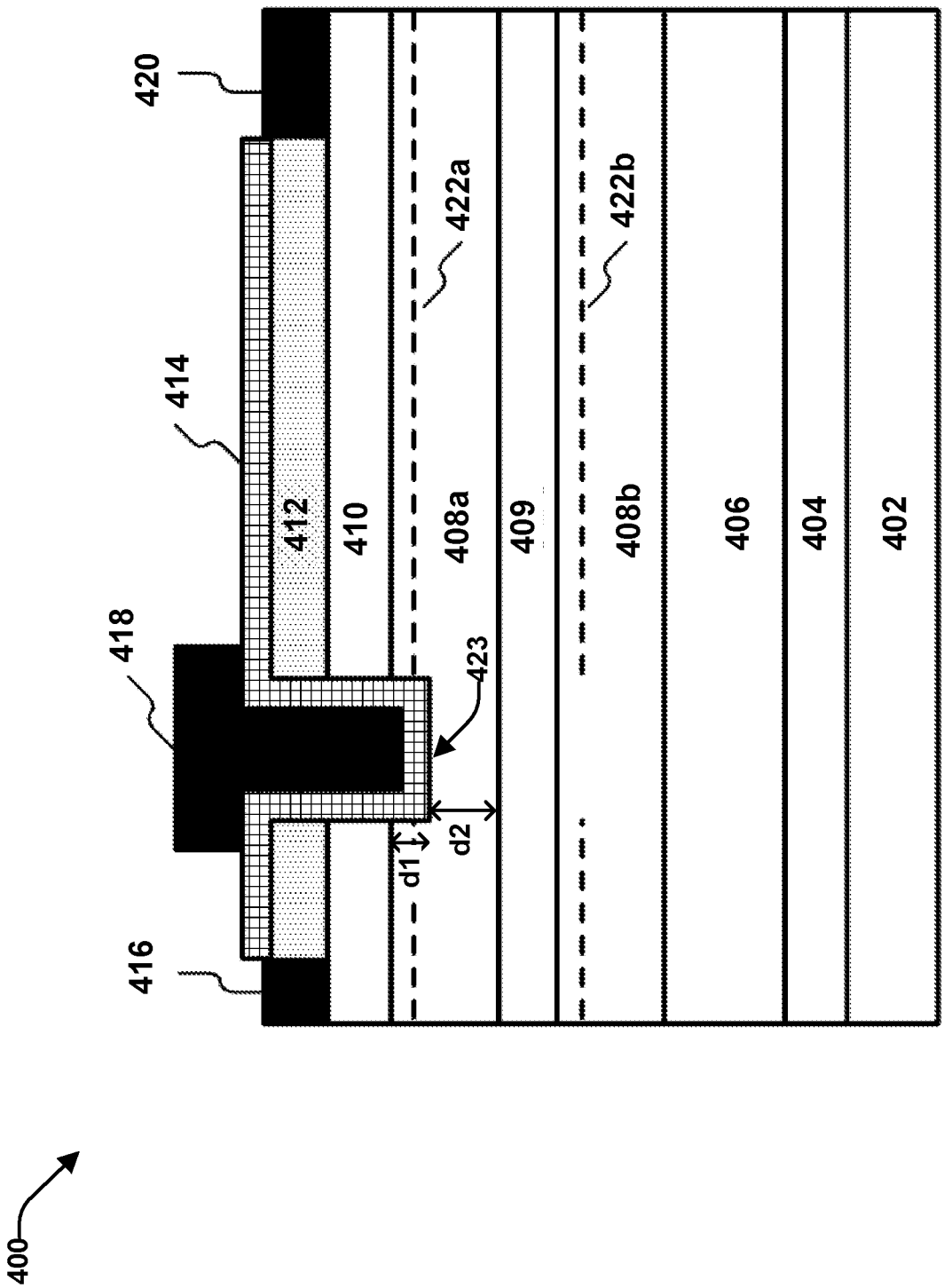

400
420
414
418
416
412
410
408a
409
408b
406
404
402
422a
422b
423
d1
d2

FIG. 4

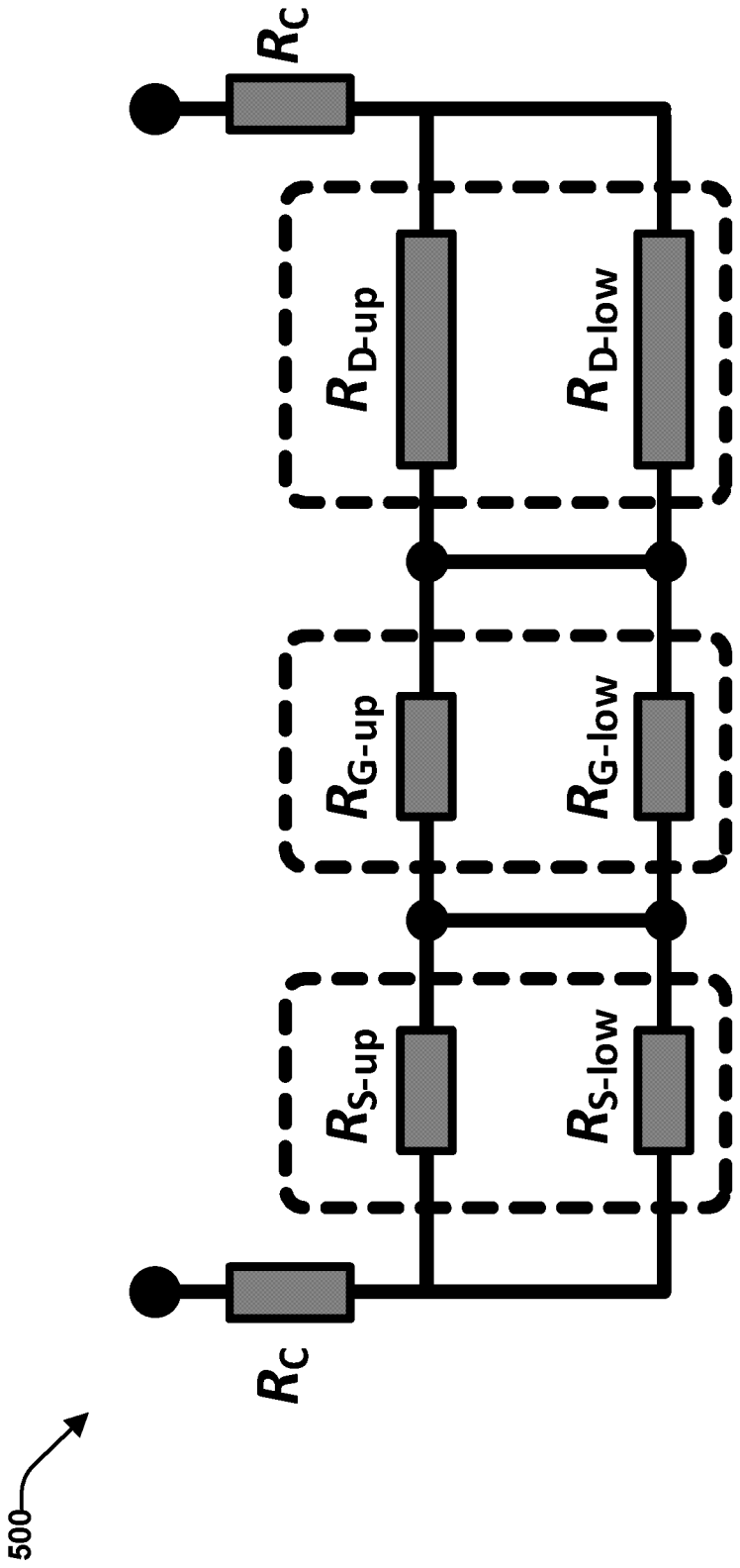

500
R_C
$R_{D\text{-}up}$
$R_{D\text{-}low}$
$R_{G\text{-}up}$
$R_{G\text{-}low}$
$R_{S\text{-}up}$
$R_{S\text{-}low}$
R_C
$R = R_S + R_G + R_D + 2R_C$
$= R_{S\text{-}up}//R_{S\text{-}low} + R_{G\text{-}up}//R_{G\text{-}low} + R_{D\text{-}up}//R_{D\text{-}low} + 2R_C$

FIG. 5

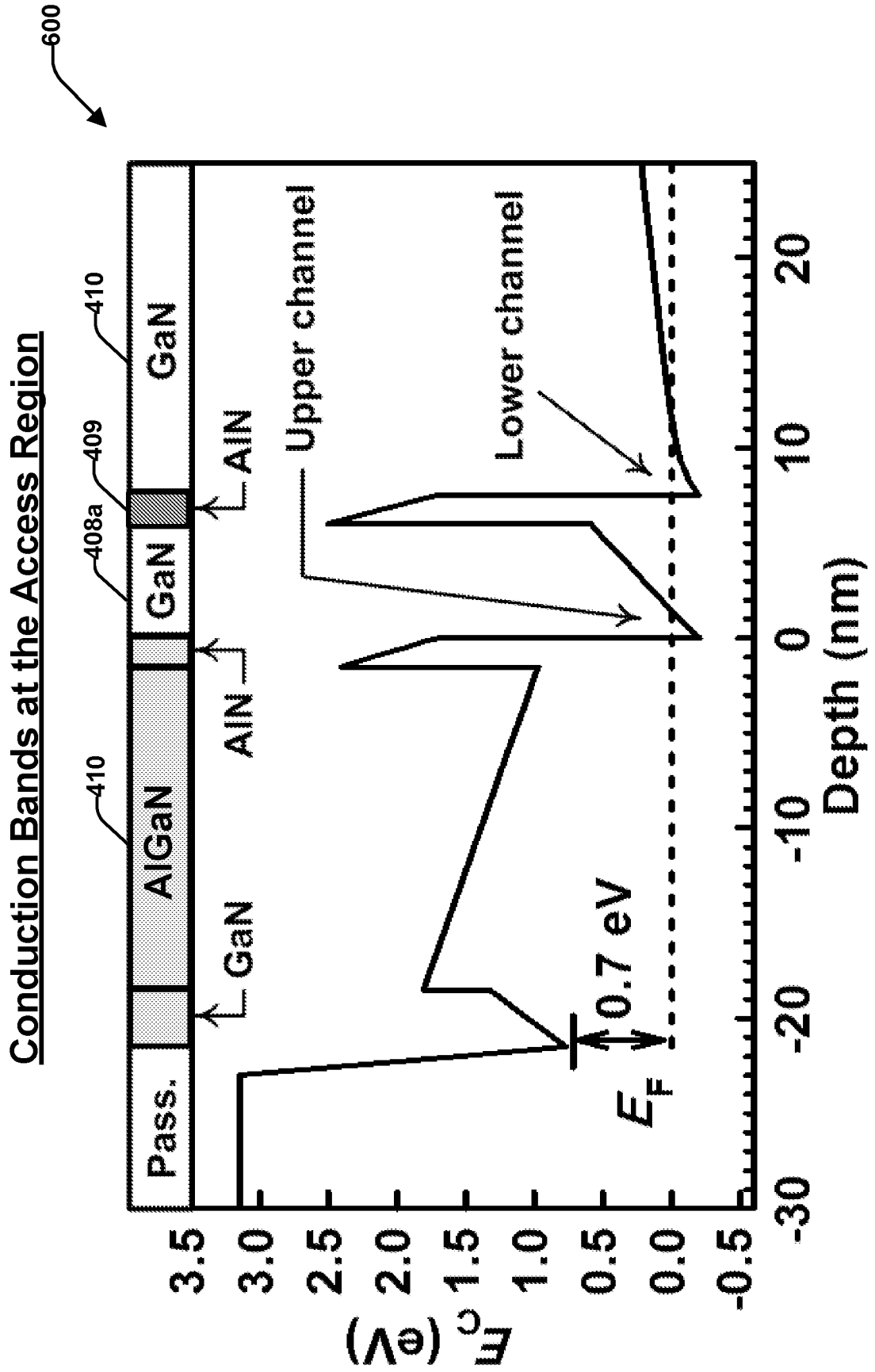

600
Conduction Bands at the Access Region
410
GaN
409
AlN
408a
GaN
AlN
410
AlGaN
GaN
Pass.
Upper channel
Lower channel
0.7 eV
E_F
E_C (eV)
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
-0.5
-30
-20
-10
0
10
20
Depth (nm)

FIG. 6

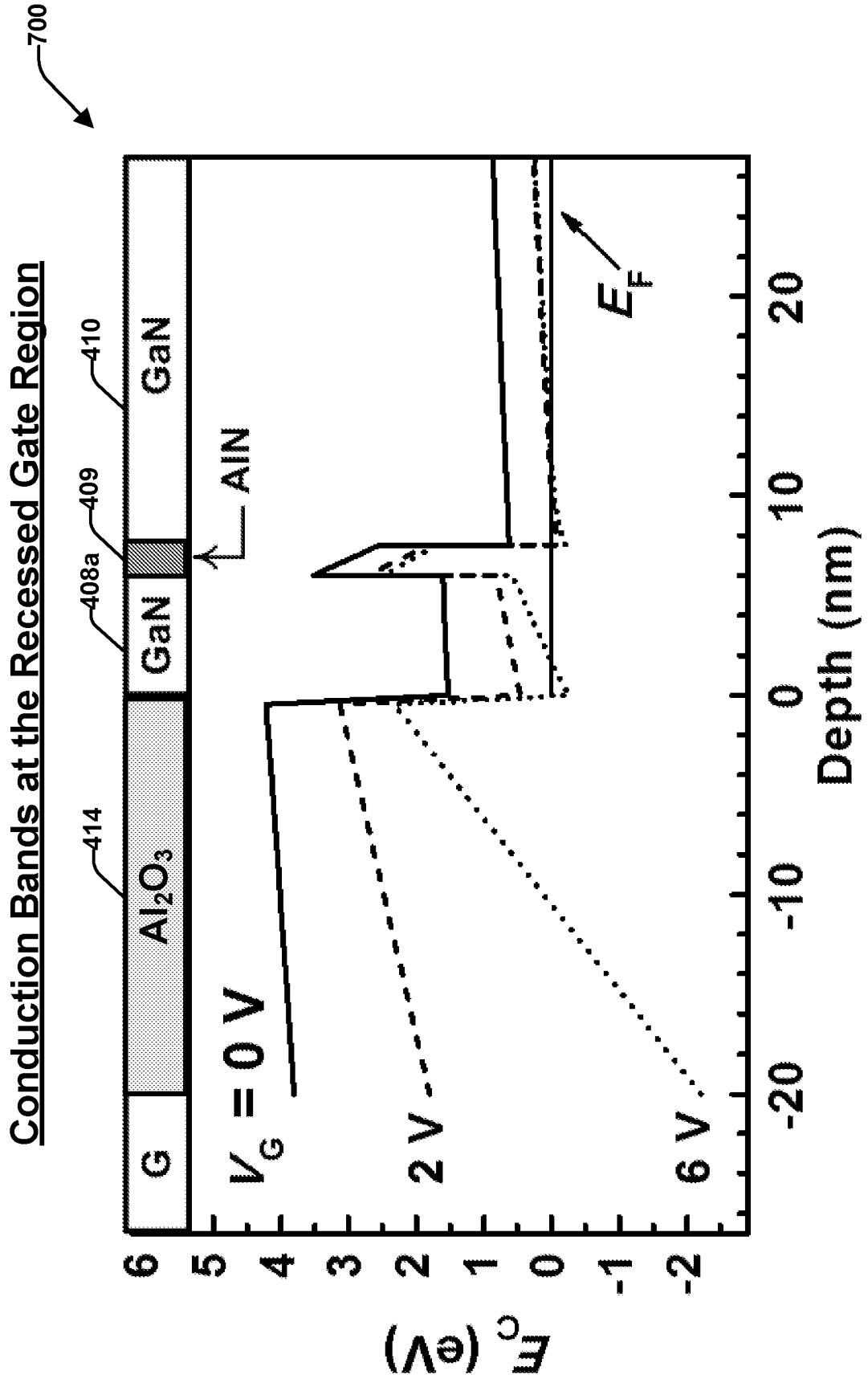

700
Conduction Bands at the Recessed Gate Region
G
Al2O3
414
GaN
408a
AlN
409
GaN
410
VG = 0 V
2 V
6 V
EF
EC (eV)
6
5
4
3
2
1
0
-1
-2
-20
-10
0
10
20
Depth (nm)

FIG. 7

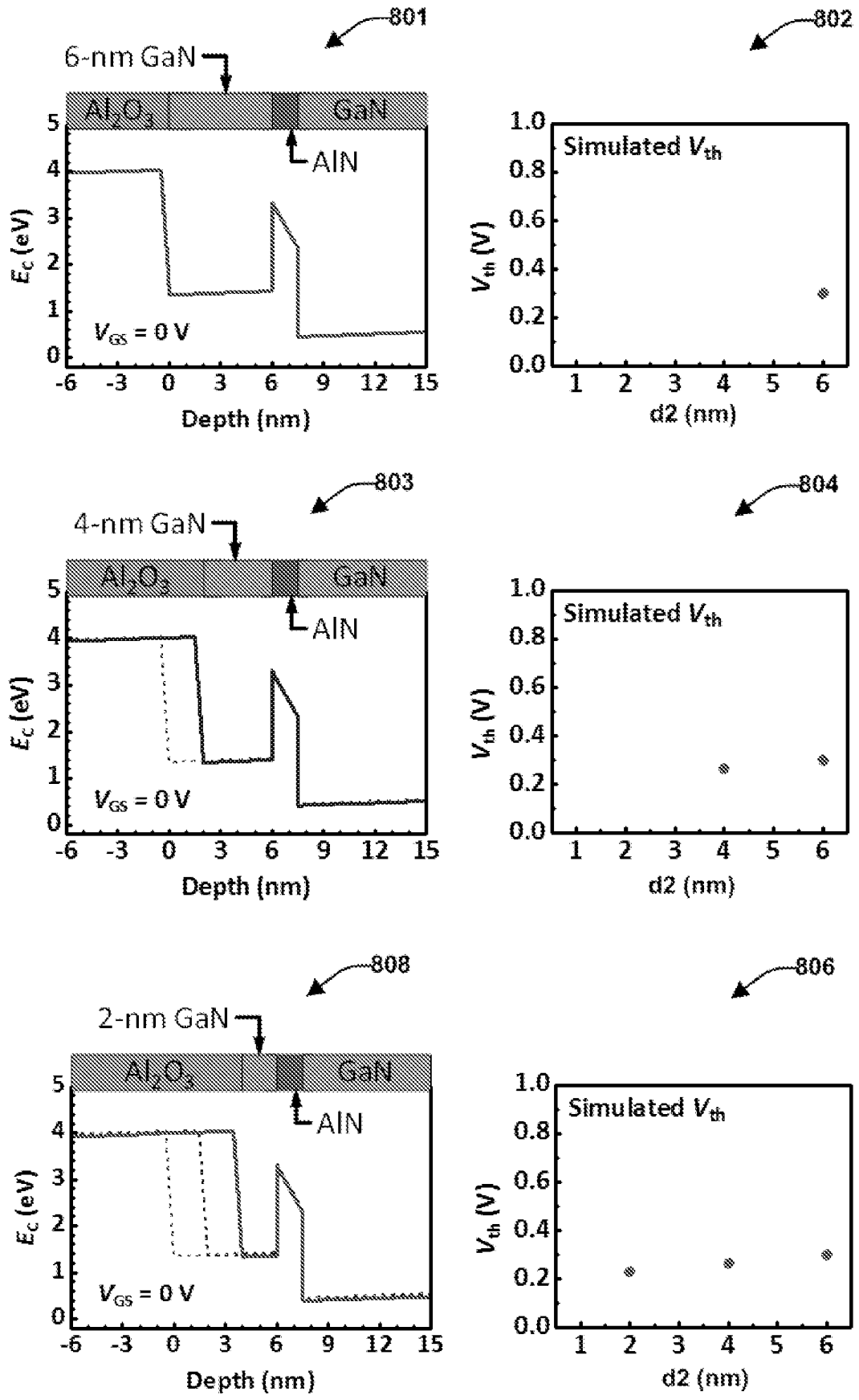

801
6-nm GaN
Al_2O_3
GaN
AlN
E_C (eV)
V_{GS} = 0 V
Depth (nm)
802
Simulated V_{th}
V_{th} (V)
d2 (nm)
803
4-nm GaN
Al_2O_3
GaN
AlN
E_C (eV)
V_{GS} = 0 V
Depth (nm)
804
Simulated V_{th}
V_{th} (V)
d2 (nm)
808
2-nm GaN
Al_2O_3
GaN
AlN
E_C (eV)
V_{GS} = 0 V
Depth (nm)
806
Simulated V_{th}
V_{th} (V)
d2 (nm)

FIG. 8

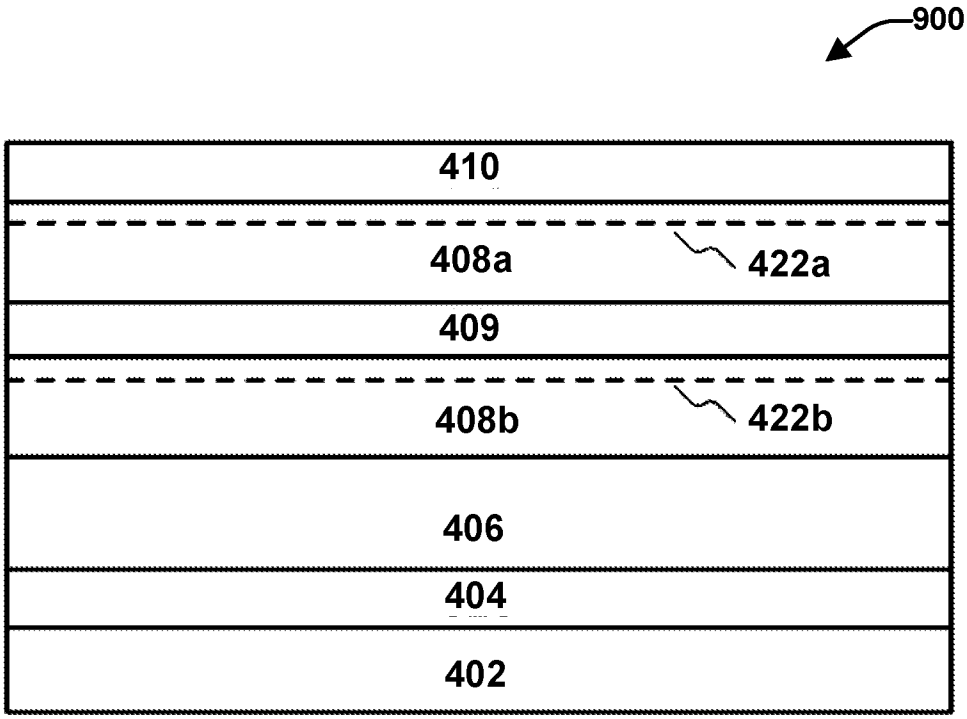

900
410
408a
422a
409
408b
422b
406
404
402

FIG. 9

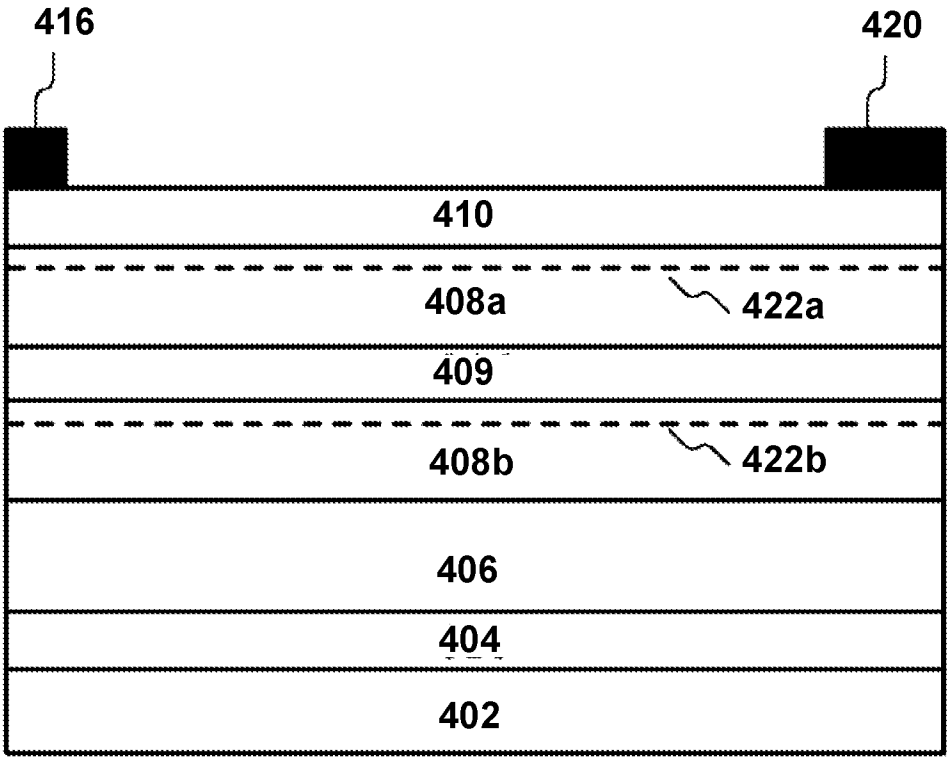

416
420
410
408a
422a
409
408b
422b
406
404
402

FIG. 10

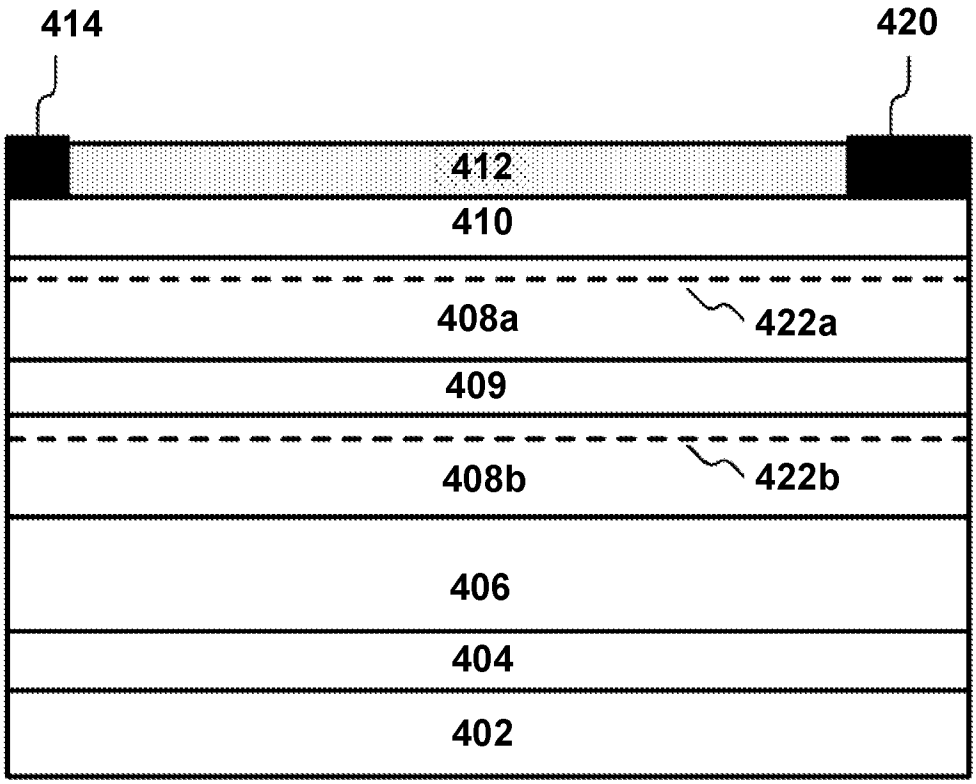

414
420
412
410
408a
422a
409
408b
422b
406
404
402

FIG. 11

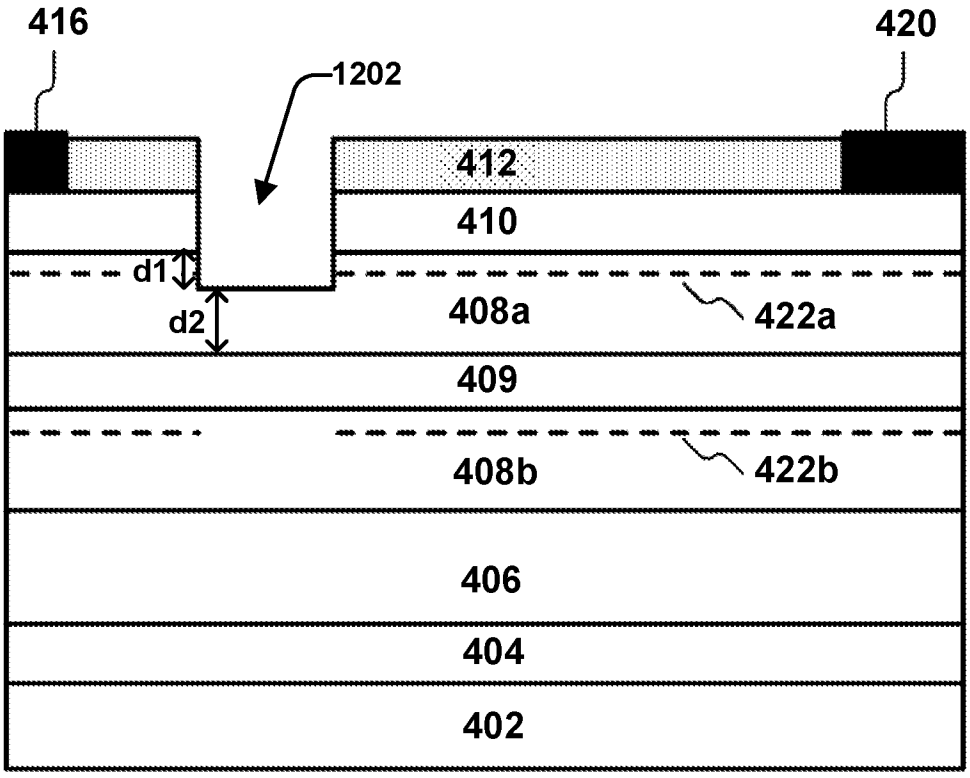

416
420
1202
412
410
d1
d2
408a
422a
409
408b
422b
406
404
402

FIG. 12

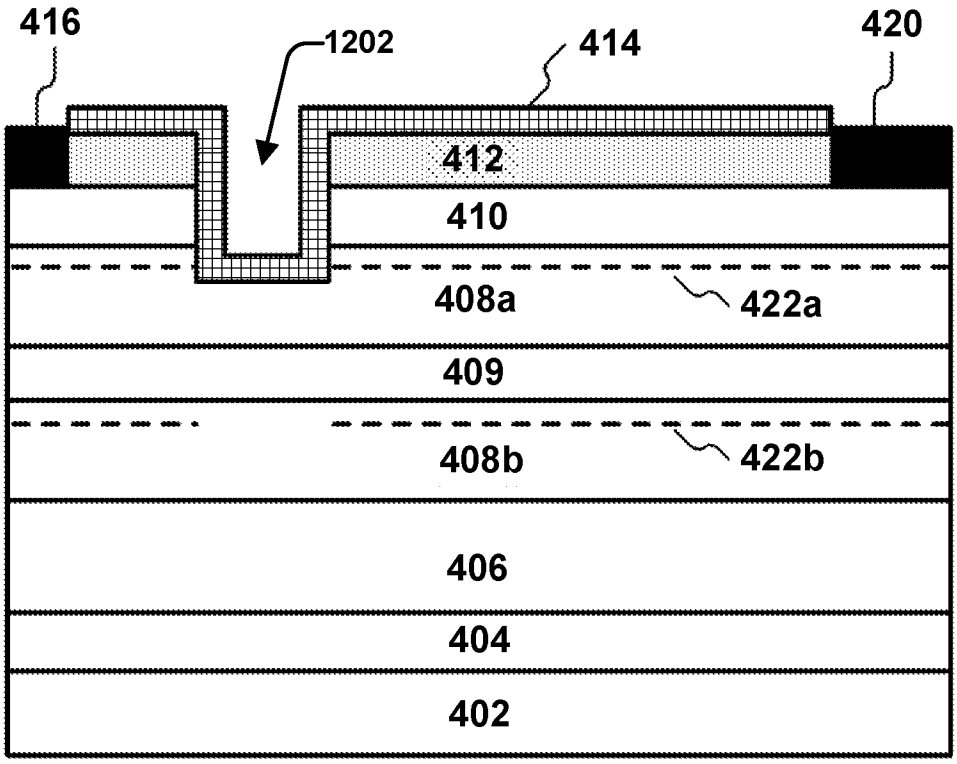

416
1202
414
420
412
410
408a
422a
409
408b
422b
406
404
402

FIG. 13

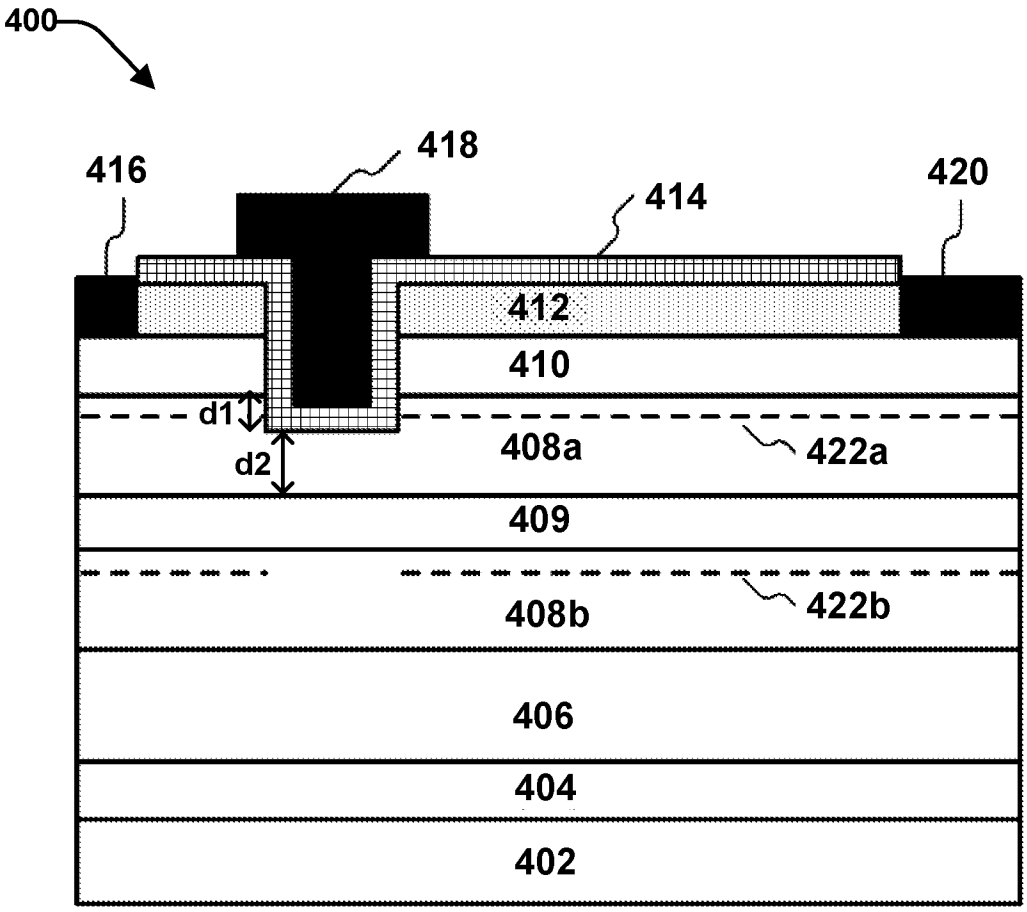

400
418
416
414
420
412
410
d1
d2
408a
422a
409
408b
422b
406
404
402

FIG. 14

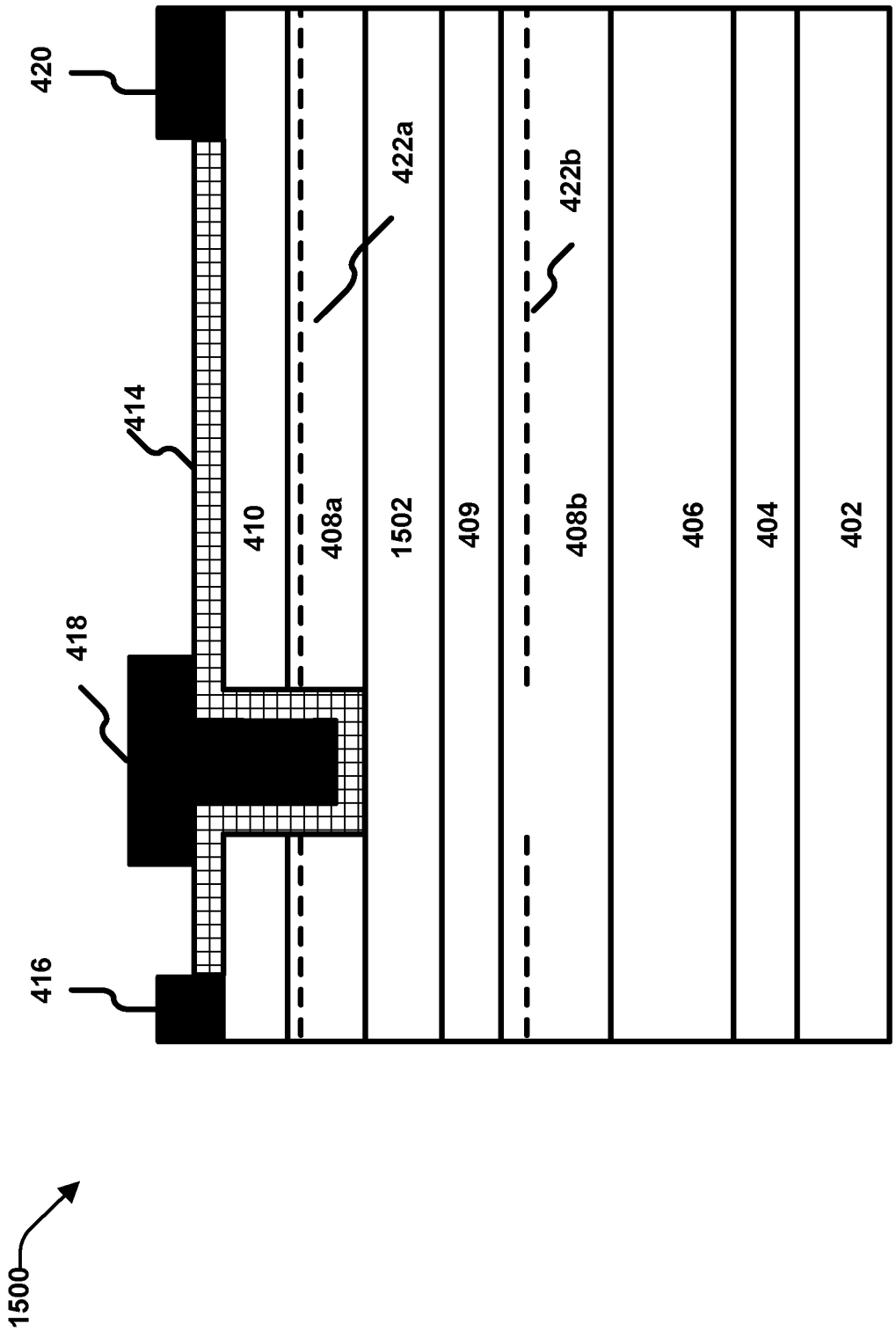

1500
420
414
418
416
410
408a
422a
1502
409
422b
408b
406
404
402

FIG. 15

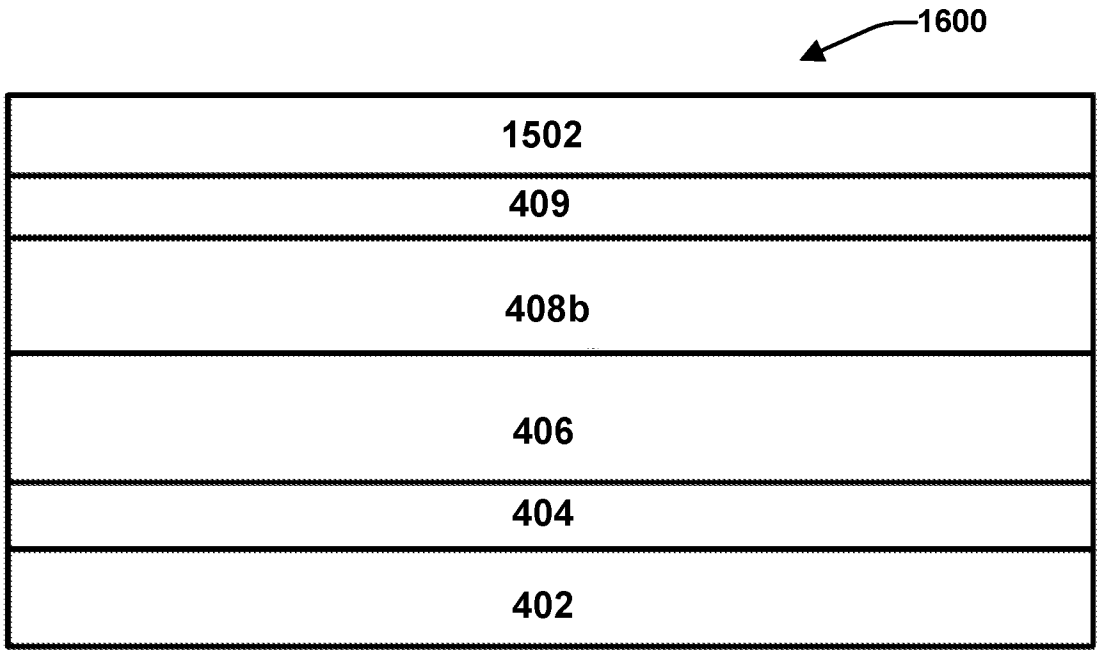


FIG. 16

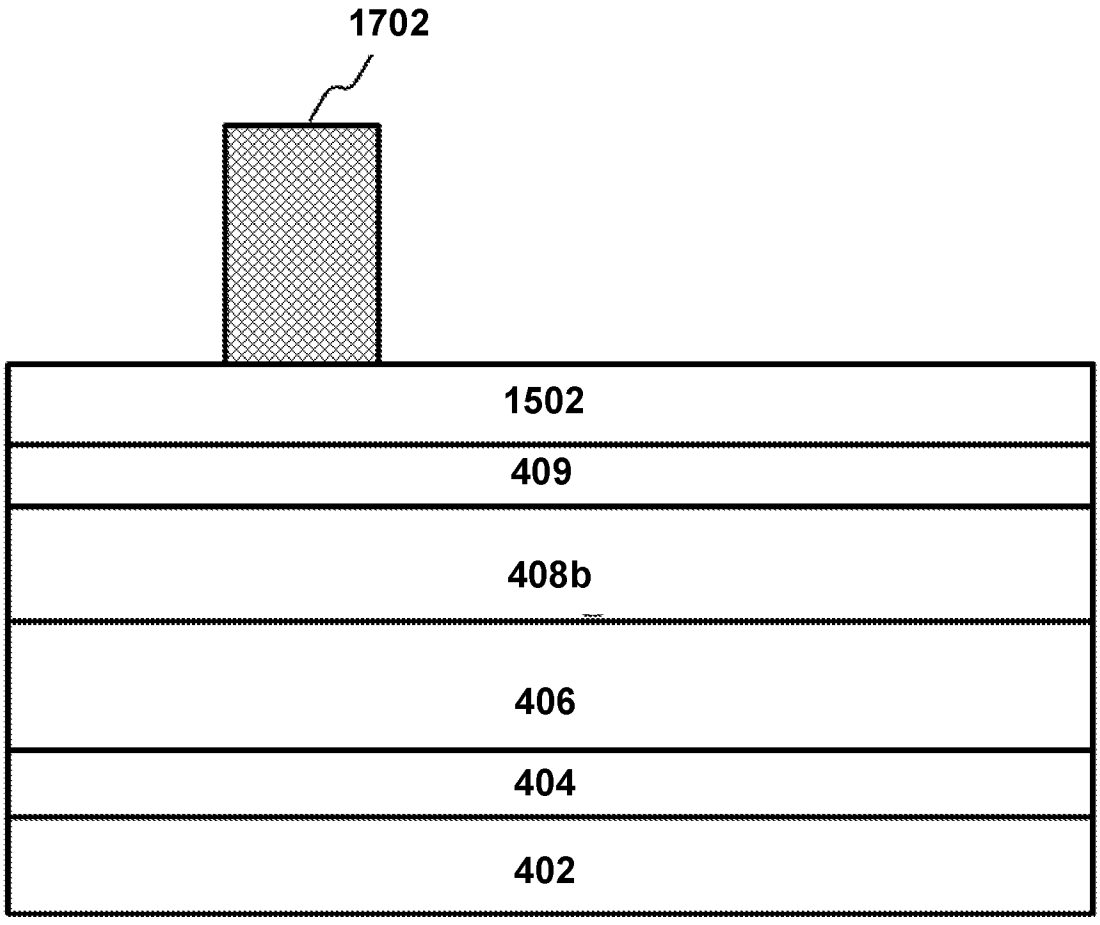


FIG. 17

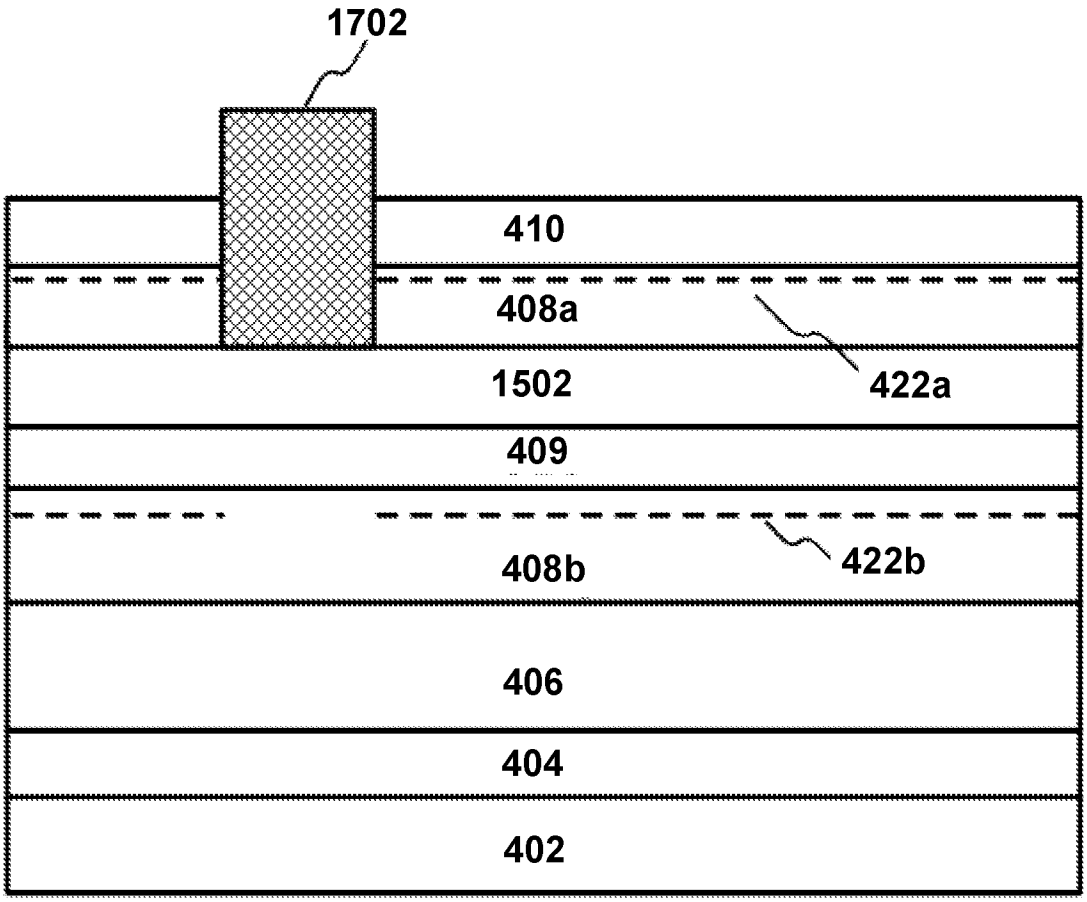

1702
410
408a
1502
422a
409
408b
422b
406
404
402

FIG. 18

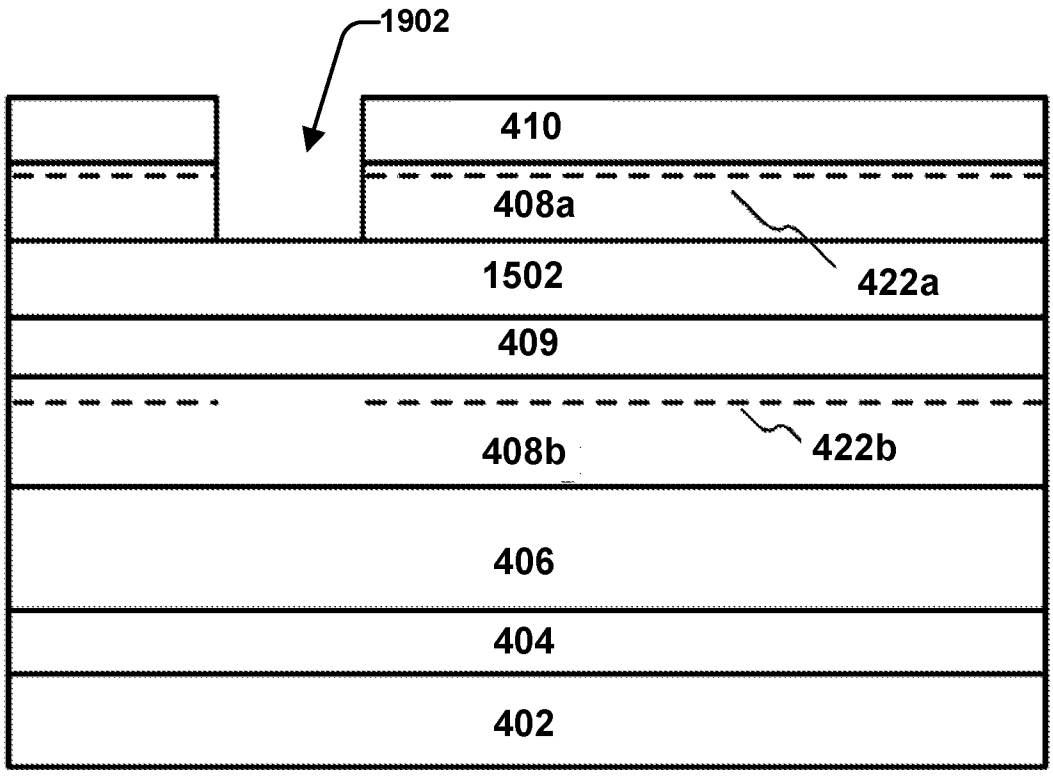

1902
410
408a
1502
422a
409
408b
422b
406
404
402

FIG. 19

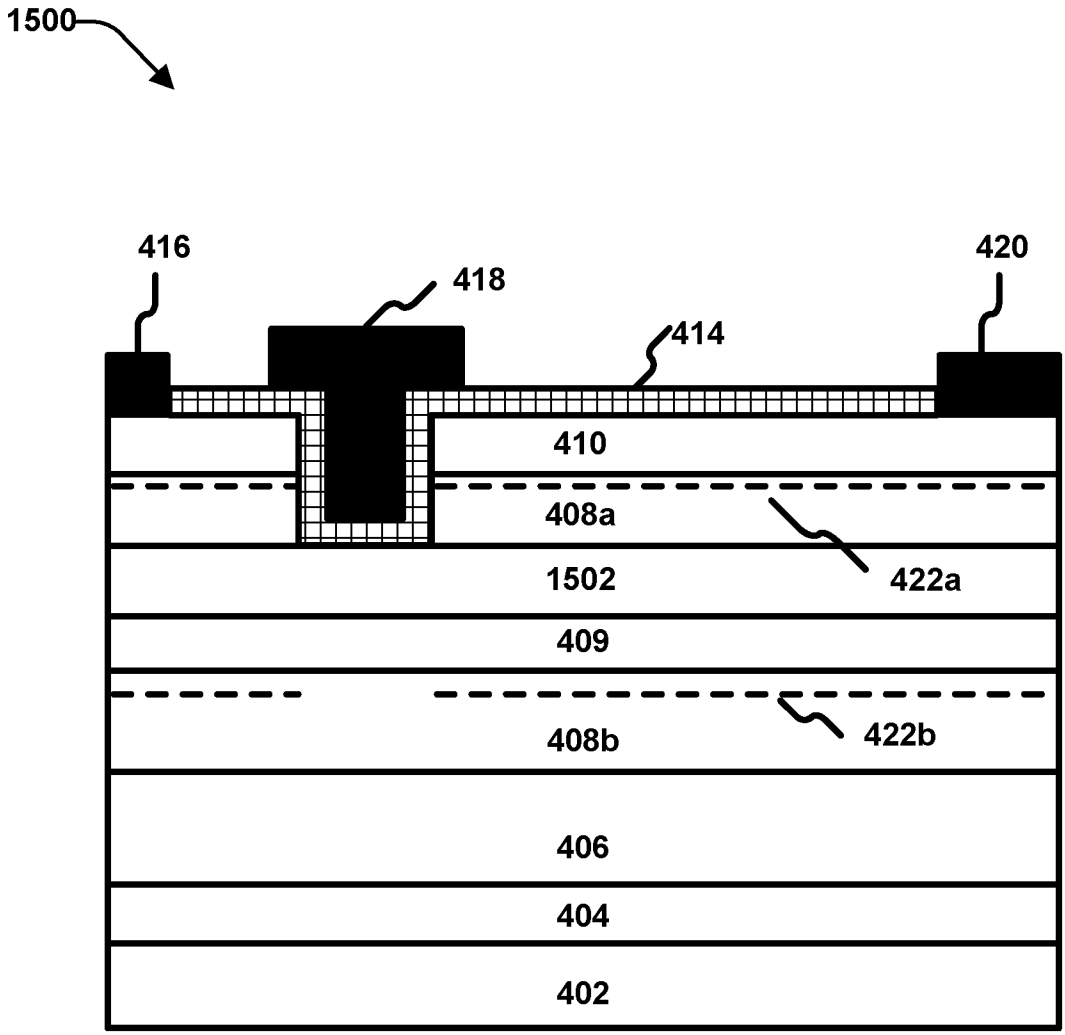

1500
416
418
414
420
410
408a
1502
422a
409
408b
422b
406
404
402

FIG. 20

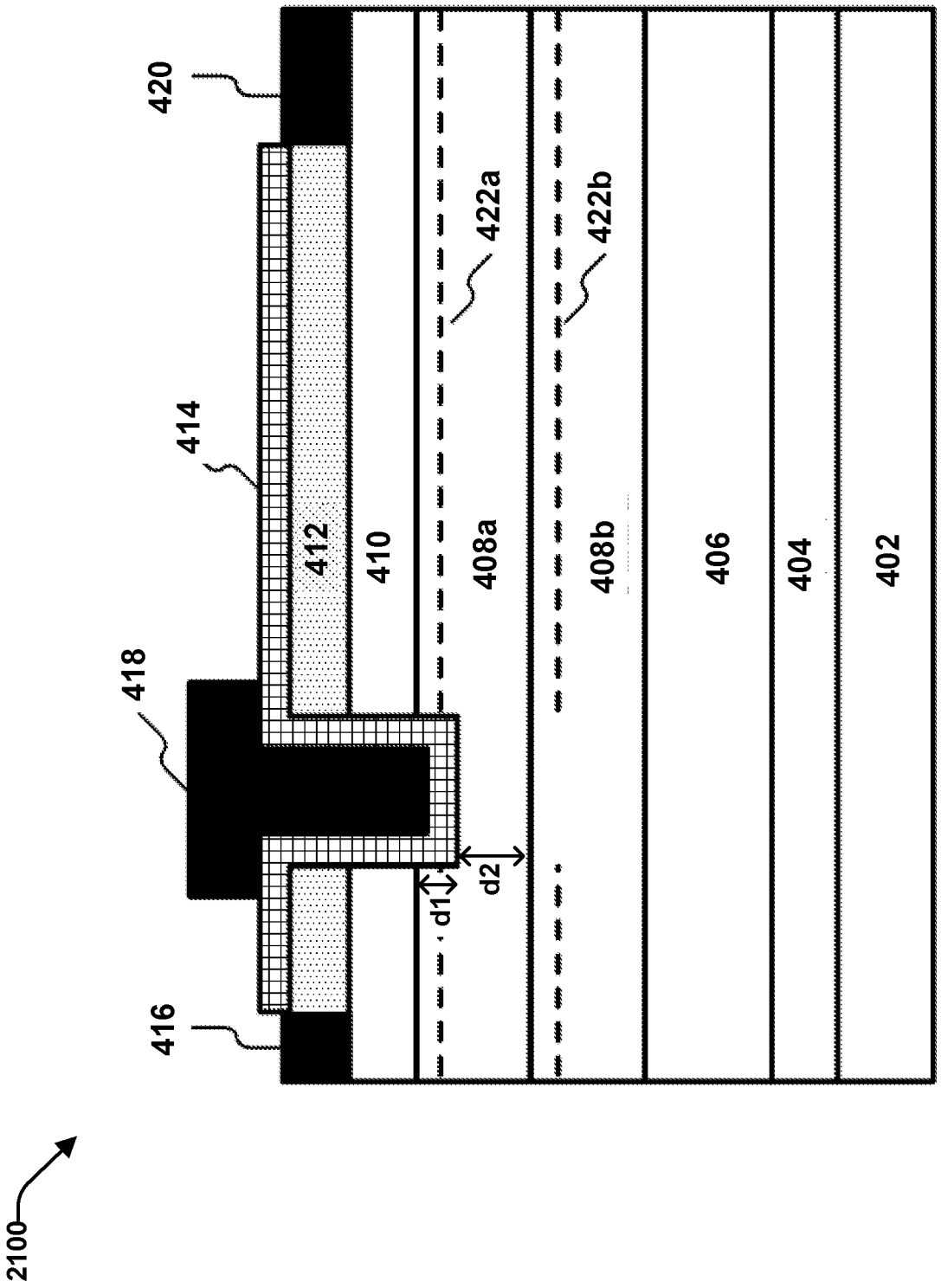

2100
420
414
418
416
412
410
408a
408b
406
404
402
422a
422b
d1
d2

FIG. 21

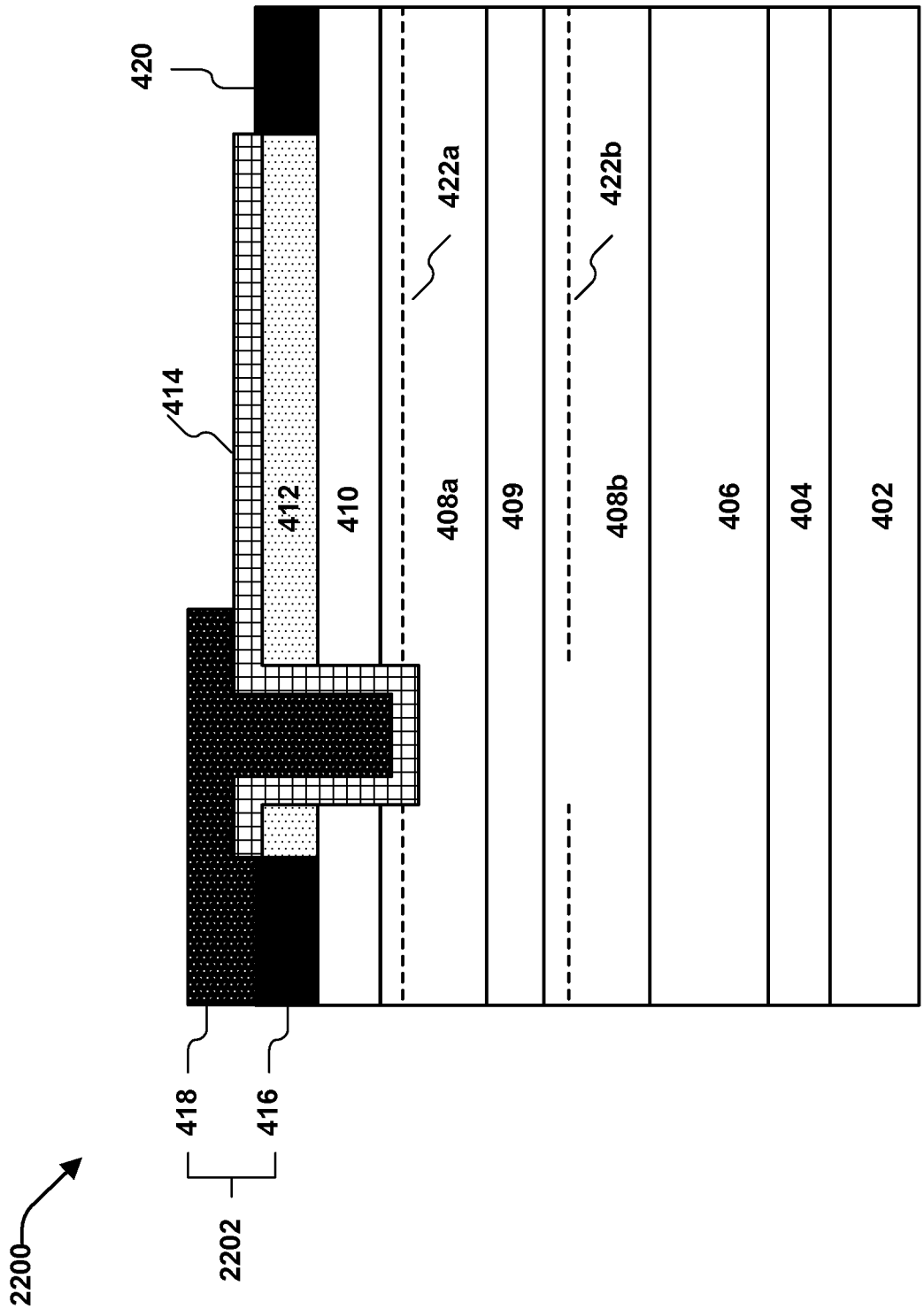
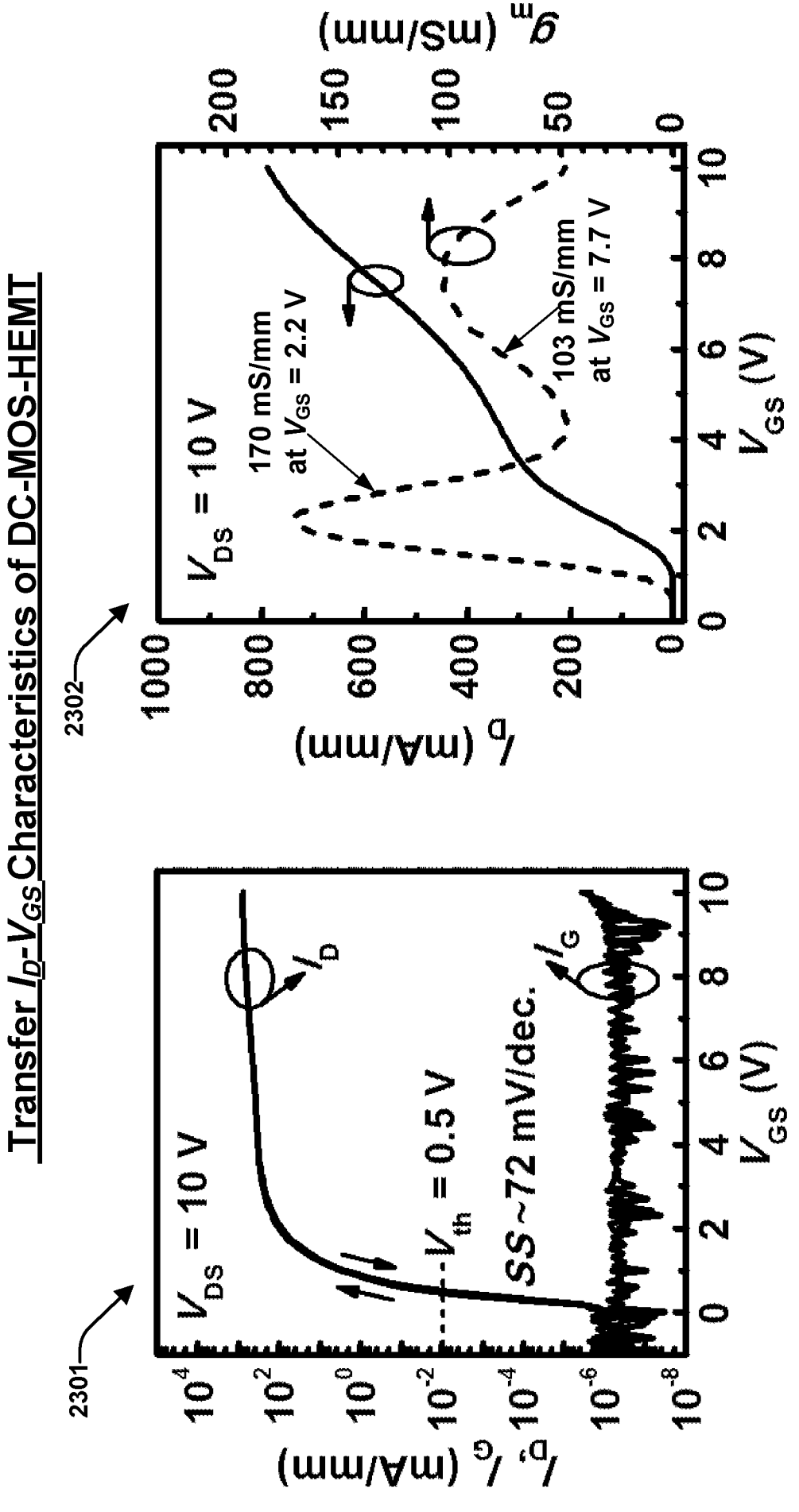

2200
2202
418
416
414
420
412
410
408a
409
408b
406
404
402
422a
422b

FIG. 22



V_{th} (V) @ I_D = 10 μA/mm	ΔV_{th} (mV)	SS (mV/dec)	I_{on}/I_{off}	$g_{m\text{-}max}$ (mS/mm) with V_{DS} = 10 V
0.5	50	72	10^9	170

FIG. 23

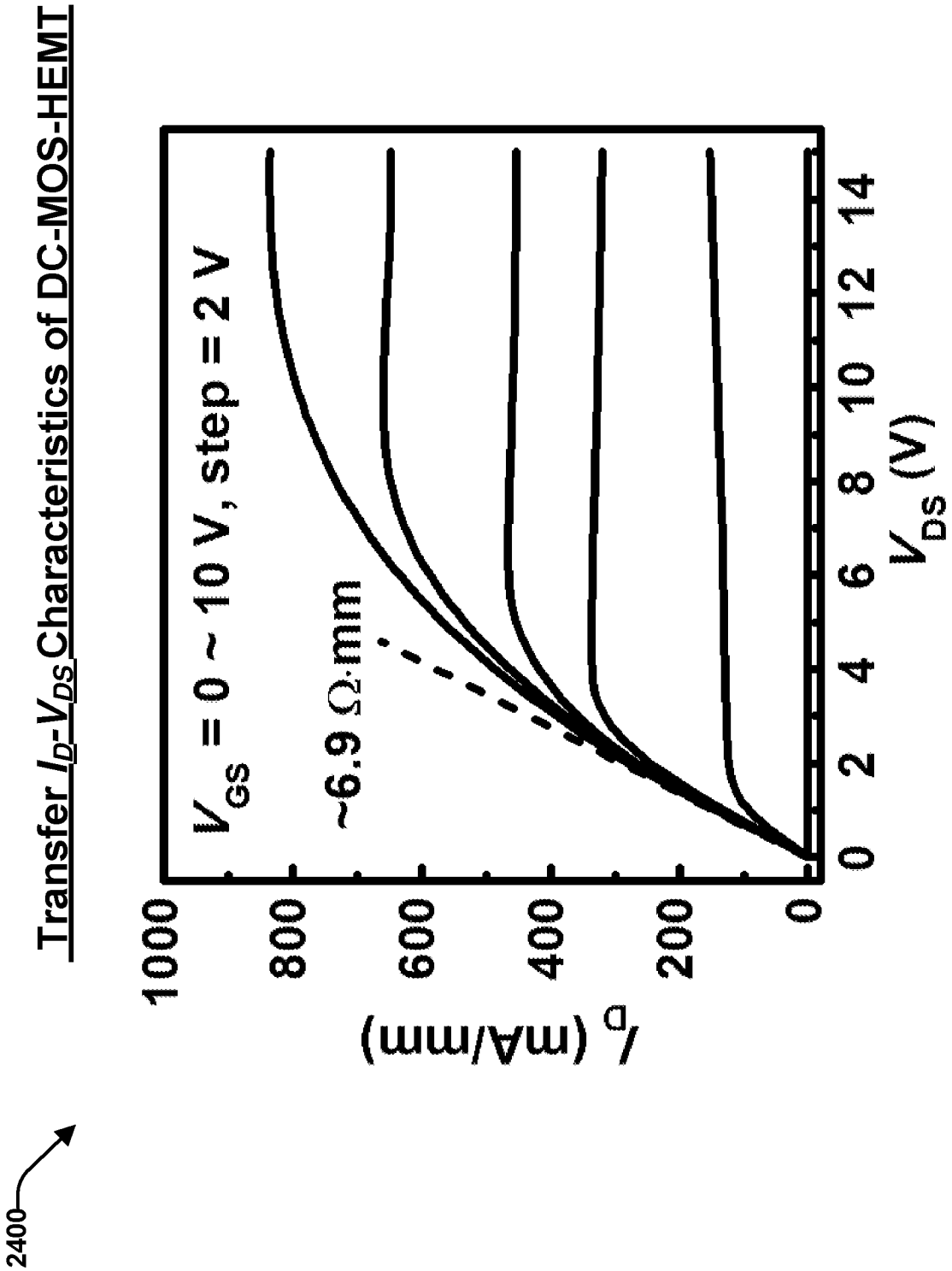

2400
Transfer I_D-V_{DS} Characteristics of DC-MOS-HEMT
I_D (mA/mm)
1000
800
600
400
200
0
0
2
4
6
8
10
12
14
V_{DS} (V)
V_{GS} = 0 ~ 10 V, step = 2 V
~6.9 Ω·mm

FIG. 24

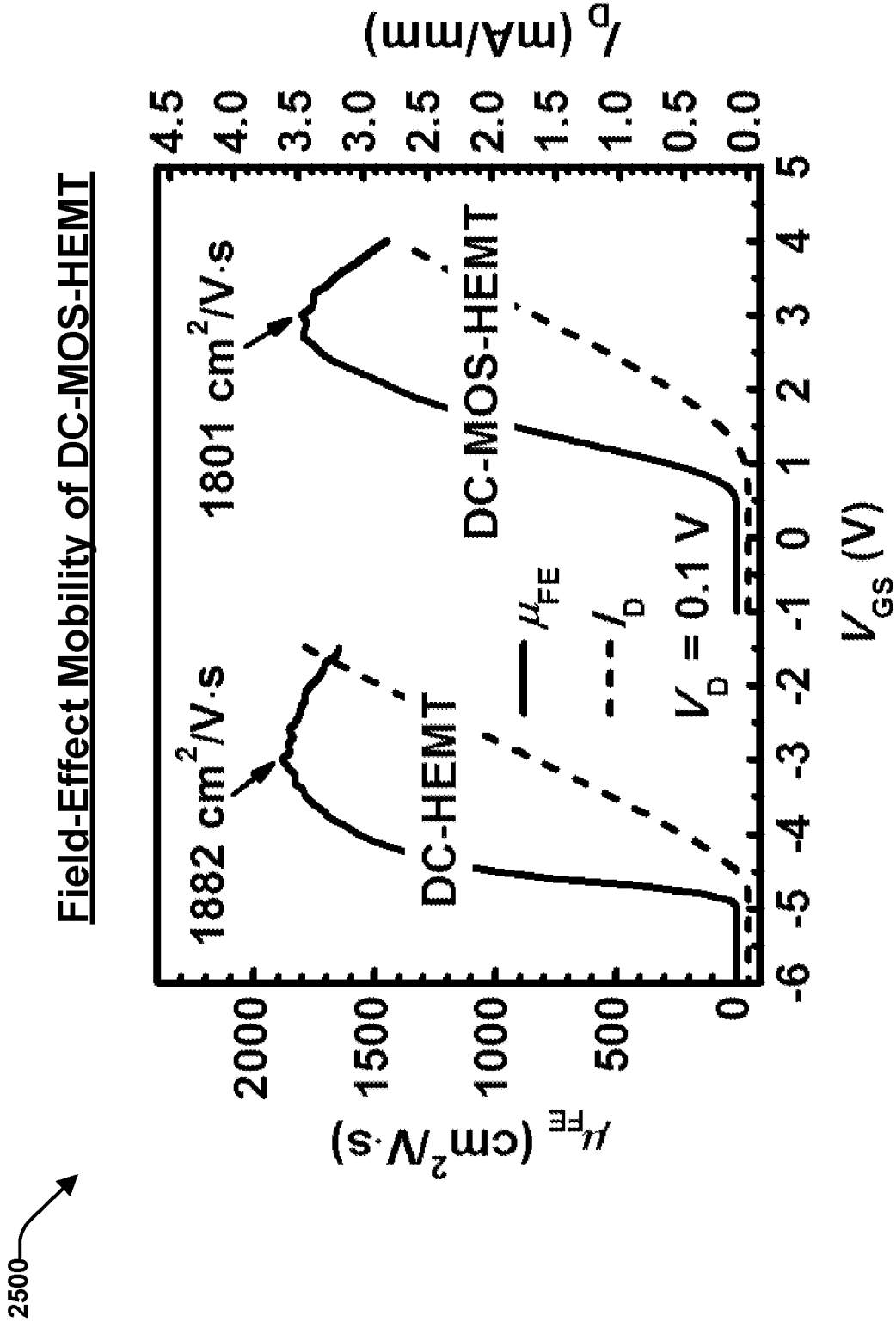

2500
Field-Effect Mobility of DC-MOS-HEMT
1882 cm²/V·s
1801 cm²/V·s
DC-HEMT
DC-MOS-HEMT
μ_{FE}
I_D
V_D = 0.1 V
μ_{FE} (cm²/V·s)
I_D (mA/mm)
V_{GS} (V)
0
500
1000
1500
2000
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
-6
-5
-4
-3
-2
-1
0
1
2
3
4
5

FIG. 25

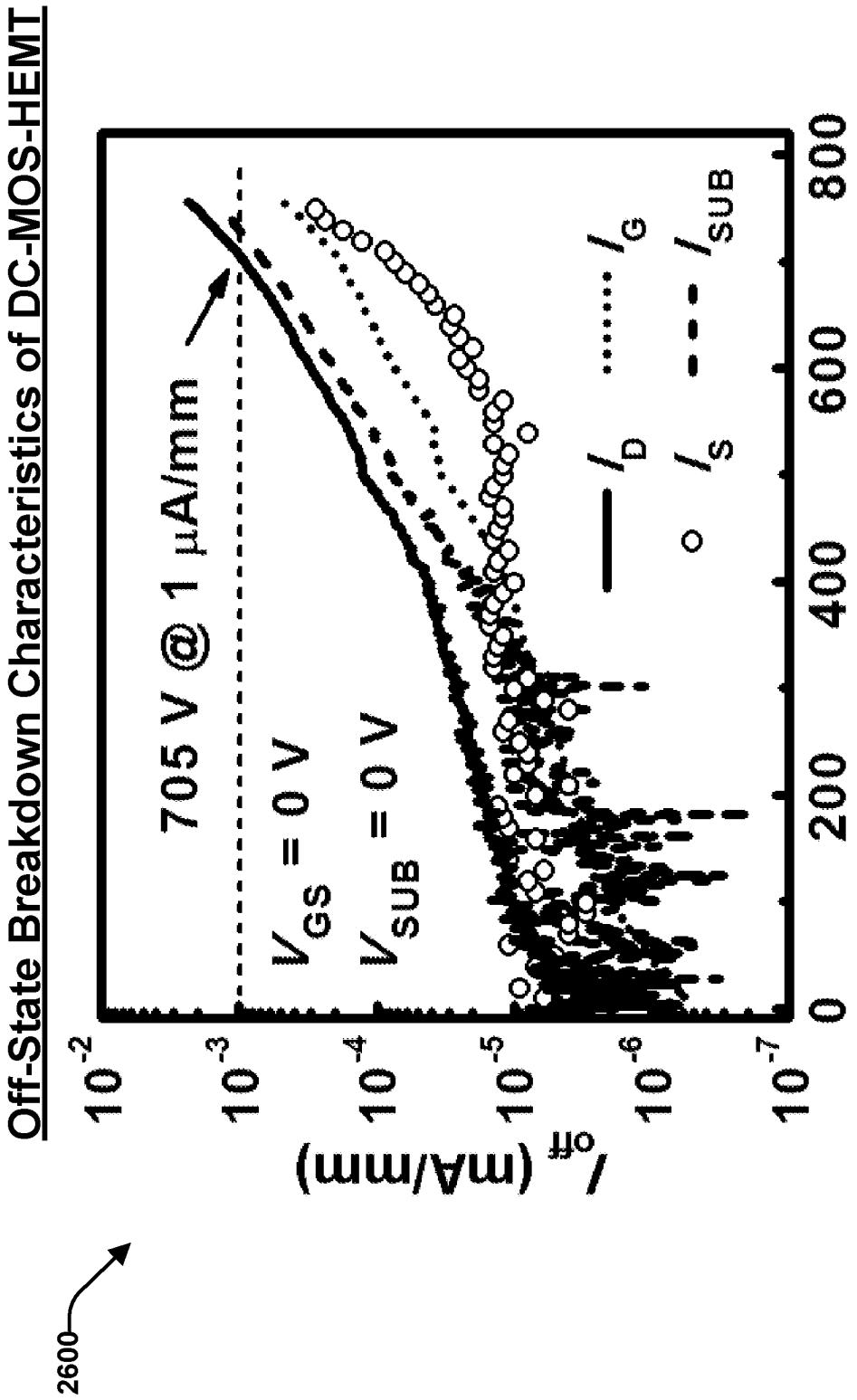

Off-State Breakdown Characteristics of DC-MOS-HEMT
705 V @ 1 μA/mm
V_{GS} = 0 V
V_{SUB} = 0 V
I_D
I_G
I_S
I_{SUB}
I_{off} (mA/mm)
V_{DS} (V)
10^-2
10^-3
10^-4
10^-5
10^-6
10^-7
0
200
400
600
800
2600

FIG. 26

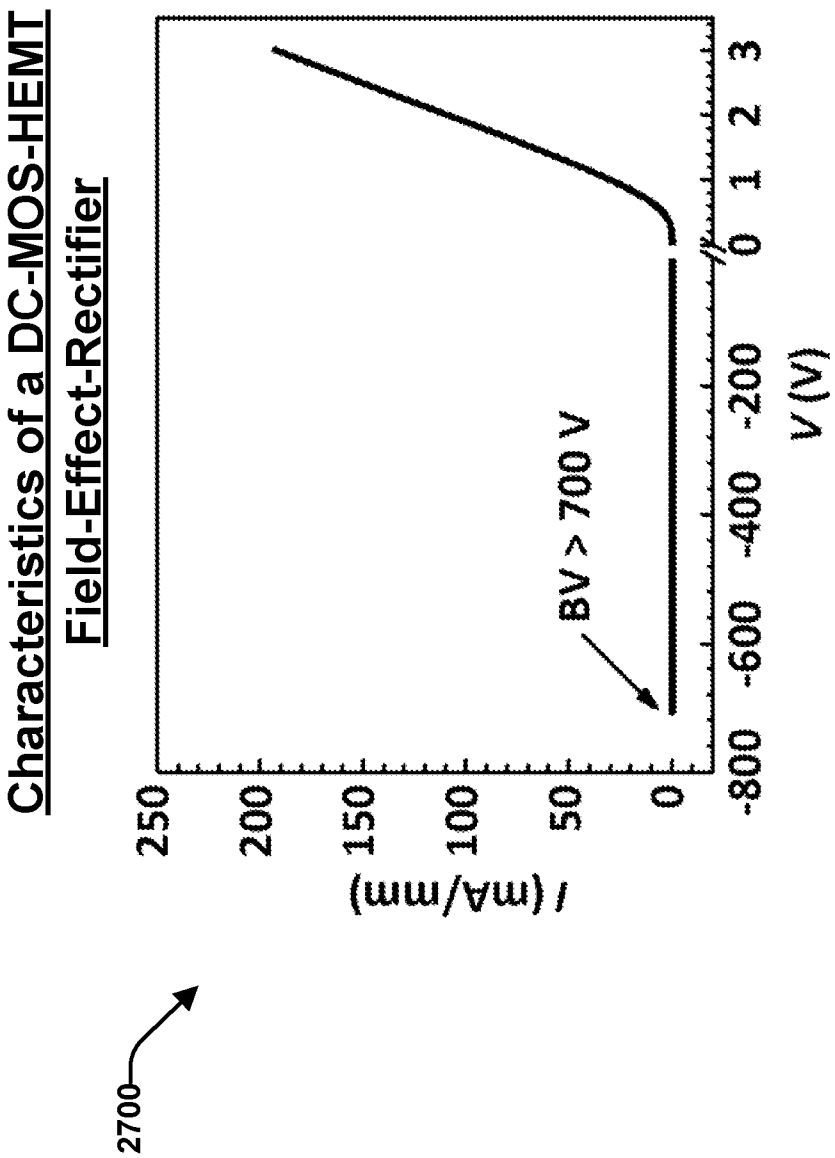

Characteristics of a DC-MOS-HEMT
Field-Effect-Rectifier
2700
I (mA/mm)
250
200
150
100
50
0
-800
-600
-400
-200
0
1
2
3
V (V)
BV > 700 V

FIG. 27

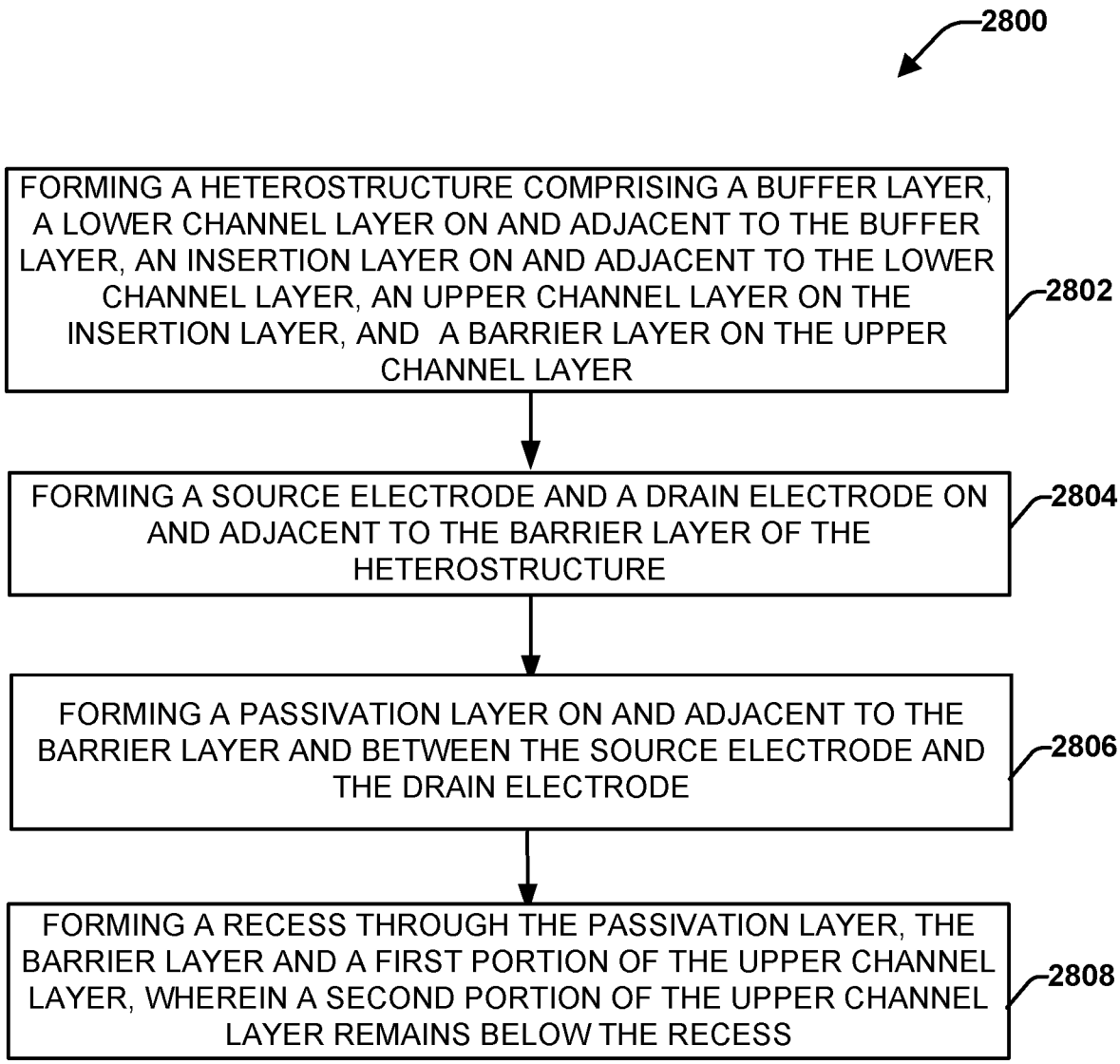

2800
FORMING A HETEROSTRUCTURE COMPRISING A BUFFER LAYER, A LOWER CHANNEL LAYER ON AND ADJACENT TO THE BUFFER LAYER, AN INSERTION LAYER ON AND ADJACENT TO THE LOWER CHANNEL LAYER, AN UPPER CHANNEL LAYER ON THE INSERTION LAYER, AND A BARRIER LAYER ON THE UPPER CHANNEL LAYER
2802
FORMING A SOURCE ELECTRODE AND A DRAIN ELECTRODE ON AND ADJACENT TO THE BARRIER LAYER OF THE HETEROSTRUCTURE
2804
FORMING A PASSIVATION LAYER ON AND ADJACENT TO THE BARRIER LAYER AND BETWEEN THE SOURCE ELECTRODE AND THE DRAIN ELECTRODE
2806
FORMING A RECESS THROUGH THE PASSIVATION LAYER, THE BARRIER LAYER AND A FIRST PORTION OF THE UPPER CHANNEL LAYER, WHEREIN A SECOND PORTION OF THE UPPER CHANNEL LAYER REMAINS BELOW THE RECESS
2808

FIG. 28

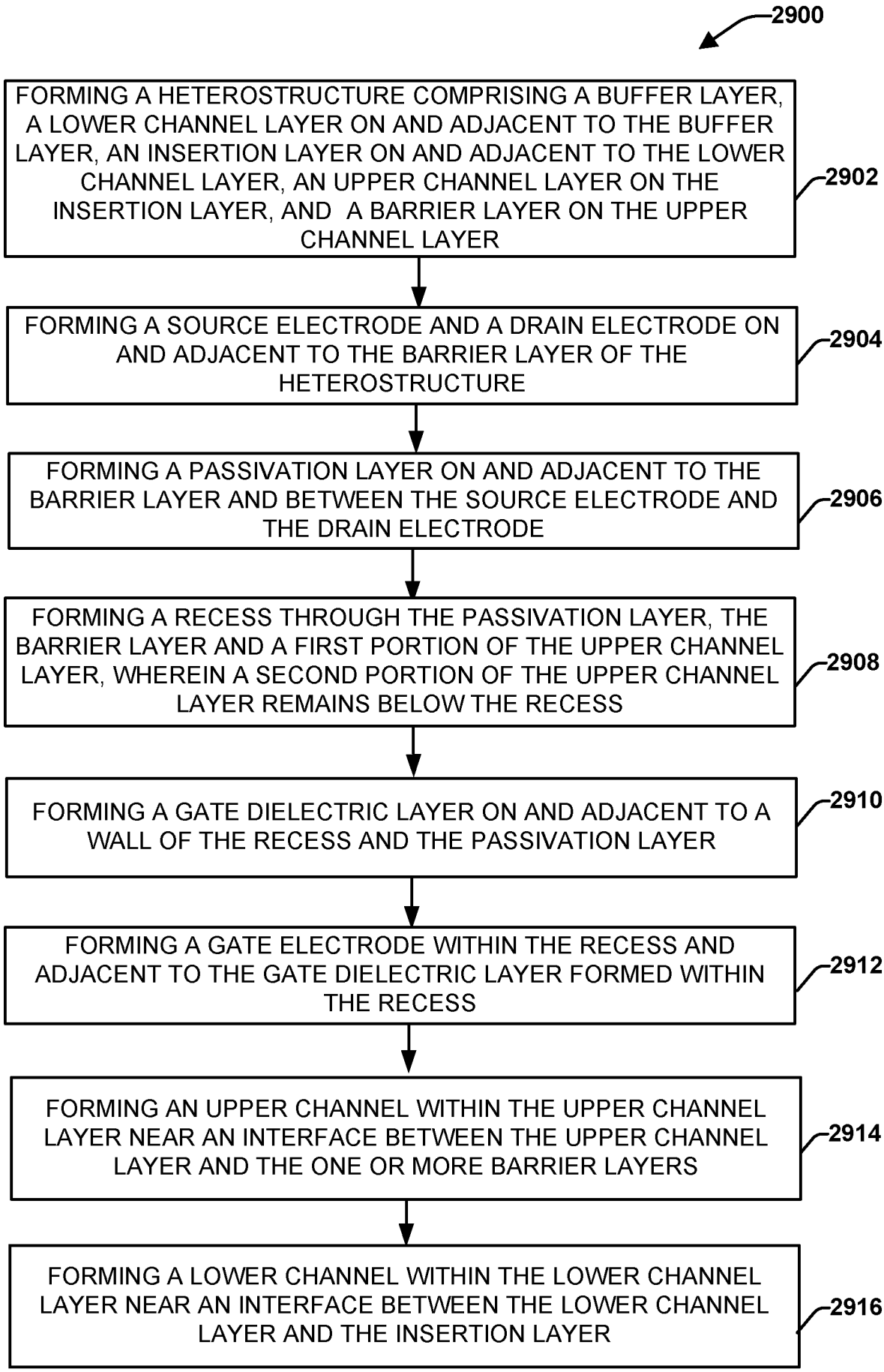

2900
FORMING A HETEROSTRUCTURE COMPRISING A BUFFER LAYER, A LOWER CHANNEL LAYER ON AND ADJACENT TO THE BUFFER LAYER, AN INSERTION LAYER ON AND ADJACENT TO THE LOWER CHANNEL LAYER, AN UPPER CHANNEL LAYER ON THE INSERTION LAYER, AND A BARRIER LAYER ON THE UPPER CHANNEL LAYER
2902
FORMING A SOURCE ELECTRODE AND A DRAIN ELECTRODE ON AND ADJACENT TO THE BARRIER LAYER OF THE HETEROSTRUCTURE
2904
FORMING A PASSIVATION LAYER ON AND ADJACENT TO THE BARRIER LAYER AND BETWEEN THE SOURCE ELECTRODE AND THE DRAIN ELECTRODE
2906
FORMING A RECESS THROUGH THE PASSIVATION LAYER, THE BARRIER LAYER AND A FIRST PORTION OF THE UPPER CHANNEL LAYER, WHEREIN A SECOND PORTION OF THE UPPER CHANNEL LAYER REMAINS BELOW THE RECESS
2908
FORMING A GATE DIELECTRIC LAYER ON AND ADJACENT TO A WALL OF THE RECESS AND THE PASSIVATION LAYER
2910
FORMING A GATE ELECTRODE WITHIN THE RECESS AND ADJACENT TO THE GATE DIELECTRIC LAYER FORMED WITHIN THE RECESS
2912
FORMING AN UPPER CHANNEL WITHIN THE UPPER CHANNEL LAYER NEAR AN INTERFACE BETWEEN THE UPPER CHANNEL LAYER AND THE ONE OR MORE BARRIER LAYERS
2914
FORMING A LOWER CHANNEL WITHIN THE LOWER CHANNEL LAYER NEAR AN INTERFACE BETWEEN THE LOWER CHANNEL LAYER AND THE INSERTION LAYER
2916

FIG. 29

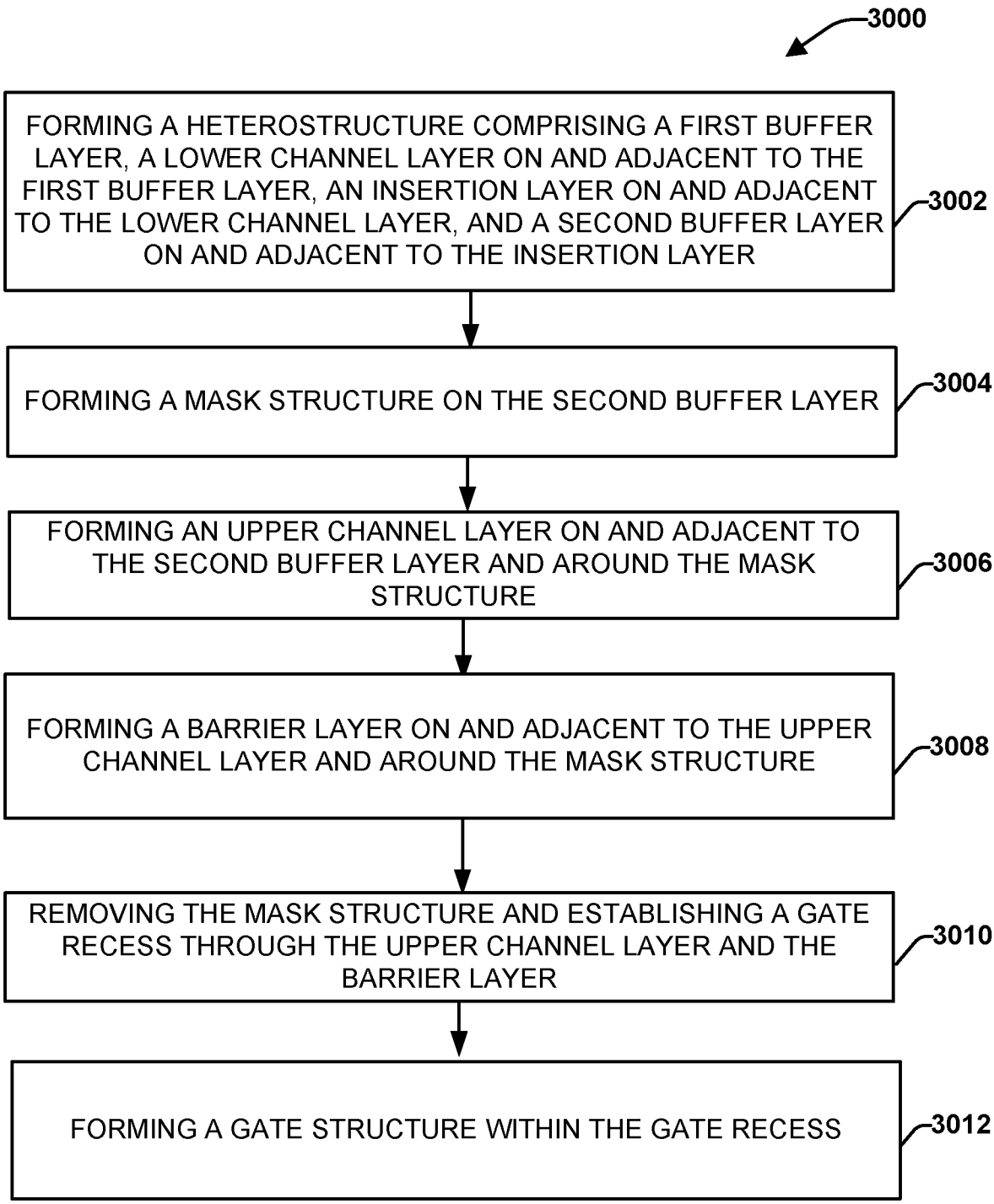

3000
FORMING A HETEROSTRUCTURE COMPRISING A FIRST BUFFER LAYER, A LOWER CHANNEL LAYER ON AND ADJACENT TO THE FIRST BUFFER LAYER, AN INSERTION LAYER ON AND ADJACENT TO THE LOWER CHANNEL LAYER, AND A SECOND BUFFER LAYER ON AND ADJACENT TO THE INSERTION LAYER
3002
FORMING A MASK STRUCTURE ON THE SECOND BUFFER LAYER
3004
FORMING AN UPPER CHANNEL LAYER ON AND ADJACENT TO THE SECOND BUFFER LAYER AND AROUND THE MASK STRUCTURE
3006
FORMING A BARRIER LAYER ON AND ADJACENT TO THE UPPER CHANNEL LAYER AND AROUND THE MASK STRUCTURE
3008
REMOVING THE MASK STRUCTURE AND ESTABLISHING A GATE RECESS THROUGH THE UPPER CHANNEL LAYER AND THE BARRIER LAYER
3010
FORMING A GATE STRUCTURE WITHIN THE GATE RECESS
3012

FIG. 30

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2016/088062

A. CLASSIFICATION OF SUBJECT MATTER

H01L 29/778(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNKI,CNPAT,WPI,EPODOC,GOOGLE,ISI WEB OF KNOWLEDGE,IEEE: electron, high, channel, HEMT, gate, mobility, double, dual, two, channel, barrier, hongkong

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2009267078 A1 (TRANSPHORM INC.) 29 October 2009 (2009-10-29) description paragraphs [0034]-[0066], figures 2, 4-6, 8A-9	1-34
A	US 2014091309 A1 (CREE, INC.) 03 April 2014 (2014-04-03) the whole document	1-34
A	CN 101969071 A (THE HONG KONG UNIVERSITY OF SCIENCE AND TECHNOLOGY) 09 February 2011 (2011-02-09) the whole document	1-34

☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
16 August 2016	**01 September 2016**

Name and mailing address of the ISA/CN	Authorized officer
STATE INTELLECTUAL PROPERTY OFFICE OF THE P.R.CHINA **6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing 100088, China**	**XIONG,Jinan**
Facsimile No. **(86-10)62019451**	Telephone No. **(86-10)62413381**

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2016/088062

Patent document cited in search report	Publication date (day/month/year)	Patent family member(s)	Publication date (day/month/year)
US 2009267078 A1	29 October 2009	US 2016071951 A1	10 March 2016
		US 2014361309 A1	11 December 2014
		TW 201010076 A	01 March 2010
		CN 102017160 A	13 April 2011
		US 2013316502 A1	28 November 2013
		WO 2009132039 A2	29 October 2009
US 2014091309 A1	03 April 2014	WO 2014055314 A2	10 April 2014
CN 101969071 A	09 February 2011	US 2011018002 A1	27 January 2011
		TW 201110345 A	16 March 2011