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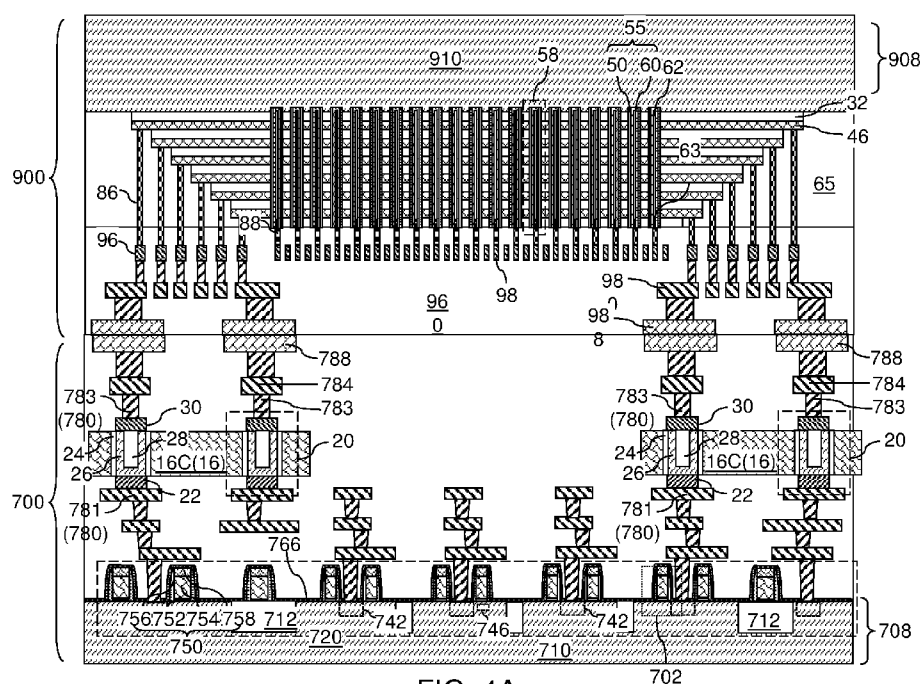


FIG. 4A

(57) Abstract: A semiconductor structure includes at least one set of vertical field effect transistors embedded within dielectric material layers overlying a substrate. Each vertical field effect transistor includes a bottom doped semiconductor electrode, a vertical transistor channel, a cylindrical gate dielectric, and a top doped semiconductor electrode. A three-dimensional NAND memory array can be provided over the first field effect transistors, and can be electrically connected to the vertical field effect transistors via metal interconnect structures. Alternatively, a three-dimensional NAND memory array can be formed on another substrate, which can be bonded to the substrate via metal-to-metal bonding. The vertical field effect transistors can be employed as switches for bit lines, word lines, or other components of the three-dimensional NAND memory array.



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THREE-DIMENSIONAL MEMORY DEVICE WITH VERTICAL FIELD EFFECT TRANSISTORS AND METHOD OF MAKING THEREOF

RELATED APPLICATIONS

[0001] This application claims the benefit of priority from U.S. Non-Provisional Application No. 17/007,761, filed August 31, 2020; and from U.S. Non-Provisional Application No. 17/007,823, filed August 31, 2020; the entire contents of which is herein incorporated by reference.

FIELD

[0002] The present disclosure relates generally to the field of semiconductor devices, and particular to a three-dimensional memory device containing vertical field effect transistors and methods of manufacturing the same.

BACKGROUND

[0003] Three-dimensional vertical NAND strings having one bit per cell are disclosed in an article by T. Endoh et al., titled “Novel Ultra High Density Memory With A Stacked-Surrounding Gate Transistor (S-SGT) Structured Cell”, IEDM Proc. (2001) 33-36.

SUMMARY

[0004] According to an aspect of the present disclosure, a bonded assembly comprising a memory die and a logic die is provided. The memory die comprises a three-dimensional memory array. The logic die comprises a logic-side substrate and at least one set of vertical field effect transistors. Each vertical field effect transistor within each set of vertical field effect transistors comprises a bottom doped semiconductor electrode, a vertical transistor

channel, a gate dielectric which surrounds the vertical transistor channel, and a top doped semiconductor electrode. Each set of vertical field effect transistors comprises a respective gate electrode that laterally surrounds each of the gate dielectrics within a same set of vertical field effect transistors. At least one set of vertical field effect transistors is electrically connected to electrical nodes of the three-dimensional memory array through sets of metal bonding pads through which the memory die and the logic die are bonded to each other.

[0005] According to another aspect of the present disclosure, a method of forming a method of forming a bonded assembly is provided, which comprises: providing the memory die comprising a three-dimensional memory array and memory-side bonding pads; forming at least one set of vertical field effect transistors over a logic-side substrate, wherein each set of vertical field effect transistor is formed by: forming bottom doped semiconductor electrodes embedded within lower logic-side dielectric material layers over the logic-side substrate, forming a gate electrode including a plurality of vertically-extending openings therethrough, wherein the bottom doped semiconductor electrodes are exposed underneath the vertically-extending openings, forming a combination of a cylindrical gate dielectric and a vertical transistor channel within each of the vertically-extending openings, forming top doped semiconductor electrodes on the vertical transistor channels; and forming logic-side bonding pads embedded in upper logic-side dielectric material layers and electrically connected to a respective one of the top doped semiconductor electrodes over the at least one set of vertical field effect transistors, whereby a logic die is provided; and bonding the memory-side bonding pads with the logic-side bonding pads.

[0006] According to yet another aspect of the present disclosure, a semiconductor structure is provided, which comprises: at least one set of vertical field effect transistors located above, and vertically spaced from, a semiconductor substrate, wherein each vertical

field effect transistor within each set of vertical field effect transistors comprises a bottom doped semiconductor electrode, a vertical transistor channel, a gate dielectric which surrounds the vertical transistor channel, and a top doped semiconductor electrode; and a three-dimensional NAND memory array located over the at least one set of vertical field effect transistors, wherein electrical nodes of the three-dimensional NAND memory array are electrically connected to a respective one of the at least one set of vertical field effect transistors.

[0007] According to still another aspect of the present disclosure, a method of forming a semiconductor structure is provided, which comprises: forming bottom doped semiconductor electrodes over first dielectric material layers that overlie a semiconductor substrate; forming a gate electrode including a plurality of vertically-extending openings over the bottom doped semiconductor electrodes wherein the bottom doped semiconductor electrodes are exposed underneath the vertically-extending openings; forming a combination of a cylindrical gate dielectric and a vertical transistor channel within each of the vertically-extending openings; forming top doped semiconductor electrodes on the vertical transistor channels; forming second dielectric material layers over the top doped semiconductor electrodes; and forming a three-dimensional NAND memory array over the second dielectric material layers, wherein electrical nodes of the three-dimensional NAND memory array are electrically connected to a respective one of the top doped semiconductor electrodes.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] FIG. 1A is a plan view of an exemplary memory die according to a first embodiment of the present disclosure.

[0009] FIG. 1B is a plan view of an exemplary logic die according to the first

embodiment of the present disclosure.

[0010] FIG. 2A is a horizontal cross-sectional view of a region of the exemplary memory die of FIG. 1A according to the first embodiment of the present disclosure.

[0011] FIG. 2B is a vertical cross-sectional view along the hinged vertical plane B – B' of the region of the exemplary structure of FIG. 2A. The horizontal plane A – A' is the plane of the horizontal cross-sectional view of FIG. 2A.

[0012] FIG. 2C is a vertical cross-sectional view along the hinged vertical plane C – C' of the region of the exemplary structure of FIG. 2A. The horizontal plane A – A' is the plane of the horizontal cross-sectional view of FIG. 2A.

[0013] FIG. 2D is a vertical cross-sectional view along the hinged vertical plane D – D' of the region of the exemplary structure of FIG. 2A. The horizontal plane A – A' is the plane of the horizontal cross-sectional view of FIG. 2A. The vertical plane B – B' is the plane of the horizontal cross-sectional view of FIG. 2B. The vertical plane C – C' is the plane of the horizontal cross-sectional view of FIG. 2C.

[0014] FIG. 3A is a first vertical cross-sectional view of a region of the exemplary logic die of FIG. 1B according to the first embodiment of the present disclosure.

[0015] FIG. 3B is a second vertical cross-sectional view of a region of the exemplary logic die of FIG. 1B.

[0016] FIG. 3C is a first exemplary layout of the region C in FIG. 3A.

[0017] FIG. 3D is a second exemplary layout of the region C in FIG. 3A.

[0018] FIG. 3E is an exemplary layout of vertical field effect transistors and logic-side bonding pads within the exemplary memory die of FIGS. 2A and 2B.

[0019] FIG. 4A is a first vertical cross-sectional view of an exemplary bonded assembly is along a vertical plane that corresponds the vertical planes of FIG. 2B and FIG. 3A according

to the first embodiment of the present disclosure.

[0020] FIG. 4B is a second vertical cross-sectional view of the exemplary bonded assembly along a vertical plane that corresponds to the hinged vertical planes of FIG. 2C and FIG. 3B according to the first embodiment of the present disclosure.

[0021] FIG. 5 is a vertical cross-sectional view of an alternative embodiment of the exemplary bonded assembly according to the first embodiment of the present disclosure.

[0022] FIGS. 6A – 6J are sequential vertical cross-sectional views of a region of the exemplary logic die during formation of a set of vertical field effect transistors according to an embodiment of the present disclosure.

[0023] FIGS. 6K – 6N are vertical cross-sectional views of alternative configurations of a region of the exemplary logic die according to embodiments of the present disclosure.

[0024] FIG. 7A is a first vertical cross-sectional view of an exemplary semiconductor die after formation of lower-level dielectric material layers embedding lower-level metal interconnect structures according to a second embodiment of the present disclosure.

[0025] FIG. 7B is a second vertical cross-sectional view of the exemplary semiconductor die of FIG. 7A.

[0026] FIG. 8A is a first vertical cross-sectional view of the exemplary semiconductor die after formation of alternating stacks of insulating layers and electrically conductive layers and memory opening fill structures according to a second embodiment of the present disclosure.

[0027] FIG. 8B is a second vertical cross-sectional view of the exemplary semiconductor die of FIG. 8A.

[0028] FIG. 9A is a first vertical cross-sectional view of the exemplary semiconductor die after formation of upper-level dielectric material layers embedding upper-level metal interconnect structures according to a second embodiment of the present disclosure.

[0029] FIG. 9B is a second vertical cross-sectional view of the exemplary semiconductor die of FIG. 9A.

[0030] FIG. 10 is a vertical cross-sectional view of an alternative embodiment of the exemplary semiconductor structure according to the second embodiment of the present disclosure.

[0031] FIG. 11A is a first vertical cross-sectional view of a first portion of the exemplary memory die after formation of an alternating stack of insulating layers and sacrificial material layers and dielectric material portions according to an embodiment of the present disclosure.

[0032] FIG. 11B is a second vertical cross-sectional view of a second portion of the exemplary memory die at the processing step of FIG. 11A.

[0033] FIG. 12A is a first vertical cross-sectional view of a first portion of the exemplary memory die after formation of memory opening fill structures according to an embodiment of the present disclosure.

[0034] FIG. 12B is a second vertical cross-sectional view of a second portion of the exemplary memory die at the processing step of FIG. 12A.

[0035] FIG. 13A is a first vertical cross-sectional view of a first portion of the exemplary memory die after formation of backside trenches according to an embodiment of the present disclosure.

[0036] FIG. 13B is a second vertical cross-sectional view of a second portion of the exemplary memory die at the processing step of FIG. 13A.

[0037] FIG. 14A is a first vertical cross-sectional view of a first portion of the exemplary memory die after formation of backside recesses according to an embodiment of the present disclosure.

[0038] FIG. 14B is a second vertical cross-sectional view of a second portion of the

exemplary memory die at the processing step of FIG. 14A.

[0039] FIG. 15A is a first vertical cross-sectional view of a first portion of the exemplary memory die after formation of electrically conductive layers according to an embodiment of the present disclosure.

[0040] FIG. 15B is a second vertical cross-sectional view of a second portion of the exemplary memory die at the processing step of FIG. 15A.

[0041] FIG. 16A is a first vertical cross-sectional view of a first portion of the exemplary memory die after formation of contact via structures according to an embodiment of the present disclosure.

[0042] FIG. 16B is a second vertical cross-sectional view of a second portion of the exemplary memory die at the processing step of FIG. 16A.

DETAILED DESCRIPTION

[0043] As discussed above, the present disclosure is directed to a three-dimensional memory device containing a logic (e.g., driver) circuit containing vertical field effect transistors and methods of manufacturing the same, the various aspects of which are described below. The vertical field effect transistors occupy less space over the substrate than lateral (i.e., horizontal) field effect transistor. This provides a more compact logic circuit. The embodiments of the disclosure can be employed to form various structures including a multilevel memory structure, non-limiting examples of which include semiconductor devices such as three-dimensional monolithic memory array devices comprising a plurality of NAND memory strings.

[0044] The drawings are not drawn to scale. Wherever physical contact between two elements is illustrated in the drawings, direct physical contact between the two elements is

provided. Multiple instances of an element may be duplicated where a single instance of the element is illustrated, unless absence of duplication of elements is expressly described or clearly indicated otherwise. Ordinals such as “first,” “second,” and “third” are employed merely to identify similar elements, and different ordinals may be employed across the specification and the claims of the instant disclosure. The same reference numerals refer to the same element or similar element. Unless otherwise indicated, elements having the same reference numerals are presumed to have the same composition. As used herein, a first element located “on” a second element can be located on the exterior side of a surface of the second element or on the interior side of the second element. As used herein, a first element is located “directly on” a second element if there exist a physical contact between a surface of the first element and a surface of the second element.

[0045] As used herein, a “semiconducting material” refers to a material having electrical conductivity in the range from 1.0×10^{-6} S/cm to 1.0×10^5 S/cm. As used herein, a “semiconductor material” refers to a material having electrical conductivity in the range from 1.0×10^{-6} S/cm to 1.0×10^5 S/cm in the absence of electrical dopants therein, and is capable of producing a doped material having electrical conductivity in a range from 1.0 S/cm to 1.0×10^5 S/cm upon suitable doping with an electrical dopant. As used herein, an “electrical dopant” refers to a p-type dopant that adds a hole to a valence band within a band structure, or an n-type dopant that adds an electron to a conduction band within a band structure. As used herein, a “conductive material” refers to a material having electrical conductivity greater than 1.0×10^5 S/cm. As used herein, an “insulator material” or a “dielectric material” refers to a material having electrical conductivity less than 1.0×10^{-6} S/cm. As used herein, a “heavily doped semiconductor material” refers to a semiconductor material that is doped with electrical dopant at a sufficiently high atomic concentration to become a conductive material,

i.e., to have electrical conductivity greater than 1.0×10^5 S/cm. A “doped semiconductor material” may be a heavily doped semiconductor material, or may be a semiconductor material that includes electrical dopants (i.e., p-type dopants and/or n-type dopants) at a concentration that provides electrical conductivity in the range from 1.0×10^{-6} S/cm to 1.0×10^5 S/cm. An “intrinsic semiconductor material” refers to a semiconductor material that is not doped with electrical dopants. Thus, a semiconductor material may be semiconducting or conductive, and may be an intrinsic semiconductor material or a doped semiconductor material. A doped semiconductor material can be semiconducting or conductive depending on the atomic concentration of electrical dopants therein. As used herein, a “metallic material” refers to a conductive material including at least one metallic element therein. All measurements for electrical conductivities are made at the standard condition.

[0046] As used herein, a “layer” refers to a material portion including a region having a thickness. A layer may extend over the entirety of an underlying or overlying structure, or may have an extent less than the extent of an underlying or overlying structure. Further, a layer may be a region of a homogeneous or inhomogeneous continuous structure that has a thickness less than the thickness of the continuous structure. For example, a layer may be located between any pair of horizontal planes between, or at, a top surface and a bottom surface of the continuous structure. A layer may extend horizontally, vertically, and/or along a tapered surface. A substrate may be a layer, may include one or more layers therein, or may have one or more layer thereupon, thereabove, and/or therebelow. As used herein, a first element is electrically connected to a second element if there exists an electrically conductive path between the first element and the second element.

[0047] A monolithic three-dimensional memory array is one in which multiple memory levels are formed above a single substrate, such as a semiconductor wafer, with no

intervening substrates. The term “monolithic” means that layers of each level of the array are directly deposited on the layers of each underlying level of the array. In contrast, two dimensional arrays may be formed separately and then packaged together to form a non-monolithic memory device. For example, non-monolithic stacked memories have been constructed by forming memory levels on separate substrates and vertically stacking the memory levels, as described in U.S. Patent No. 5,915,167 titled “Three-dimensional Structure Memory.” The substrates may be thinned or removed from the memory levels before bonding, but as the memory levels are initially formed over separate substrates, such memories are not true monolithic three-dimensional memory arrays. The various three-dimensional memory devices of the present disclosure include a monolithic three-dimensional NAND string memory device, and can be fabricated employing the various embodiments described herein.

[0048] Generally, a semiconductor die, or a semiconductor package, can include be a single memory chip. Each semiconductor package contains one or more dies (for example one, two, or four). The die is the smallest unit that can independently execute commands or report status. Each die contains one or more planes (typically between 1 and 8). Identical, concurrent operations can take place on each plane, although with some restrictions. Each plane contains a number of blocks (i.e., memory blocks), which are the smallest unit that can be erased by in a single erase operation. Each block contains a number of pages, which are the smallest unit that can be programmed, i.e., a smallest unit on which a read operation can be performed.

[0049] Referring to FIG. 1A, a plan view of an exemplary memory die 900 according to a first embodiment of the present disclosure is illustrated. The memory die 900 includes at least one memory plane, such as two to four planes (P0 – P3), each of which can concurrently

execute identical operations. Multiple alternating stacks of insulating layers and electrically conductive layers can be provided within each plane (P0 – P3). Each plane (P0 – P3) can include a three-dimensional memory array that includes a respective three-dimensional array of memory elements. Each alternating stack can laterally extend along a first horizontal direction (e.g., word line direction) hd1, and can be laterally spaced apart along a second horizontal direction (e.g., bit line direction) hd2. Each plane (P0 – P3) can include a respective memory array region 100 and at least one staircase region 200 in which stepped surfaces of alternating stacks of insulating layers and electrically conductive layers are provided to enable formation of layer contact via structures. The memory array region 100 of each plane (P0 – P3) includes memory openings and memory opening fill structures. Each memory opening fill structure can include a memory stack structure, which contains a vertical semiconductor channel and a vertical stack of memory elements. A three-dimensional array of memory elements is provided within portions of the memory stack structure located within a memory array region. The electrically conductive layers of each alternating stack functions as word lines for the vertical stack of memory elements.

[0050] Electrical contacts to the electrically conductive layers (e.g., word lines and select lines) are provided with memory-side word-line hookup regions 222, which overlaps with the staircase regions in which the alternating stacks have stepped surfaces. The memory-side word-line hookup regions 222 can include memory-side bonding pads that are electrically connected to the electrically conductive layers. A bottom end of each vertical semiconductor channel can be adjoined to a horizontal semiconductor channel or a source region located within a semiconductor (e.g., silicon) material layer, which may be a memory-die substrate semiconductor layer. A top end of each vertical semiconductor channel is adjoined to a drain region, which can be located at a topmost portion of a respective memory opening fill

structure. Bit lines laterally extending along the second horizontal direction hd2 can be provided over the drain regions, and can be electrically connected to a respective subset of the drain regions via drain contact via structures. Connection between the bit line and overlying metal interconnect structures can be formed in memory-side bit-line hookup regions 111, which can laterally extend along the first horizontal direction hd1 and can be located between alternating stacks of insulating layers and electrically conductive layers. The memory-side bit-line hookup regions 111 can include memory-side bonding pads that are electrically connected to the bit lines. While two memory-side bit-line hookup regions 111 are illustrated in FIG. 1A, the number of the bit-line hookup regions may be increased as needed.

[0051] Referring to FIG. 1B, a plan view of an exemplary logic die 700 according to the first embodiment of the present disclosure is illustrated. The logic die 700 can have the same size as the memory die 900 illustrated in FIG. 1A, and can be divided into a same number of plane logic regions (which is also referred to as “planes” for brevity) (Q0 – Q3) as the number of planes (P0 – P3) in the memory die 900. Generally, the layout of each plane (Q0 – Q3) can be similar to a mirror image of the layout of the memory die 900 to minimize electrical routing distances for the metal interconnect structures employed within the logic die 700. The logic die 700 includes logic (i.e., driver / peripheral) circuits that can be employed to control operation of the three-dimensional array of memory elements within the memory die 900. Each plane (Q0 – Q3) can include logic-side word-line hookup regions 722 and logic-side bit-line hookup regions 711. The logic-side word-line hookup regions 722 includes word line driver circuits and logic-side bonding pads electrically connected to the word line driver circuits. The logic-side bit-line hookup regions 711 includes sense amplifiers and bit line bias circuits (i.e., bit line drivers) and logic-side bonding pads

electrically connected to the sense amplifiers and the bit line bias circuits. The areas of the logic die that are not occupied by the logic-side word-line hookup regions 722 or the logic-side bit-line hookup regions 711 can be occupied by additional circuits of a peripheral circuitry that are needed for operation of the memory die 900. For example, such areas can be occupied by bit line decoders, word line decoders, power supply circuits, data buffers, input/output circuits, etc.

[0052] Referring to FIGS. 2A – 2D, structural elements within the memory die 900 of FIG. 1A are illustrated in various views. The memory die 900 can include a memory-side substrate 908 that includes a memory-side substrate semiconductor layer 910, which is a semiconductor material layer. The memory-side substrate 908 may include a commercially available single crystalline semiconductor substrate such as a single crystalline silicon wafer. The memory-side substrate semiconductor layer 910 can be an epitaxial silicon layer or a doped well in the silicon wafer and have a doping of a first conductivity type at an atomic concentration in a range from $1.0 \times 10^{14}/\text{cm}^3$ to $1.0 \times 10^{18}/\text{cm}^3$, although lesser and greater atomic concentrations may also be employed.

[0053] At least one alternating stack of insulating layers 32 and spacer material layers can be formed over the memory-side substrate 908. The spacer material layers are formed are, or are subsequently replaced with, electrically conductive layers 46, which function as word lines and select gate electrodes. Each alternating stack (32, 46) can be patterned to form stepped surfaces. The area including the stepped surfaces constitute the staircase region 200. Dielectric material portions 65 can be formed over the stepped surfaces. Further, additional dielectric material portions 65 can be formed between alternating stacks (32, 46) that are laterally spaced apart. Memory openings are formed through the portions of the alternating stack in which each layer of the alternating stack is present, i.e., within a memory array

region 100. Memory opening fill structures 58 are formed within the memory openings. Each of the memory opening fill structures comprises a respective set of a memory film 50, a vertical semiconductor channel 60, and a drain region 63, and optionally includes a dielectric core 62. Each contiguous combination of a vertical semiconductor channel 60 and a memory film 50 constitutes a memory stack structure 55. Each memory film 50 includes a vertical stack of memory elements that are located at levels of the electrically conductive layers 46. In one embodiment, each memory film 50 may include a layer stack including, from outside to inside, a blocking dielectric layer, a charge storage layer or a vertical stack of discrete charge storage material portions (e.g., floating gates or discrete charge storage dielectric portions), and a tunneling dielectric layer. Portions of the charge storage layer located at levels of the electrically conductive layers, or the vertical stack of discrete charge storage material portions constitute a vertical stack of memory elements. The drain regions 63 are formed at a top end portion of a respective one of the vertical semiconductor channels 60.

[0054] In case the spacer material layers are formed as sacrificial material layers, backside trenches laterally extending along the first horizontal direction can be formed through the alternating stacks such that each alternating stack is divided into a respective plurality of alternating stacks by the backside trenches. Source regions 61 can be formed at the bottom of each backside trench, and the sacrificial material layers can be removed selective to the insulating layers 32 and the memory opening fill structures 58. Backside recesses are formed in volumes from which the sacrificial material layers are removed. The electrically conductive layers 46 can be formed by depositing at least one electrically conductive material in the backside recesses and removing excess portions of the electrically conductive material from inside the backside trenches and from above the alternating stacks. Each backside trench can be filled with a respective backside trench fill structure, which may

include, for example, an insulating spacer 74 and a backside contact via structure 76 that can function as a source contact via structure.

[0055] The memory die 900 comprises a three-dimensional memory array including a three-dimensional array of memory elements that includes portions of the memory films 50 that are located adjacent to a respective one of vertical semiconductor channels 60. The electrically conductive layers 46 comprise word lines and select gate lines of the three-dimensional memory array. A contact-level dielectric layer can be formed over the alternating stacks (32, 46), and various contact via structures can be formed through the contact-level dielectric layer. For example, layer contact via structures 86 can be formed directly on a surface of a respective one of the electrically conductive layers 46, and drain contact via structures 88 can be formed directly on a top surface of a respective one of the drain regions 63. Bit lines 98 can be formed over the memory opening fill structures 58. Each of the bit lines 98 can be electrically connected to a respective subset of the drain regions 63 through a respective set of drain contact via structures 88. Word-line-connection metal lines 96 can be formed on a respective one of the layer contact via structures 86. Memory-side metal interconnect structures 980 embedded within memory-side dielectric material layers 960 can be formed. The memory-side dielectric material layers 960 include the contact-level dielectric layer. Memory-side bonding pads 988 can be formed within a top portion of the memory-side dielectric material layers 960. Thus, the memory die 900 comprising a three-dimensional memory array and memory-side bonding pads 988 can be provided.

[0056] Referring to FIGS. 3A – 3E, structural elements within the logic die 700 of FIG. 1B are illustrated in various views. The logic die 700 can include a logic-side substrate 708 that includes a logic-side substrate semiconductor layer 710, which is a semiconductor

material layer (e.g., an epitaxial layer or a doped well in the substrate 708). The logic-side substrate 708 may include a commercially available single crystalline semiconductor substrate, such as a single crystalline silicon wafer. Field effect transistors 702 can be formed on the logic-side substrate semiconductor layer 710. The field effect transistors include a respective semiconductor channel comprising a portion of, or comprising a same material as, the logic-side substrate semiconductor layer 710 in the logic-side substrate. Thus, the field effect transistors are herein referred to as substrate field effect transistors 702. The substrate field effect transistors 702 may comprise conventional planar (i.e., lateral / horizontal) field effect transistors, fin field effect transistors, or gate-all-around field effect transistors, which may be arranged in a CMOS configuration. Generally, the substrate field effect transistors 702 can comprise active regions 742 (such as source regions and drain regions), semiconductor channels 746 (which extend parallel to the top surface of the substrate 708), and a gate structures 750. Each gate structure 750 may include a gate dielectric 752, a gate electrode 754, a gate cap dielectric 758, and an optional gate spacer 756. Shallow trench isolation structures 712 may be formed in an upper portion of the logic-side substrate semiconductor layer 710 to provide electrical isolation among the substrate field effect transistors. A dielectric liner 766 (such as a silicon nitride liner) may be formed over the substrate field effect transistors to block diffusion of impurities and hydrogen, and/or to provide stress effects to the substrate field effect transistors.

[0057] The substrate field effect transistors collectively form a peripheral circuit 720, which is a logic circuit that is configured to control operation of the three-dimensional memory array within the memory die 900. The peripheral circuit 720 includes sense amplifier circuits and bit line bias circuits. A first subset of the logic-side metal interconnect structures 780, which is herein referred to as lower logic-side metal interconnect structures

780A, can be formed over the substrate field effect transistors. The lower logic-side metal interconnect structures 780 can be embedded in a first subset of logic-side dielectric material layers 760, which is herein referred to as first dielectric material layers. The lower logic-side metal interconnect structures comprise metallic bottom pads 781, which can be arranged within areas of vertical field effect transistors to be subsequently formed. In one embodiment, the metallic bottom pads 781 may be formed within the areas of the sense amplifier circuits and the bit line bias circuits, and/or outside the areas of the amplifier circuits and the bit line bias circuits.

[0058] At least one set of vertical field effect transistors 20 can be formed over the logic-side substrate 708. Each set of vertical field effect transistors 20 shares a common gate electrode 16. Each set of vertical field effect transistor 20 can be formed by forming bottom electrodes 22 (e.g., heavily doped semiconductor electrodes) embedded within the lower logic-side dielectric material layers over the logic-side substrate 708, forming a gate electrode 16 including a plurality of vertically-extending openings therethrough such that the bottom doped semiconductor electrodes 22 are exposed underneath the vertically-extending openings, forming a combination of a cylindrical gate dielectric 24 and a vertical transistor channel 26 within each of the vertically-extending openings, and forming top electrodes 30 (e.g., heavily doped semiconductor electrodes) on the vertical transistor channels 26. The bottom and top electrodes (22, 30) that contact the vertical transistor channels 26 function as source and drain regions over the vertical field effect transistors 20. Optionally, a dielectric channel core 28 can be formed within each vertical transistor channel 26. The method of forming the least one set of vertical field effect transistors 20 are described in detail in a subsequent section. In one embodiment, the vertical transistor channels 26 comprises, and/or consist essentially of, a respective elemental semiconductor material (e.g., polysilicon) or a

respective III-V compound semiconductor material. In one embodiment, each gate electrode 16 of each set of vertical field effect transistors 20 comprises a respective elemental semiconductor material (e.g., heavily doped polysilicon) or a respective III-V compound semiconductor material. The vertical field effect transistors 20 may comprise vertical thin film transistors.

[0059] The bottom doped semiconductor electrodes 22 of the at least one set of vertical field effect transistors 20 can be electrically connected to a first subset of the substrate field effect transistors via a first subset of lower logic-side metal interconnect structures 780A embedded within the lower logic-side dielectric material layers 760. A second subset of the logic-side metal interconnect structures 780 can be subsequently formed over the vertical field effect transistors 20. The second subset of the logic-side metal interconnect structures 780 are herein referred to as second metal interconnect structures, and are embedded in a second subset of the logic-side dielectric material layers 760. The second subset of the logic-side metal interconnect structures 780 may include upper electrode contact via structures 783 each contacting a respective one of the top doped semiconductor electrodes 30, and upper-electrode-connection metal lines 784 each contacting at least one of the upper electrode contact via structures 783, and thus, is electrically connected to at least one of the top doped semiconductor electrodes 30. The second subset of the logic-side metal interconnect structures 780 may include gate contact via structures 785 each contacting a respective one of the gate electrodes 16, and gate-connection metal lines 786 each contacting a top surface of a respective gate contact via structure 785 and located at the same level as the upper-electrode-connection metal lines 784. Logic-side bonding pads 788 can be formed in a top portion of the logic-side dielectric material layers 760. The logic-side bonding pad 788 can be electrically connected to the substrate field effect transistors and/or to the upper-electrode-

connection metal lines 784 through a respective subset of the logic-side metal interconnect structures 780.

[0060] In one embodiment, the at least one set of vertical field effect transistors 20 can comprise a plurality of sets of vertical field effect transistors 20. In one embodiment, the at least one set of vertical field effect transistors 20 can comprise a first set of vertical field effect transistors 20A including a respective bottom doped semiconductor electrode 22 that is electrically connected to a respective one of the sense amplifier circuits and sharing a first gate electrode 16A (as illustrated in FIG. 3C or 3D), and a second set of vertical field effect transistors 20B including a respective bottom doped semiconductor electrode 22 that is electrically connected to a respective one of the bit line bias circuits and sharing a second gate electrode 16B that is located adjacent to, and laterally spaced from, the first gate electrode 16A. The upper-electrode-connection metal lines 784 can be electrically connected to a respective set of a top doped semiconductor electrode 30 within the first set of vertical field effect transistors 20 and a top doped semiconductor electrode 30 within the second set of vertical field effect transistors. Further, the upper-electrode-connection metal lines 784 can be subsequently connected to a respective one of the bit lines in the three-dimensional memory array in the memory die 900. During operation, the first set of vertical field effect transistors 20 can be turned on and the second set of vertical field effect transistors 20 can be turned off to electrically connect the upper-electrode-connection metal lines 784 to the sense amplifier circuits (e.g., during a read operation on the three-dimensional memory array), or the first set of vertical field effect transistors 20 can be turned off and the second set of vertical field effect transistors 20 can be turned on to electrically connect the upper-electrode-connection metal lines 784 to the bit line bias circuits e.g., during an erase operation on the three-dimensional memory array). Thus, the combination of the first set of vertical field

effect transistors 20 and the second set of vertical field effect transistors 20 can function as an electrical switch for the bit lines of the three-dimensional memory array.

[0061] In one embodiment, the at least one set of vertical field effect transistors 20 can comprise at least one set of vertical field effect transistors 20C (as illustrated in FIG. 3E) including a respective bottom doped semiconductor electrode 22 that is electrically connected to a respective output node of a word line driver provided within the peripheral circuit 720. The upper-electrode-connection metal lines 784 can be electrically connected to a respective top doped semiconductor electrode 30 and multiple electrically conductive layers (e.g., word lines) located in different alternating stacks (32, 46) and at a same vertical spacing from the memory-side substrate 908. During operation, each set of vertical field effect transistors 20 can be turned on or turned off.

[0062] Generally, upper logic-side metal interconnect structures 780B embedded within the upper logic-side dielectric material layers can be formed over the at least one set of vertical field effect transistors 20. The upper logic-side metal interconnect structures 780B electrically connect the upper doped semiconductor electrodes 30 of the at least one set of vertical field effect transistors 20 to the logic-side bonding pads 788. The logic-side bonding pads 788 are embedded in the upper logic-side dielectric material layers 760, and are electrically connected to a respective one of the top doped semiconductor electrodes 30 over the at least one set of vertical field effect transistors 20. The pattern of the logic-side bonding pads 788 may overlap with the pattern of the underlying vertical field effect transistors 20 (as illustrated in FIG. 3E). The total number of a set of vertical field effect transistors 20 sharing a same gate electrode 16 and employed to drive the bit lines 98 may be the same as a total number N of the bit lines 98, or a fraction of the total number N of the bit lines 98. The total number of a set of vertical field effect transistors 20 sharing a same gate electrode 16 and

employed to drive the word lines may be the same as a total number M of the word lines (as embodied as the electrically conductive layers 46), or a fraction of the total number M of the word lines.

[0063] Referring to FIGS. 4A and 4B, the memory die 900 and the logic die 700 can be bonded to each other, for example, by metal-to-metal bonding or by hybrid bonding. Each memory-side bonding pad 988 can be bonded to a respective one of the logic-side bonding pads 788. In one embodiment, a subset of the top doped semiconductor electrodes 30 of the at least one set of vertical field effect transistors 20 can be electrically connected to a respective one of the bit lines 98. Additionally or alternatively, another subset of the top doped semiconductor electrodes 30 of the at least one set of vertical field effect transistors 20 can be electrically connected to a respective one of the word lines (i.e., the electrically conductive layers 46) via mating pairs of the memory-side bonding pads 988 and the logic-side bonding pads 788.

[0064] Referring to FIG. 5, an alternative embodiment of the first exemplary structure is illustrated, which can be derived from the first exemplary structure by rearranging the layout of the substrate field effect transistors 702 such that the areas of the vertical field effect transistors 20 is laterally offset, at least partially, from the area of the sense amplifier circuits and the bit line bias circuits. Generally, the percentage overlap between the total area of the at least one set of vertical field effect transistors 20 and the total area including each sense amplifier circuit and each bit line bias circuit may be from 0 % to 100 % of the lesser of the total area of the at least one set of vertical field effect transistors 20 and the total area including each sense amplifier circuit and each bit line bias circuit.

[0065] FIGS. 6A – 6J are sequential vertical cross-sectional views of a region of the exemplary logic die 700 during formation of a set of vertical field effect transistors 20

according to an embodiment of the present disclosure.

[0066] Referring to FIG. 6A, a region of the logic die 700 for forming a set of vertical field effect transistors 20 is illustrated after formation of the metallic bottom pads 781. The metallic bottom pads 781 are a subset of the lower logic-side metal interconnect structures 780A, and can be embedded within a line-level dielectric material layer 761, which is a subset of the lower logic-side dielectric material layers of the logic die 700. The line-level dielectric material layer 761 includes a dielectric material such as undoped silicate glass, a doped silicate glass, or organosilicate glass. The thickness of the metallic bottom pads 781 may be in a range from 50 nm to 200 nm, although lesser and greater thicknesses may also be employed. The metallic bottom pads 781 may include Cu, W, Ru, Co, Mo, TiN, TaN, WN, or any metallic material that can be employed for interconnect-level metal structures. The lateral dimensions (such as a diameter) of the metallic bottom pads 781 may be in a range from 300 nm to 1,000 nm, although lesser and greater lateral dimensions may also be employed.

[0067] Referring to FIG. 6B, a bottom-pad-level dielectric material layer 762 can be formed over the metallic bottom pads 781. The bottom-pad-level dielectric material layer 762 includes a dielectric material such as undoped silicate glass, a doped silicate glass, or organosilicate glass. The thickness of the bottom-pad-level dielectric material layer 762 may be in a range from 50 nm to 200 nm, although lesser and greater thicknesses may also be employed. Pad cavities are formed within the bottom-pad-level dielectric material layer 762 over each of the metallic bottom pads 781. A doped semiconductor material can be deposited in the pad cavities directly on physically exposed surfaces of the metallic bottom pads 781. The doped semiconductor material may include a respective doped elemental semiconductor material (such as silicon (e.g., polysilicon), germanium, or a silicon-germanium alloy) or a

respective III-V compound semiconductor material (such as GaAs). The doped semiconductor material can include electrical dopants (which may be p-type dopants or n-type dopants) at an atomic concentration in a range from $5.0 \times 10^{18}/\text{cm}^3$ to $2.0 \times 10^{21}/\text{cm}^3$, although lesser and greater atomic concentrations may also be employed. Excess portions of the doped semiconductor material can be removed from above the horizontal plane including the top surface of the bottom-pad-level dielectric material layer 762. Remaining portions of the doped semiconductor material comprise bottom doped semiconductor electrodes 22.

[0068] Referring to FIG. 6C, a gate-level dielectric material layer 763 can be deposited over the bottom-pad-level dielectric material layer 762. The gate-level dielectric material layer 763 includes a dielectric material such as undoped silicate glass, a doped silicate glass, or organosilicate glass. The thickness of the gate-level dielectric material layer 763 may be in a range from 300 nm to 2,000 nm, such as from 500 nm to 1,000 nm, although lesser and greater thicknesses may also be employed. A photoresist layer (not shown) can be applied over the gate-level dielectric material layer 763, and can be lithographically patterned to form openings therein. Each opening in the photoresist layer may overlie a set of bottom doped semiconductor electrodes 22 that are employed to form a set of vertical field effect transistors 20 that are controlled by a same gate electrode. An anisotropic etch process can be performed to form a recess cavity, which is herein referred to as a gate cavity 15, within each opening in the photoresist layer. An array of bottom doped semiconductor electrodes 22 can be physically exposed at the bottom of each gate cavity 15. The photoresist layer can be subsequently removed, for example, by ashing.

[0069] Referring to FIG. 6D, a gate electrode material can be deposited in the gate cavities 15. The gate electrode material can include a doped semiconductor material (such as heavily doped polysilicon) or a metallic material (such as TiN, TaN, WN, W, or any of metal

gate materials known in the art). The gate electrode material may be deposited as a blanket conductive material layer, i.e., an unpatterned conductive material layer. Excess portions of the gate electrode material can be removed from outside the gate cavities 15, i.e., from above the horizontal plane including the top surface of the gate-level dielectric material layer 763, by a planarization process such as a chemical mechanical planarization process. Each remaining portion of the gate electrode material that fills a gate cavity 15 comprises a gate electrode 16. In one embodiment, each gate electrode 16 comprises a respective elemental semiconductor material or a respective III-V compound semiconductor material.

[0070] Referring to FIG. 6E, a photoresist layer (not shown) can be applied over the gate-level dielectric material layer 763 and the gate electrodes 16, and can be lithographically patterned to form an opening over each area of the bottom doped semiconductor electrodes 22. In one embodiment, the periphery of each opening in the photoresist layer may be laterally offset outward from a periphery of a respective underlying bottom doped semiconductor electrode 22. An anisotropic etch process can be performed to transfer the pattern of the openings in the photoresist layer through each gate electrode 16. The anisotropic etch can be terminated upon physical exposure of the top surfaces of the bottom doped semiconductor electrodes 22. In one embodiment, each bottom doped semiconductor electrode 22 can have a top surface having a periphery that is laterally offset inward from a bottom periphery of an overlying opening through a gate electrode 16. A channel cavity 21 is formed above each bottom doped semiconductor electrode 22. Each channel cavity 21 can have a cylindrical sidewall, which is a sidewall of a gate electrode 16.

[0071] Referring to FIG. 6F, a gate dielectric material such as silicon oxide can be conformally deposited over the gate electrodes 16, the bottom doped semiconductor electrodes 22, and the gate-level dielectric material layer 763. The gate dielectric material

can be subsequently anisotropically etched to remove horizontal portions. Each vertically-extending cylindrical portion of the gate dielectric material that remains in a respective channel cavity 21 constitutes a cylindrical gate dielectric 24. The lateral thickness of each cylindrical gate dielectric 24 can be in a range from 10 nm to 60 nm, such as from 15 nm to 40 nm, although lesser and greater thicknesses may also be employed.

[0072] Referring to FIG. 6G, a channel semiconductor material can be conformally deposited to form a channel semiconductor layer 26L. The channel semiconductor material can include a doped or intrinsic elemental semiconductor material (e.g., intrinsic (i.e., not intentionally doped) polysilicon) or a doped III-V compound semiconductor material. The channel semiconductor material can have a doping of an opposite conductivity type as the doping of the bottom doped semiconductor electrodes 22, thereby forming a first p-n junction at interfaces with the bottom doped semiconductor electrodes 22. The atomic concentration of electrical dopants in the channel semiconductor material may be in a range from $1.0 \times 10^{14}/\text{cm}^3$ to $3.0 \times 10^{18}/\text{cm}^3$, although lesser and greater atomic concentrations may also be employed. The thickness of the channel semiconductor layer 26L can be in a range from 10 nm to 30 nm, although lesser and greater thicknesses may also be employed. In case the channel cavities 21 are not completely filled with the channel semiconductor layer 26L, a dielectric channel core material layer 28L can be deposited over the channel semiconductor layer 26L. The dielectric channel core material layer 28L includes a dielectric material such as silicon oxide.

[0073] Referring to FIG. 6H, portions of the dielectric channel core material layer 28L and the channel semiconductor layer 26L located above the horizontal plane including the top surface of the gate-level dielectric material layer 763 can be removed by a chemical mechanical planarization process. Each remaining portion of the channel semiconductor

layer 26L that remains in a respective channel cavity comprises a vertical transistor channel 26. Each remaining portion of the dielectric channel core material layer 28L that remains in a respective channel cavity comprises a dielectric channel core 28.

[0074] Referring to FIG. 6I, a top-pad-level dielectric material layer 764 can be formed over the gate electrodes 16 and the vertical transistor channels 26. The top-pad-level dielectric material layer 764 includes a dielectric material such as undoped silicate glass, a doped silicate glass, or organosilicate glass. The thickness of the top-pad-level dielectric material layer 764 may be in a range from 50 nm to 200 nm, although lesser and greater thicknesses may also be employed. Pad cavities are formed within the top-pad-level dielectric material layer 764 over each of the vertical transistor channels 26. A doped semiconductor material can be deposited in the pad cavities directly on physically exposed surfaces of the vertical transistor channels 26. The doped semiconductor material may include a respective doped elemental semiconductor material (such as silicon (e.g., polysilicon), germanium, or a silicon-germanium alloy) or a respective III-V compound semiconductor material (such as GaAs). The doped semiconductor material can include electrical dopants (which may be p-type dopants or n-type dopants) of the same conductivity type as the doping of the bottom doped semiconductor electrodes 22 at an atomic concentration in a range from $5.0 \times 10^{18}/\text{cm}^3$ to $2.0 \times 10^{21}/\text{cm}^3$, although lesser and greater atomic concentrations may also be employed. Excess portions of the doped semiconductor material can be removed from above the horizontal plane including the top surface of the top-pad-level dielectric material layer 764. Remaining portions of the doped semiconductor material comprise top doped semiconductor electrodes 30. Each top doped semiconductor electrode 30 is formed on a top surface of a respective vertical transistor channel 26.

[0075] Referring to FIG. 6J, an interconnect-level dielectric layer 765 can be deposited

over the top-pad-level dielectric material layer 764. Via cavities and line cavities can be formed through the interconnect-level dielectric layer 765, and can be filled with at least one conductive material to form various upper logic-side metal interconnect structures 780B, which include upper electrode contact via structures 783 that contact a respective one of the top doped semiconductor electrodes 30, upper-electrode-connection metal lines 784 that contact at least one of the upper electrode contact via structures 783, gate contact via structures 785 that contact a respective one of the gate electrodes 16, and gate-connection metal lines 786 that contact a top surface of a respective gate contact via structure 785 and located at the same level as the upper-electrode-connection metal lines 784.

[0076] Referring to FIG. 6K, a first alternative embodiment of a set of vertical field effect transistors 20 is illustrated, which can be derived from the set of vertical field effect transistors of FIG. 6J by omitting formation of the dielectric channel cores 28.

[0077] Referring to FIG. 6L, a second alternative embodiment of a set of vertical field effect transistors 20 is illustrated, which can be derived from the set of vertical field effect transistors of FIG. 6J by vertically recessing the vertical transistor channels 26 and the dielectric channel cores 28 prior to formation of the top doped semiconductor electrodes 30 and omitting the top-pad-level dielectric material layer 764.

[0078] Referring to FIG. 6M, a third alternative embodiment of a set of vertical field effect transistors 20 is illustrated, which can be derived from the set of vertical field effect transistors of FIG. 6L by omitting formation of the dielectric channel cores 28.

[0079] Referring to FIG. 6N, a third alternative embodiment of a set of vertical field effect transistors 20 is illustrated, which can be derived from the set of vertical field effect transistors of FIG. 6L by vertically recessing only the vertical transistor channels 26 without recessing the dielectric channel cores 28 prior to formation of the top doped semiconductor

electrodes 30 and omitting top-pad-level dielectric material layer 764.

[0080] Within each vertical field effect transistor 20, one of the bottom doped semiconductor electrodes 22 and the top doped semiconductor electrodes 30 comprises a source region, and another of the bottom doped semiconductor electrodes 22 and the top doped semiconductor electrodes 30 comprises a drain region.

[0081] Referring to FIGS. 1A – 6N and according to various embodiments of the present disclosure, a bonded assembly comprising a memory die 900 and a logic die 700 is provided. The memory die 900 comprises a three-dimensional memory array. The logic die 700 comprises a logic-side substrate 708 and at least one set of vertical field effect transistors 20. Each vertical field effect transistor 20 within each set of vertical field effect transistors 20 comprises a bottom doped semiconductor electrode 22, a vertical transistor channel 26, a gate dielectric 24 which surrounds the vertical transistor channel 26 and a top doped semiconductor electrode 30. Each set of vertical field effect transistors 20 comprises a respective gate electrode 16 that laterally surrounds each of the gate dielectrics 24 within a same set of vertical field effect transistors 20. At least one set of vertical field effect transistors 20 is electrically connected to electrical nodes of the three-dimensional memory array through sets of metal bonding pads (988, 788) through which the memory die 900 and the logic die 700 are bonded to each other.

[0082] In one embodiment, the logic die 700 comprises substrate field effect transistors including a respective semiconductor channel 746 comprising a portion of, or comprising a same material as, the logic-side substrate 708. The bottom doped semiconductor electrodes 22 of the at least one set of vertical field effect transistors 20 are electrically connected to a first subset of the substrate field effect transistors via a first subset of lower logic-side metal interconnect structures 780A embedded within lower logic-side dielectric material layers,

which are portions of the logic-side dielectric material layers 760 located below the vertical field effect transistors 20.

[0083] In one embodiment, the bonded assembly comprises upper logic-side metal interconnect structures 780B electrically connecting the upper doped semiconductor electrodes 30 of the at least one set of vertical field effect transistors 20 to logic-side bonding pads 788 within the sets of metal bonding pads (988, 788), and embedded within upper logic-side dielectric material layers, which are portions of the logic-side dielectric material layers 760 located above the vertical field effect transistors 20. In one embodiment, the gate electrode 16 of each set of vertical field effect transistors 20 is electrically connected to a second subset of the substrate field effect transistors via a second subset of lower logic-side metal interconnect structures 780A.

[0084] In one embodiment, the memory die 900 comprises: an alternating stack of insulating layers 32 and electrically conductive layers 46 located on a memory-side substrate 908; memory openings vertically extending through the alternating stack (32, 46); and memory opening fill structures 58 located within the memory openings and comprising a respective set of a memory film 50 and a vertical semiconductor channel 60. In one embodiment, the three-dimensional memory array comprises a three-dimensional array of memory elements that includes portions of the memory films 50 that are located adjacent to a respective one of vertical semiconductor channels 60.

[0085] In one embodiment, the memory die 900 comprises: drain regions 64 located within the memory opening fill structures 58 and contacting an end portion of a respective one of the vertical semiconductor channels 60; bit lines 98 electrically connected to a respective subset of the drain regions 63 through a respective set of drain contact via structures 88. A subset of the top doped semiconductor electrodes 30 of the at least one set of

vertical field effect transistors 20 is electrically connected to a respective one of the bit lines 98.

[0086] In one embodiment, the at least one set of vertical field effect transistors 20 comprise: a first set of vertical field effect transistors 20A including a respective bottom doped semiconductor electrode 22 that is electrically connected to a respective sense amplifier circuit located on the logic-side substrate 708; and a second set of vertical field effect transistors 20B including a respective bottom doped semiconductor electrode 22 that is electrically connected to a bit line bias circuit located on the logic-side substrate 708. In one embodiment, the logic die 700 comprises upper logic-side metal interconnect structures 780B located between the at least one set of vertical field effect transistors 20 and the sets of metal bonding pads 788; and the upper logic-side metal interconnect structures 780B comprises upper-electrode-connection metal lines 784 that are electrically connected to a respective set of a top doped semiconductor electrode 30 within the first set of vertical field effect transistors 20A and a top doped semiconductor electrode 30 within the second set of vertical field effect transistors 20B.

[0087] In one embodiment, at least 50 % of a total area of the at least one set of vertical field effect transistors 20 has an areal overlap with a total area including each sense amplifier circuit and each bit line bias circuit in a plan view. In one embodiment, at least 90 % of a total area of the at least one set of vertical field effect transistors 20 has an areal overlap with a total area including each sense amplifier circuit and each bit line bias circuit in a plan view. In one embodiment, 100 % of a total area of the at least one set of vertical field effect transistors 20 has an areal overlap with a total area including each sense amplifier circuit and each bit line bias circuit in a plan view. In one embodiment, at least 50 % of a total area of the at least one set of vertical field effect transistors 20 is located outside a total area

including each sense amplifier circuit and each bit line bias circuit in a plan view. In one embodiment, at least 90 % of a total area of the at least one set of vertical field effect transistors 20 is located outside a total area including each sense amplifier circuit and each bit line bias circuit in a plan view. In one embodiment, 100 % of a total area of the at least one set of vertical field effect transistors 20 is located outside a total area including each sense amplifier circuit and each bit line bias circuit in a plan view.

[0088] In one embodiment, the electrically conductive layers 46 comprise word lines of the three-dimensional memory array. The memory die 900 comprises layer contact via structures 86 extending vertically through a dielectric material portion 65 and contacting a surface of a respective one of the electrically conductive layers 46. A subset of the top doped semiconductor electrodes 30 of the at least one set of vertical field effect transistors 20 is electrically connected to a respective one of the word lines.

[0089] In one embodiment, each bottom doped semiconductor electrode 22 of the at least one set of vertical field effect transistors 20 contacts a top surface of a respective lower logic-side metal interconnect structure 780A within the logic die 700. Each top doped semiconductor electrode 30 of the at least one set of vertical field effect transistors 20 contacts a bottom surface of a respective upper logic-side metal interconnect structure 780B within the logic die 700.

[0090] Referring to FIGS. 7A and 7B, a second exemplary structure is illustrated, which comprises an exemplary semiconductor die after formation of lower-level dielectric material layers 360 embedding lower-level metal interconnect structures according to a second embodiment of the present disclosure. The second exemplary structure comprises a semiconductor substrate 308 including a substrate semiconductor layer 310. In one embodiment, the semiconductor substrate 308 may be the same as the logic-side substrate

708, and the substrate semiconductor layer 310 may be the same as the logic-side substrate semiconductor layer 710. A peripheral circuit for controlling operation of a three-dimensional memory array can be formed on the substrate semiconductor layer 310. The peripheral circuit of the second exemplary structure may be the same as the peripheral circuit formed on the logic-side substrate semiconductor layer 710 described above. The peripheral circuit can include substrate field effect transistors 702, which include a respective semiconductor channel comprising a portion of, or comprising a same material as, the semiconductor substrate 308. First metal interconnect structures 380A embedded within first dielectric material layers can be formed. The first metal interconnect structures 380A can be electrically connected to a respective node of the peripheral circuit on the semiconductor substrate 308.

[0091] At least one set of vertical field effect transistors can be formed by performing the processing steps of FIGS. 6A – 6J and/or FIGS. 6K to 6N. The bottom doped semiconductor electrodes 22 of the at least one set of vertical field effect transistors 20 can be electrically connected to a first subset of the substrate field effect transistors via a first subset of first metal interconnect structures 380A. Generally, the bottom doped semiconductor electrodes 22 can be formed over first dielectric material layers (which are a subset of lower-level dielectric material layers 360) that overlie the semiconductor substrate 308. For each set of vertical field effect transistors 20, a gate electrode 16 including a plurality of vertically-extending openings (channel cavities) can be formed over the bottom doped semiconductor electrodes 22 so that the bottom doped semiconductor electrodes 22 are exposed underneath the vertically-extending openings. A combination of a cylindrical gate dielectric 24 and a vertical transistor channel 26 can be formed within each of the vertically-extending openings. Top doped semiconductor electrodes 30 can be formed on the vertical transistor channels 26.

Second metal interconnect structures 380B embedded in second dielectric material layers (i.e., portions of the lower-level dielectric material layers 360 overlying the vertical field effect transistors 20) can be formed over the top doped semiconductor electrodes 30. The second metal interconnect structures 380B can include, for example, upper electrode contact via structures 783 that contact a respective one of the top doped semiconductor electrodes 30, upper-electrode-connection metal lines 784 that contact at least one of the upper electrode contact via structures 783, gate contact via structures 785 that contact a respective one of the gate electrodes 16, and gate-connection metal lines 786 that contact a top surface of a respective gate contact via structure 785 and located at the same level as the upper-electrode-connection metal lines 784. The second metal interconnect structures 380B can include metallic landing pad structures 790 which can be subsequently employed as contact pad for metallic connection via structures to be subsequently formed. A topmost surface of the lower-level dielectric material layers 360 can include a planar dielectric surface.

[0092] Referring to FIGS. 8A and 8B, a semiconductor material layer 10 can be formed over the lower-level dielectric material layers 360 by depositing a polycrystalline semiconductor material (e.g., polysilicon), or by bonding and patterning a single crystalline semiconductor material (e.g., single crystal silicon) layer employing a layer transfer method. A three-dimensional memory array can be formed in the same manner as the three-dimensional memory array illustrated in FIGS. 2A – 2D. The semiconductor material layer 10 can be employed in lieu of the memory-side substrate semiconductor layer 910.

[0093] Generally, an alternating stack of insulating layers 32 and spacer material layers can be formed over a semiconductor substrate 308. The spacer material layers are formed as, or are subsequently replaced with, electrically conductive layers 46. Dielectric material portion 65 are formed adjacent to the alternating stack (32, 46). Memory openings are

formed through the alternating stack (32, 46), and memory opening fill structures 58 can be formed within the memory openings. Each of the memory opening fill structures 58 comprises a respective set of a memory film 50 and a vertical semiconductor channel 60. Drain regions 63 can be formed at an end portion of a respective one of the vertical semiconductor channels 60. A three-dimensional memory array can be formed over the second dielectric material layers, which are upper portions of the lower-level dielectric material layers 360. The electrically conductive layers comprise word lines of the three-dimensional memory array.

[0094] Referring to FIGS. 9A and 9B, layer contact via structures 86 can be formed directly on a surface of a respective one of the electrically conductive layers 46. Memory-level connection via structures 488 can be formed through the dielectric material portions 65 onto a top surface of respective one of the metallic landing pad structures 790. Upper-level metal interconnect structures 480 embedded in upper-level dielectric material layers 460 can be formed over the alternating stack (32, 46). The upper-level metal interconnect structures 480, the memory-level connection via structures 488, and the second metal interconnect structures 380B electrically connect the upper doped semiconductor electrodes 30 of the at least one set of vertical field effect transistors 20 to electrical nodes of the three-dimensional memory array. The upper-level metal interconnect structures 480 can include bit lines 98 that are formed over the memory opening fill structures 58. Each of the bit lines 98 can be electrically connected to a respective subset of the drain regions 63 through a respective set of drain contact via structures 88. Electrical nodes of the three-dimensional memory array can be electrically connected to a respective one of the top doped semiconductor electrodes 30. In one embodiment, a subset of the top doped semiconductor electrodes 30 of the at least one set of vertical field effect transistors 20 can be electrically connected to a respective one

of the bit lines 98. In one embodiment, a subset of the top doped semiconductor electrodes 30 of the at least one set of vertical field effect transistors 20 can be electrically connected to a respective one of the word lines.

[0095] Referring to FIG. 10, an alternative embodiment of the second exemplary structure is illustrated, which can be derived from the second exemplary structure of FIGS. 9A and 9B by rearranging the layout of the substrate field effect transistors such that the areas of the vertical field effect transistors 20 is laterally offset, at least partially, from the area of the sense amplifier circuits and the bit line bias circuits. Generally, the percentage overlap between the total area of the at least one set of vertical field effect transistors 20 and the total area including each sense amplifier circuit and each bit line bias circuit may be from 0 % to 100 % of the lesser of the total area of the at least one set of vertical field effect transistors 20 and the total area including each sense amplifier circuit and each bit line bias circuit.

[0096] Referring to FIGS. 6A – 10 and according to various embodiments of the present disclosure, a semiconductor structure is provided, which comprises: at least one set of vertical field effect transistors 20 located above, and vertically spaced from, a semiconductor substrate 308, wherein each vertical field effect transistor 20 within each set of vertical field effect transistors 20 comprises a bottom doped semiconductor electrode 22, a vertical transistor channel 26, a gate dielectric 24 which surrounds the vertical transistor channel 26, and a top doped semiconductor electrode 30; and a three-dimensional NAND memory array located over the at least one set of vertical field effect transistors, wherein electrical nodes of the three-dimensional NAND memory array are electrically connected to a respective one of the at least one set of vertical field effect transistors 20.

[0097] In one embodiment, the three-dimensional NAND memory array comprises: an alternating stack of insulating layers 32 and electrically conductive layers 46 located over the

at least one set of vertical field effect transistors 20; memory openings vertically extending through the alternating stack (32, 46); and memory opening fill structures 58 located within the memory openings and comprising a respective set of a memory film 50 and a vertical semiconductor channel 60. In one embodiment, a semiconductor material layer 10 can be located between the alternating stack (32, 46) and the at least one set of vertical field effect transistors 20. The semiconductor material layer 10 may comprise at least one of a horizontal semiconductor channel and a source region 61.

[0098] Metal interconnect structures (480, 488, 280) can electrically connect the electrical nodes of the three-dimensional NAND memory array to the respective one of the at least one set of vertical field effect transistors 20. The metal interconnect structures (480, 488, 280) can comprise: lower-level metal interconnect structures 380 underlying the alternating stack (32, 46); upper-level metal interconnect structures 480 overlying the alternating stack (32, 46); and memory-level connection via structures 488 vertically extending between a horizontal plane including a top surface of the alternating stack (32, 46) and a horizontal plane including a bottom surface of the alternating stack (32, 46) and connecting the lower-level metal interconnect structures 380 to the upper-level metal interconnect structures 480.

[0099] In one embodiment, the three-dimensional NAND memory array comprises a three-dimensional NAND array of memory elements that includes portions of the memory films 50 that are located adjacent to a respective one of vertical semiconductor channels 60.

[00100] In one embodiment, the semiconductor structure comprises: drain regions 63 located within the memory opening fill structures 58 and contacting an end portion of a respective one of the vertical semiconductor channels 60; bit lines 98 electrically connected to a respective subset of the drain regions 63 through a respective set of drain contact via

structures 88, wherein a subset of the top doped semiconductor electrodes 30 of the at least one set of vertical field effect transistors 20 is electrically connected to a respective one of the bit lines 98.

[00101] In one embodiment, the at least one set of vertical field effect transistors 20 comprises: a first set of vertical field effect transistors 20 including a respective bottom doped semiconductor electrode 22 that is electrically connected to a respective sense amplifier circuit located on the semiconductor substrate 308; and a second set of vertical field effect transistors 20 including a respective bottom doped semiconductor electrode 22 that is electrically connected to a bit line bias circuit located on the semiconductor substrate 308.

[00102] In one embodiment, upper-electrode-connection metal lines 784 can be located between the alternating stack (32, 46) and the at least one set of vertical field effect transistors 20, wherein each of the upper-electrode-connection metal lines 784 is electrically connected to a respective set of a top doped semiconductor electrode 30 within the first set of vertical field effect transistors 20 and a top doped semiconductor electrode 30 within the second set of vertical field effect transistors 20.

[00103] In one embodiment, at least 50 % of a total area of the at least one set of vertical field effect transistors 20 has an areal overlap with a total area including each sense amplifier circuit and each bit line bias circuit in a plan view. In one embodiment, at least 90 % of a total area of the at least one set of vertical field effect transistors 20 has an areal overlap with a total area including each sense amplifier circuit and each bit line bias circuit in a plan view. In one embodiment, 100 % of a total area of the at least one set of vertical field effect transistors 20 has an areal overlap with a total area including each sense amplifier circuit and each bit line bias circuit in a plan view. In one embodiment, at least 50 % of a total area of the at least one set of vertical field effect transistors 20 is located outside a total area

including each sense amplifier circuit and each bit line bias circuit in a plan view. In one embodiment, at least 90 % of a total area of the at least one set of vertical field effect transistors 20 is located outside a total area including each sense amplifier circuit and each bit line bias circuit in a plan view. In one embodiment, 100 % of a total area of the at least one set of vertical field effect transistors 20 is located outside a total area including each sense amplifier circuit and each bit line bias circuit in a plan view.

[00104] In one embodiment, the electrically conductive layers 46 comprise word lines of the three-dimensional NAND memory array; contact via structures 86 extend vertically through a dielectric material portion 65 and contact a surface of a respective one of the electrically conductive layers 46; and a subset of the top doped semiconductor electrodes 30 of the at least one set of vertical field effect transistors 20 is electrically connected to a respective one of the word lines.

[00105] In one embodiment, each set of vertical field effect transistors 20 comprises a respective gate electrode 16 that laterally surrounds each of the gate dielectrics 24 within a same set of vertical field effect transistors 20.

[00106] In one embodiment, the semiconductor structure comprises substrate field effect transistors including a respective semiconductor channel comprising a portion of, or comprising a same material as, the semiconductor substrate 308, wherein the bottom doped semiconductor electrodes 22 of the at least one set of vertical field effect transistors 20 are electrically connected to a first subset of the substrate field effect transistors via a first subset of first metal interconnect structures 380A embedded within first dielectric material layers 360 that underlie the at least one set of vertical field effect transistors 20.

[00107] In one embodiment, the gate electrode 16 of each set of vertical field effect transistors 20 is electrically connected to a second subset of the substrate field effect

transistors via a second subset of the first metal interconnect structures 380A.

[00108] FIGS. 11A – 16B illustrate a sequence of processing steps that can be employed to form a three-dimensional NAND memory array within the memory die 900 of the first exemplary structure or within the second exemplary structure. In the case of the second exemplary structure, the memory-side substrate semiconductor layer 910 can be replaced with a semiconductor material layer 10.

[00109] Referring to FIGS. 11A and 11B, at least one alternating stack of insulating layers 32 and spacer material layers can be formed over the memory-side substrate semiconductor layer 910 or over the semiconductor material layer 10. The spacer material layers are formed are, or are subsequently replaced with, electrically conductive layers 46, which function as word lines. In the illustrated example, the spacer material layers may be formed as sacrificial material layers 42. Each alternating stack (32, 42) can be patterned to form stepped surfaces. The area including the stepped surfaces constitute the staircase region 200. Dielectric material portions 65 can be formed over the stepped surfaces. Further, additional dielectric material portions 65 can be formed between alternating stacks (32, 46) that are laterally spaced apart.

[00110] Referring to FIGS. 12A and 12B, memory openings are formed through the portions of the alternating stack (32, 42) in which each layer of the alternating stack (32, 42) is present, i.e., within a memory array region 100. Memory opening fill structures 58 are formed within the memory openings. Each of the memory opening fill structures comprises a respective set of a memory film 50, a vertical semiconductor channel 60, and a drain region 63, and optionally includes a dielectric core 62. Each contiguous combination of a vertical semiconductor channel 60 and a memory film 50 constitutes a memory stack structure 55. Each memory film 50 includes a vertical stack of memory elements that are located at levels

of the electrically conductive layers 46. In one embodiment, each memory film 50 may include a layer stack including, from outside to inside, a blocking dielectric layer, a charge storage layer or a vertical stack of discrete charge storage material portions, and a tunneling dielectric layer. Portions of the charge storage layer located at levels of the electrically conductive layers, or the vertical stack of discrete charge storage material portions constitute a vertical stack of memory elements. The drain regions 63 are formed at a top end portion of a respective one of the vertical semiconductor channels 60.

[00111] Referring to FIGS. 13A and 13B, an insulating cap layer 960A can be formed over the alternating stack (32, 42), and backside trenches 79 laterally extending along a first horizontal direction can be formed through the alternating stacks (32, 42) such that each alternating stack (32, 42) is divided into a respective plurality of alternating stacks (32, 42) by the backside trenches 79. Source regions 61 can be formed at the bottom of each backside trench 79.

[00112] Referring to FIGS. 14A and 14B, the sacrificial material layers 42 can be removed selective to the insulating layers 32 and the memory opening fill structures 58. Backside recesses 43 are formed in volumes from which the sacrificial material layers 42 are removed.

[00113] Referring to FIGS. 15A and 15B, the electrically conductive layers 46 can be formed by depositing at least one electrically conductive material in the backside recesses 43 and removing excess portions of the electrically conductive material from inside the backside trenches 79 and from above the alternating stacks (32, 46).

[00114] Referring to FIGS. 16A and 16B, each backside trench 79 can be filled with a respective backside trench fill structure, which may include, for example, an insulating spacer 74 and a backside contact via structure 76 that can function as a source contact via structure. A contact-level dielectric layer 960B can be deposited over the insulating cap layer 960A.

Drain contact via structures 88 can be formed on the drain regions 63, and layer contact via structures 86 can be formed on the electrically conductive layers 46.

[00115] Subsequently, memory-side dielectric material layers 960 embedding memory-side metal interconnect structures 980 may be formed to provide a memory die 900 of the first exemplary structure, or upper-level dielectric material layers 460 embedding upper-level metal interconnect structures 480 may be formed to provide the semiconductor die of the second exemplary structure.

[00116] Although the foregoing refers to particular preferred embodiments, it will be understood that the disclosure is not so limited. It will occur to those of ordinary skill in the art that various modifications may be made to the disclosed embodiments and that such modifications are intended to be within the scope of the disclosure. Compatibility is presumed among all embodiments that are not alternatives of one another. The word “comprise” or “include” contemplates all embodiments in which the word “consist essentially of” or the word “consists of” replaces the word “comprise” or “include,” unless explicitly stated otherwise. Where an embodiment employing a particular structure and/or configuration is illustrated in the present disclosure, it is understood that the present disclosure may be practiced with any other compatible structures and/or configurations that are functionally equivalent provided that such substitutions are not explicitly forbidden or otherwise known to be impossible to one of ordinary skill in the art. All of the publications, patent applications and patents cited herein are incorporated herein by reference in their entirety.

WHAT IS CLAIMED IS:

1. A bonded assembly comprising a memory die and a logic die, wherein:

the memory die comprises a three-dimensional memory array;

the logic die comprises a logic-side substrate and at least one set of vertical field effect transistors;

each vertical field effect transistor within each set of vertical field effect transistors comprises a bottom doped semiconductor electrode, a vertical transistor channel, a gate dielectric which surrounds the vertical transistor channel, and a top doped semiconductor electrode;

each set of vertical field effect transistors comprises a respective gate electrode that laterally surrounds each of the gate dielectrics within a same set of vertical field effect transistors; and

at least one set of vertical field effect transistors is electrically connected to electrical nodes of the three-dimensional memory array through sets of metal bonding pads through which the memory die and the logic die are bonded to each other.

2. The bonded assembly of Claim 1, wherein:

the logic die comprises substrate field effect transistors including a respective semiconductor channel comprising a portion of, or comprising a same material as, the logic-side substrate; and

the bottom doped semiconductor electrodes of the at least one set of vertical field effect transistors are electrically connected to a first subset of the substrate field effect transistors via a first subset of lower logic-side metal interconnect structures embedded

within lower logic-side dielectric material layers.

3. The bonded assembly of Claim 2, further comprising upper logic-side metal interconnect structures electrically connecting the upper doped semiconductor electrodes of the at least one set of vertical field effect transistors to logic-side bonding pads within the sets of metal bonding pads, and embedded within upper logic-side dielectric material layers.

4. The bonded assembly of Claim 2, wherein the gate electrode of each set of vertical field effect transistors is electrically connected to a second subset of the substrate field effect transistors via a second subset of lower logic-side metal interconnect structures.

5. The bonded assembly of Claim 1, wherein the memory die comprises:

an alternating stack of insulating layers and electrically conductive layers located on a memory-side substrate;

memory openings vertically extending through the alternating stack; and

memory opening fill structures located within the memory openings and comprising a respective set of a memory film and a vertical semiconductor channel.

6. The bonded assembly of Claim 5, wherein the three-dimensional memory array comprises a three-dimensional array of memory elements that includes portions of the memory films that are located adjacent to a respective one of vertical semiconductor channels.

7. The bonded assembly of Claim 5, wherein the memory die comprises:

drain regions located within the memory opening fill structures and contacting an end portion of a respective one of the vertical semiconductor channels; and

bit lines electrically connected to a respective subset of the drain regions through a respective set of drain contact via structures,

wherein a subset of the top doped semiconductor electrodes of the at least one set of vertical field effect transistors is electrically connected to a respective one of the bit lines.

8. The bonded assembly of Claim 7, wherein the at least one set of vertical field effect transistors comprise:

a first set of vertical field effect transistors including a respective bottom doped semiconductor electrode that is electrically connected to a respective sense amplifier circuit located on the logic-side substrate; and

a second set of vertical field effect transistors including a respective bottom doped semiconductor electrode that is electrically connected to a bit line bias circuit located on the logic-side substrate.

9. The bonded assembly of Claim 8, wherein:

the logic die comprises upper logic-side metal interconnect structures located between the at least one set of vertical field effect transistors and the sets of metal bonding pads; and

the upper logic-side metal interconnect structures comprises upper-electrode-connection metal lines that are electrically connected to a respective set of a top doped semiconductor electrode within the first set of vertical field effect transistors and a top doped semiconductor electrode within the second set of vertical field effect transistors.

10. The bonded assembly of Claim 8, wherein at least 50 % of a total area of the at least one set of vertical field effect transistors has an areal overlap with a total area including each sense amplifier circuit and each bit line bias circuit in a plan view.

11. The bonded assembly of Claim 5, wherein:

the electrically conductive layers comprise word lines of the three-dimensional memory array;

the memory die comprises layer contact via structures extending vertically through a dielectric material portion and contacting a surface of a respective one of the electrically conductive layers; and

a subset of the top doped semiconductor electrodes of the at least one set of vertical field effect transistors is electrically connected to a respective one of the word lines.

12. The bonded assembly of Claim 1, wherein:

the vertical transistor channels comprise a respective elemental semiconductor material or a respective III-V compound semiconductor material;

one of the bottom doped semiconductor electrode or the top doped semiconductor electrode of the vertical field effect transistor comprises a source region of the vertical field effect transistor; and

another of the bottom doped semiconductor electrode or the top doped semiconductor electrode comprises a drain region of the vertical field effect transistor.

13. The bonded assembly of Claim 1, wherein:

each bottom doped semiconductor electrode of the at least one set of vertical field effect transistors contacts a top surface of a respective lower logic-side metal interconnect structure within the logic die; and

each top doped semiconductor electrode of the at least one set of vertical field effect transistors contacts a bottom surface of a respective upper logic-side metal interconnect structure within the logic die.

14. A method of forming a bonded assembly, comprising:

providing the memory die comprising a three-dimensional memory array and memory-side bonding pads;

forming at least one set of vertical field effect transistors over a logic-side substrate, wherein each set of vertical field effect transistor is formed by:

forming bottom doped semiconductor electrodes embedded within lower logic-side dielectric material layers over the logic-side substrate,

forming a gate electrode including a plurality of vertically-extending openings therethrough, wherein the bottom doped semiconductor electrodes are exposed underneath the vertically-extending openings,

forming a combination of a cylindrical gate dielectric and a vertical transistor channel within each of the vertically-extending openings,

forming top doped semiconductor electrodes on the vertical transistor channels; and

forming logic-side bonding pads embedded in upper logic-side dielectric material

layers and electrically connected to a respective one of the top doped semiconductor electrodes over the at least one set of vertical field effect transistors, whereby a logic die is provided; and

bonding the memory-side bonding pads with the logic-side bonding pads.

15. The method of Claim 14, further comprising:

forming substrate field effect transistors including a respective semiconductor channel comprising a portion of, or comprising a same material as, a logic-side substrate semiconductor layer in the logic-side substrate; and

forming lower logic-side metal interconnect structures within the lower logic-side dielectric material layers, wherein the bottom doped semiconductor electrodes of the at least one set of vertical field effect transistors are electrically connected to a first subset of the substrate field effect transistors via a first subset of lower logic-side metal interconnect structures embedded within lower logic-side dielectric material layers.

16. The method of Claim 15, further comprising forming upper logic-side metal interconnect structures embedded within upper logic-side dielectric material layers over the at least one set of vertical field effect transistors, wherein the upper logic-side metal interconnect structures electrically connect the upper doped semiconductor electrodes of the at least one set of vertical field effect transistors to the logic-side bonding pads.

17. The method of Claim 14, wherein providing the memory die comprises forming the memory die by:

forming an alternating stack of insulating layers and spacer material layers over a memory-side substrate, wherein the spacer material layers are formed are, or are subsequently replaced with, electrically conductive layers;

forming memory openings through the alternating stack; and

forming memory opening fill structures within the memory openings, wherein each of the memory opening fill structures comprises a respective set of a memory film and a vertical semiconductor channel,

wherein the memory die comprises a three-dimensional memory array including a three-dimensional array of memory elements that includes portions of the memory films that are located adjacent to a respective one of vertical semiconductor channels.

18. The method of Claim 17, wherein forming the memory die comprises:

forming drain regions at an end portion of a respective one of the vertical semiconductor channels; and

forming bit lines over the memory opening fill structures, wherein each of the bit lines is electrically connected to a respective subset of the drain regions through a respective set of drain contact via structures,

wherein a subset of the top doped semiconductor electrodes of the at least one set of vertical field effect transistors is electrically connected to a respective one of the bit lines.

19. The method of Claim 17, wherein:

the method comprises forming sense amplifier circuits and bit line bias circuits on the logic-side substrate;

the at least one set of vertical field effect transistors comprise:

a first set of vertical field effect transistors including a respective bottom doped semiconductor electrode that is electrically connected to a respective one of the sense amplifier circuits, and

a second set of vertical field effect transistors including a respective bottom doped semiconductor electrode that is electrically connected to a respective one of the bit line bias circuits; and

the method comprises forming upper-electrode-connection metal lines that are electrically connected to a respective set of a top doped semiconductor electrode within the first set of vertical field effect transistors and a top doped semiconductor electrode within the second set of vertical field effect transistors.

20. The method of Claim 17, wherein:

the electrically conductive layers comprise word lines of the three-dimensional memory array;

the method comprises forming layer contact via structures directly on a surface of a respective one of the electrically conductive layers; and

a subset of the top doped semiconductor electrodes of the at least one set of vertical field effect transistors is electrically connected to a respective one of the word lines via mating pairs of the memory-side bonding pads and the logic-side bonding pads.

21. A semiconductor structure comprising:

at least one set of vertical field effect transistors located above, and vertically spaced

from, a semiconductor substrate, wherein each vertical field effect transistor within each set of vertical field effect transistors comprises a bottom doped semiconductor electrode, a vertical transistor channel, a gate dielectric which surrounds the vertical transistor channel, and a top doped semiconductor electrode; and

a three-dimensional NAND memory array located over the at least one set of vertical field effect transistors, wherein electrical nodes of the three-dimensional NAND memory array are electrically connected to a respective one of the at least one set of vertical field effect transistors.

22. The semiconductor structure of Claim 21, wherein the three-dimensional NAND memory array comprises:

an alternating stack of insulating layers and electrically conductive layers located over the at least one set of vertical field effect transistors;

memory openings vertically extending through the alternating stack; and

memory opening fill structures located within the memory openings and comprising a respective set of a memory film and a vertical semiconductor channel.

23. The semiconductor structure of Claim 22, further comprising a semiconductor material layer located between the alternating stack and the at least one set of vertical field effect transistors and comprising at least one of a horizontal semiconductor channel and a source region.

24. The semiconductor structure of Claim 22, further comprising metal interconnect

structures electrically connecting the electrical nodes of the three-dimensional NAND memory array to the respective one of the at least one set of vertical field effect transistors, wherein the metal interconnect structures comprise:

- lower-level metal interconnect structures underlying the alternating stack;
- upper-level metal interconnect structures overlying the alternating stack; and
- memory-level connection via structures vertically extending between a horizontal plane including a top surface of the alternating stack and a horizontal plane including a bottom surface of the alternating stack and connecting the lower-level metal interconnect structures to the upper-level metal interconnect structures.

25. The semiconductor structure of Claim 22, wherein the three-dimensional NAND memory array comprises a three-dimensional NAND array of memory elements that includes portions of the memory films that are located adjacent to a respective one of vertical semiconductor channels.

26. The semiconductor structure of Claim 22, further comprising:

- drain regions located within the memory opening fill structures and contacting an end portion of a respective one of the vertical semiconductor channels;

- bit lines electrically connected to a respective subset of the drain regions through a respective set of drain contact via structures,

- wherein a subset of the top doped semiconductor electrodes of the at least one set of vertical field effect transistors is electrically connected to a respective one of the bit lines.

27. The semiconductor structure of Claim 26, wherein the at least one set of vertical field effect transistors comprises:

a first set of vertical field effect transistors including a respective bottom doped semiconductor electrode that is electrically connected to a respective sense amplifier circuit located on the semiconductor substrate; and

a second set of vertical field effect transistors including a respective bottom doped semiconductor electrode that is electrically connected to a bit line bias circuit located on the semiconductor substrate.

28. The semiconductor structure of Claim 27, further comprising upper-electrode-connection metal lines located between the alternating stack and the at least one set of vertical field effect transistors, wherein each of the upper-electrode-connection metal lines is electrically connected to a respective set of a top doped semiconductor electrode within the first set of vertical field effect transistors and a top doped semiconductor electrode within the second set of vertical field effect transistors.

29. The semiconductor structure of Claim 27, wherein at least 50 % of a total area of the at least one set of vertical field effect transistors has an areal overlap with a total area including each sense amplifier circuit and each bit line bias circuit in a plan view.

30. The semiconductor structure of Claim 22, wherein:

the electrically conductive layers comprise word lines of the three-dimensional NAND memory array;

layer contact via structures extend vertically through a dielectric material portion and contact a surface of a respective one of the electrically conductive layers; and

a subset of the top doped semiconductor electrodes of the at least one set of vertical field effect transistors is electrically connected to a respective one of the word lines.

31. The semiconductor structure of Claim 21, wherein each set of vertical field effect transistors comprises a respective gate electrode that laterally surrounds each of the gate dielectrics within a same set of vertical field effect transistors.

32. The semiconductor structure of Claim 21, further comprising substrate field effect transistors including a respective semiconductor channel comprising a portion of, or comprising a same material as, the semiconductor substrate, wherein the bottom doped semiconductor electrodes of the at least one set of vertical field effect transistors are electrically connected to a first subset of the substrate field effect transistors via a first subset of first metal interconnect structures embedded within first dielectric material layers that underlie the at least one set of vertical field effect transistors.

33. The semiconductor structure of Claim 32, wherein the gate electrode of each set of vertical field effect transistors is electrically connected to a second subset of the substrate field effect transistors via a second subset of the first metal interconnect structures.

34. A method of forming a semiconductor structure, comprising:

forming bottom doped semiconductor electrodes over first dielectric material layers

that overlie a semiconductor substrate;

forming a gate electrode including a plurality of vertically-extending openings over the bottom doped semiconductor electrodes wherein the bottom doped semiconductor electrodes are exposed underneath the vertically-extending openings;

forming a combination of a cylindrical gate dielectric and a vertical transistor channel within each of the vertically-extending openings;

forming top doped semiconductor electrodes on the vertical transistor channels;

forming second dielectric material layers over the top doped semiconductor electrodes; and

forming a three-dimensional NAND memory array over the second dielectric material layers, wherein electrical nodes of the three-dimensional NAND memory array are electrically connected to a respective one of the top doped semiconductor electrodes.

35. The method of Claim 34, further comprising:

forming substrate field effect transistors including a respective semiconductor channel comprising a portion of, or comprising a same material as, the semiconductor substrate; and

forming first metal interconnect structures within the first dielectric material layers, wherein the bottom doped semiconductor electrodes of the at least one set of vertical field effect transistors are electrically connected to a first subset of the substrate field effect transistors via a first subset of first metal interconnect structures.

36. The method of Claim 34, wherein forming the three-dimensional NAND memory array comprises:

forming an alternating stack of insulating layers and spacer material layers over a memory-side substrate, wherein the spacer material layers are formed as, or are subsequently replaced with, electrically conductive layers;

forming memory openings through the alternating stack; and

forming memory opening fill structures within the memory openings, wherein each of the memory opening fill structures comprises a respective set of a memory film and a vertical semiconductor channel.

37. The method of Claim 36, further comprising:

forming a dielectric material portion adjacent to the alternating stack;

forming memory-level connection via structures through the dielectric material portion; and

forming upper-level metal interconnect structures embedded in upper-level dielectric material layers over the alternating stack, wherein the upper-level metal interconnect structures, the memory-level connection via structures, and a subset of lower-level metal interconnect structures embedded within the second dielectric material layers electrically connect the upper doped semiconductor electrodes of the at least one set of vertical field effect transistors to electrical nodes of the three-dimensional NAND memory array.

38. The method of Claim 37, further comprising:

forming drain regions at an end portion of a respective one of the vertical semiconductor channels; and

forming bit lines over the memory opening fill structures, wherein each of the bit lines

is electrically connected to a respective subset of the drain regions through a respective set of drain contact via structures.

39. The method of Claim 38, wherein a subset of the top doped semiconductor electrodes of the at least one set of vertical field effect transistors is electrically connected to a respective one of the bit lines.

40. The method of Claim 38, wherein:

the electrically conductive layers comprise word lines of the three-dimensional NAND memory array;

the method further comprises forming layer contact via structures directly on a surface of a respective one of the electrically conductive layers; and

a subset of the top doped semiconductor electrodes of the at least one set of vertical field effect transistors is electrically connected to a respective one of the word lines.

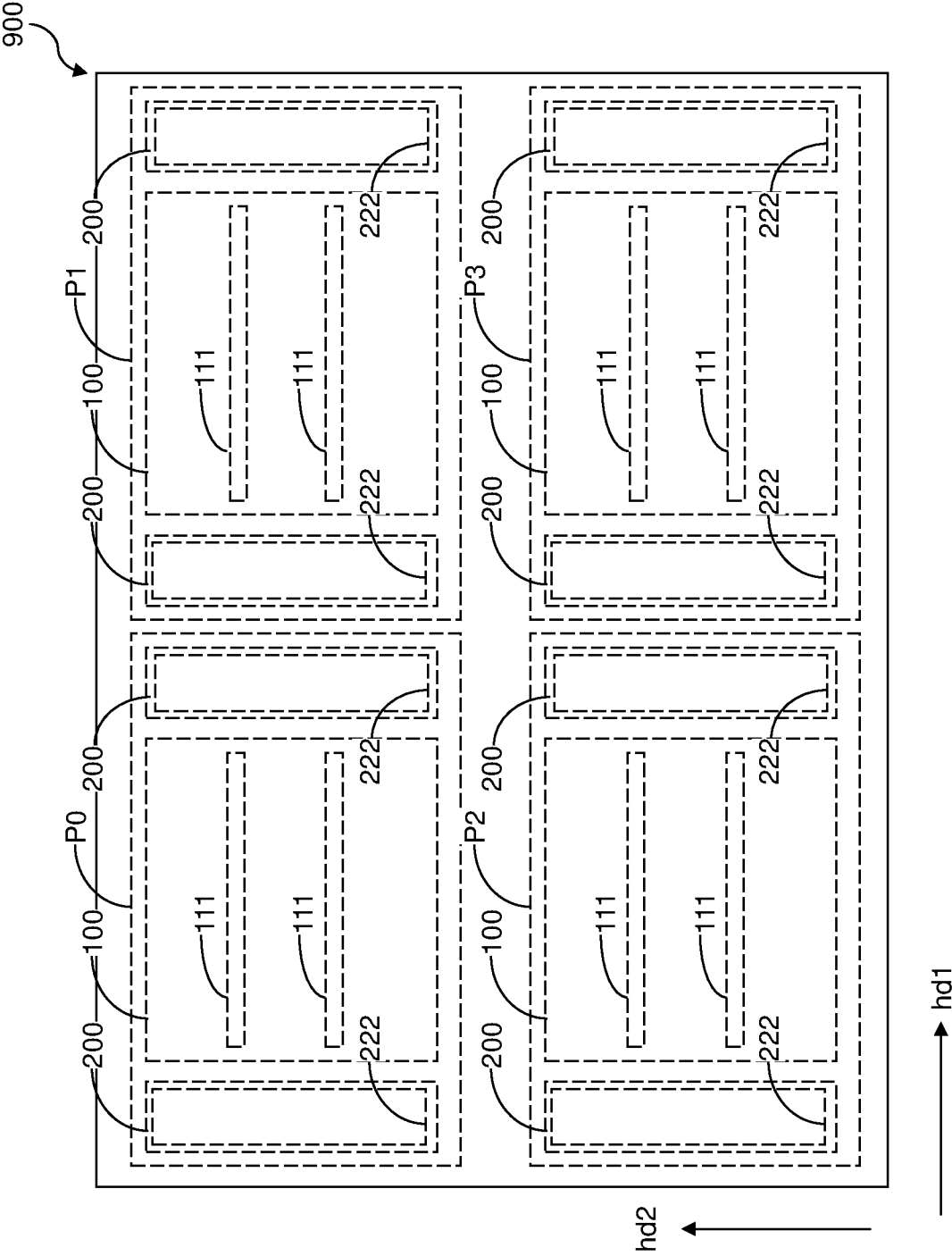


FIG. 1A

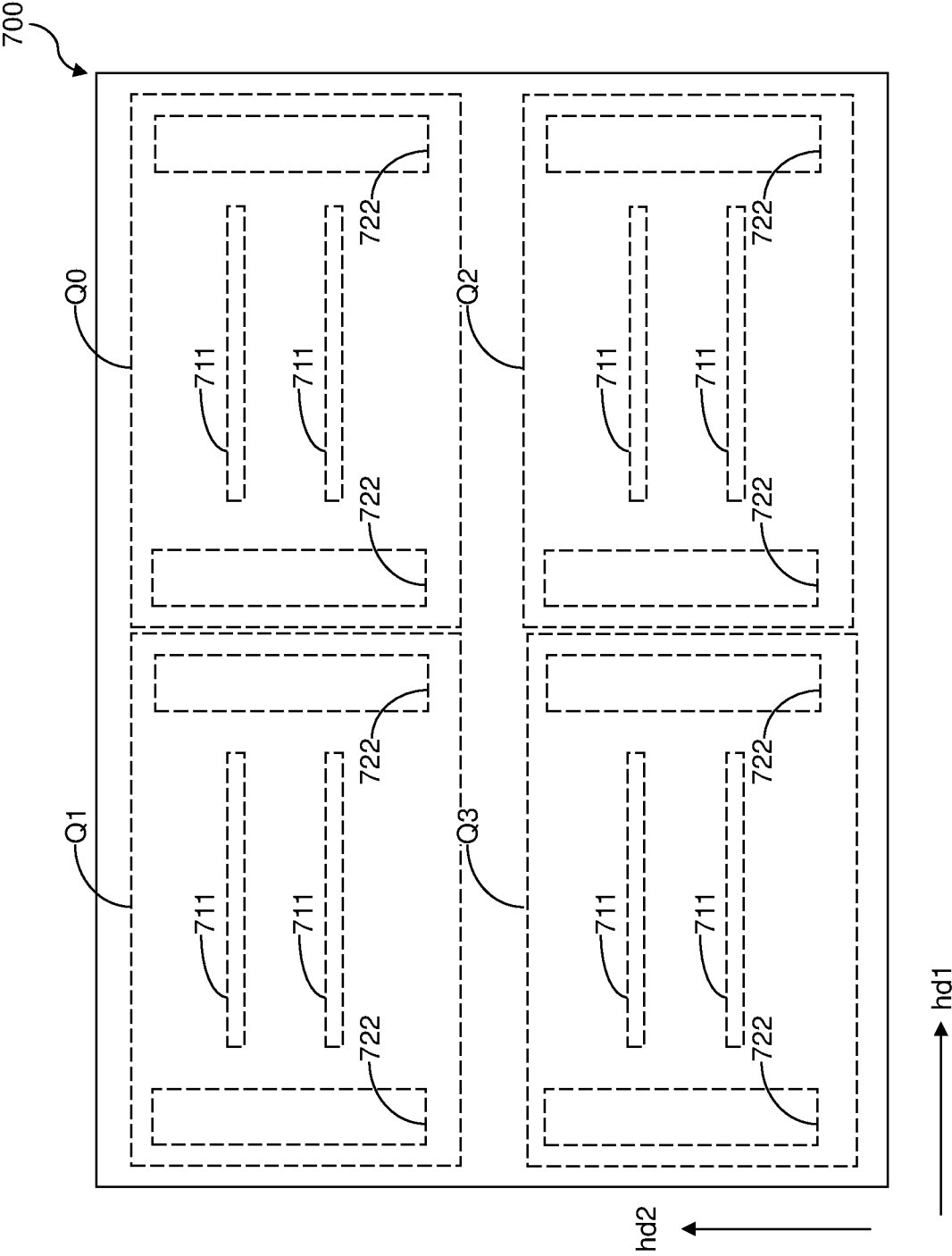


FIG. 1B

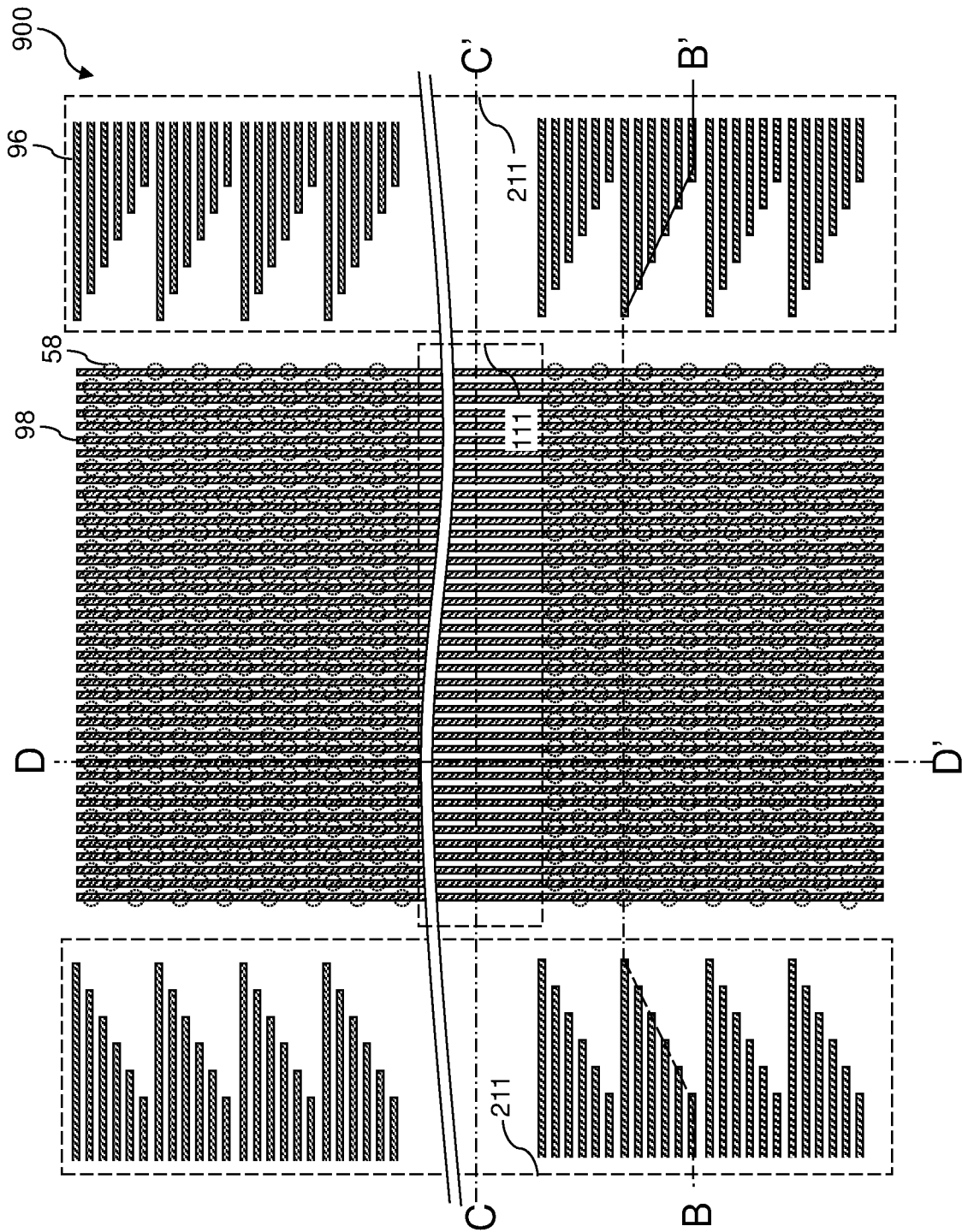


FIG. 2A

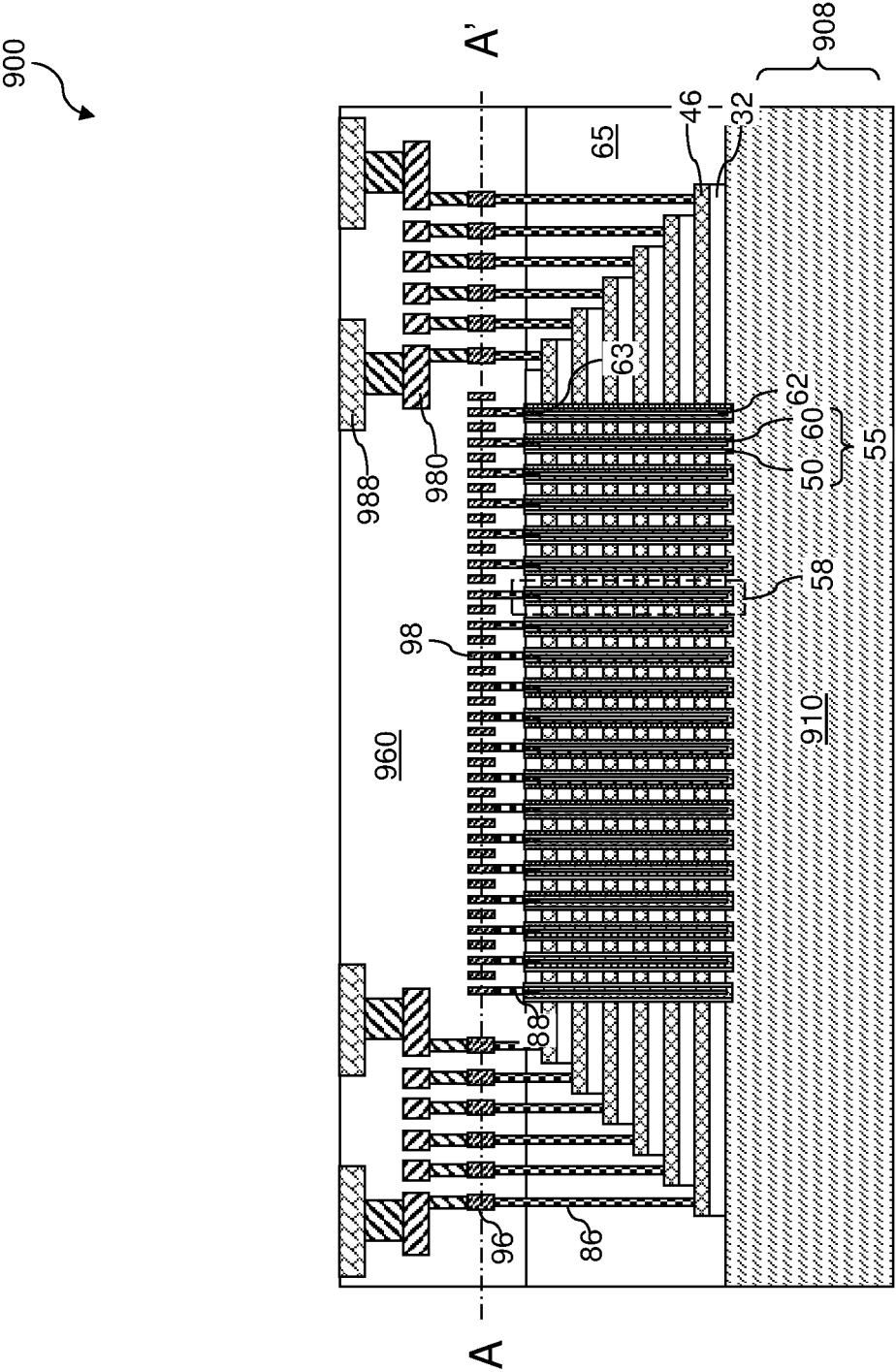


FIG. 2B

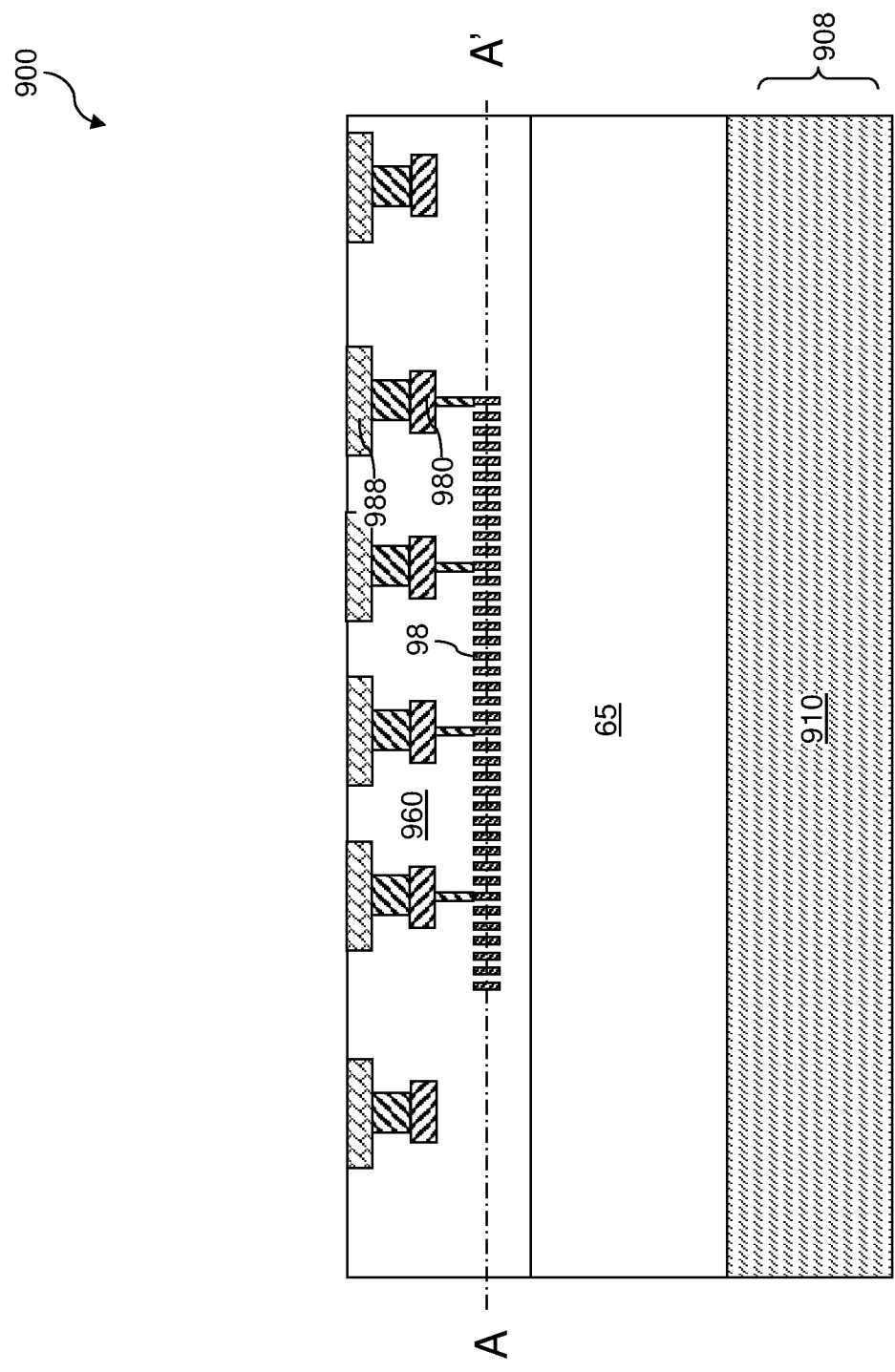


FIG. 2C

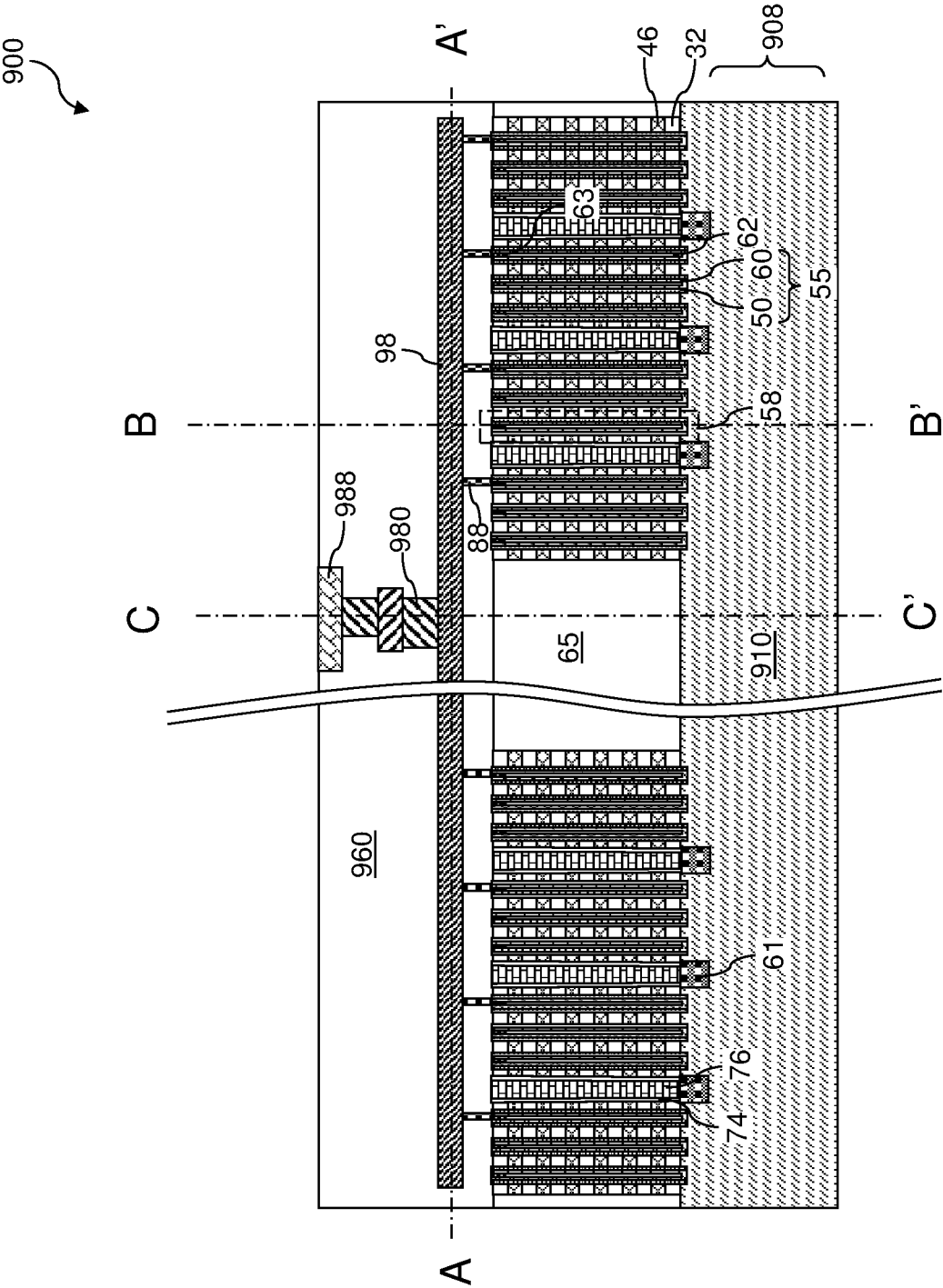
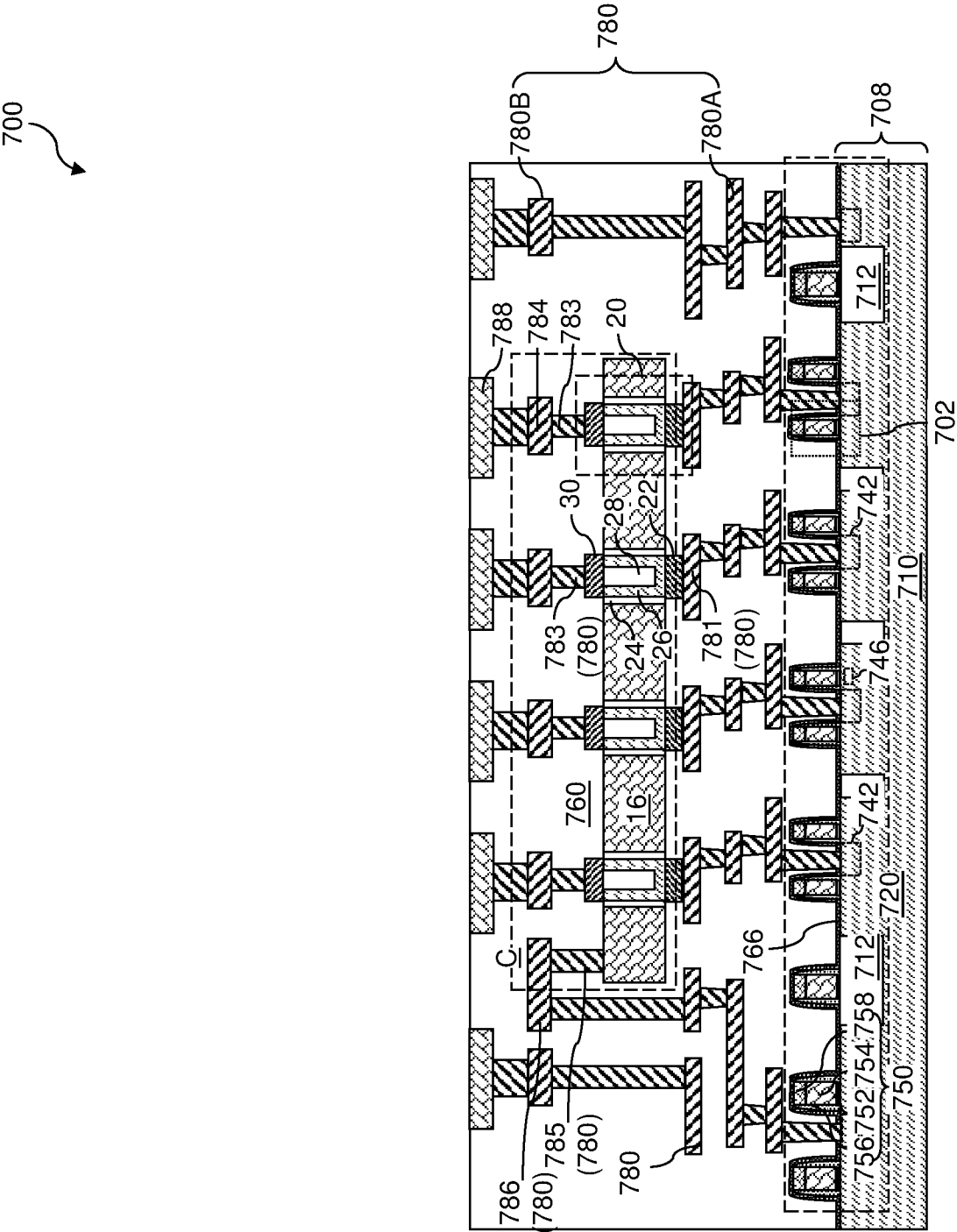


FIG. 2D



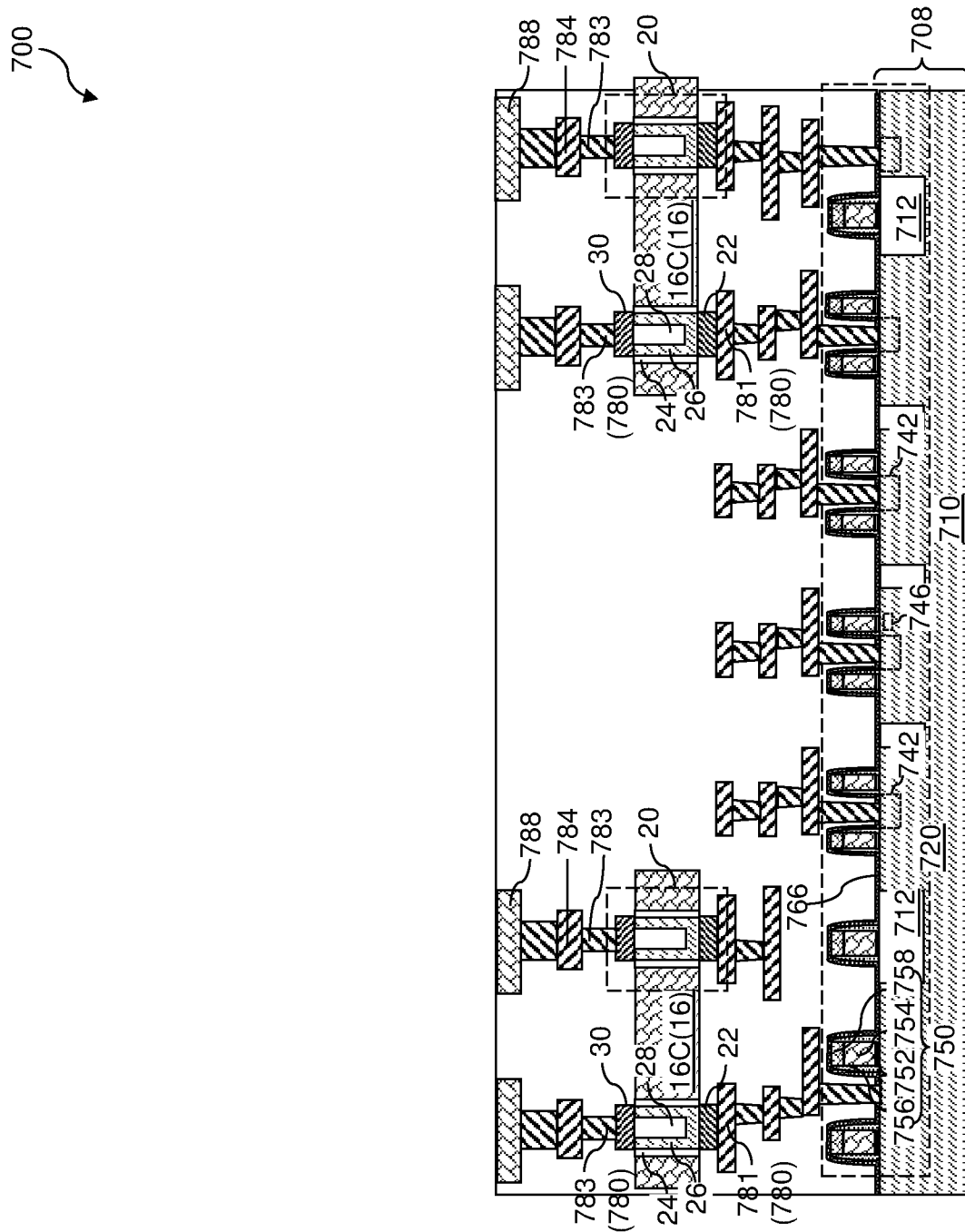


FIG. 3B

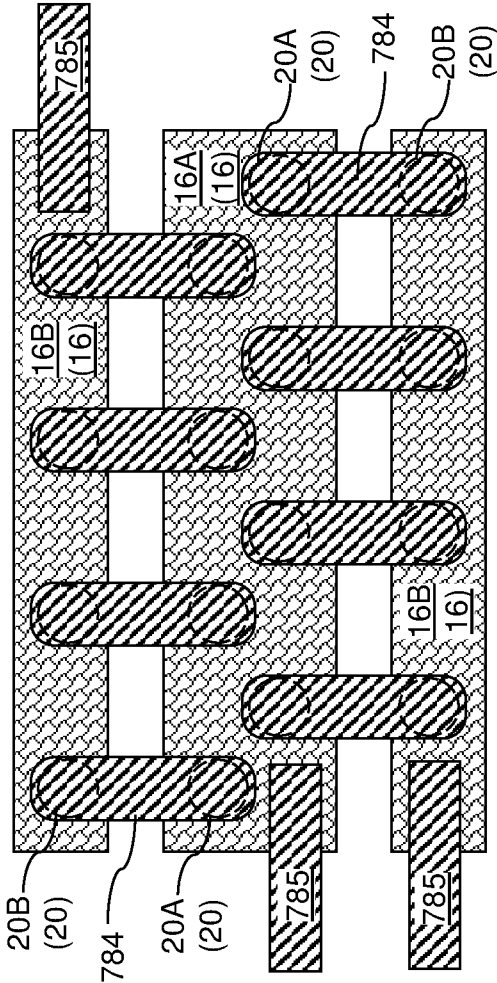


FIG. 3C

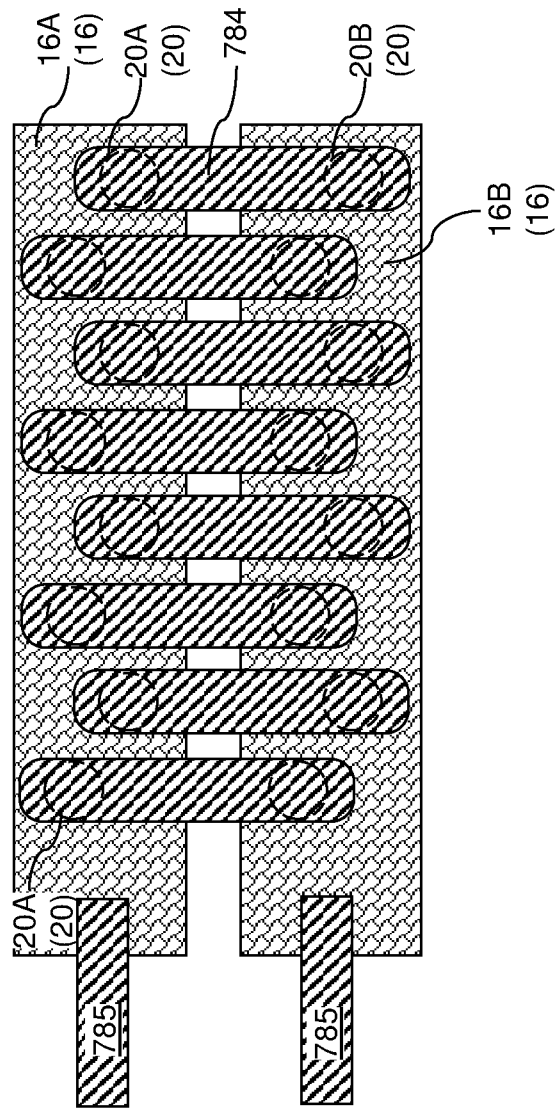


FIG. 3D

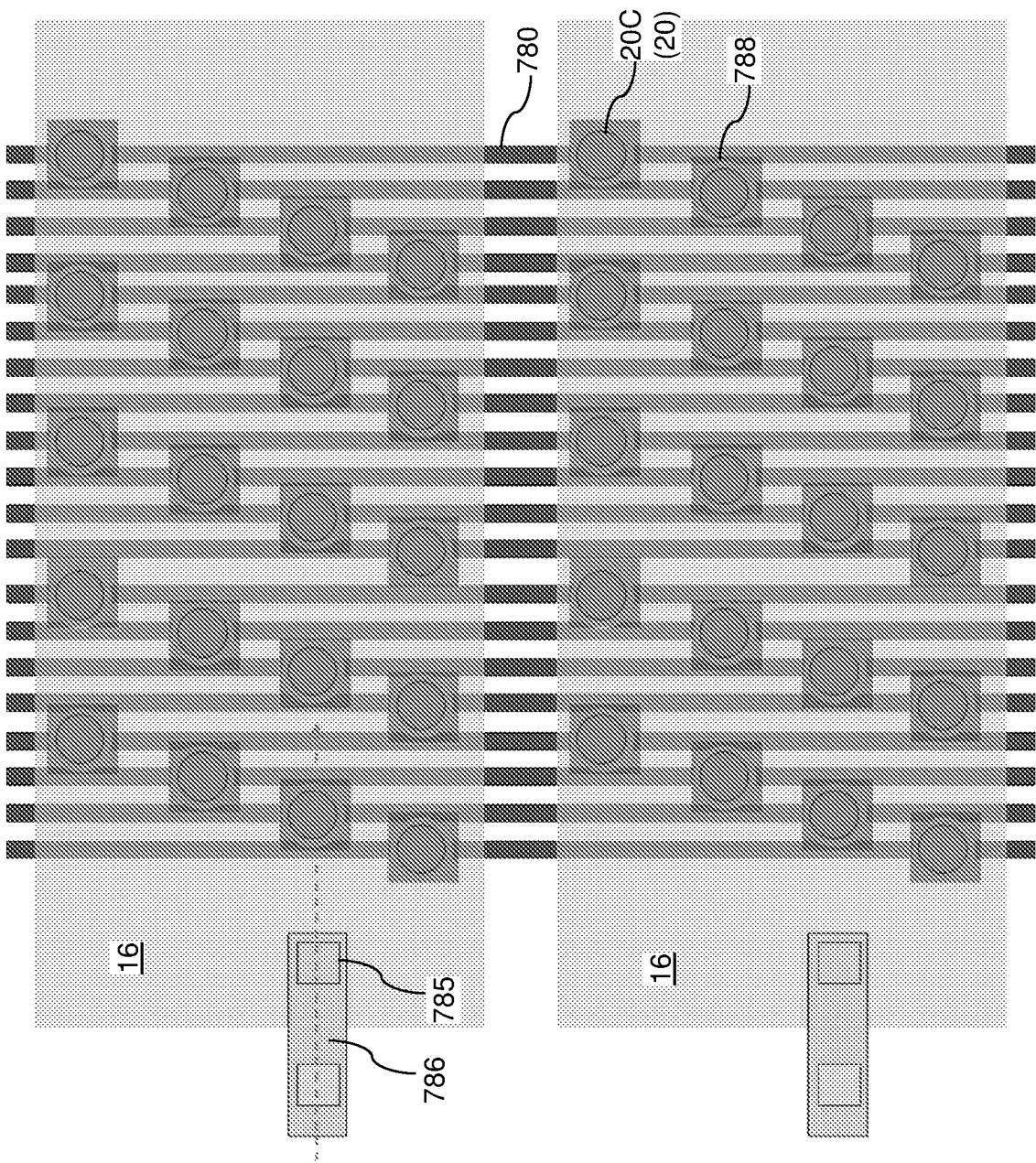
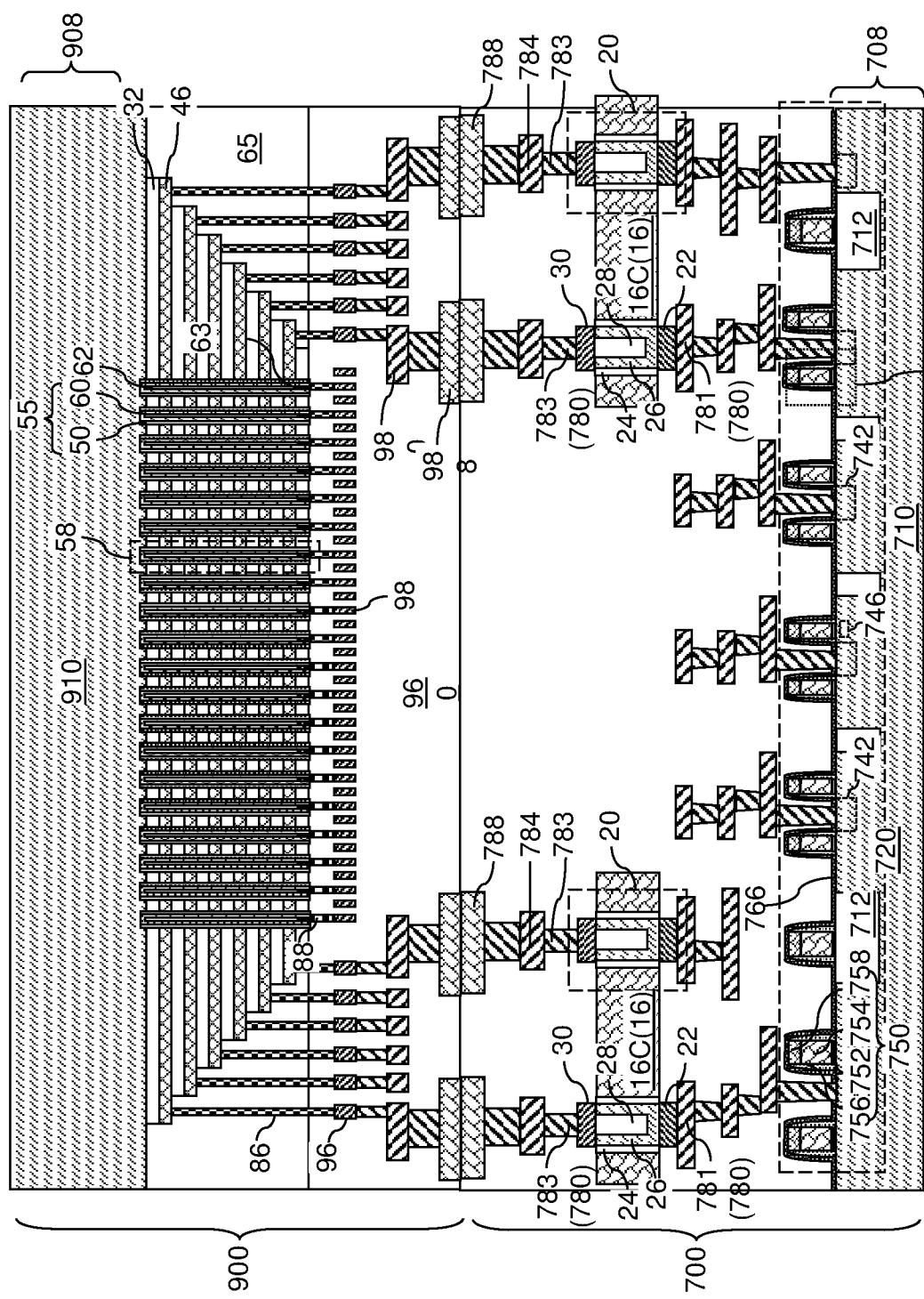


FIG. 3E



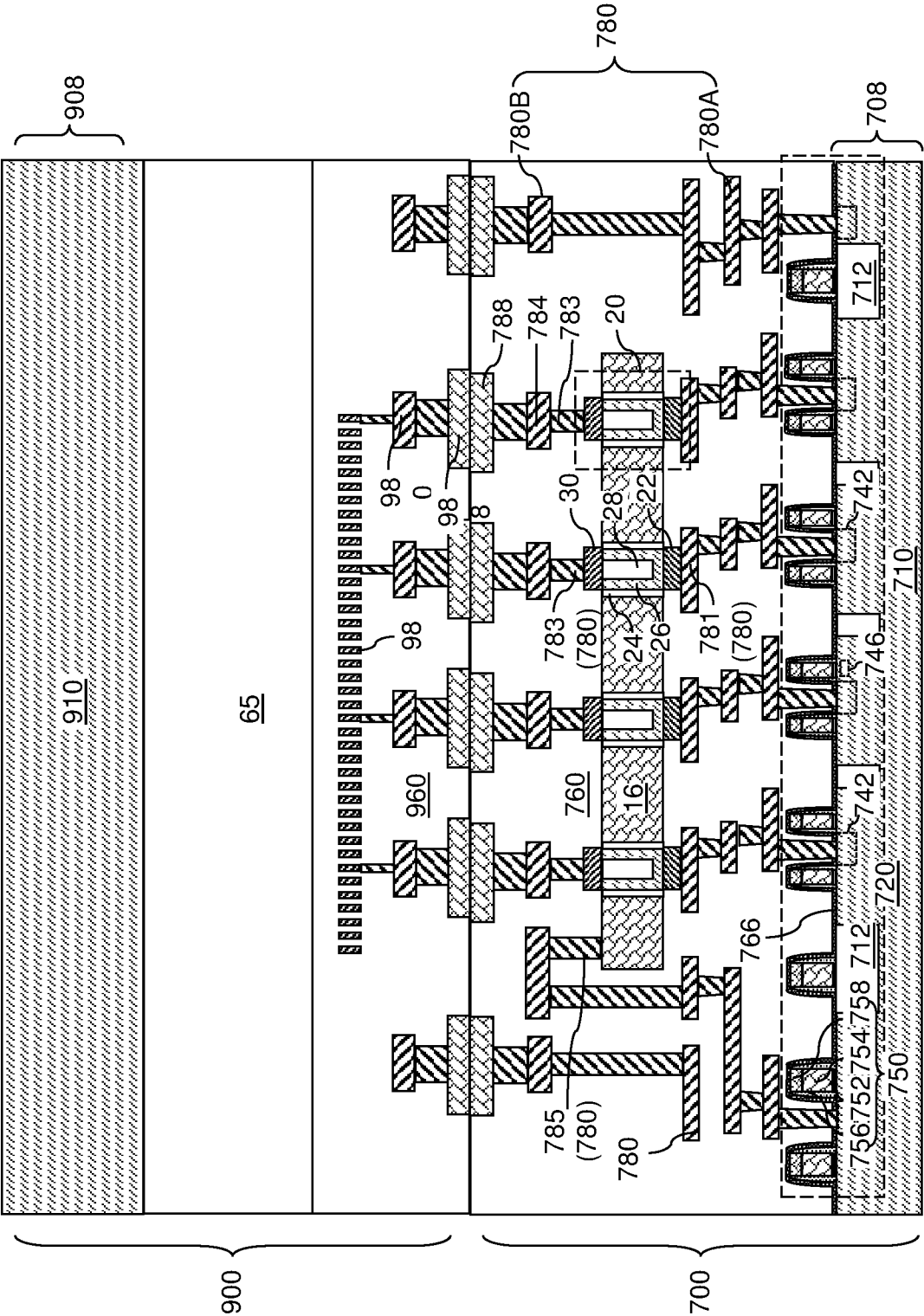


FIG. 4B

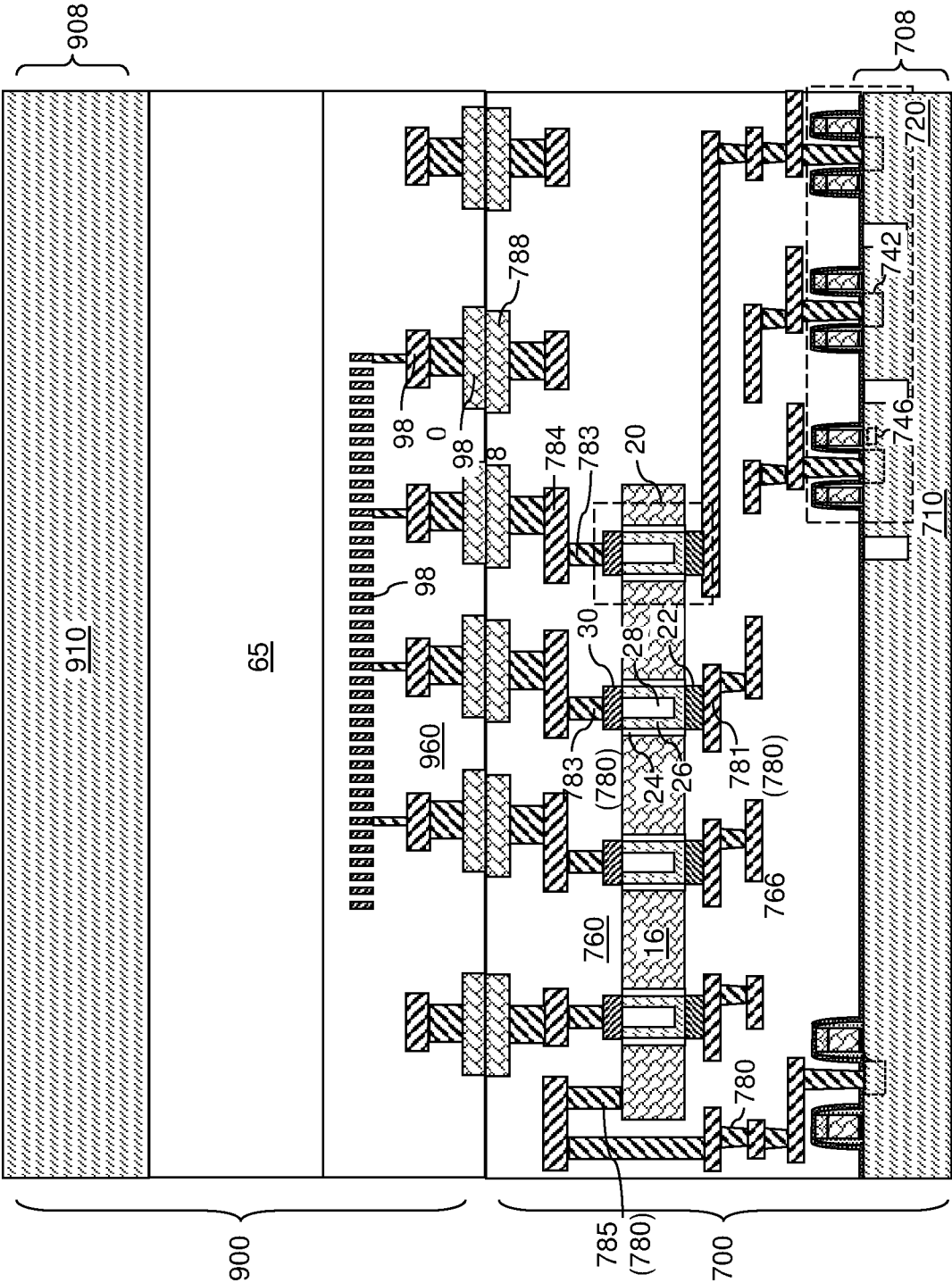


FIG. 5

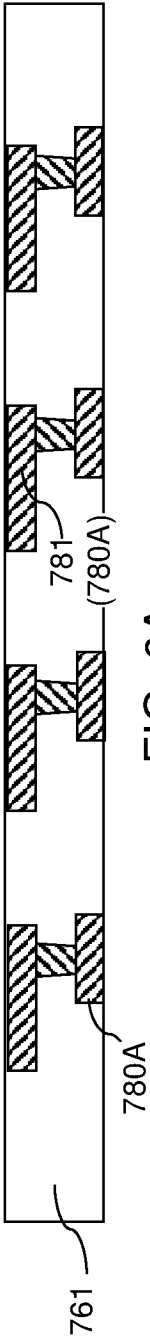


FIG. 6A

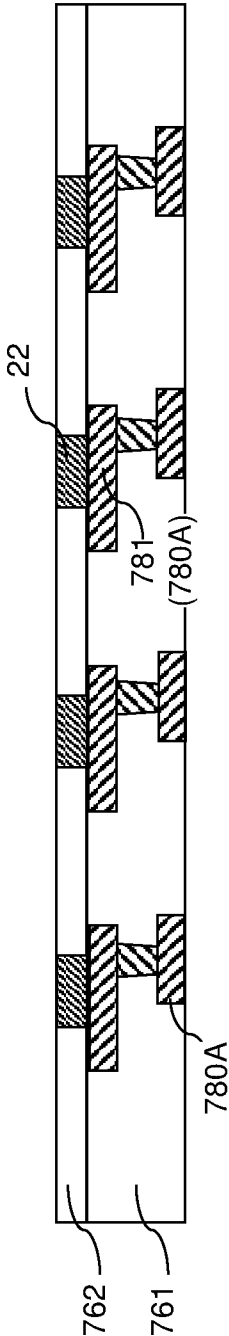


FIG. 6B

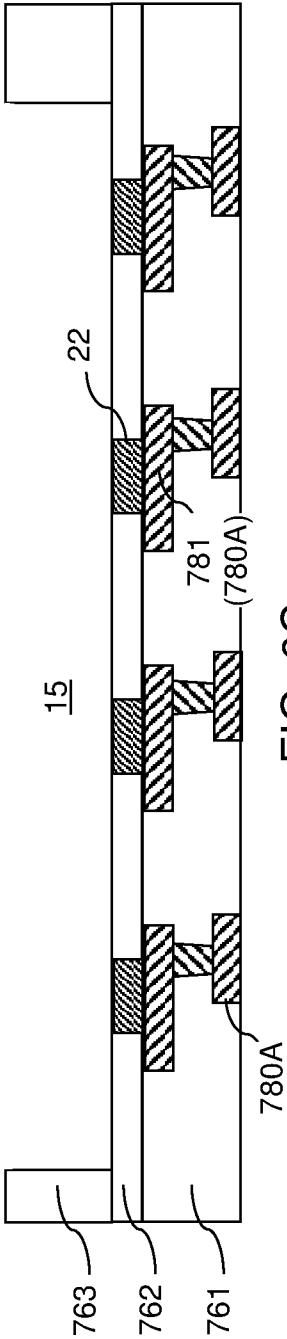


FIG. 6C

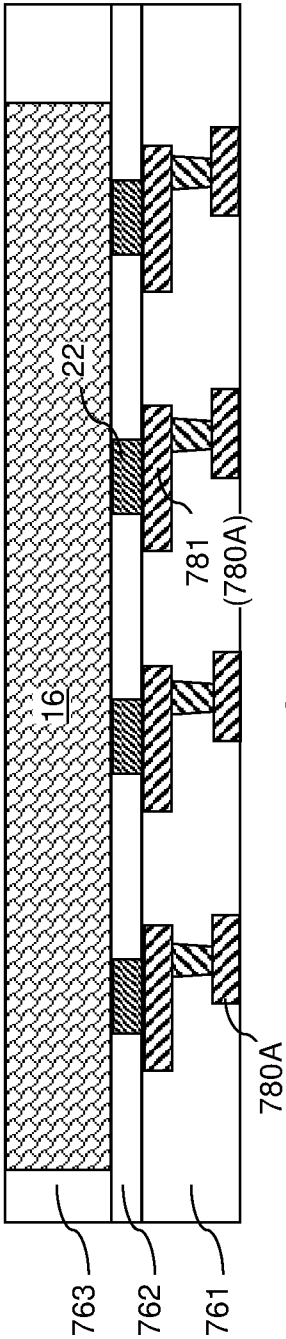
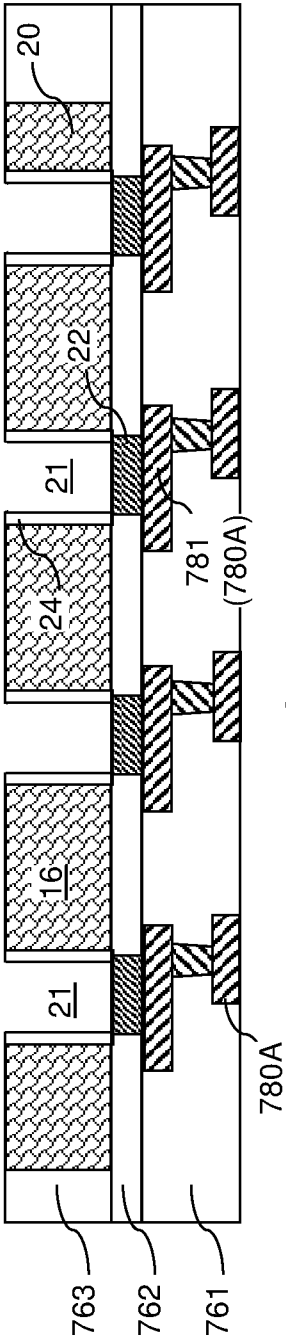
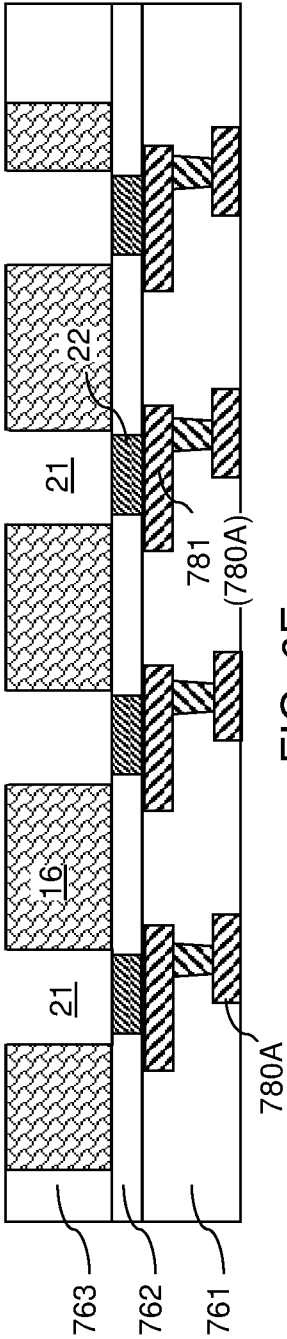


FIG. 6D



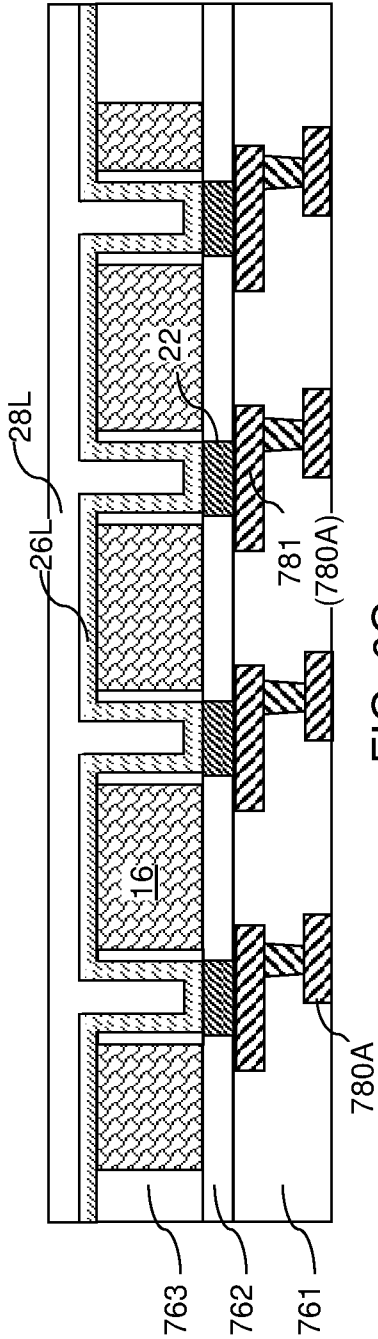


FIG. 6G

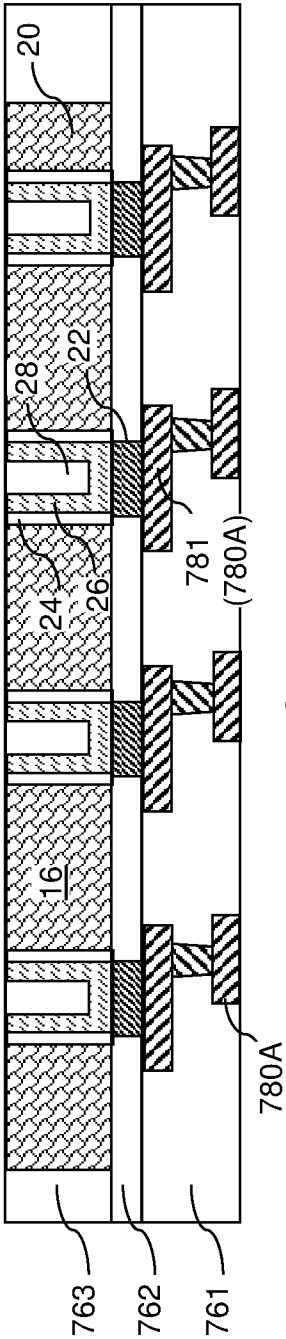
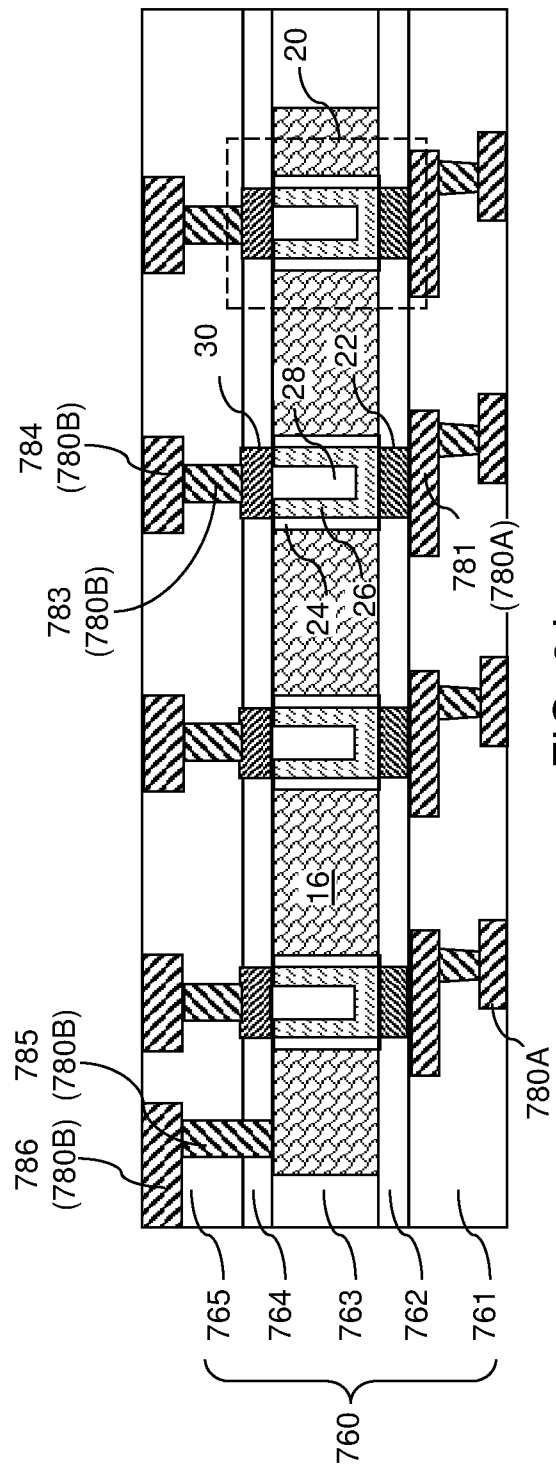
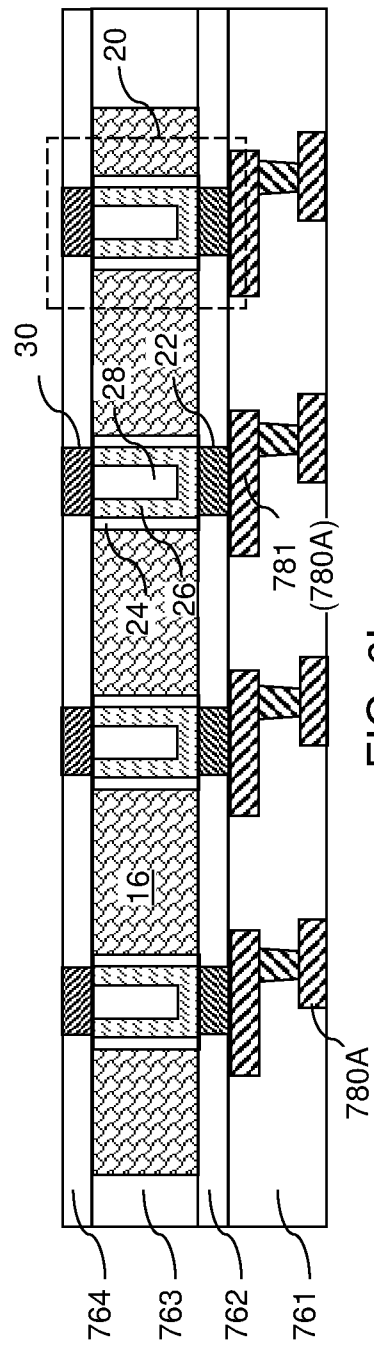


FIG. 6H



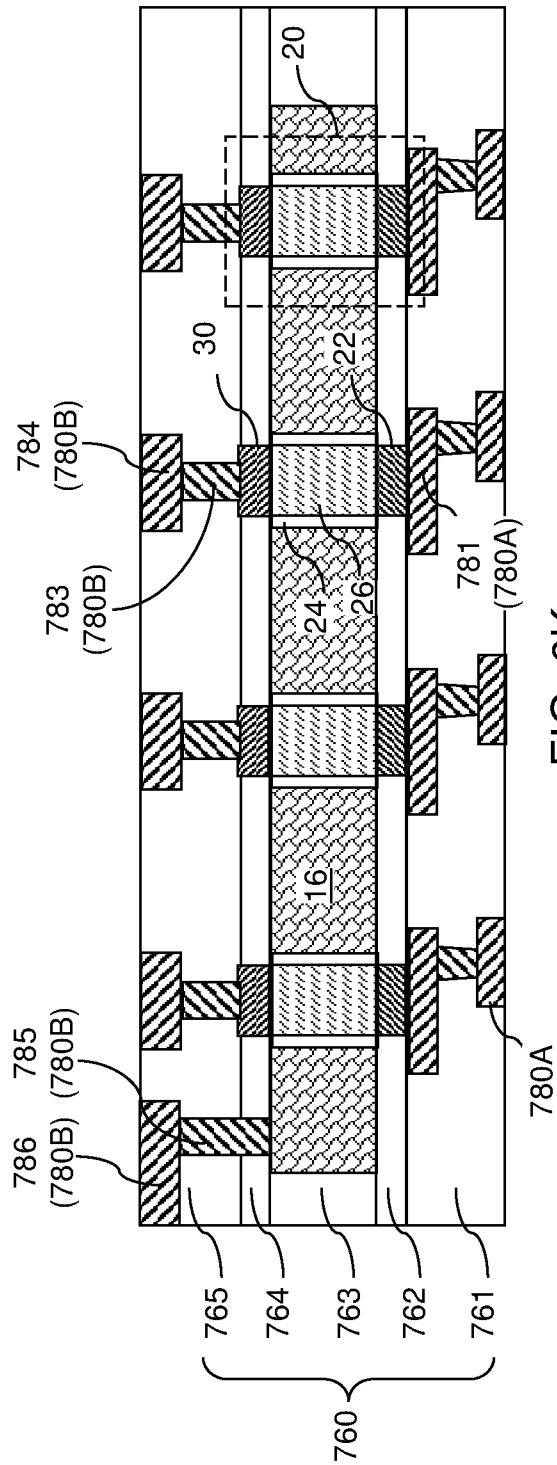


FIG. 6K

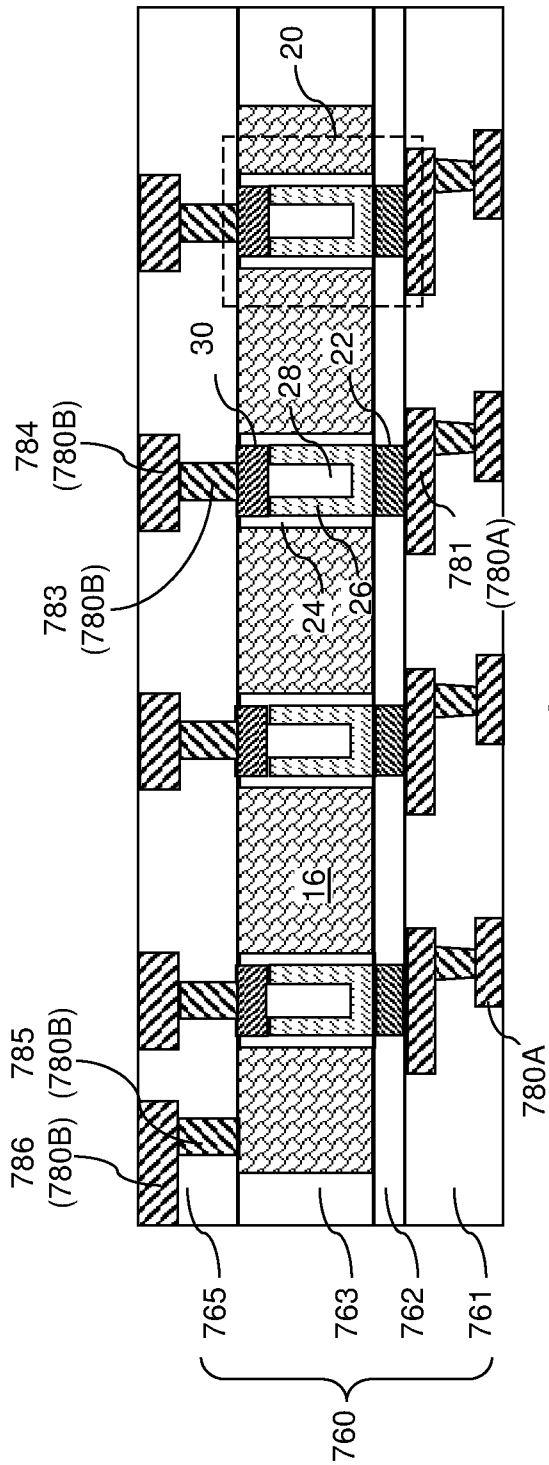


FIG. 6L

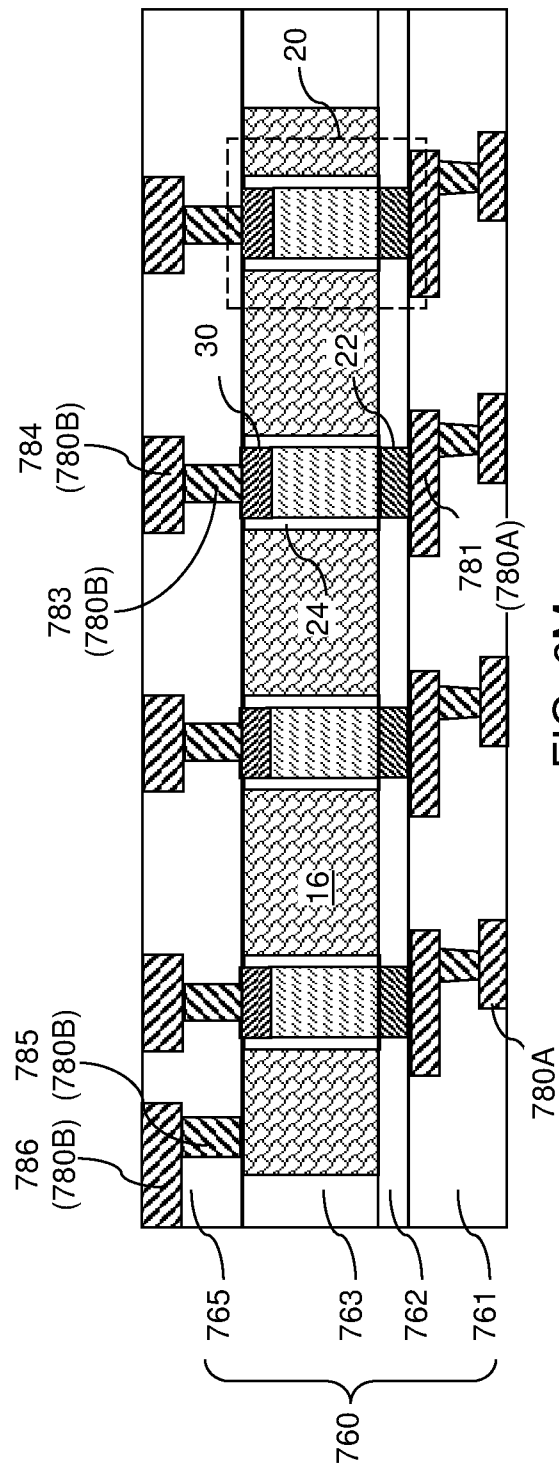


FIG. 6M

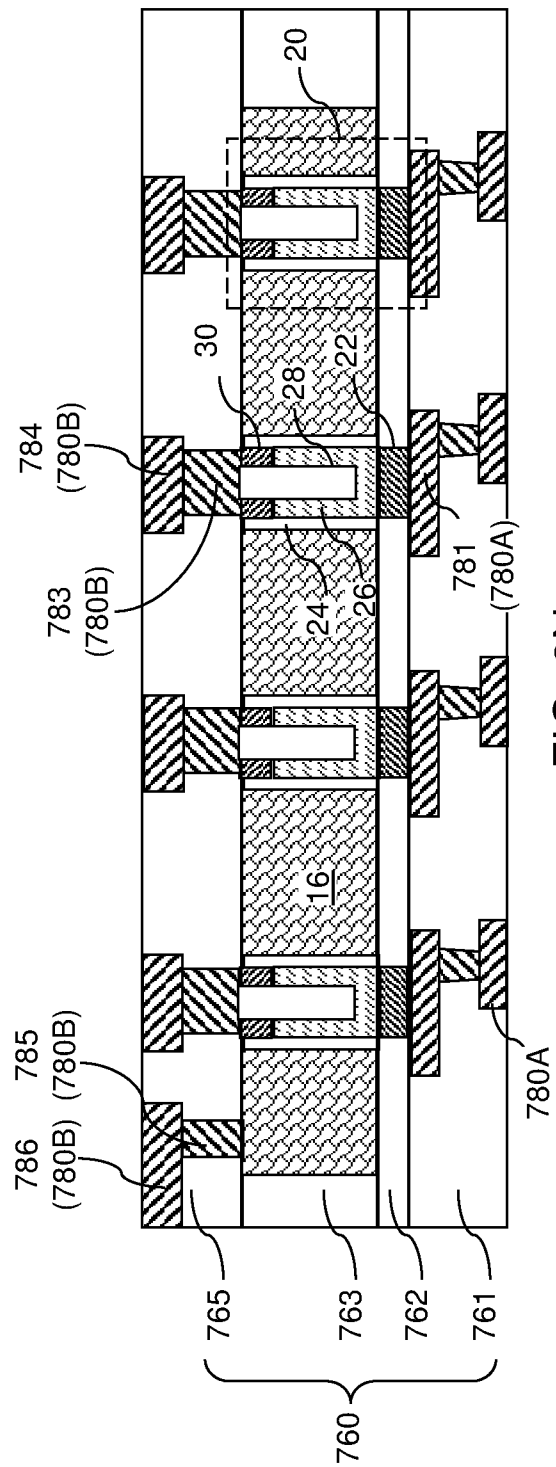


FIG. 6N

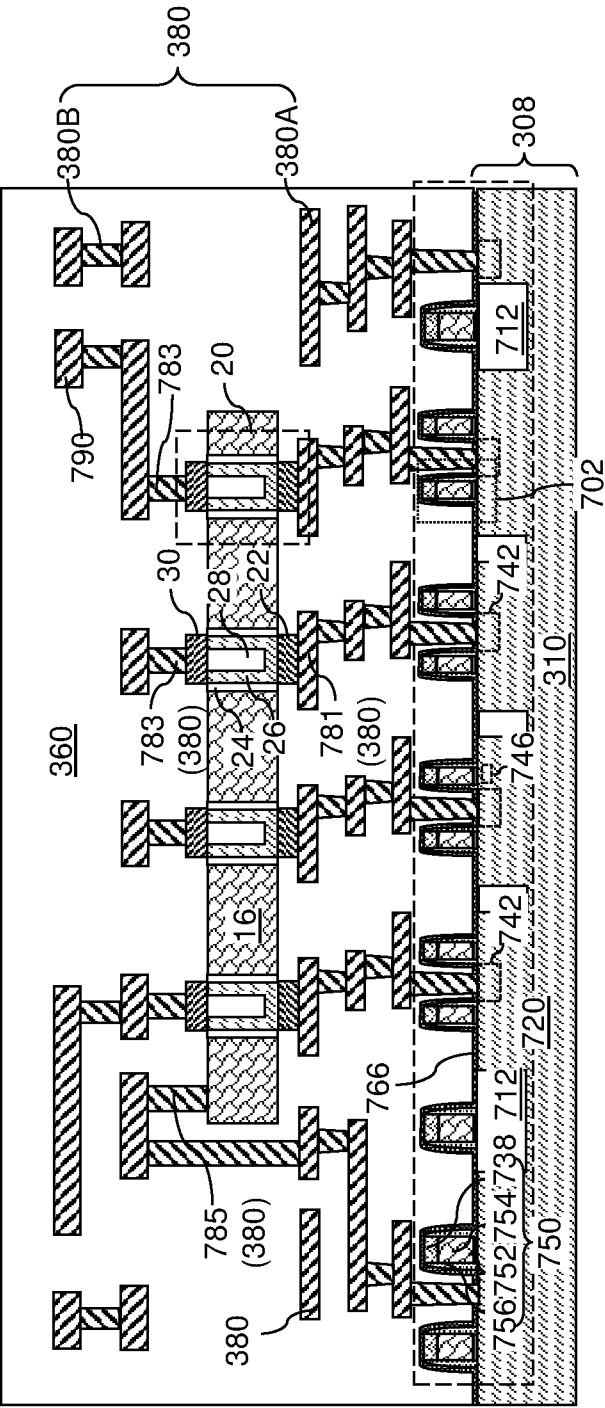


FIG. 7A

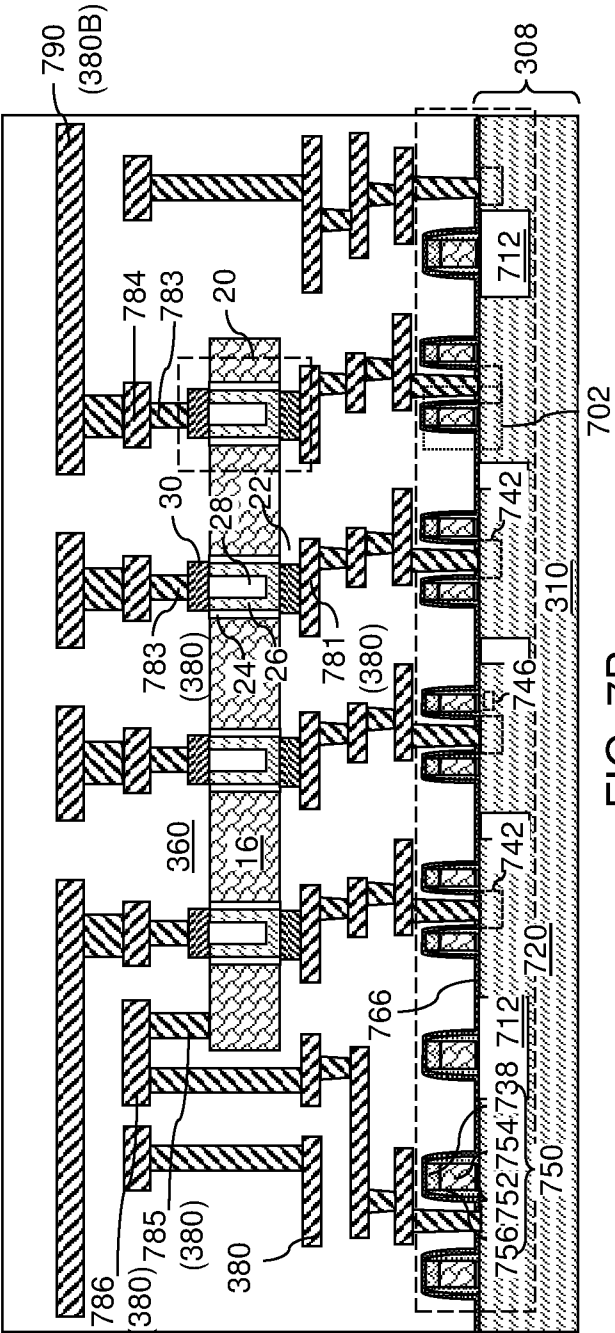


FIG. 7B

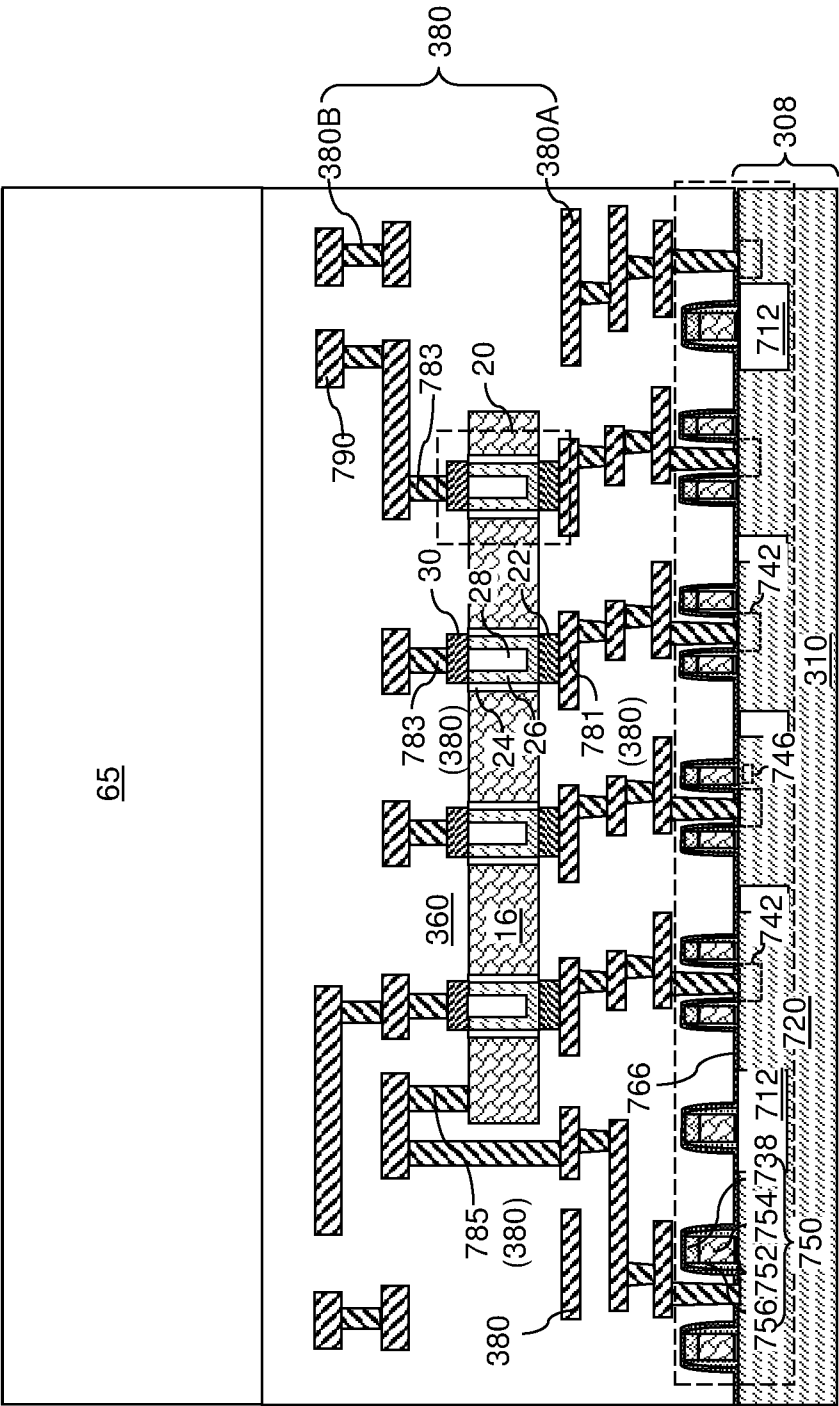


FIG. 8A

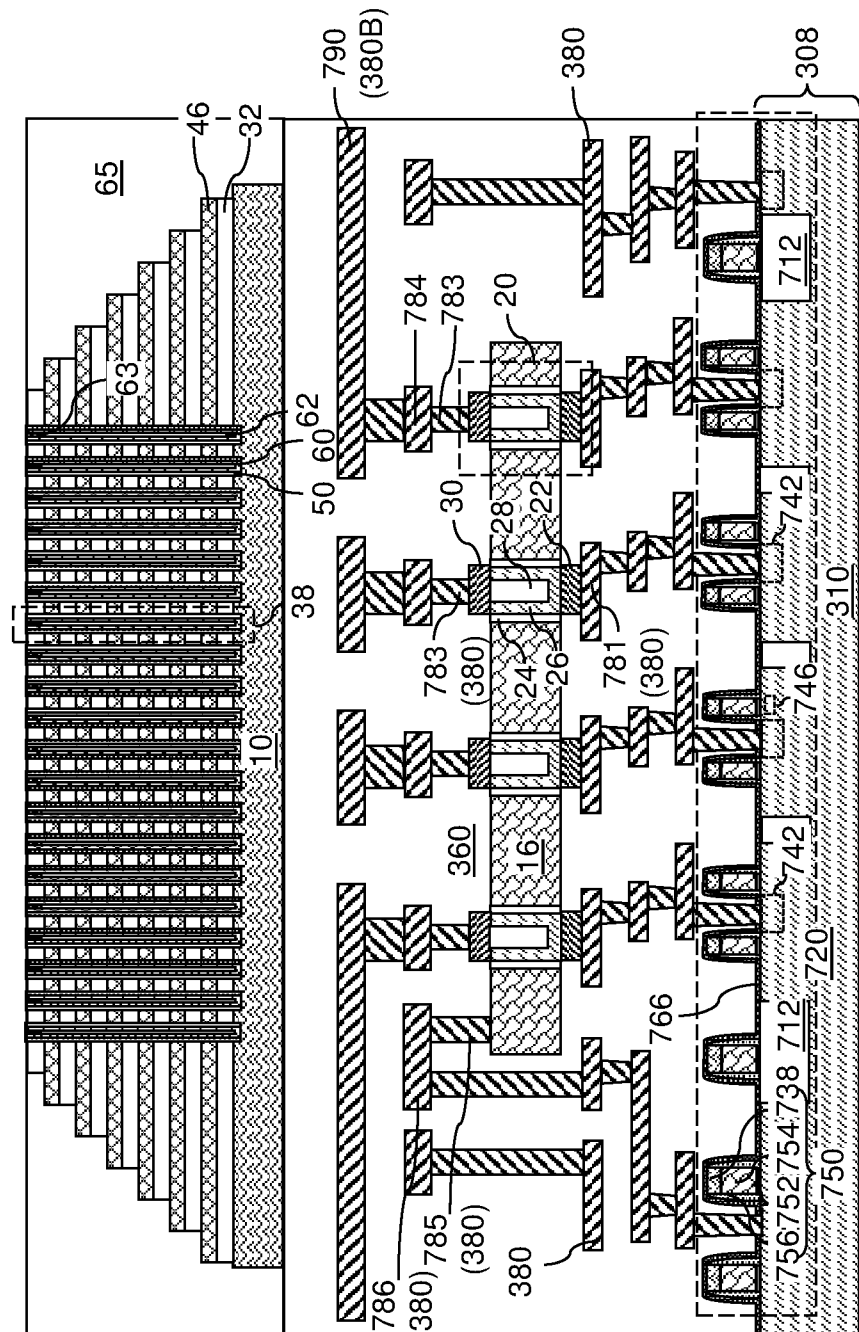


FIG. 8B

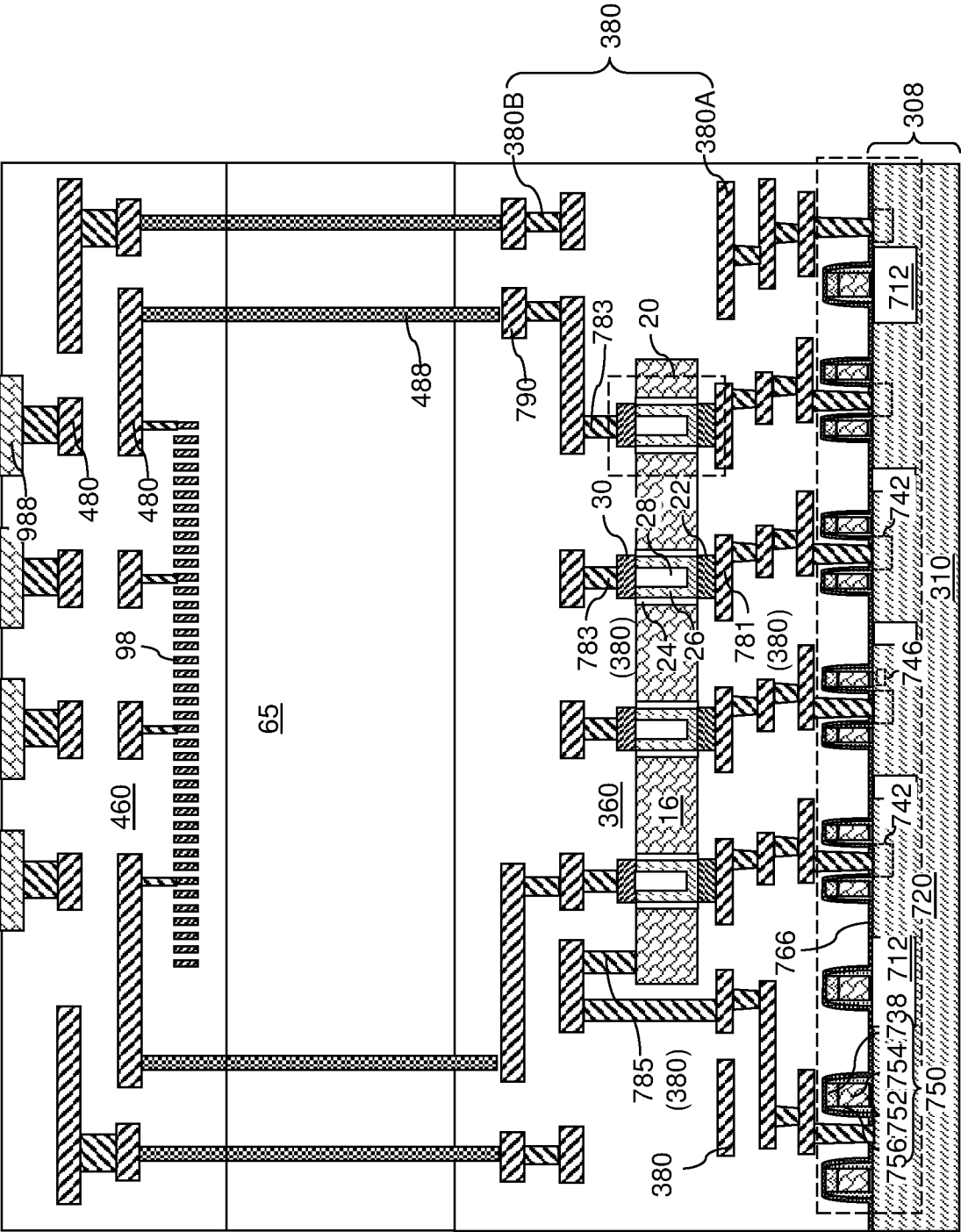


FIG. 9A

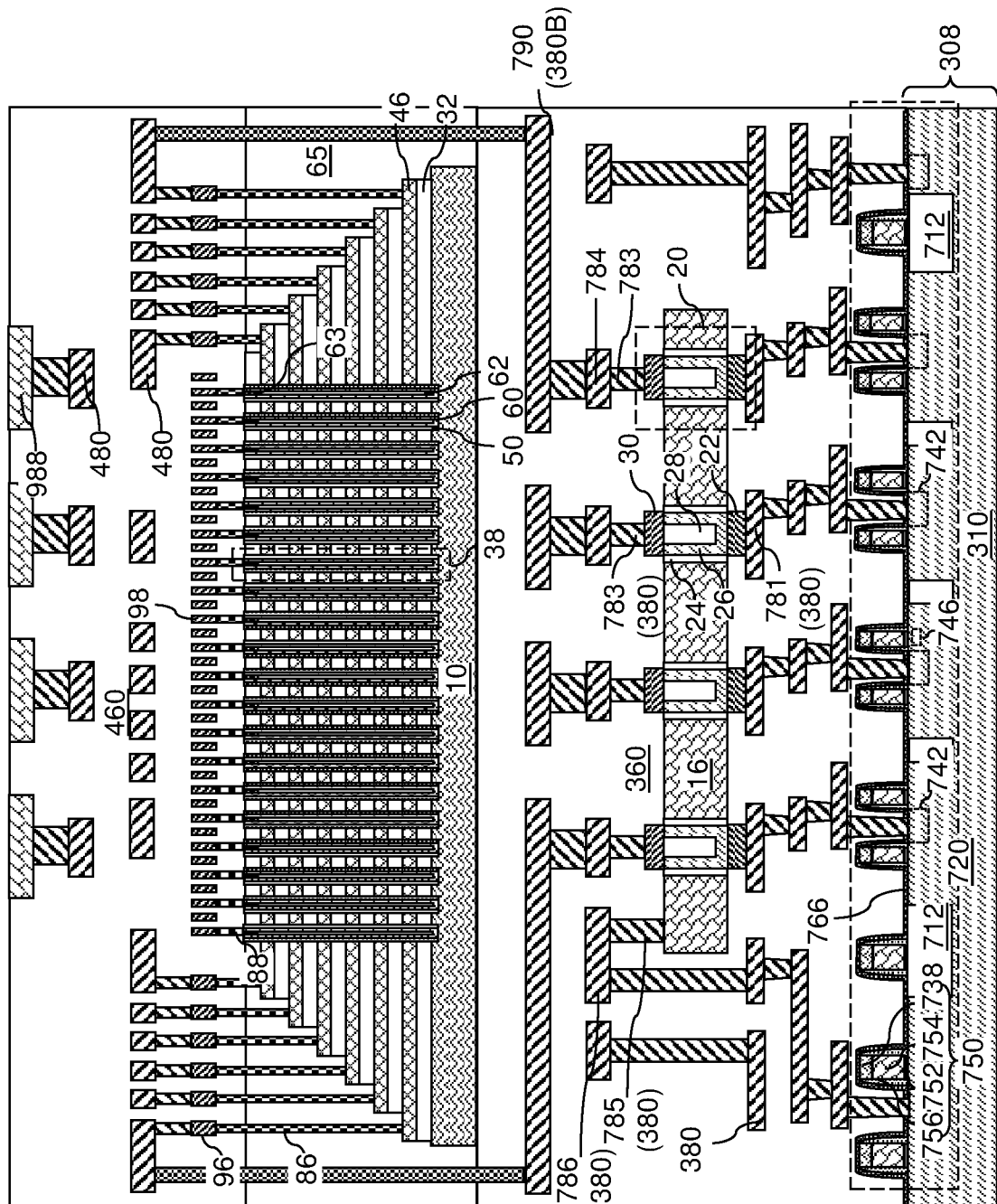


FIG. 9B

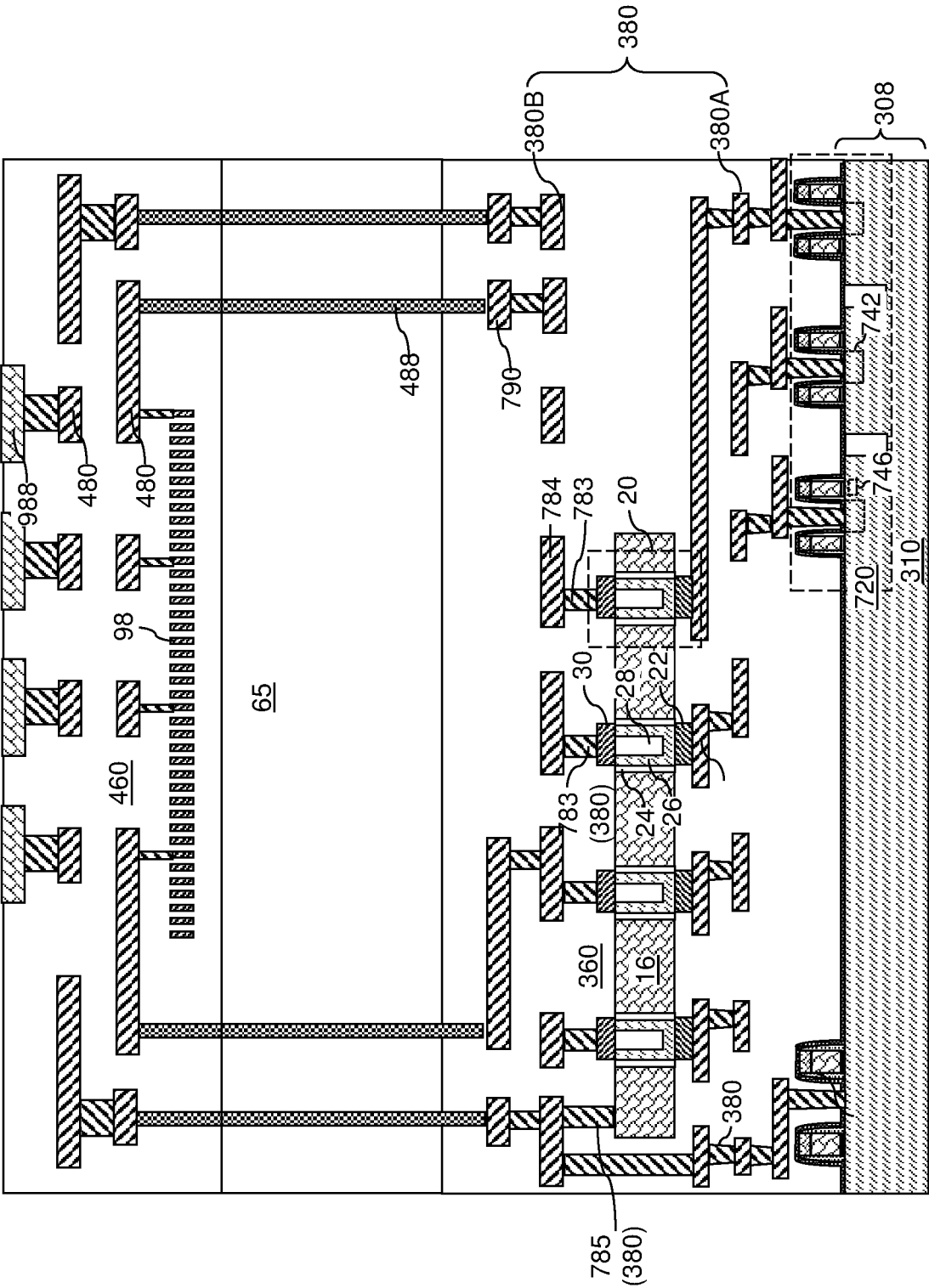


FIG. 10

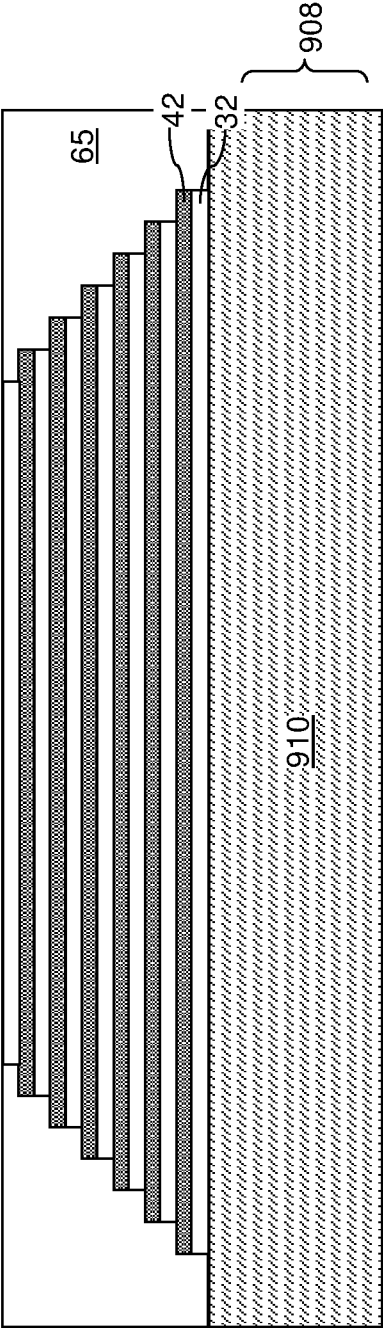


FIG. 11A

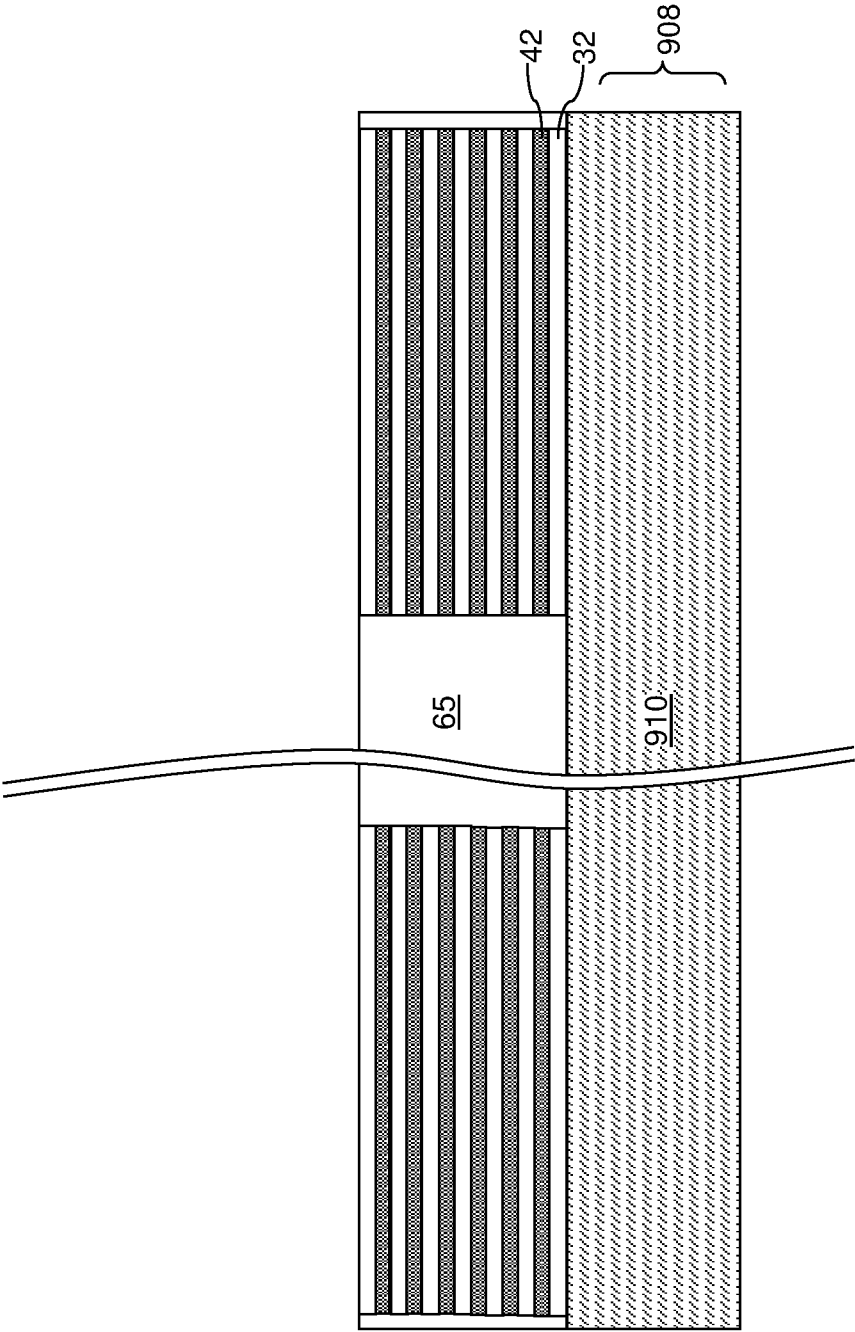


FIG. 11B

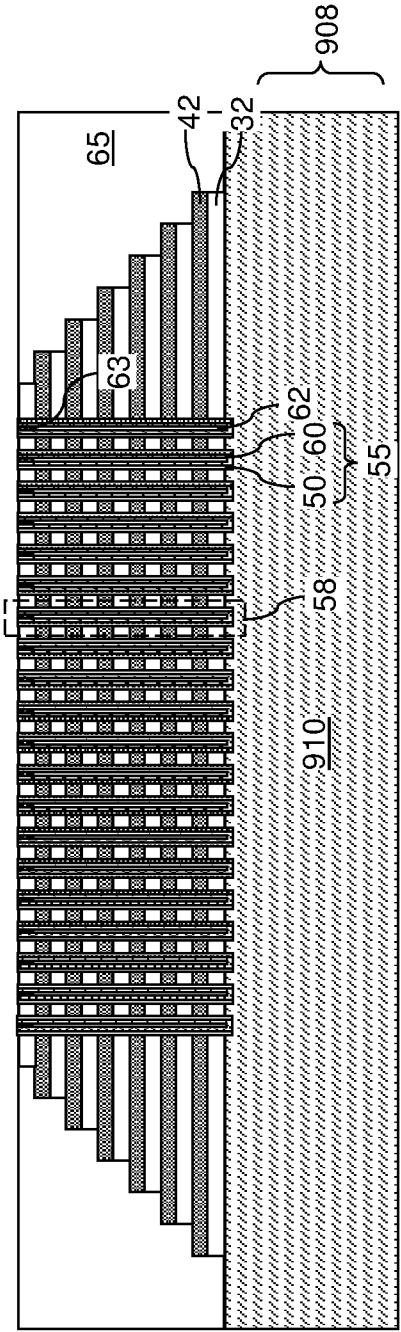


FIG. 12A

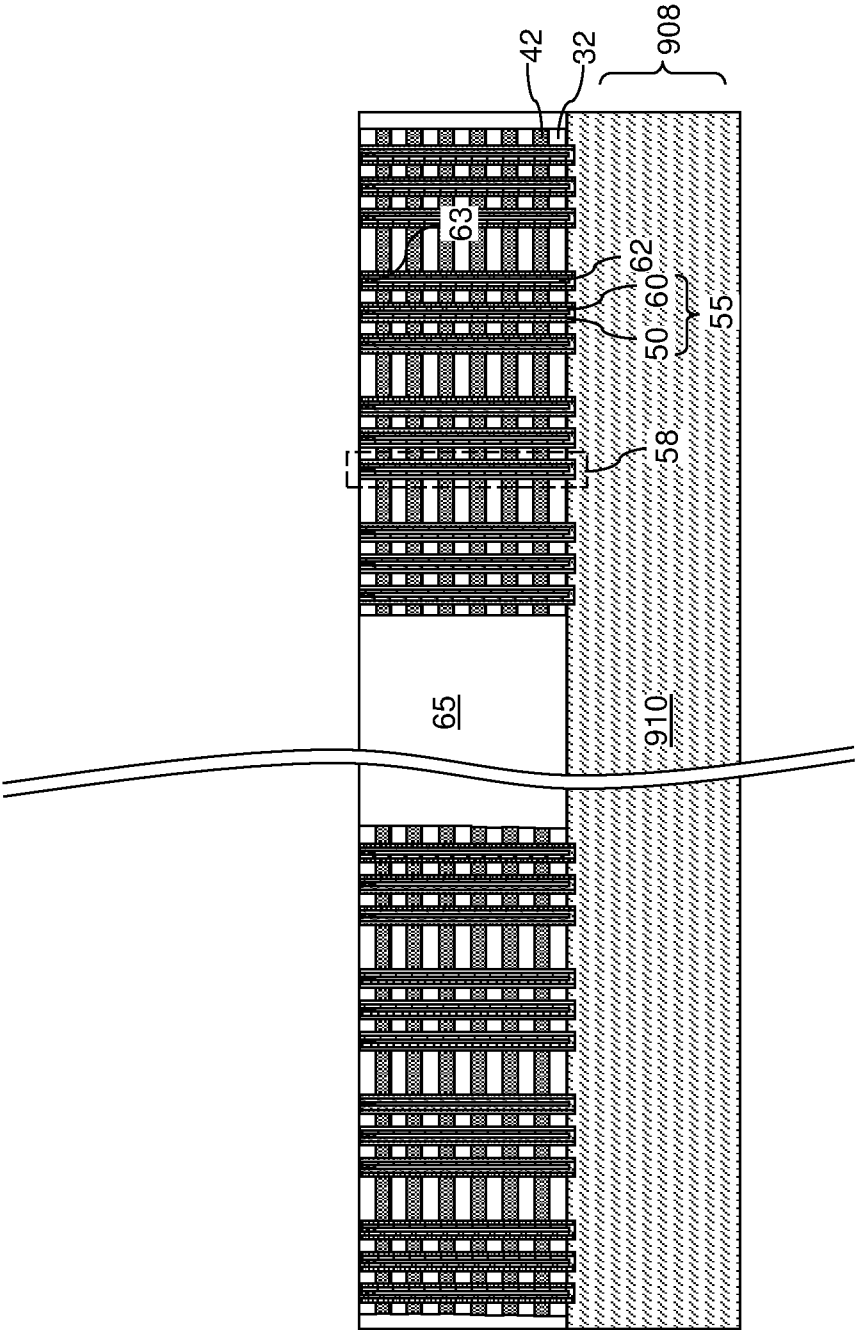


FIG. 12B

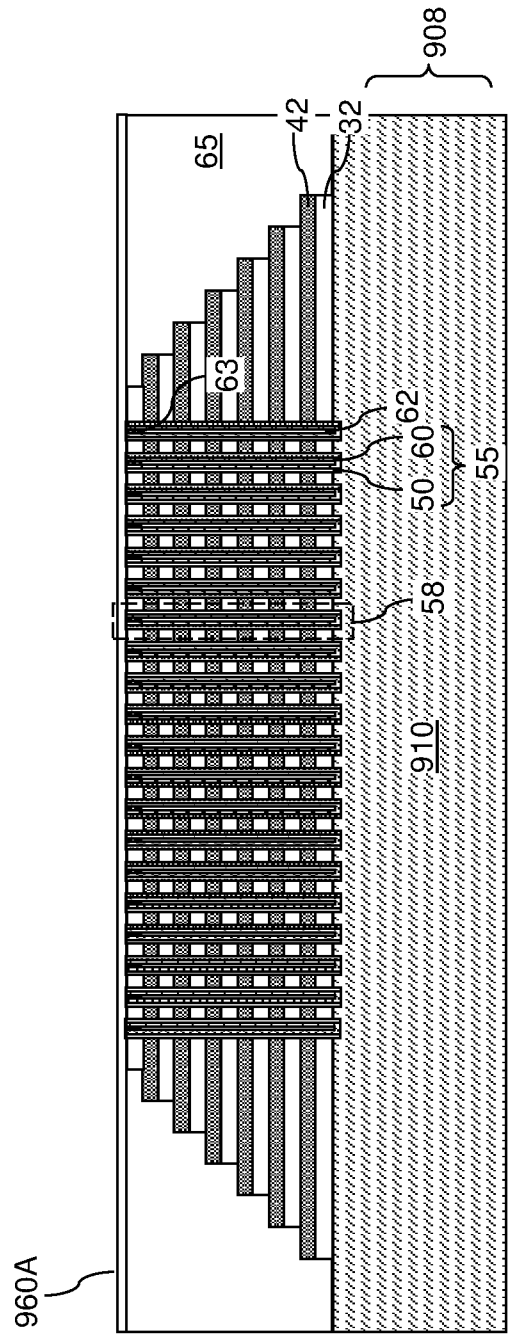


FIG. 13A

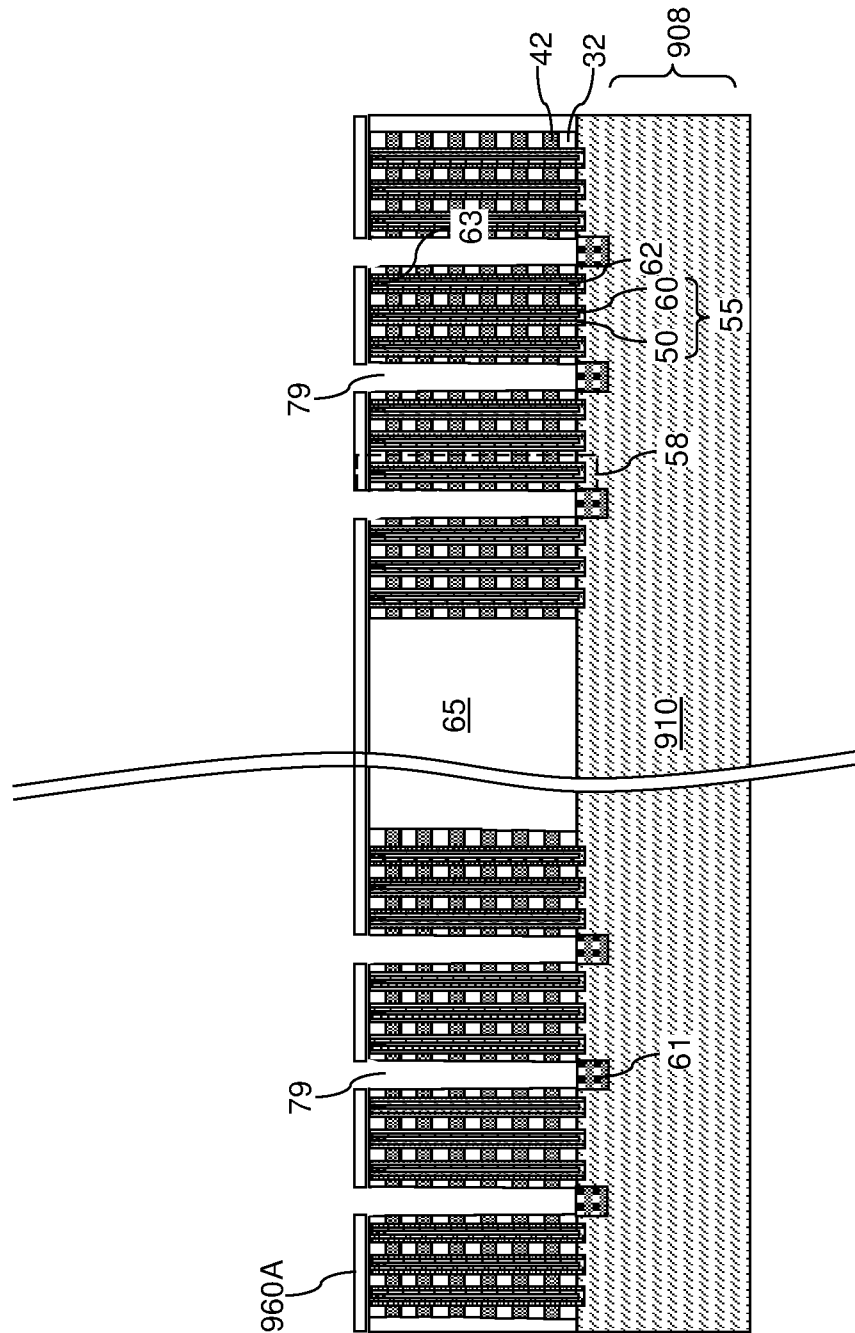


FIG. 13B

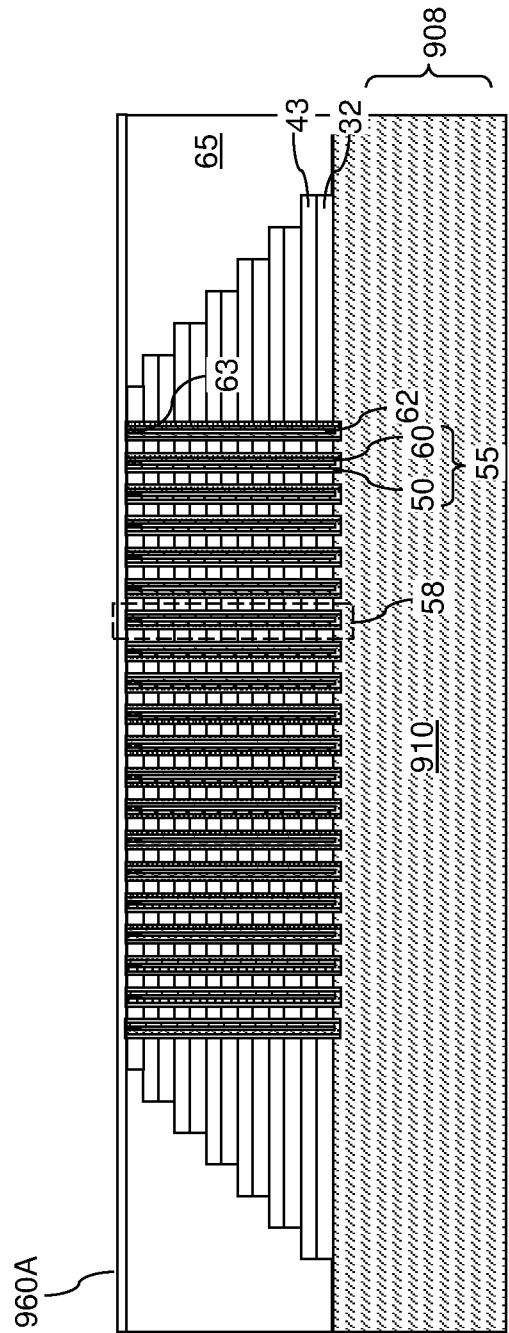


FIG. 14A

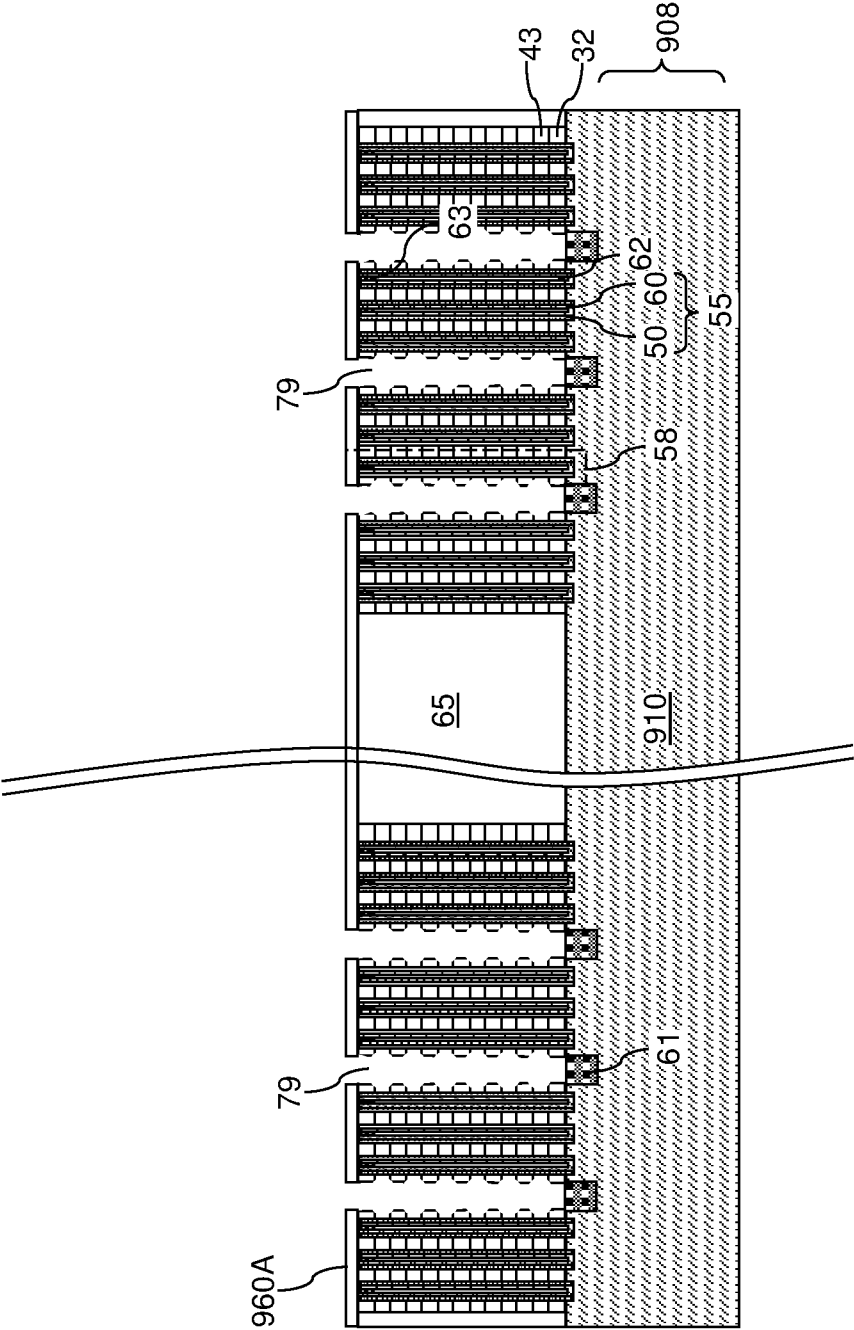


FIG. 14B

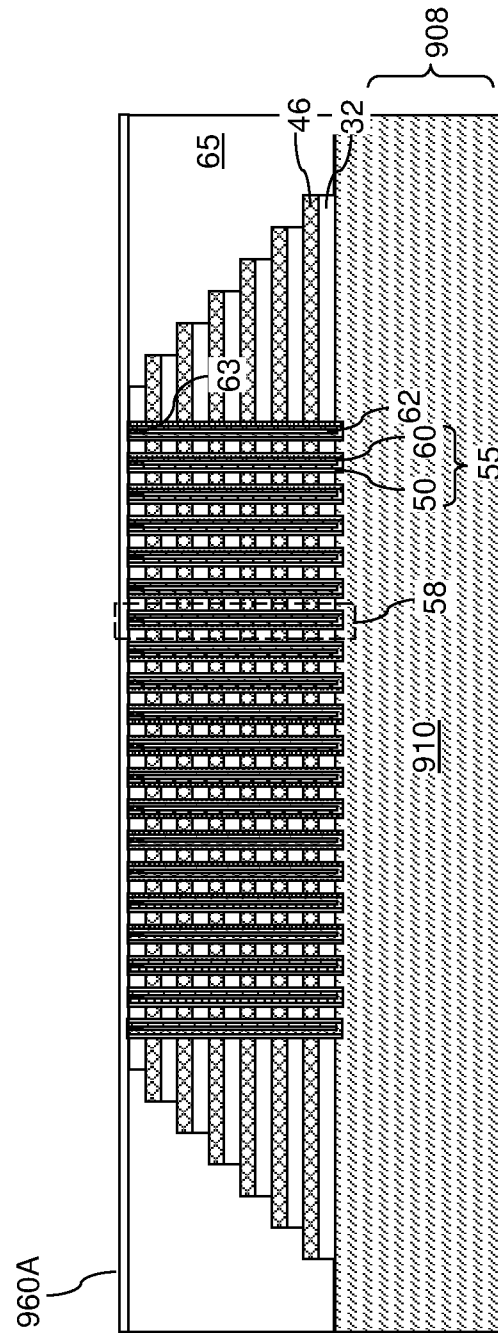


FIG. 15A

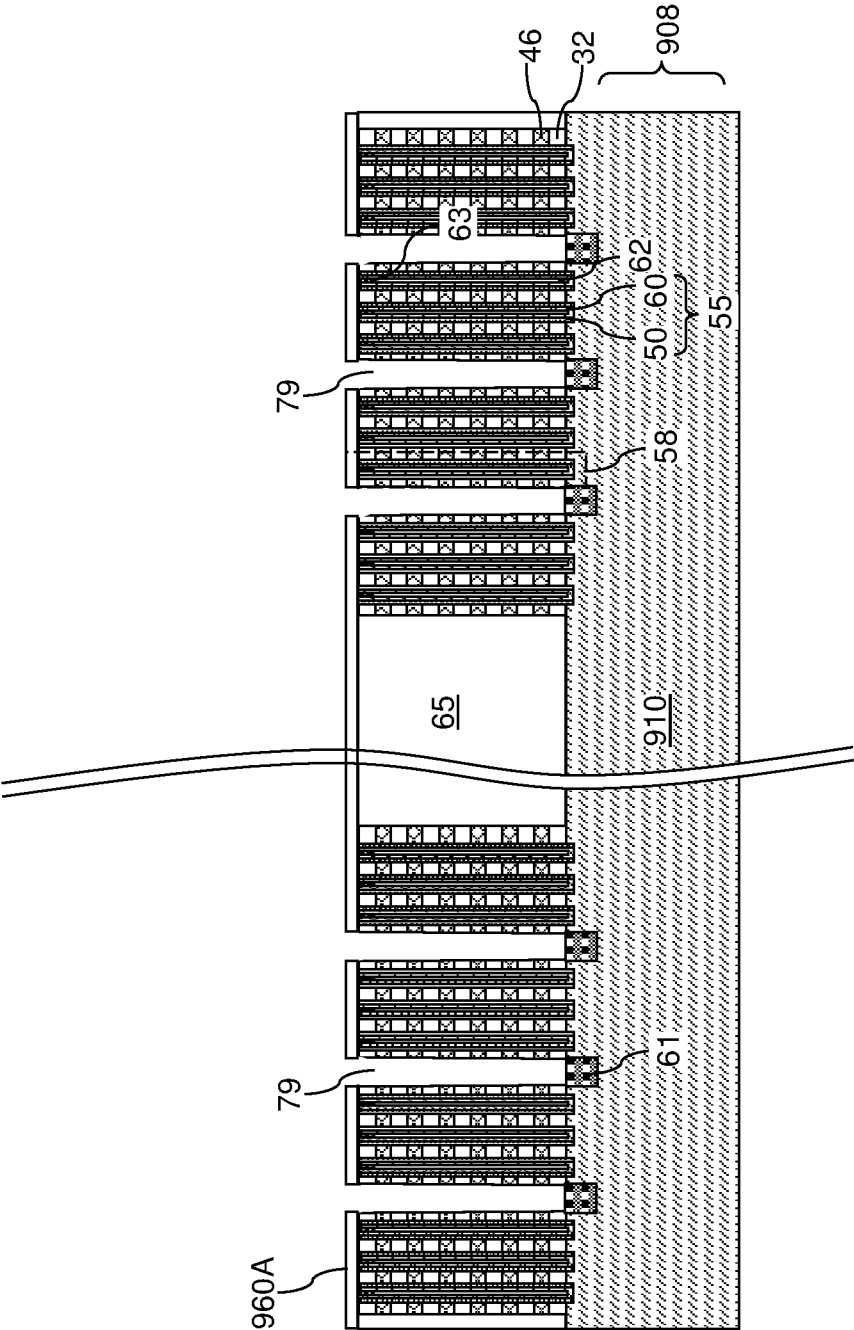


FIG. 15B

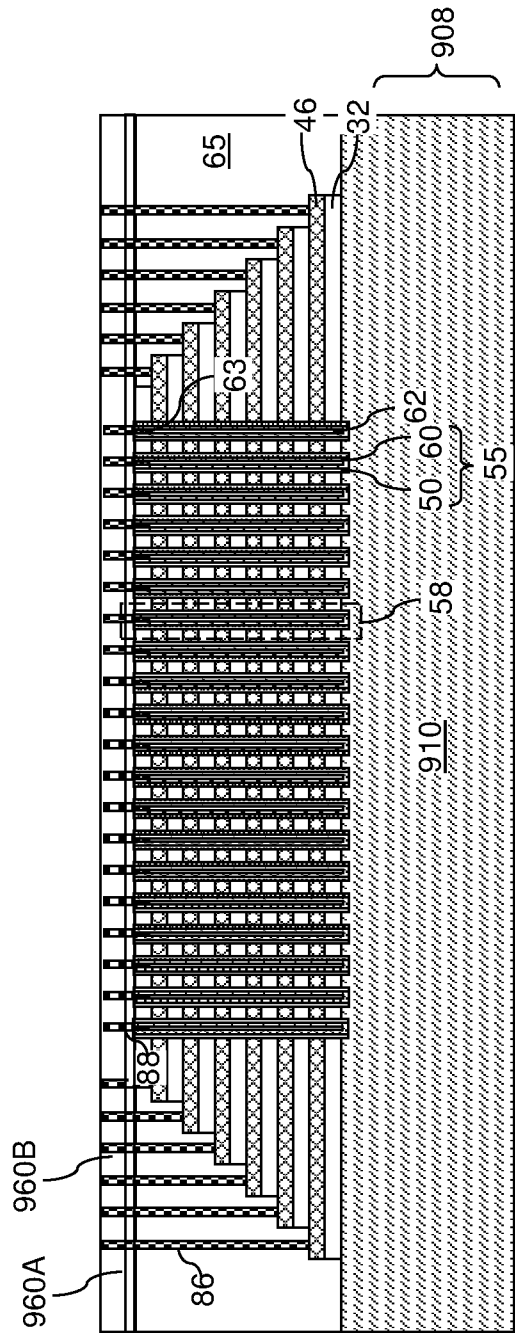


FIG. 16A

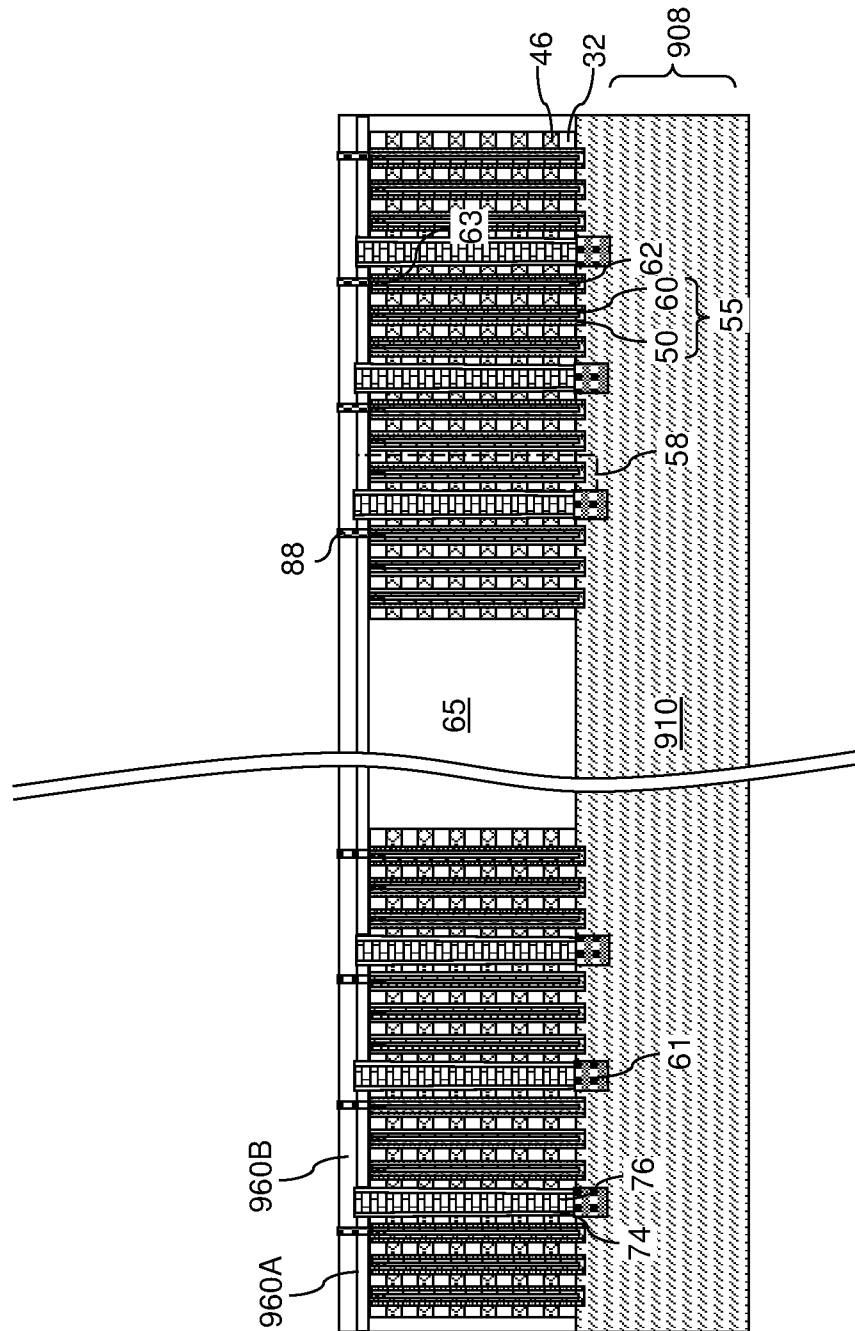


FIG. 16B

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2021/036187

A. CLASSIFICATION OF SUBJECT MATTER		
H01L 25/065(2006.01)i; H01L 27/11551(2017.01)i; H01L 27/11578(2017.01)i; H01L 27/11575(2017.01)i; H01L 27/11573(2017.01)i; H01L 27/1157(2017.01)i; H01L 27/11529(2017.01)i; H01L 27/11548(2017.01)i		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols)		
H01L 25/065(2006.01); G06F 17/50(2006.01); G11C 8/08(2006.01); G11C 8/10(2006.01); H01L 23/00(2006.01); H01L 23/522(2006.01); H01L 23/528(2006.01); H01L 27/1157(2017.01); H01L 27/11582(2017.01)		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Korean utility models and applications for utility models Japanese utility models and applications for utility models		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)		
eKOMPASS(KIPO internal) & Keywords: bonded, three-dimensional, memory, logic, vertical-field-effect-transistor		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2020-0105721 A1 (SAMSUNG ELECTRONICS CO., LTD.) 02 April 2020 (2020-04-02) Paragraphs 9-161; claim 1; and figures 7A-15F.	1-40
Y	WO 2017-142619 A1 (SANDISK TECHNOLOGIES LLC) 24 August 2017 (2017-08-24) Paragraphs 29-123; claims 1-5; and figures 2-14.	1-40
A	US 2015-0370947 A1 (SYNOPSYS, INC.) 24 December 2015 (2015-12-24) Paragraphs 147-151; and figure 13.	1-40
A	WO 2019-182657 A1 (SANDISK TECHNOLOGIES LLC) 26 September 2019 (2019-09-26) The entire document.	1-40
A	US 2018-0366487 A1 (SANDISK TECHNOLOGIES LLC) 20 December 2018 (2018-12-20) The entire document.	1-40
☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.		
* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "D" document cited by the applicant in the international application "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search		Date of mailing of the international search report
28 October 2021		28 October 2021
Name and mailing address of the ISA/KR		Authorized officer
Korean Intellectual Property Office 189 Cheongsa-ro, Seo-gu, Daejeon 35208, Republic of Korea		PARK, Hye Lyun
Facsimile No. +82-42-481-8578		Telephone No. +82-42-481-3463

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/US2021/036187

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
US	2020-0105721	A1	02 April 2020	CN	110970439	A	07 April 2020
				KR	10-2020-0037894	A	10 April 2020
WO	2017-142619	A1	24 August 2017	CN	108475682	A	31 August 2018
				US	9595535	B1	14 March 2017
US	2015-0370947	A1	24 December 2015	CN	106575600	A	19 April 2017
				CN	106575600	B	27 October 2020
				EP	3158576	A1	26 April 2017
				EP	3158576	A4	14 February 2018
				EP	3158576	B1	02 December 2020
				US	10037397	B2	31 July 2018
				US	2016-0335387	A1	17 November 2016
				WO	2015-200343	A1	30 December 2015
WO	2019-182657	A1	26 September 2019	CN	111247636	A	05 June 2020
				EP	3669398	A1	24 June 2020
				KR	10-2020-0037444	A	08 April 2020
				KR	10-2297701	B1	06 September 2021
				US	10354980	B1	16 July 2019
				US	10354987	B1	16 July 2019
US	2018-0366487	A1	20 December 2018	EP	3639300	A1	22 April 2020
				US	10381373	B2	13 August 2019
				WO	2018-231290	A1	20 December 2018