(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
27 December 2013 (27.12.2013)

WIPO | PCT

(10) International Publication Number
WO 2013/189009 A1

(51) International Patent Classification:
G06F 13/28 (2006.01)

(21) International Application Number:
PCT/CN2012/077071

(22) International Filing Date:
18 June 2012 (18.06.2012)

(25) Filing Language: English

(26) Publication Language: English

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *of inventorship (Rule 4.17(iv))*

Published:

— *with international search report (Art. 21(3))*

WO 2013/189009 A1

(54) **Title**: ADAPTIVE OFFSET SYNCHRONIZATION OF DATA BASED ON RING BUFFERS

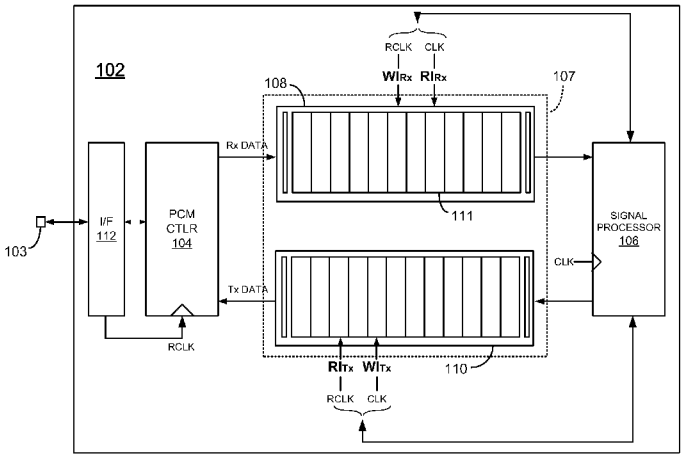

FIG. 1

(57) **Abstract**: A method and apparatus for synchronizing operations between a first circuit and a second circuit is disclosed. The method involves writing receive data from the first circuit to a first ring buffer at a first rate. The first ring buffer has a fixed-length of buffer elements and respective read and write buffer pointers. The buffered receive data is read from the first ring buffer to the second circuit at a second data rate. The respective positions of the read and write buffer pointers are detected, and a relative position between the read and write pointers is dynamically adjusted to enforce at least a predetermined minimum spacing. The dynamic adjustment comprises selectively adding or deleting portions of the data to or from the ring buffer.

ADAPTIVE OFFSET SYNCHRONIZATION OF DATA BASED ON RING BUFFERS

TECHNICAL FIELD

[0001] The present embodiments relate generally to data communications, and more particularly to methods and apparatus that provide flow control for buffering data.

BACKGROUND OF RELATED ART

[0002] Data transfers between circuits often become unsynchronized due to many factors. For example, in voice-over-IP (VOIP) applications, the analog-to-digital codecs (such as a pulse-code-modulation PCM codec) may generate data at a rate different than the rate at which a signal processor can accept it. Buffer circuits typically provide a dynamic way to absorb and handle the ebb and flow of data being communicated between such circuits.

[0003] One typical buffering solution employs ring or circular buffers that have a fixed number of buffer elements. Respective read and write pointers or indices track the available buffer storage capacity. In some circumstances, the buffer may become full, causing an overwrite of the oldest data in the buffer. The indices identify this state by both pointing to the same buffer element location. When data is lost due to overwrites, noise in the system may result.

[0004] To minimize overwrites, large buffer configurations may be employed. The large buffers may be able to handle the various delays in operation between, for example, a PCM controller and a digital signal processor (DSP). Unfortunately, employing large buffers causes a corresponding increase in system latency and circuit space.

SUMMARY

[0005] A method of synchronizing operations between a first circuit and a second circuit is disclosed. The method involves receiving data at a first data rate, and

buffering the data. The buffering is handled by a buffer circuit having a fixed length of buffer elements and respective read and write buffer indicators. The buffered data is delivered to the second circuit at a second data rate. The second data rate is based on a minimum offset enforced between the read and write buffer indicators. Enforcement of the offset is handled by detecting the respective locations of the read and write buffer indicators, and dynamically adjusting a relative spacing between the indicators to maintain at least the minimum offset.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] The present embodiments are illustrated by way of example and are not intended to be limited by the figures of the accompanying drawings, where:

[0007] FIG. 1 is a block diagram of one embodiment of a system that employs a buffer circuit to provide adaptive offset synchronization of data;

[0008] FIG. 2 is a flowchart illustrating steps involved in one mode of operation for the system of Figure 1; and

[0009] FIG. 3 illustrates a flowchart that shows steps involved in a second mode of operation for the system of Figure 1.

DETAILED DESCRIPTION

[0010] In accordance with the present embodiments, a method and apparatus for synchronizing operations between a first circuit and a second circuit is disclosed. The method involves writing receive data from the first circuit to a first ring buffer at a first rate. The buffer has a fixed-length of buffer elements and respective read and write buffer indicators. The buffered receive data is read from the ring buffer to the second circuit at a second data rate. The respective positions of the read and write buffer indicators are detected, and a relative position between the indicators is dynamically adjusted to enforce at least a predetermined minimum spacing. The dynamic adjustment comprises selectively adding or deleting portions of the data to or from the ring buffer. As a result, overwrites to buffered data may be minimized while also optimizing system latency.

[0011] In the following description, numerous specific details are set forth such

as examples of specific components, circuits, and processes to provide a thorough understanding of the present disclosure. Also, in the following description and for purposes of explanation, specific nomenclature is set forth to provide a thorough understanding of the present embodiments. However, it will be apparent to one skilled in the art that these specific details may not be required to practice the present embodiments. In other instances, well-known circuits and devices are shown in block diagram form to avoid obscuring the present disclosure. The term "coupled" as used herein means connected directly to or connected through one or more intervening components or circuits. Any of the signals provided over various buses described herein may be time-multiplexed with other signals and provided over one or more common buses. Additionally, the interconnection between circuit elements or software blocks may be shown as buses or as single signal lines. Each of the buses may alternatively be a single signal line, and each of the single signal lines may alternatively be buses, and a single line or bus might represent any one or more of a myriad of physical or logical mechanisms for communication between components. The present embodiments are not to be construed as limited to specific examples described herein but rather to include within their scopes all embodiments defined by the appended claims.

[0012] More specifically, and referring generally to Figure 1, an integrated circuit (IC) device 102 for carrying out signal processing operations is shown. In one specific embodiment, the signal processing involves Voice-Over-Internet-Protocol (VOIP) communications. VOIP communications generally involve capturing analog audio signals, digitizing and encoding the audio signals, and processing the digitized audio in a manner suitable for transmission via the Internet. A conversation via VOIP thus involves bidirectional communication between two remote points, and the round-trip latency associated with the communications. In one specific embodiment, to carry out VOIP processing, the IC device 102 employs a pulse code modulation (PCM) controller 104 that interacts with a signal processor 106 such as a digital signal processor (DSP) via a buffer circuit 107.

[0013] Further referring to Figure 1, in one specific embodiment, the integrated circuit device 102 receives audio data at one or more pins 103 which are coupled to a dataI/O interface circuit 112. The interface circuit 112 generally includes transmit and receive circuitry (not shown) that allows the IC device 102 to interface with various physical transmission media. While only one pin 103 is shown for purposes of clarity,

it should be understood that plural interface pins may be employed to transfer data in a parallel or serial scheme. In one embodiment, timing information accompanies the received audio data to form a timing reference in the form of a recovered clock signal RCLK. Further, while a wired data interface for the IC is shown and described, a wireless interface may also be employed, and in such circumstances, the interface would include appropriate RF modulation circuitry and associates antenna circuitry.

[0014] The interface 112 couples to the PCM controller 104 to effect an analog-to-digital conversion of received audio signals, and digital-to-analog conversion of signals processed by and transmitted from the signal processor 106. A PCM controller is but one way of encoding the audio signals, and a variety of different encoding algorithms may be employed. Respective analog-to-digital (ADC) and digital-to-analog (DAC) converters (not shown) carry out the signal conversion as is well-known to those skilled in the art. The PCM controller 104 generally operates at a consistent data rate with respect to the recovered clock signal RCLK and carries out analog-digital and digital-analog conversions of receive Rx and transmit Tx data transferred via the interface 112. While the PCM controller 104 is shown and described as disposed on the IC device 102, it may reside on a separate IC device and packaged together or separate from the signal processor 106.

[0015] The signal processor 106 may take one of several forms, including a dedicated digital signal processor (DSP) or host-based soft-DSP. The signal processor 106 may be clocked by a local clock signal CLK generated by an on-chip clock (not shown) and operates at a rate similar to that of the PCM controller 104. However, due to occasional priority conflicts, the signal processor 106 may not be able to synchronize with the PCM controller 104.

[0016] Further referring to Figure 1, the buffer circuit 107 is disposed between the PCM controller 104 and the signal processor 106 to handle mismatches in data rates there between. In one embodiment, the buffer circuit 107 includes respective receive and transmit buffers 108 and 110 that take the form of ring buffers. Each ring buffer may include a fixed number of buffer storage cells 111 and respective read and write indices or pointers. The receive buffer 108 thus employs a receive read pointer RIR_x and a receive write pointer WIR_x, and the transmit buffer 110 employs a transmit read pointer RIT_x and a transmit write pointer WIT_x.

[0017] For the receive buffer 108, the receive read pointer RIR_x indicates through its pointer position how much data has been delivered to the signal processor 106. This indication of position may take the form of a count that represents the address of a buffer storage cell 111 that will be read in the next read operation. In one embodiment, the receive read pointer RIR_x responds to the local clock signal CLK as its timing reference for read operations. In other words, the receive read pointer RIR_x increments to its next cell location for reading the contents of that cell every clock cycle, using the local clock CLK as its timing reference.

[0018] The receive write pointer WIR_x for the receive buffer 108, on the other hand, utilizes the recovered clock signal RCLK as its timing signal, and indicates through a count value similar to the receive read pointer RIR_x how much data has been loaded into the receive buffer 108. When the read and write pointers indicate respective positions at the same receive buffer storage cell, the amount of data written into the buffer matches the amount of data read from the buffer, thus indicating a full buffer. As a result, any further write operations without further buffer capacity will overwrite existing data.

[0019] The timing references for clocking the read and write indices of the receive and transmit buffers 108 and 110 are configured between the recovered and local clocks RCLK and CLK in a manner that maximizes data quality and synchronization between the PCM controller 104 and the signal processor 106. To this end, the receive write pointer WIR_x for the receive buffer 108 and the transmit read pointer RIT_x for the transmit buffer 110 are clocked by the recovered clock RCLK, while the receive read pointer RIR_x for the receive buffer 108 and the transmit write pointer WIT_x for the transmit buffer 110 are clocked by the local clock CLK.

[0020] In an effort to avoid overwrites and yet minimize the buffer size and latency, in one embodiment the signal processor 106 operates in a mode that monitors and detects the relative spacing between the read and write pointers of each ring buffer. Based on the detecting, the signal processor 106 enforces a minimum spacing between the read and write pointers to minimize occurrences where the buffer overwrites existing data. The “spacing” thus represents the number of read/write cycles worth of asynchronous operation that can be absorbed by the buffer circuit 107 before overwrites occur.

[0021] The signal processor 106 also operates in a second mode that detects undesirable latency between the PCM controller 104 and the signal processor 106 that may significantly impact the quality of service between audio transmissions. In response, the signal processor 106 adaptively adjusts the spacing between the transmit buffer read and write pointers RIT_x and WIT_x to match the latency of the signal processor 106. This is carried out even if data may be lost through the adjustment. Thus, not only are overwrites may be avoided, but an optimum level of synchronization between the PCM controller 104 and the signal processor 106 may be attained.

[0022] FIG. 2 illustrates a flowchart of steps that sets out a method of operation corresponding to the first mode of operation alluded to above. During a VOIP communication, audio data is received by the IC device 102 at the interface 112 and fed to the PCM controller 104 for PCM encoding at the rate corresponding to the clock signal RCLK recovered from the received audio data, at step 202. The PCM encoded data is then written into the receive buffer 108 at positions indicated by the receive write pointer WIRx at a rate dictated by the recovered clock RCLK, at step 204. Previously written buffered data is then read from the receive buffer 108 into the signal processor 106 at the local clock rate CLK, at step 206. The signal processor 106 enforces a minimum spacing between the write and read pointers by first determining whether the pointers in-fact exhibit the minimum spacing (through a comparison of the write and read pointer counts, or the like), at step 208. If the counts reflect a proper minimum spacing, then further data is cycled through the buffer, beginning with step 202. However, if the counts reflect a smaller offset than the desired threshold, the pointers are adjusted in relation to each other to achieve the offset, at step 210. At this point, the method may iterate back to the data receive step at 202, or engage in a further mode (via bubble "A") that addresses latency between the PCM controller 104 and the signal processor 106.

[0023] Referring now to Figure 3, undesirable latency between the PCM controller 104 and the signal processor 106 may be compensated by detecting the latency or delay in operations between the circuits, at 302, and determining whether a latency threshold is exceeded, at step 304. Extreme latencies may cause significant quality issues over and above periodic lost data problems caused, for example, by buffer overwrites. If the latency threshold is within limits, then operation resumes with the data receive step 202 of Figure 2 (via bubble "B").

[0024] However, if the latency threshold is exceeded, at step 304, the relative position of the transmit buffer read and write pointers is adaptively adjusted to match the processor latency, at step 306. In one embodiment this is carried out by adjusting the position of the transmit write pointer WIT_x in an iterative manner until the latency falls within limits. In some instances, this may cause a temporary data loss of the data residing in the buffer cell location(s) eliminated due to the adaptive adjustment of the transmit write pointer WIT_x. While losing data is contrary to conventional wisdom, this has been determined to be more beneficial for optimal quality of service than keeping the data and tolerating the latency.

[0025] Those skilled in the art will appreciate the benefits and advantages afforded by the embodiments described herein. By providing a first mode of operation capable of enforcing a minimal read and write pointer offset, loss of data due to buffer overwrites may be minimized. By also providing a second mode of operation to adaptively adjust transmit pointers based on latency considerations, an optimal quality of service may be attained.

[0026] In the foregoing specification, the present embodiments have been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the disclosure as set forth in the appended claims. For example, much of the description provided herein relates to audio data synchronization in a VOIP context. However, a variety of applications may benefit from the teachings herein, including video-based data applications, basic networking data transfer applications, and the like. The specification and drawings are, accordingly, to be regarded in an illustrative sense rather than a restrictive sense.

CLAIMS

What is claimed is:

1. A method of synchronizing operations between a first circuit and a second circuit, the method comprising:

writing data from the first circuit to a first ring buffer at a first rate, the first ring buffer having a fixed-length of buffer elements and respective read and write buffer indicators;

reading the buffered data from the first ring buffer to the second circuit at a second data rate;

detecting the respective positions of the read and write buffer indicators; and

dynamically adjusting a relative position between the indicators to enforce at least a predetermined minimum spacing, wherein the dynamically adjusting comprises selectively adding or deleting portions of the data to or from the first ring buffer.

2. The method of claim 1 further comprising:

writing transmit data from the second circuit to a second ring buffer at the second data rate, the second ring buffer having respective write and read pointers;

reading the buffered transmit data from the second ring buffer to the first circuit at the first data rate; and

adaptively adjusting the positions of the second ring buffer read and write pointers based on a delay parameter.

3. The method of claim 2, wherein the delay parameter comprises a latency in operation of the second circuit with respect to the first circuit, and adaptively adjusting comprises adaptively adjusting the relative position between the second ring buffer read and write pointers to match the latency.

4. The method of claim 3 wherein the write pointer for the second ring buffer is responsive to a first timing reference associated with the second circuit, and the read pointer of the second ring buffer is responsive to a second timing reference associated with the first circuit.

5. The method of claim 4 wherein a phase difference between the first and second timing references corresponds to the latency.

6. The method of claim4, wherein the first timing reference comprises a clock recovered with data received by the first circuit, and the second timing reference comprises a local clock that clocks the second circuit.

7. A method of synchronizing operations between an audio codec circuit associated with a first timing reference and a signal processor associated with a second timing reference, the method comprising:

in a first mode, enforcing a minimum timing offset between write and read pointers of respective receive and transmit buffer circuits, the receive and transmit buffer circuits disposed between respective receive and transmit paths between the audio codec circuit and the signal processor; and

in a second mode, adaptively adjusting a timing offset between the read and write pointers of the transmit buffer circuit to match a latency exhibited by the signal processor with respect to the audio codec circuit.

8. The method of claim 7, wherein the write pointer of the transmit buffer circuit is responsive to the second timing reference, and the read pointer of the transmit buffer circuit is responsive to the first timing reference.

9. The method of claim 8, wherein the first timing reference comprises a clock that is recovered from data associated with the audio codec circuit, and the second timing reference comprises a local clock that clocks the signal processor.

10. An integrated circuit device comprising:

a first circuit responsive to a first timing reference;

a second circuit responsive to a second timing reference; and

a buffer circuit including a receive ring buffer operative to receive data from the first circuit in response to a receive write pointer, the receive ring buffer operative to

deliver data to the second circuit in response to a receive read pointer;

wherein the second circuit adjusts the relative positions between the receive read and write pointers to enforce a predetermined minimal spacing there between.

11. The integrated circuit device of claim 10, further comprising:

a transmit ring buffer to receive data from the second circuit in response to a transmit write pointer and deliver transmit data to the first circuit in response to a transmit read pointer, wherein the transmit write pointer is synchronized to the second timing reference, and the transmit read pointer is synchronized to the first timing reference.

12. The integrated circuit device of claim 10, wherein the first circuit comprises a Pulse Code Modulation (PCM) controller, and the second circuit comprises a soft-DSP circuit.

13. The integrated circuit device of claim 10 wherein the first timing reference is a recovered clock signal recovered from data associated with the first circuit and the second timing reference comprises a local clock signal.

14. The integrated circuit device of claim 10, wherein the second circuit comprises:

logic operative to detect the relative positions between the transmit read and write pointers and to adaptively adjust the relative positions based on a threshold level of delay detected between the transmit read and write pointers.

15. The integrated circuit device of claim 14wherein the second circuit exhibits a latency with respect to the first circuit, and the adaptive adjustment repositions the relative spacing between the transmit read and write pointers to match the latency.

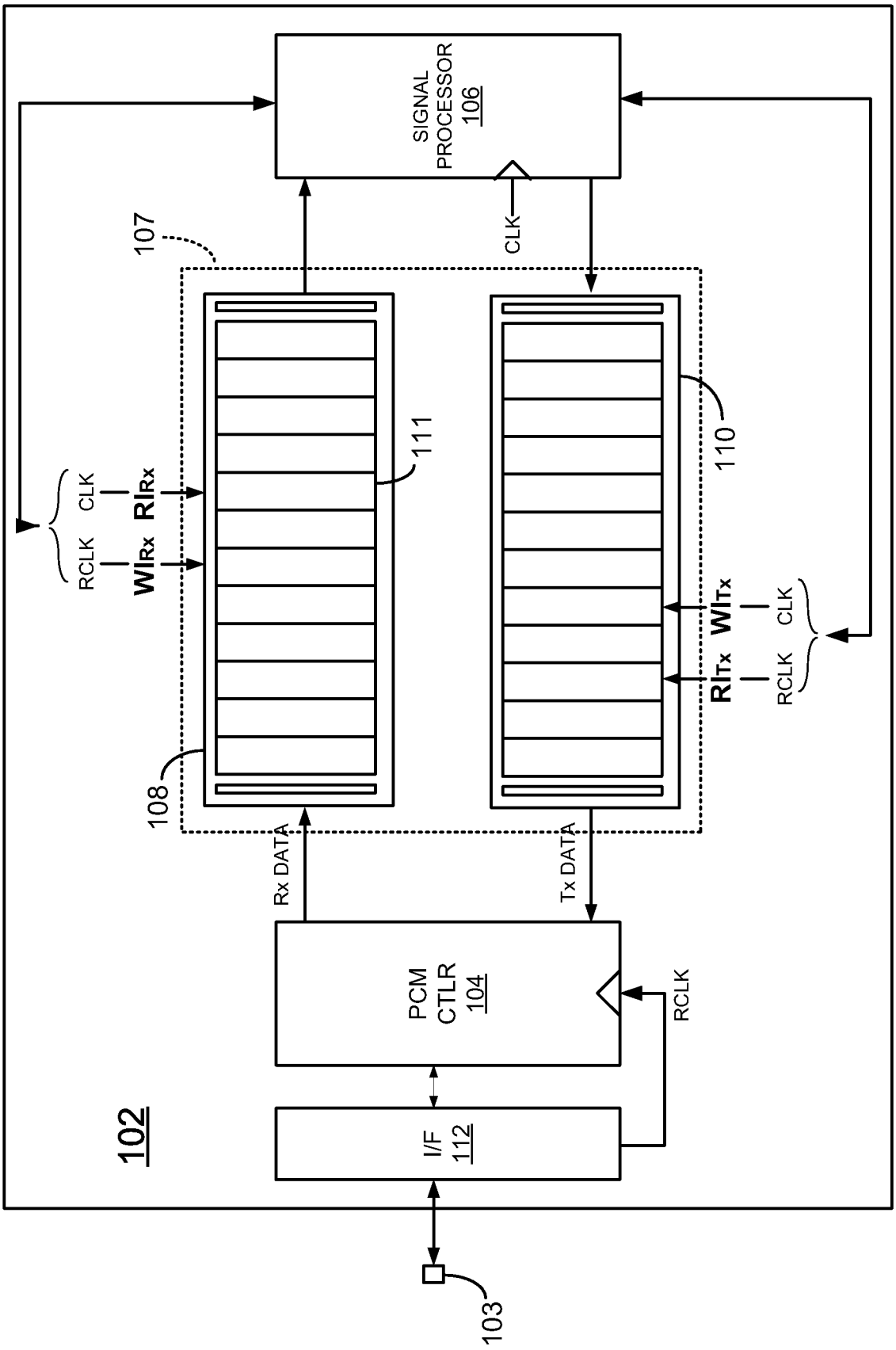
SIGNAL PROCESSOR 106
CLK
107
111
110
108
RCLK
CLK
WIRx
RIRx
RITx
WITx
RCLK
CLK
Rx DATA
Tx DATA
PCM CTLR 104
RCLK
I/F 112
102
103

FIG. 1

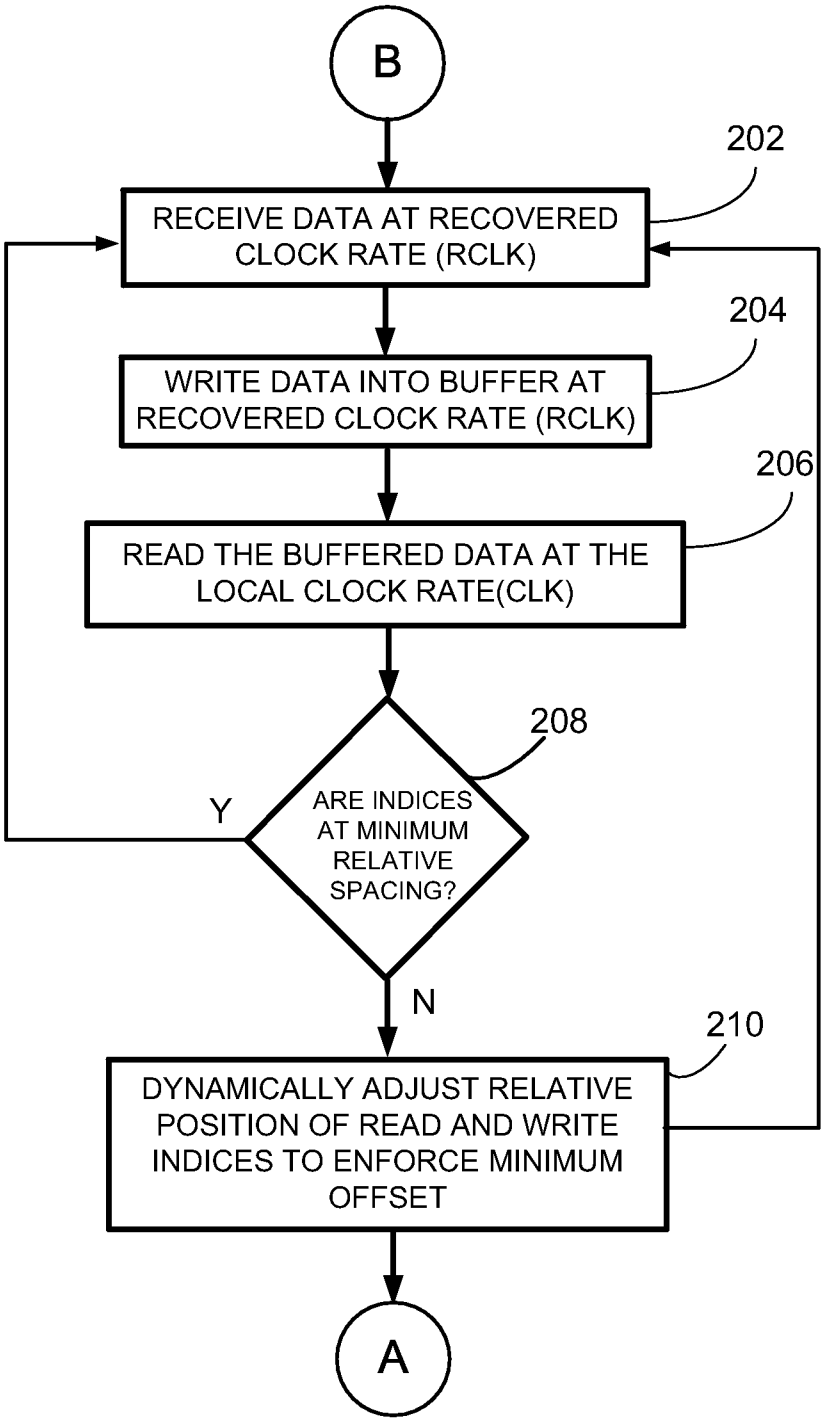
B
202
RECEIVE DATA AT RECOVERED CLOCK RATE (RCLK)
204
WRITE DATA INTO BUFFER AT RECOVERED CLOCK RATE (RCLK)
206
READ THE BUFFERED DATA AT THE LOCAL CLOCK RATE(CLK)
208
ARE INDICES AT MINIMUM RELATIVE SPACING?
Y
N
210
DYNAMICALLY ADJUST RELATIVE POSITION OF READ AND WRITE INDICES TO ENFORCE MINIMUM OFFSET
A

FIG. 2

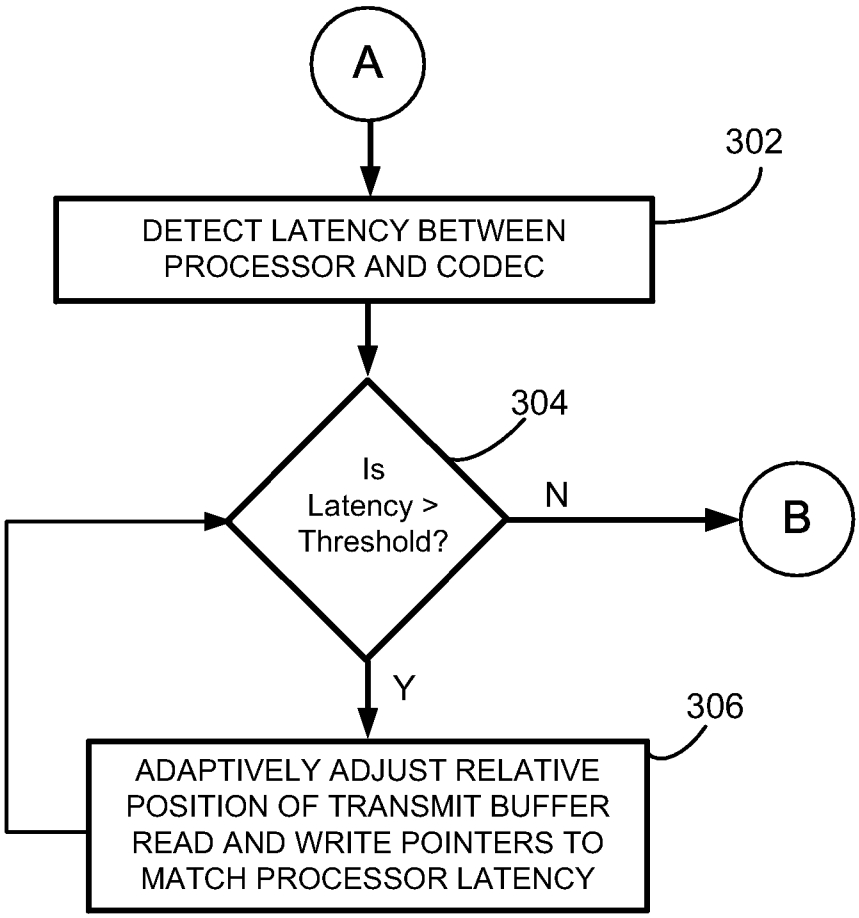
A
302
DETECT LATENCY BETWEEN PROCESSOR AND CODEC
304
Is Latency > Threshold?
N
B
Y
306
ADAPTIVELY ADJUST RELATIVE POSITION OF TRANSMIT BUFFER READ AND WRITE POINTERS TO MATCH PROCESSOR LATENCY

FIG. 3

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2012/077071

A. CLASSIFICATION OF SUBJECT MATTER

G06F 13/28 (2006.01) i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: G06F13/-, G06F12/-,

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WPI,EPODOC,CNKI,CNPAT,IEEE: buffer, offset, synchronizat+, data , ring, read, write, transmit, receive, queue, path, processor, controller, adaptive, adjust, update, latency, threshold

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US6799227B2 (SATHE, Prachi S.) 28 Sept. 2004 (28.09.2004) see the whole document	1-15
A	US2010/0174877A1 (YAGIHASHI, Kiyoto) 08 Jul. 2010 (08.07.2010) see the whole document	1-15
A	CN101930416A (ABLAZE WIRELESS CO., LTD.) 29 Dec. 2010 (29.12.2010) see the whole document	1-15
A	CN101212490A (INDUSTRIAL TECHNOLOGY RESEARCH INSTITUTE) 02 Jul. 2008 (02.07.2008) see the whole document	1-15

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:

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"L" document which may throw doubts on priority claim (S) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&"document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
06 Mar. 2013 (06.03.2013)	**28 Mar. 2013 (28.03.2013)**
Name and mailing address of the ISA/CN The State Intellectual Property Office, the P.R.China 6 Xitucheng Rd., Jimen Bridge, Haidian District, Beijing, China 100088 Facsimile No. 86-10-62019451	Authorized officer ZHANG, Mingxia Telephone No. (86-10)62414429

Form PCT/ISA /210 (second sheet) (July 2009)

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2012/077071

Patent Documents referred in the Report	Publication Date	Patent Family	Publication Date
US6799227B2	28.09.2004	None	
US2010/0174877A1	08.07.2010	JP2010160653A	22.07.2010
CN101930416A	29.12.2010	US2010325334A1	23.12.2010
		EP2309396A2	13.04.2011
		TW201102829A	16.01.2011
CN101212490A	02.07.2008	None	