(12) UK Patent Application (19) GB (11) 2 401 971 (13) A

(43) Date of Printing by UK Office 24.11.2004

(21) Application No: 0420863.3

(22) Date of Filing: 14.02.2003

(30) Priority Data:
(31) 10119391 (32) 08.04.2002 (33) US

(86) International Application Data:
PCT/US2003/004611 En 14.02.2003

(87) International Publication Data:
WO2003/088260 En 23.10.2003

(71) Applicant(s):
Advanced Micro Devices, Inc
(Incorporated in USA - Delaware)
One AMD Place, Sunnyvale,
CA 94088-3453, United States of America

(72) Inventor(s):
Binh Q Le
Pau-Ling Chen

(continued on next page)

(51) INT CL[7]:
G11C 16/04 // G11C 16/34

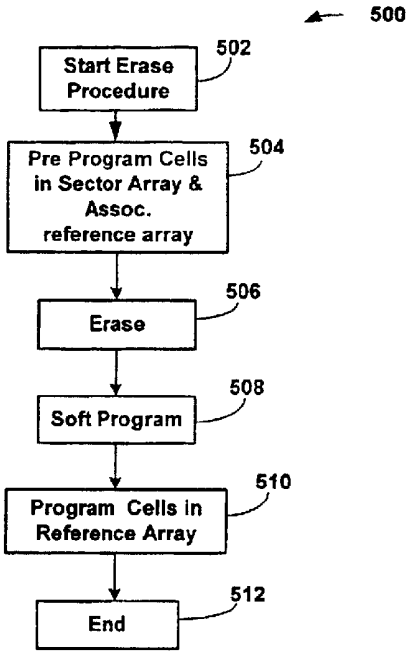
(52) UK CL (Edition W):
G4C C1604 C1606P2

(56) Documents Cited by ISA:
EP 1271550 A2 US 6538922 A
US 5754475 A US 5163021 A

(58) Field of Search by ISA:
INT CL[7] G11C, H01L
Other: EPO-Internal, WPI Data, PAJ, INSPEC

(54) Abstract Title: **Algorithm dynamic reference programming**

(57) A method of cycling dual bit flash memory arrays having a plurality of dual bit flash memory cells (10) arranged in a plurality of sectors (302) with each sector having an associated reference array that have dual bit flash memory cells (10) that are cycled with the plurality of dual hit flash memory cells (10) in the sectors. The dual bit flash memory cells (10) in the associated reference array are then programmed.



GB 2 401 971 A

GB 2401971 A continuation

(74) Agent and/or Address for Service:
Brookes Batchellor LLP
102-108 Clerkenwell Road, LONDON,
EC1M 5SA, United Kingdom