324-77 CROSS REFERENCE SEARCH ROOM

Sept. 11, 1962

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SYMMETRIC SAW-TOOTH WAVE GENERATOR FOR FREQUENCY CONVERSION SYSTEMS

3,054,063

Filed Jan. 19, 1960

3 Sheets-Sheet 1

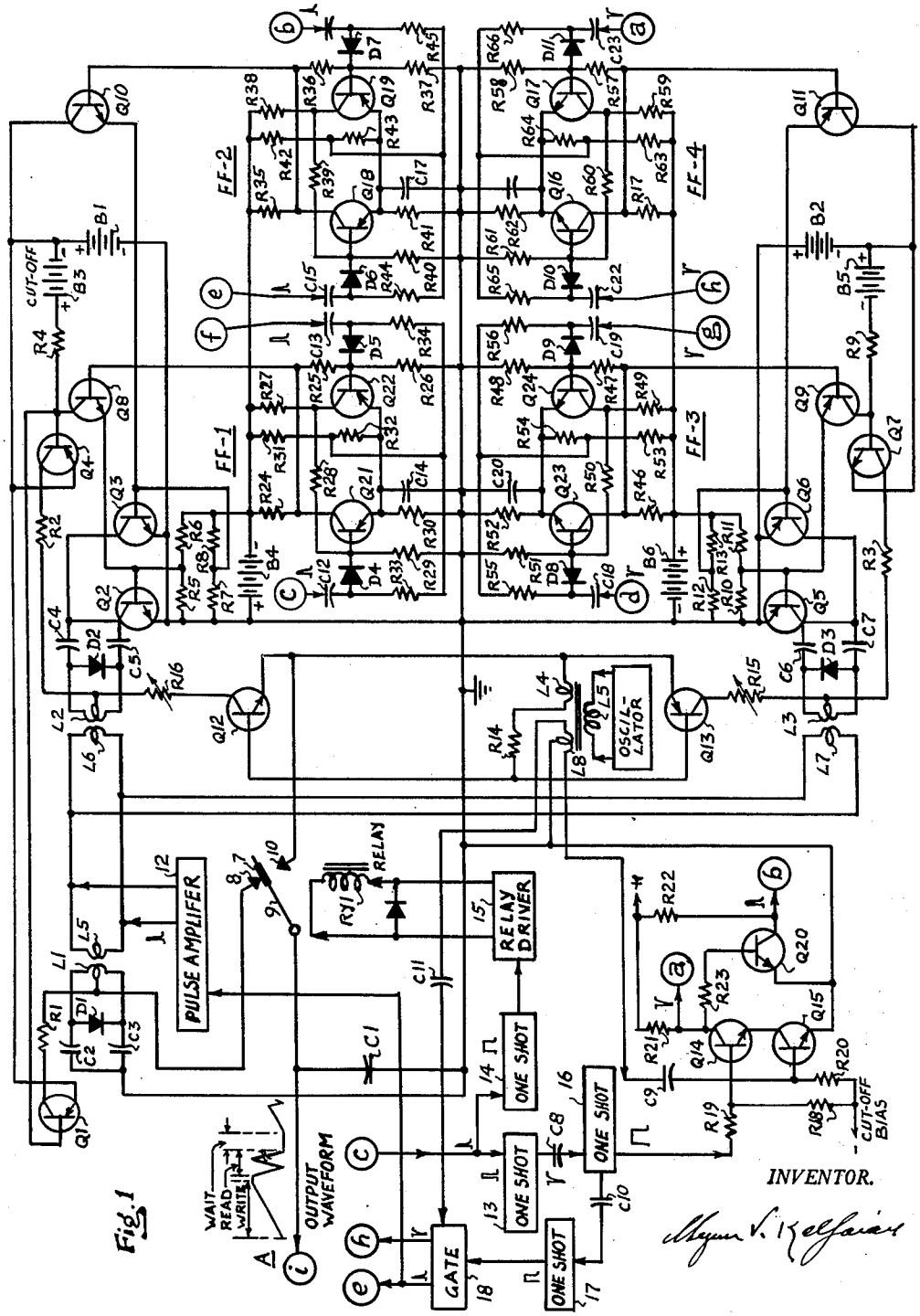

Fig. 1

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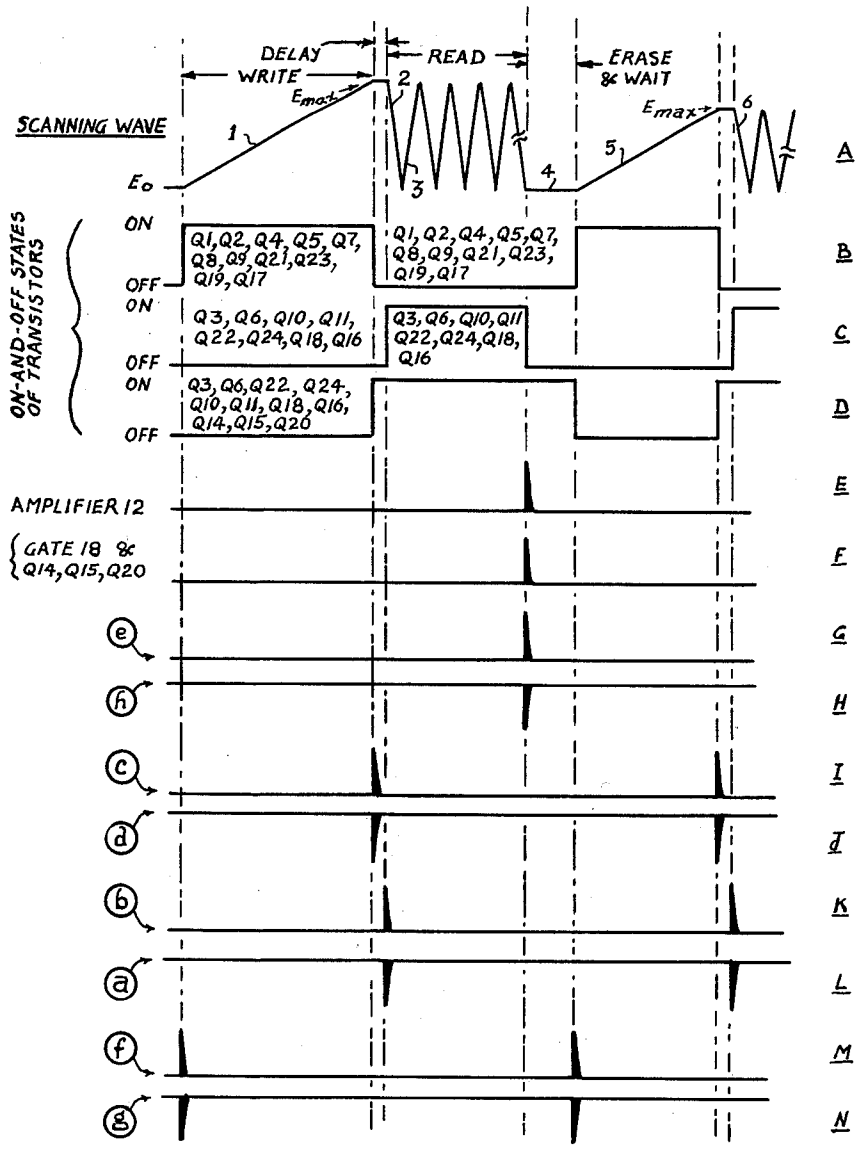

Fig. 2

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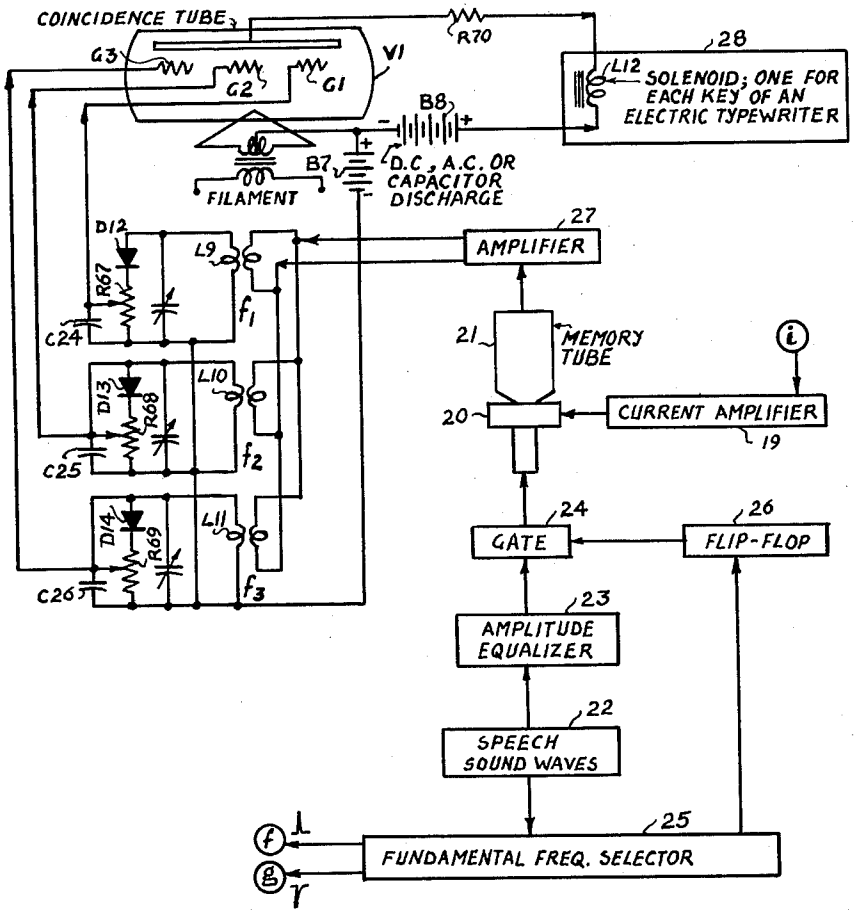

Fig. 3

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SYMMETRIC SAW-TOOTH WAVE GENERATOR FOR FREQUENCY CONVERSION SYSTEMS

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Filed Jan. 19, 1960, Ser. No. 3,350
11 Claims. (Cl. 328—185)

This invention relates to a scanning system for shifting variably changing basic resonances in speech sound waves to predetermined reference frequency regions, for phonetic analysis of the spoken sound, and it is particularly an improvement over the systems disclosed in my U.S. Patents No. 2,705,260 March 29, 1955; No. 2,708,688 May 17, 1955; No. 2,921,133 January 12, 1960, and patent application Serial No. 723,510 March 24, 1958, now Patent No. 2,921,133, January 12, 1960. Its main object is to provide improved methods and means for standardizing the frequency positions of the basic resonances of the propagated speech sound waves, prior to analysis, for final translation into visible intelligible indicia, for example, by electric typing devices. A further object of the present invention is to provide a novel scanning system for said frequency-conversion of the propagated speech sound waves.

In order that a machine, or the like, may be devised to simulate the interpretive mechanism of human intelligence, in printing spoken words, as spoken by all qualities and ranges of voices, without environment control adjustments, or pre-adjustments to any particular voice, it is necessary that all environmental variables are first standardized during propagation of the sound waves, so that standard sets of parameters may be derived to collectively define different phonetic sounds of the spoken words. To accomplish such standardization, advantage is taken of the fact that all phonetic sounds are composed of definite sets of resonances whose ratios in frequency positions with respect to a fundamental remain contant, no matter what band of the voice spectrum they are produced in; this theoretical concept is disclosed in my above mentioned patents and application. Accordingly, the object of the present invention is to select the varying fundamental frequencies during propagation of the sound waves, and shift all frequency components to regions where their frequency ratios become constant with respect to a pre-assigned fundamental frequency. The said sets of parameters may then be derived, without variables, to collectively define each phonetic sound of the spoken words in speech.

Frequency standardizing methods and systems had been disclosed in my above mentioned Patent No. 2,708,688 and Serial No. 723,510. The systems utilized in both of these disclosures provide two storage tubes of the cathode ray type, in a manner that the wave pattern contained in one cycle portion of the selected fundamental (during propagation of the sound waves) is recorded in one storage tube, and the wave pattern contained in the following one cycle portion of the selected fundamental is recorded in the other storage tube. While the first recording is processed, its time length (from inception to termination of the wave pattern) is measured and stored in the form of a first signal quantity. Then, while the second recording is processed, the first recorded wave pattern is reproduced under control of the first quantity, so adjusted that the first recorded wave pattern is reproduced in a predetermined standard time base period. The same process is repeated with the second recorded wave pattern, so that the end result is a cyclic reproduction of the wave pattern of the propagated sound wave at a standard time base period. In order to allow time for reproduction of the recorded wave patterns prior to

the arrival of successive wave patterns, the standard time base period is adjusted to be several times shorter than the shortest time base period occurring in ordinary speech sound waves. Thus, the number of reproduced wave patterns will be many more (randomly varying) than the actual recorded wave patterns, which condition is found to be more advantageous for more accurate resonance analysis of the wave patterns. Improved frequency conversion systems for the above noted purpose have been described in my patent applications Serial No. 773,064 November 10, 1958, now Patent No. 2,942,198; No. 781,103 December 17, 1958; and No. 857,121 December 3, 1959.

It has been described in my above mentioned Patent No. 2,705,260 and patent application Serial No. 723,510 that a wave pattern contained in one cycle time period of a fundamental frequency will yield all the information necessary for recognizing the particular phonetic sound. But since it is difficult to select the different resonances from a single wave pattern, the recorded wave pattern is reproduced a number of times so as to be capable of energizing a set of pretuned resonant circuits therefor. However, it is not necessary to render contiguity between succeedingly recorded wave patterns. In fact, such contiguity may sometimes cause ambiguity of resonance selection, as a succeeding wave pattern may change its shape from that of the preceding one. Thus, it is more desirable to energize the frequency selecting resonant circuits during reproduction of a wave pattern, and dissipate rapidly prior to selection of the resonances of a succeeding wave pattern. Also, the repeated reproduction of the recorded wave pattern does not have to be continually in forward direction, and accordingly, a back and forward sweeping scanning system may be utilized, with greater advantage of avoiding any time lost during retrace period. Such time lost during retrace period may randomly cause sudden phase reversal of the reproduced wave pattern, and prevent proper energization of said pre-tuned resonant circuits by way of heavy filter action. Further yet, if the number of wave pattern reproduction is random, and less than the band pass of said pre-tuned resonant circuits, the amplitude built-up in said resonant circuits, for each phonetic sound, may not be the same for different pitched voices. It is therefore more desirable to standardize the number of reproduction of a recorded wave pattern. Accordingly, it is the principle object of the present invention to provide a frequency conversion scanning system for first recording a wave pattern of the speech sound wave during propagation of same, and reproducing the recorded wave repeatedly in forward and backward sweeping directions at a predetermined reference time base period, including means for stopping said reproduction after reaching a predetermined number of counts. Such a system had been disclosed in my patent application Serial No. 857,121 filed December 3, 1959, and the present invention is contemplated as an improvement over it, utilizing transistors in a specifically different apparatus, instead of conventional vacuum tubes.

In order to distinguish between the presently proposed mode of scanning and the conventional mode of scanning having retrace time lag periods, consider for one example, that a complex waveform having equal signal levels at its beginning and ending is recorded along a single line across the screen of a cathode beam type storage tube. When this recorded wave is reproduced several times continuously by conventional saw tooth scanning waves having retrace time lag periods, contiguity between each reproduced waveform is broken by the retrace periods, which may deviate from the original accuracy with regard to frequency components contained;

when critical narrow band pass circuits are involved. In a second example, assume that the signal levels commencing and terminating the recorded waveform are widely different. In this case, even if the retrace periods of the scanning waves were zero, there will occur sudden changes in signal levels, which when oppositely poled, will cause high filtering action through the associate narrow pass band circuits; this filtering action varying intermediately depending upon the differences in signal levels at the beginning and ending of the recorded waveform.

The recorded complex waveform is herein referred to as representation of some sound in intelligence, for example, in speech sound waves. As such recording may be a portion of a repetitious sound wave, to be reproduced continuously at a later time period, for example, after being transmitted through a narrow band transmission channel, it does not matter whether the recorded wave is scanned in forward direction or in backward direction, or further yet, alternately in forward and backward directions. This condition is true, because intelligence of the sound is not transmitted through phase variations of the wave, but through its various frequency components, which would not alter through the latter mode of scanning. Thus instead of utilizing reproduction scanning saw tooth waves having only forward direction, and including retrace time periods between repetitions, we may use symmetric forward and backward saw tooth waves, with complete elimination of the retrace periods. By such mode of scanning, an associated band pass circuit would not see a sudden change in signal level either at the beginning or at the ending of the recorded waveform, and therefore, avoid filtering action. This latter mode of scansion may not be considered as ideal, because the wave curve at the beginning or ending of the recorded waveform may not be tangential at all times, and the sharp reversal of signal at these points may introduce some unwanted frequency components in the output circuit; but these components will be of small magnitudes in comparison with the effects introduced in conventional mode of scanning, and therefore, they may be considered as negligible.

In the particular embodiment of the present invention, the time period of a waveform to be recorded is not predicted beforehand, and accordingly, the distance of recording, for example, across the screen of a storage type cathode ray tube, may vary widely for each recording. For this reason, and with reference to above given explanation and the advantages with respect to conventional modes of scanning, the present invention contemplates to first provide means for producing a recording saw tooth scanning wave rising from a reference point. During this recording scansion of the incoming waveform, a signal voltage is proportionally derived and stored, the quantity of which represents the time dimension of the recording saw tooth wave; for further control. Further means is provided for reproducing symmetric scansion saw tooth waves, the amplitudes of which are controlled by said stored quantity, in a manner that, they scan the recorded wave beginning from the same reference point to the ending of the record; and backward alternately.

For further understanding of the objects and features of the present invention, reference will now be made to the following specification, in conjunction with the accompanying drawings, wherein: FIG. 1 is a schematic diagram in accordance with the invention; FIG. 2 is a graph of waveforms involved in describing the arrangement of FIG. 1; and FIG. 3 is a supplemental addition to the arrangement of FIG. 1.

Referring now to the waveforms of FIG. 2, the scanning waveform at A illustrates the mode of recording and reproducing a wave pattern of the speech sound waves. The sweeping wave **1** represents the recording, or write, saw tooth voltage, rising from zero voltage level to a maximum voltage level E_{max}. After the wave pattern is written during write period, symmetric saw teeth voltages **2**, **3**, etc. are produced during reproduction, or read period, at repetition of a reference frequency rate. The fall **2** and rise **3** of these symmetric saw teeth voltages are produced in equal amplitudes as of the saw tooth voltage of wave **1**, and their maximums and minimums coincide exactly with that of zero and E_{max}. After a predetermined number of read saw teeth voltages are produced, they are stopped during waiting period **4**, until a new writing saw tooth voltage **5** is produced, the latter of which may have a different amplitude than the voltage of **1**; the rate of rise of voltages **1** and **5**, however, being always constant. After the writing scan voltage **5** is produced, the read scan voltages **6** follow in the previously explained manner. Due to deviation from the ideal conditions, as desired, by the use of certain electrical component parts in conjunction with the presently disclosed electronic circuit arrangement, a slight delay is introduced between the ending of write period and the beginning of read period, as indicated in the graphical illustration at A. Such a delay, however, has no effect upon the operation of the system, and will not deteriorate any analytical conditions during reading time.

With the brief explanation of the presently disclosed scanning system, by way of the graphical illustration at A, in FIG. 2, reference is now made to the schematic arrangement of FIG. 1, wherein the scanning voltage waves at A are produced across capacitor C1. This capacitor is normally connected in parallel with the parallel connected capacitors C2 and C3, through normally closed contacts **7** and **8** of relay RY1. The inductance L1 is assumed to have very low internal resistance, and accordingly, its presence may be considered as a short circuit with respect to the parallel connections of capacitors C2 and C3. The parallel combination of capacitors C1, C2 and C3 is connected to the positive terminal of battery B1 in series with timing resistor R1 and PNP transistor Q1. This transistor is utilized as an on-and-off switch, for example, during write period it is rendered conductive, so that the capacitors C1, C2 and C3 charge with a rising positive voltage, at a time constant depending upon the series connected resistor R1.

During write period, there are three sets of capacitors charging at the same time, which are: the parallel combination of capacitors C1, C2, C3; the parallel combination of capacitors C4, C5; and the parallel combination of capacitors C6, C7. These parallel combinations contain series connected inductances L1, L2 and L3, the presence of which is considered as short circuit, and their purpose will be described later. The parallel combination of capacitors C4 and C5 is connected at one terminal to ground in series with parallel connected NPN switching transistors Q2, Q3, and connected at the other terminal to the positive terminal of battery B1, in series with timing resistor R2 and PNP switching transistor Q4. Thus, when one of the transistors Q2 or Q3 is in conductive state, and simultaneously the transistor Q4 is in conductive state, the parallel combination of capacitors C4, C5 starts charging positively with rising potential at a time constant depending upon the resistive value of R2. The parallel combination of capacitors C6, C7 is connected at one terminal to ground in series with parallel connected PNP switching transistors Q5, Q6, and at the other terminal connected to the negative terminal of battery B2 in series with timing resistor R3 and NPN switching transistor Q7. Thus, when either one of the transistors Q5 or Q6 is rendered conductive simultaneously with conductance of the transistor Q7, the parallel combination of capacitors C6 and C7 starts charging with rising negative potential at a time constant depending upon the resistive value of R3.

The base terminals of PNP transistors Q1 and Q4 are connected in parallel, and to a positive bias potential of battery B3 through input load resistor R4, so that normally they are both rendered inoperative. The base ter-

minal of NPN transistor Q2 is normally reverse biased to current cut off, by receiving negative potential from the junction terminal of resistors R5 and R6, which are connected across battery B4. Similarly, the base terminal of NPN transistor Q3 is normally reverse biased to current cut off, by receiving negative potential from the junction terminal of resistors R7 and R8, which are connected across battery B4. The base terminal of NPN transistor Q7 is normally reverse biased to current cut off, by connecting to the negative terminal of battery B5, through input load resistor R9. The base terminal of PNP transistor Q5 is normally reverse biased to current cut off, by receiving positive potential from the junction terminal of resistors R10 and R11, which are connected across battery B6. Similarly, the base terminal of PNP transistor Q6 is normally reverse biased to current cut off, by receiving positive potential from the junction terminal of resistors R12 and R13, which are connected across the battery B6.

Simultaneous conductive states of the transistors Q2 and Q4 is established by the driving NPN transistor Q8, which when in conductive state, it draws emitter current through resistor R5 and collector current through R4. Thus there is produced forward biases across R4 and R5 for the on-operation of transistors Q2 and Q4. Simultaneous conductive states of the transistors Q5 and Q7 is established by the driving PNP transistor Q9, which when in conductive state, it draws emitter current through resistor R10 and collector current through resistor R9. Thus there is produced forward biases across R10 and R9 for the on-operation of transistors Q5 and Q7.

During write period the parallel combinations of capacitors C4, C5 and C6, C7 are charged in series with R2, Q2, Q4 and R3, Q5, Q7, respectively, by the conductive states of driver transistors Q8, and Q9, respectively. During read period, however, all of said last transistors are rendered inoperative, and transistors Q3, Q6 are rendered conductive. The operation of transistors Q3 and Q6 is established by conductance of the normally inoperative driver NPN and PNP transistors Q10 and Q11, respectively. The on-and-off switching states of driver transistors Q8 to Q11 are established by forward and backward biases impressed upon their base elements at proper time periods by the four flip-flop circuits, indicated as FF–1 to FF–4, respectively, the operating conditions of which will be described further.

Referring now to the functional operation of the circuit in FIG. 1, assume that writing of an incoming sound wave pattern has started. The parallel combination of capacitors C1, C2 and C3 start charging in positive direction in series with timing resistor R1 and conductive transistor Q1 to the positive potential of battery B1; the contact 7 and 8 of relay RY1 being normally closed during this period. The parallel combination of capacitors C4 and C5 start charging in positive direction in series with timing resistor R2, and conductive transistors Q2, Q4 to the positive potential of battery B1. The parallel combination of capacitors C6 and C7 start charging in negative direction in series with the timing resistor R3 and conductive transistors Q5, Q7 to the negative potential of battery B2. The timing resistors R1 and R2 are so adjusted that the potentials across said charging capacitors do not exceed about 60% of the potentials of batteries B1 and B2 during the longest time period that a wave pattern may be written; so as to retain linearity of the charging rate. When the writing wave pattern is ended, the conductive transistors Q1, Q2, Q4, Q5, Q7 are all simultaneously rendered inoperative, and further charging of said capacitors stops. At this point, the relay RY1 is energized, which pulls the armature 9 downward, disengaging its contact 7 from normal contact 8, and making contact with 10. The contact 10 is connected to the emitter elements of alternately switching transistors Q12 and Q13, which are alternately switched on-and-off by the alternate current across secondary inductance L4 in series with current limiting resistor R14. This alternate current is induced from primary inductance L5, which receives its energy from constant frequency oscillator block 11. Due to NPN and PNP characteristics of transistors Q12 and Q13, respectively, the parallel impressed currents to their base elements causes alternate on-and-off operation, due to the fact that while one is forward biased the other becomes backward biased. It is desired that the alternate on-and-off operations of Q12 and Q13 be in the form of a square form. This is substantially possible by first arranging the oscillator 11 to produce close to square waves, instead of sine waves. The output transformer is arranged with iron core with low impedance primary and driven at the primary by low impedance source of the square wave oscillator 11, allowing to hold the current across the secondary substantially constant during the square wave period. The base elements of Q12 and Q13 are then driven extra hard, but without damaging physically, due to the current limiting resistor R14. This further converts the switching conditions of Q12 and Q13 to nearly square waveform. And finally, due to the very low emitter to collector impedances of transistors, any transient impedance variation will be considered negligible for the purpose involved herein.

Referring again to the closing of contacts 7 and 10 of relay RY1, the capacitor C1 is now connected to the emitter elements of alternately switching transistors Q12 and Q13. With a timing arrangement (the function of which will be described later, the PNP transistor Q6 is rendered conductive by the driving transistor Q11, at such time instant that the alternate switching PNP transistor Q13 has initiated its conductive state. By such act, the positively charged capacitor C1 has now an electrical path through Q13, timing resistor R15, negatively charged combination of capacitors C6, C7, and transistor Q6, to ground. Due to the inherent low impedances of Q13 and Q6, the positive charge of capacitor C1 starts falling in the negative direction at a time speed mainly depending upon the timing resistor R15. The capacitive value of parallel connected capacitors C6 and C7 is substantially higher than the value of C1, for example, at least 100 times or more, so that during discharge of C1 any loss of stored electrical quantity in capacitors C6 and C7 will be negligible. The frequency of oscillator block is prefixed, and crystal control may be utilized if precision is required. The exact frequency of oscillation may be determined for a specific use, and for practical purposes required herein may be anywhere between 5 to 10 kilocycles; producing 10 to 20 thousand switching operations per second by transistors Q12 and Q13. Thus assuming that a frequency of 10 kc. is chosen as a standard, the value of timing resistor R15, as well as the voltage magnitude developed across capacitors C6 and C7, is so adjusted that the capacitor C1 discharges to zero value in exactly 90 microseconds before reverse charging to the stored quantities of C6 and C7 starts. The principal purpose of the negative charge across capacitors C6 and C7 is to provide linear discharge of capacitor C1 down to zero value, before curvature takes place. Thus, the higher potential across capacitors C6 and C7, the greater linearity of discharge across C1; the value of R15 being adjusted accordingly, for the required timing of discharge. Once these adjustments are fixed, it is seen that the switching PNP transistor Q13 will always assume an off-state at the instant that capacitor C1 has discharged to zero value, and the switching NPN transistor Q12 will assume an on-state at the same instant.

The capacitor C1 now starts charging in positive direction to the potential of charged capacitors C4 and C5, in series with Q12, Q3, and timing resistor R16. In a similar mode, as described above, the charged voltage across capacitors C4 and C5 is preararnged to be greater than the charged voltage across capacitors C2

and C3, by pre-adjusting the value of resistor R2, and the potential of battery B1. Thus by further adjustment of timing resistor R16, the capacitor C1 charges with a linear rise across the charge of capacitors C4 and C5, until the potential across C1 reaches the exact level as it had assumed when it was connected in parallel with the capacitors C2 and C3. At this instant, the NPN transistor Q12 assumes an off-state and the PNP transistor Q13 assumes an on-state so as to repeat forward and backward charge across capacitor C1, for the production of required read scanning wave, as indicated by the illustration at A. After a predetermined number of read scanning waves are produced, all transistors Q1 to Q11 are rendered inoperative, and the capacitors C2, C3 and C4, C5 and C6, C7 are discharged to zero values, for a new start of scanning when a following sound wave pattern arrives upon the input of a particular memory device employed. The transistors Q12 and Q13 may be left operating alternately at all times, as their presence will not disturb charging conditions of the storage capacitors. For example, due to the high capacitive ratio between the capacitor C1 and the storage capacitors, the timing resistors R16 and R15 are much larger than the timing resistors R2 and R3, and any switching action of transistors Q12 and Q13 during write period will be negligible in disturbing the charging rates of capacitors C4, C5 and C6, C7.

The discharge of parallel connected capacitors C2, C3 and C4, C5 and C6, C7 are similar in nature, and they are discharged at the same time. Accordingly, description of the function of capacitors C2 and C3, as a typical example, will also refer to the functions of the other capacitors. During discharge period, a pulse current is supplied to the primary inductance L5 by the pulse amplifier block 12. This pulse is induced across the secondary inductance L1, and the voltage developed across it is made sufficiently high to overcome the highest voltage stored in capacitors C2 and C3. The inductance L1 is wound with low resistance wire, which causes the original like poled voltages across capacitors C2 and C3 to immediately change into unlike poled voltages, equal to the voltage developed across L1. When the pulse voltage across L1 subsides, the voltage across C2 and C3 drop at the same time, due to the low resistance of L1. Thus the capacitors may be discharged within an extremely short pulse period, without the necessity of conventional electric discharge devices being connected in parallel with the capacitors; although such devices may be used, if so desired. The diode D1 is used to prevent oscillation across L1, after the pulse voltage has been completed. Thus the capacitors C4, C5 receive their discharging voltage induced from across primary inductance L6, and the capacitors C6, C7 receive their discharging voltage induced from across primary inductance L7; the diodes D2 and D3 being in parallel with the secondary inductances L2 and L3, respectively. The inductances L1, L2 and L3 do not have to be center tapped, as their low inductances will not produce signal energy during charging period. If center tap is desired, and not available, however, the resistors R1, R2, R3 and R16 may be divided in parallel arrangement, and connected to the end terminals of said inductances.

In reference to the capacitor C1, it was stated that C1 must be coupled to the charged capacitors C6 and C7 at the instant of conductance of the PNP switching transistor Q13; this coupling being establshed by the conductance of driver transistor Q11. Since Q11 is a PNP transistor, its base must be connected to a positive potential during off-state, and to a negative potential (causing forward base current) during on-state. The emitter element of Q11 is connected to the junction terminal of resistors R12 and R13, which normally offers reverse bias for current cut off action. But the base of Q11 is connected to the positive terminal of battery B6 in series with collector circuit resistor R17 of NPN transistor Q16, which in operation draws sufficient current to effect forward bias upon the base element of Q11. Thus the flip-flop circuit FF–4 comprising NPN transistors Q16 and Q17 may be set and reset for the on-and-off operation of Q11. Accordingly, a negative pulse is applied upon the base element of Q17, from terminal (*a*), so that transistor Q16 of FF–4 is set into conductive state for the coupling of capacitor C1 to the parallel connected capacitors C6 and C7. The proper timing of this negative pulse is obtained, as in the following:

At the instant that the writing period has ended, a pulse is applied, from terminal (*c*), to the inputs of one-shot circuit blocks 13 and 14. Various one-shot circuits are known and used both in commercial and specialized electronic devices, and accordingly, detailed circuitry is avoided herein for simplicity of drawing. A one-shot circuit, however, is known to change its state of conduction in response to an incoming pulse signal; remain in such state for a predetermined time period; and reset itself automatically to the original conductive state. The time period during which it stays in a changed state depends upon the value of a capacitor contained therein, and it may be varied to any suitable time delay period. Accordingly, a one-shot circuit may be used as a delay circuit, and due to the sharp rise and fall of the delayed output signal, either negative or positive pulses may be obtained by differentiation, for example, by coupling to associated circuits with a small capacitor. Thus referring again to the input pulse from terminal (*c*), the one-shot circuit in black 14 changes its state of conduction and applies a prolonged signal to the relay driver block 15, which in turn energizes the relay coil RY1 and pulls the armature 9 downward to close contacts 7 and 10. A relay with mechanical contact closure within 200 microseconds is presently manufactured commercially. But even such high speed of operation cannot match the speed of operation of electronic circuits, and accordingly, the block 13 of one-shot circuit is operated by the pulse arriving from terminal (*c*), as a compensation for the mechanical delay. After a slight delay, the resetting condition of one-shot circuit in block 13 produces a pulse by way of small coupling capacitor C8, and operates the one-shot circuit in block 16. The output of one-shot block 16 is directly applied upon the base element of NPN transistor Q14 and load resistor R18, in series with current limiting resistor R19. Transistor Q14, however, being connected in series with transistor Q15, cannot respond to the signal upon its base element until a simultaneous signal is applied upon the base element of Q15. As the prolonged signal from one-shot block 16 lingers upon the base of Q14, a properly timed signal from oscillator block 11 finally arrives upon the base element of Q15 and load resistor R20, by way of differentiating capacitor C9. Since transistor Q15 is of NPN characteristics, and transistor Q13 is of PNP characteristics, the center tapped secondary inductance L8 is oppositely terminated with respect to the inductance L4, so that operations of Q13 and Q15 become simultaneous. Thus a pulse current passes through gate transistors Q14 and Q15, in series with collector circuit resistor R21, the current through which produces a negative pulse output terminals (*a*) and applies upon the base element of Q17, at terminal (*a*), for the on-operation of Q16 of the flip-flop circuit FF–4. During this pulse period (the pulse may be prolonged if so desired), the NPN transistor Q10 must also be rendered conductive, by way of conduction of PNP transistor Q18 of flip-flop FF–2. Due to the PNP characteristics of transistor Q19, of FF–2, a positive pulse must be applied to its base to render it inoperative. Accordingly, the negative pulse from the collector element of Q14 is phase inverted in the collector circuit resistor R22 of NPN transistor Q20, through coupling resistor R23, and applied from terminal (*b*) to the terminal (*b*) of the base ele-

ment of transistor Q19, for the on-operation of NPN transistor Q10.

With the above explained conditions of flip-flop circuits FF–2 and FF–4, the capacitor C1 becomes in a state of charging and discharging for the production of reading saw-tooth waves. After a number of readings, the flip-flops FF–2 and FF–4 reverse their states of operations, and the storage capacitors are discharged, as explained in the foregoing. The capacitor C1, however, must be isolated from the rest of the circuits at the instant that it had assumed zero potential, as no discharging element is provided for it; although a discharge element may also be easily provided for it, if so desired. At the instant that one-shot circuit in block 16 resets itself, an output pulse is produced through the differentiator coupling capacitor C10, and applied upon the one-shot circuit in block 17, so that it produces an output signal prolonged to a period of about one and one-half cycles of the oscillations in oscillator block 11; allowing enough time for a signal from inductance L8 to arrive upon the gate circuit in block 18, through differentiating capacitor C11, in the form of a pulse. The circuitry of gate in block 18 is similar to the circuitry of gate, comprising transistors Q14, Q15 and Q20, the operation of which had already been described. As stated, the capacitor C1 is isolated from the charged capacitors at the instant that it has assumed zero potential, during which time the switching NPN transistor Q12 must assume conductance. Accordingly, the signal delivered to the differentiating capacitors C9 and C11 are taken from the opposite terminals of center tapped inductance L8. The positive and negative output pulses at terminals (*e*) and (*h*) of gate 18 are then applied to the input terminals (*e*) and (*h*) of flip-flops FF–2 and FF–3 for their reversal to normal operating conditions. Simultaneously, a pulse signal is applied to the pulse amplifier block 12, for discharge action of the parallel connected capacitors, as explained in the foregoing. The prolonged output signal of one-shot circuit in block 14 is adjusted so that it ends approximately at the instant of capacitor discharging action starts, so that the relay RY1 releases armature 9 from contact point 10 and establishes normally closed contacts 7 and 8, for a new start of writing when a following sound wave pattern arrives at the input of a particular memory device utilized.

The flip-flop circuits FF–1 to FF–4 are of conventional design, and their functions have been described in various literature. For references of component parts, however, the flip-flop FF–1 consist of PNP transistors Q21, Q22; cross coupling resistors R24 to R29; emitter circuit resistor R30; and voltage dividing resistors R31, R32 from the junction terminal of which is obtained a negative bias for the diode inputs, by way of load resistors R33 and R34 to the diodes D4 and D5, respectively, so that the flip-flop will operate by input signals, as received through coupling capacitors C12 and C13, only when their magnitudes are higher than said bias. The capacitor C14 is utilized as a bypass across emitter resistor R30. The flip-flop FF–2 consists of PNP transistors Q18, Q19; cross coupling resistors R35 to R40; emitter circuit resistor R41 across which is included a bypass capacitor C17; and voltage dividing resistors R42 and R43 from the junction terminal of which is obtained a negative bias for the diode inputs, by way of load resistors R44 and R45 to the diodes D6 and D7, respectively, so that the flip-flop will operate by input signals, as received through coupling capacitors C15 and C16, only when their magnitudes are higher than said bias. The flip-flop FF–3 consists of NPN transistors Q23, Q24; cross coupling resistors R46 to R51; emitter circuit resistor R52 across which is included a bypass capacitor C20; and voltage dividing resistors R53 and R54 from the junction terminal of which is obtained a positive bias for the diode inputs, by way of load resistors R55 and R56 to the diodes D8 and D9, respectively, so that the flip-flop will operate by input signals, as received through coupling capacitors C18 and C19, only when their magnitudes are higher than said bias. The flip-flop FF–4 consists of NPN transistors Q16 and Q17, cross coupling resistors R17 and R57 to R61; emitter circuit resistor R62 across which is included a bypass capacitor C21; and voltage dividing resistors R63 and R64 from the junction terminal of which is obtained a positive bias for the diode inputs, by way of load resistors R65 and R66 to the diodes D10 and D11, respectively, so that the flip-flop will operate by input signals, as received through coupling capacitors C22 and C23, only when their magnitudes are higher than said bias.

The graphical illustration in FIG. 2 shows the time periods of various on-and-off states of the switching transistors, as a guide in following the functional operation of the arrangements of FIG. 1. The pulse waves (*f*) and (*g*) shown in graphs I and J are obtained from the fundamental frequencies of the speech sound waves, for a complete description of which reference may be made to my Patent No. 2,872,517 February 3, 1959, wherein is included a schematic arrangement of a practical fundamental frequency selector from speech sound waves. A fundamental frequency selector is also shown in block diagram 25.

FIG. 3 shows an arrangement that can be used in conjunction with the scanning system of FIG. 1. As described in the foregoing, the scanning system of FIG. 1 is particularly contemplated to be used for standardization of the varying frequency components of speech sound waves. In reference to the theoretical aspects of speech sound waves, each phonetic sound comprises a set of basic resonances. In ordinary speech, however, the frequency positions of these sets of basic resonances vary widely, although their frequency ratios remain constant, regardless of the band in which they are produced. In order to standardize the frequency positions of these basic resonances, the frequency conversion scanning wave, as produced by the arrangement in FIG. 1, had been contemplated herein. Accordingly, the scanning wave produced across capacitor C1, at terminal (*i*) is first applied to an amplifier block 19, which current amplifies said waveform and applies upon the beam deflection yoke 20 of a cathode ray memory tube 21. The writing wave is received from the block 22, which is the source of speed sound waves. The output of block 22 is first applied upon amplitude equilizer block 23, the function of which is to expand and contract the wide amplitude variations of the originally propagated sound waves, so that the peaks will always have a constant reference amplitude. Such an amplitude equalizer is described in my U.S. patent application Serial No. 773,065 filed November 10, 1958. The output of block 23 is then applied to the memory tube 21 for writing, in series with gate block 24. This gate admits the sound waves from block 23 during every other one cycle time periods of the fundamental frequencies of the speech sound waves. Accordingly, the speech sound waves from block 22 are applied to the block 25, consisting of a fundamental frequency selector, which in turn produces output pulses at the peaks of said fundamental frequencies. These pulses are applied to a block 26 consisting of a flip-flop circuit, which in turn operates the gate 24 in alternate on-and-off states. The block 25 also supplies positive and negative output pulses (*f*) and (*g*) to the like terminals in FIG. 1. The operation timing of gate 24 is such that, it is gated-on during writing time period, and gated-off during reading time period. Thus the output of memory tube 21 contains the required frequency converted speech sound waves in periodic sequence. These waves are applied to an amplifier block 27, the output of which is terminated to a plurality of sets of tuned circuits, each set being tuned to fixed sets of resonances, as representation of a specific phonetic sound. Only one set of tuned circuits is shown in the drawings, which comprises secondary inductances L9,

L10 and L11, tuned to frequencies f_1, f_2, and f_3, respectively. The oscillatory voltages across L9 to L11 are rectified by diodes D12 to D14, respectively, in series with variable resistors R67 to R69, respectively. The amplitude ratios of these rectified waves are preadjusted in fixed positions across resistors R67 to R69, and bypassed by capacitors C24 to C26, respectively, so as to cancel out the high frequency components across the tapped terminals of said resistors. The output signals of these tapped terminals are then applied to the three separate control electrodes G1, G2 and G3 of a coincidence thyratron tube VI. When the three resonances at frequencies f_1 to f_3 are present, suggesting that a specific phonetic sound is present, and three separate voltages are applied upon the control elements of VI simultaneously, raising the bias from B7 to zero volts, the thyratron tube V1 energizes and current flows through its anode circuit, energizing the solenoid L12 in an electric typing device 28, for actuating a specific printing key therein.

Coincidence devices are possible to make in the art of electronics, and the particular device shown schematically in FIG. 3 represents an ion deflection thyratron, having three control electrodes of equal sensitivities, and is operated in a manner that, when the three control electrodes receive simultaneous signal voltages, raising their normal negative bias of 4.5 volts to zero volts, the gas contained therein ionizes and fires, in similar mode as a thyratron. Such a tube is presently labeled as KP–80, and manufactured by Kip Electronics. Other forms, of course, may eventually be made, for example, in semiconductor form, which will eliminate filament supply. The battery B8 may be in the form of A.C. supply, so that the tube V1 will automatically stop conduction after operating the solenoid L12; in series with current limiting resistor R70.

The descriptive matter in conjunction with the arrangements shown in FIG. 1 and F3, have shown a mode flexibility and broad possibilities. For example, the output of amplifier 27 may be heterodyned to low pitched frequencies for narrow band transmission of the speech sound waves. A second section as of the arrangement of FIG. 1 may be included, so that both are operated alternately, for contiguous scanning of writing and reading, instead of periodic scanning. Accordingly, the specific arrangements shown herein are only exemplary, as various modifications, substitutions and adaptations are possible without departing from the true spirit and scope of the invention.

What I claim is:

1. In a frequency conversion system where a complex wave is recorded during an unknown time period and reproduced repeatedly during constant time base periods, and wherein phase variation of said complex wave during reproduction time is allowable, the system of producing frequency conversion scanning energy waves in symmetric forward and backward directions for the reproduction of said recorded complex wave, comprising first and second voltage sources of oppposite polarities from a common terminal point; first and second capacitors; a series connected first circuit comprising a first capacitor, a first resistor, and a first gate across said first voltage source, whereby charging the first capacitor in series with the first resistor when the first gate is in on-position; a series connected second circuit comprising a second capacitor, a second resistor, and a second gate across said first voltage source, whereby charging the second capacitor in series with the second resistor when the second gate is in on-position; a series connected third circuit comprising a third capacitor, a third resistor, and a third gate across said second voltage source, whereby charging the third capacitor in series with the third resistor when the third gate is in on-position; means for rendering said first, second and third gates in on-states from the beginning to end of said recording time period, thereby effecting charge of said first, second and third capacitors at a speed determined by the predetermined values of said first, second and third series-connected resistors; a fourth capacitor having substantially smaller capacitive value than said first, second and third capacitors; a multiconnecting switching means; means for connecting the fourth capacitor in parallel to said first capacitor by said switching means during said recording time period, so as to acquire similar potential charge; a fourth resistor from the charged terminal of said second capacitor; a fifth resistor from the charged terminal of said third capacitor; fourth and fifth on-and-off gates connected in series with said fourth and fifth resistors from a common terminal point, respectively; means for rendering said first, second and third gates in off-positions at the end of said recording time period, thereby said first, second and third capacitors to retain their acquired charges in steady states without disturbance; means for connecting said fourth capacitor to the common terminal point of said fourth and fifth gates by said switching means after said first, second and third gates have been rendered in off-states; a generator of alternate energy wave at a constant predetermined frequency for the constant time base periods aforesaid; means for applying said alternate wave to said fourth and fifth gates alternately for rendering same in on-and-off states alternately, said application being so timed as to render the fifth gate in on-state first, thereby allowing the fourth capacitor to discharge first in series with said fifth gate and fifth resistor and repeat thereon charging in series with the fourth resistor for continuous production of rising and falling potentials across the fourth capacitor; and means for utilizing the varying voltages across said fourth capacitor as the frequency conversion forward and backward scanning wave aforesaid.

2. The system as set forth in claim 1, wherein is included a discharging means for discharging any previously charged potentials in said first, second and third capacitors prior to the said charging.

3. The system as set forth in claim 1, wherein said first, second, third, fourth and fifth gates comprise transistors.

4. The system as set forth in claim 1, wherein said switching means consists of a high speed relay having double throw electrical contacts.

5. The system as set forth in claim 1, wherein the charging speed of said second capacitor is adjusted faster than the speed of said first capacitor, so as to acquire a higher charging potential than the first; and the values of said fourth and fifth resistors are so adjusted that said fourth capacitor charges to exact potential as it had acquired during said parallel connection with said first capacitor, at the exact moment when said fourth gate is in off-state, and to zero value when said fifth gate is in off-state, thereby improving linearity of said charge and discharge.

6. In a frequency conversion system where a complex wave is recorded during an unknown time period and reproduced repeatedly during constant time base periods, and wherein phase variation of said complex wave during reproduction time is allowable, the system of producing frequency conversion scanning energy waves in symmetric forward and backward directions for the reproduction of said recorded complex waves, comprising first and second voltage sources of opposite polarities from a common terminal point; a first capacitor, a first resistor and a first on-and-off gate; means for series coupling last said parts across said first voltage source, whereby charging the first capacitor in series with the first resistor when the first gate is in on-position; a second capacitor, a second resistor and a second on-and-off gate; means for series coupling last said parts across said first voltage source, whereby charging the second capacitor in series with the second resistor when the second gate is in on-positions; a third capacitor, a third resistor and a third on-and-off gate; means for series coupling last said parts across said second voltage source, whereby charging the third capacitor in series with the third re-

sistor when the third gate is in on-position; fourth and fifth gates, and means for electrically connecting same in parallel with said second and third gates, respectively, whereby providing electrical path for said second and third capacitors through either one of said parallel connected gates; means for rendering said fourth and fifth gates in off-states, and said first, second and third gates in on-states from the beginning to end of said recording time period, thereby effecting charge of said first, second and third capacitors at a speed determined by the predetermined values of said first, second and third series-connected resistors; a fourth capacitor having substantially smaller capacitive value that said first, second and third capacitors; a multiconnecting switching means; means for connecting the fourth capacitor in parallel to said first capacitor by said switching means during said recording time period, so as to acquire similar potential charge; a fourth resistor from the charged terminal of said second capacitor; a fifth resistor from the charged terminal of said third capacitor; sixth and seventh on-and-off gates connected in series with said fourth and fifth resistors from a comon terminal point, respectively; means for rendering said first, second and third gates in off-states at the end of said recording time period, thereby said first, second and third capacitors to retain their acquired charges in steady states without disturbance; means for electrically connecting said fourth capacitor to the common terminal point of said sixth and seventh gates by said switching means after said first, second and third gates have been rendered in off-states; a generator of alternate energy wave at a constant predetermined frequency for the constant time base periods aforesaid; means for applying said alternate wave to said sixth and seventh gates alternately for rendering same in on-and-off states alternately; and means for rendering said fourth and fifth gates in on-states at the instant said seventh gate is rendered in on-state by said alternate wave, so that said fourth capacitor first begins discharging its acquired charge in the direction of said second voltage source, and repeat thereon charging and discharging at the frequency of said alternate wave, whereby the energy waveform across said fourth capacitor may be represented as the frequency conversion symmetric forward and backward scanning wave aforesaid.

7. The system as set forth in claim 6, wherein said fourth and fifth gates are rendered in on-states at time instants as in the following: an eighth on-and-off gate having first and second input terminals, said gate being rendered in on-state only when excited at its first and second terminals simultaneously; means for producing first electrical pulses at the instants when said seventh gate is rendered in on-states; means for producing a second electrical pulse at the end of said recording time period, the second pulse having a time duration within which at least one on-state of said seventh gate may occur; means for applying said first and second pulses to said first and second input terminals, thereby rendering the eighth gate in on-state; means for deriving an electrical signal from the on-state condition of said eighth gate; and means for rendering said fourth and fifth gates in on-states at time instants when said signals are derived.

8. The system as set forth in claim 6, wherein is included a discharging means for discharging any previously charged potentials in said first, second and third capactors prior to the said charging.

9. The system as set forth in claim 6, wherein all of said gates comprise transistors.

10. The system as set forth in claim 6, wherein said switching means consists of a high speed relay having double throw electrical contacts.

11. The system as set forth in claim 6, wherein the charging speed of said second capacitor is adjusted faster than the speed of said first capacitor, so as to acquire a higher charging potential than the first; and the values of said fourth and fifth resistors are so adjusted that said fourth capacitor charges to exact potential as it had acquired during said parallel connection with said first capacitor, at the exact moment when said gate is in off-state, and to zero value when said fifth gate is in off-state, thereby effecting charge of said fourth capacitor substantially linearly in series with said fourth and fifth resistors.

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