(54) Title: REDUCING IMPACT OF COUPLING NOISE IN SIGNAL LINES

(57) Abstract: An integrated circuit comprising a first bitline pair (310) on a first bitline level which is adjacent to a second bitline pair (320) on a second bitline level is provided. The first bitline pair comprises m twists (340), where m is a whole number $\geq 1$ and the second bitline pair comprises n twists (350) and (351), where n is a whole number $\neq m$. The twists transform coupling noise from adjacent bitline pairs into common mode noise, which results in improved signal margin.
REDUCING IMPACT OF COUPLING NOISE IN SIGNAL LINES

Field of the Invention

The present invention relates generally to reducing the adverse impact of noise coupling in signal lines of, for example, an integrated circuit (IC). In particular, the invention relates to bitline architectures which reduce the impact of noise to improve sensing of memory cells.

BACKGROUND OF THE INVENTION

Referring to Fig. 1, a conventional dynamic random access memory cell 101 is shown. The memory cell comprises a cell transistor 110 and a cell capacitor 150 for storing information. A first junction 111 of the transistor is coupled to a bitline 125, and a second junction 112 is coupled to the capacitor. A gate electrode 113 of the transistor is coupled to a wordline 126. A reference or constant voltage ($V_{RH}$) can be coupled to a plate of the capacitor. The plate which is coupled to the reference voltage can serve as a common plate in the memory array.

A plurality of cells are arranged in rows and columns, connected by wordlines in the row direction and bitlines in the column direction. The bitlines can be arranged in various types of bitline architectures, such
as open, folded, open-folded, diagonal, multi-level, split-level, or split-level diagonal. Multi-level or split-level bitline architectures are described in, for example, Hamada et al., A Split Level Diagonal Bitline Stack Capacitor Cell for 256 Mb DRAMs, IEDM 92-7990, which is herein incorporated by reference for all purposes.

The bitlines are coupled to sense amplifiers to facilitate memory accesses. Typically, a pair of bitlines is coupled to a sense amplifier. The bitline containing the selected memory cell is referred to as the bitline or bitline true and the other is referred to as the reference bitline or bitline complement.

A memory access typically comprises precharging the bitlines to a predefined voltage (e.g., equalization voltage or $V_{\text{bieq}}$). A memory cell within a bitline pair is selected after the bitlines are precharged and floated. The memory cell is selected by rendering the transistor of the memory cell conductive, coupling the memory cell’s capacitor to the bitline true. Depending on the value stored in the capacitor, the bitline true is pulled above or below $V_{\text{bieq}}$. The reference bitline, in the ideal case, remains at $V_{\text{bieq}}$. The voltage difference between the reference bitline and bitline true is the differential voltage. A sense amplifier coupled to the bitline pair senses and amplifies the differential voltage, which is
indicative of the data stored in the selected memory cell.

An important issue to consider in designing memory ICs is to provide an adequate sensing signal (i.e., differential voltage) to the sense amplifier in order for the data to be read accurately from memory. The differential signal sensed by a sense amplifier, in an ideal situation, depends on the charge sharing between the bitline and the memory cell. The ratio of the bitline capacitance (and the capacitance of the sense amplifier) to the cell capacitance determines the magnitude of the differential signal. However, the voltage on the reference bitline increases or decreases along with the voltage swing on the bitline true due to noise coupling between the bitlines (intra-bitline coupling). This results in a decrease in the magnitude of the differential signal, which is undesirable as this may lead to incorrect evaluation of the data stored in the memory cell.

Noise coupling from neighboring bitline pairs (inter-bitline coupling) can also reduce the signal margin. This sense amplifiers of the array may not be activated simultaneously. This occurs as a result of, for example, different amplification speeds for a "0" and a "1", difference in the threshold voltage of the various latch transistors, or a skew in the activation of the
sense amplifiers in the top and bottom bank in an interleaved arrangement. Coupling noise from a bitline pair whose differential signal is amplified can reduce the differential signal of a neighboring bitline pair whose differential signal has yet to be amplified.

The problems associated with bitline coupling noise become worse as technology migrates to smaller groundrules due to the fact that the fraction bitline-to-bitline capacitance contribution to the total bitline capacitance increases with smaller dimensions.

As evidenced from the foregoing discussion, it is desirable to reduce the impact of coupling noise to avoid degrading or reducing the signal margin of a differential signal.

**SUMMARY OF THE INVENTION**

The invention relates to reducing the adverse impacts of coupling noise from neighboring signal lines in integrated circuits with multiple signal line levels. In one embodiment, a memory IC comprises a first bitline pair with first and second bitlines on a first bitline level and a second bitline pair with first and second bitline on a second bitline level. The first bitline pair is adjacent to the second bitline pair. The first bitline pair comprises m twists, where m is a whole number ≥ 1. The second bitline pair comprises n twists,
where \( n \) is a whole number not equal to \( m \). The twists switch the bitline paths of the bitlines within the bitline pair. The twists are located along the bitline pairs to transform coupling noise between the bitline pairs into common mode noise, which does not adversely impact signal margin.

**BRIEF DESCRIPTION OF DRAWINGS**

Fig. 1 shows a memory cell;

Fig. 2-4 show embodiments of the invention for reducing the impact of bitline coupling noise; and

Fig. 5 shows another embodiment of the invention for reducing the impact of bitline coupling noise.

**DETAILED DESCRIPTION OF THE INVENTION**

The invention relates to reducing the adverse impact of coupling noise in signal lines. In one embodiment, the invention reduces the impact of coupling noise in bitlines of ICs such as, for example, random access memories (RAMs) including dynamic RAMs (DRAMs), high speed DRAMs such as Rambus DRAMs and SLDRAMs, ferroelectric RAMs (FRAMs), synchronous DRAMs (SDRAMs), merged DRAM-logic chips (embedded DRAMs), or other types of memory ICs or logic ICs.

Fig. 2 shows a plan view of a portion of an IC with signal line pairs on first and second signal line levels
for reducing the impact of coupling noise in accordance with one embodiment of the invention. The signal lines, for example, can be differential signal lines, internal differential data lines, differential clock lines, or other types of differential signal lines.

In one embodiment, the signal lines comprise bitline pairs of a multi-level or split-level bitline architecture. A first bitline pair 210 (dotted lines) and a second bitline pair 220 (solid lines) are provided in first and second bitline planes or levels. A bitline pair comprises first and second bitlines (211 and 212 or 221 and 222). One bitline within the pair is referred to as the bitline or bitline true while the other is referred to as a reference bitline or bitline complement. The bitlines are located along bitline paths (identified by the letter p after a reference number). The different bitline levels can be realized in metal 0 (M0) and metal 1 (M1) of an IC.

The first bitline pair on the first bitline level is adjacent to the second bitline pair on the second level. The bitline paths of one bitline pair can be substantially aligned with the bitline paths of the other bitline pair. Offsetting the bitline paths of the different bitline pairs can also be useful, for example, to facilitate the coupling of memory cells to bitlines on the upper bitline level.
To reduce the impact of coupling noise between the bitline pairs, one bitline pair (either the first or the second bitline pair) comprises a twist. In one embodiment, the first bitline pair 210 comprises a twist 240. The twist divides bitline 211 and 212 into segments 211a-b and 212a-b. The twist switches the positions of the bitlines within the bitline pair (i.e., the segments of a bitline on different sides of the twist are located in different bitline paths of the bitline pair). Bitline segment 211a on the left side of the twist is in bitline path 211p while segment 211b on the right side of the twist is in bitline path 212p. Likewise bitline segments 212a and 212b are in different bitline paths.

In one embodiment, the first bitline pair comprises one twist which is located at about the middle of the bitlines, dividing the bitlines in two segments that are about equal in length (about ½ the length of the bitline). The total lengths of the bitline true and bitline complement segments on the same bitline path are about equal. By having such a configuration, the noise components from the bitlines of one bitline pair impact the bitlines of an adjacent bitline pair in the same manner, creating common mode noise which does not adversely impact the signal margin.

In another embodiment, the first bitline pair comprises m twists, where m is a whole number ≥ 1; the
second bitline pair comprises \( n \) twists, where \( n \) is a whole number \( \neq m \). The twists are employed to switch the bitline paths of the bitlines within the bitline pair. The twists separate the bitlines into a plurality of bitline segments \((m + 1 \text{ or } n + 1 \text{ if } n > 0)\). The first and second bitline pairs comprise a different number of segments since each contains a different number of twists.

The total lengths of the first and second bitline segments in a bitline path are about equal. The twist or twists are located along the bitlines such that the bitlines from one bitline pair and the bitlines from the other bitline pair along adjacent bitline paths impact each other in the same manner, causing coupling noise to be common mode noise.

Fig. 3 shows another embodiment of the invention. As shown, twists are provided in bitline pairs in upper and lower bitline levels to cause noise coupling from the bitline pairs to be common mode noise. In one embodiment, a first bitline pair 310 (dotted lines) in a first metal level comprises a twist 340; a second bitline pair 320 (solid lines) on a second metal level comprises twists 350 and 351.

The twist 340 separates bitline 311 into segments 311a-b and reference bitline 312 into segments 312a-b. The segments are substantially equal to about \( \frac{1}{4} \) the
length of the bitlines. Twists 350 and 351 separate
bitline 321 into segments 321a-c and reference bitline
322 into segments 322a-c. Segments 321a, 321c, 322a, and
322c are substantially equal to about \( \frac{1}{4} \) the length of the
bitlines while segments 321b and 322b are substantially
equal to about \( \frac{1}{4} \) the length of the bitlines. The twists
alternate the positions of the bitline segments within
the bitline pair. The total lengths of the first and
second bitline segments along a bitline path are about
equal. The twists are placed along the bitline pairs
such that the coupling noise between the bitline pairs is
transformed into common mode noise.

Fig. 4 shows yet another embodiment of the
invention. As shown, a first bitline pair 410 (dotted
lines) on a first bitline level comprises twists 450,
451, and 452. A second bitline pair 420 (solid lines) on
a second bitline level comprises a twist 440. Twists
450, 451, and 452 separate bitlines 411 and 412 of the
first bitline pair into segments 411a-d and 412a-d; twist
440 separates bitlines 421 and 422 of the second bitline
pair into segments 421a-b and 422a-b. Segments 421a-b
and 422a-b are substantially equal to about \( \frac{1}{4} \) the length
of the bitlines and segments 411a-d and 412a-d are
substantially equal to about \( \frac{1}{4} \) the length of the
bitlines. The twists alternate the positions of the
bitline segments within the bitline pair, which results
in the total lengths of the first and second bitline segments along a bitline path to be about equal. By appropriately locating the twists along the bitline pairs, coupling noise is transformed into common mode noise.

In a split-level or multi-level bitline architecture, the array comprises a plurality of bitline pairs in different bitline levels. Coupling noise from adjacent bitline pairs in the same and other bitline levels can reduce signal margin. To reduce the adverse impact of coupling noise with adjacent bitline pairs from the same and different bitline levels, twists are provided in bitline pairs in the different bitline levels.

Fig. 5 shows an array 500 in accordance with one embodiment of the invention. The array comprises building blocks 501 having bitline pairs on different bitline levels. As shown, a building block comprises a first bitline pair 510 on a first bitline level (depicted by dotted lines) which is adjacent to a second bitline pair 520 on a second bitline level (depicted by solid lines).

To reduce the impact of coupling noise between adjacent bitline pairs on the different bitline levels (inter-level bitline noise coupling), twists are provided in the bitline pairs. For example, in building block
501_j, the first bitline pair comprises \( m_j \) twists 540, where \( m_j \) is a whole number \( \geq 1 \). The second bitline pair comprises \( n_j \) twists, where \( n_j \) is a whole number not equal to \( m_j \). In one embodiment, the first bitline pair is provided with one twist 540 (\( m_j = 1 \)) while the second bitline pair has two twists 550 a - b (\( n_j = 2 \)). The twists transform coupling noise between bitline pairs 510 and 520 into common mode noise.

Adjacent building blocks 501_{j+1} comprise bitline pairs on first and second bitline levels. The adjacent building blocks similarly comprise at least one twist in one of the bitline pairs while the other bitline pair can be provided with any number (including 0) of twists that is not equal to the number of twists in the one bitline pair. The twist or twists are provided on the bitline pairs to reduce coupling noise problems between bitline pairs within the building block.

In a preferred embodiment, twists are provided in the bitline pairs of the array to reduce the impact of coupling noise with adjacent bitline pairs on different bitline levels as well as on the same bitline level (i.e., noise coupling between bitline pairs within a building block as well as with bitline pairs in neighboring or adjacent building blocks). In one embodiment, a first bitline pair 510 within a building block 501_j comprises \( m_j \) twists, where \( m_j \) is a whole number
$\geq 1$. The second bitline pair within the building block 501_j comprises $n_j$ twists, where $n_j$ is a whole number not equal to $m_j$. Illustratively, $m_j = 1$ (twist 540) and $n_j = 2$ (twists 550a-b).

In adjacent building blocks 501_j±1, the constraints of $m$ (whole number $\geq 1$) and $n$ (whole number $\neq m$) are assigned to the other bitline pair. That is, in adjacent building blocks, the first bitline pair comprises $n$ twists while the second bitline pair comprises $m$ twists. In one embodiment, the first bitline pair comprises twists 540a-b ($n_j±1 = 2$), and the second bitline pair comprises a twist 550 ($m_j±1 = 1$). The values of $m$ and $n$ need not be the same in all the building blocks of the array, as long as adjacent bitline pairs (same or different bitline level) do not contain the same number of twists. For example, $m_j±1$ does not have to be equal to $m_j{-}1$; $n_j±1$ does not have to be equal to $n_j{-}1$. By providing such a configuration, degradation of the sensing signal due to coupling noise is reduced or avoided.

As described, the building blocks are similar to the building block of Fig. 3 except that in alternating building blocks, the twist configuration in the first and second bitline pairs is switched. The use of building blocks such as those described in Fig. 2, Fig. 4, or other configurations are also useful. Also, every other
n or every other m need not be the same. The building blocks can also be interleaved together. Interleaving the building blocks causes the bitline paths of a bitline pair to be adjacent to bitline paths of another bitline pair.

While the invention has been particularly shown and described with reference to various embodiments, it will be recognized by those skilled in the art that modifications and changes may be made to the present invention without departing from the spirit and scope thereof. Merely by way of example, the invention can be useful for reducing the impact of coupling noise in any type of differential signal lines. The scope of the invention should therefore be determined not with reference to the above description but with reference to the appended claims along with their full scope of equivalents.
What is claimed is:

1. An integrated circuit comprising:
   A first signal line pair having first and second signal lines on a first signal level;
   a second signal line pair having first and second signal lines on a second signal level, the first signal pair is adjacent to the second signal pair; and
   m twists in the first signal pair, where m is a whole number equal to at least 1.

2. The integrated circuit of claim 1 wherein the twists switch signal paths of the first and second signal lines within the first signal pair.

3. The integrated circuit of claim 2 wherein the m twists separate a first and second signal lines of the first signal pair into m+1 segments.

4. The integrated circuit of claim 3 wherein a total length of the first signal line segments and a total length of the second signal line segments of the first signal pair along a signal path are substantially equal.

5. The integrated circuit of claim 4 where m = 1.
6. The integrated circuit of claim 1 wherein the m twists separate a first and second signal lines of the first signal pair into m+1 segments.

7. The integrated circuit of claim 6 wherein a total length of the first signal line segments and a total length of the second signal line segments of the first signal pair along a signal path are substantially equal.

8. The integrated circuit of claim 7 where m = 1.

9. The integrated circuit of claim 1, 2, 3, 5, 6, 7 or 8 wherein the second signal pair comprises n twists, where n is a whole number not equal to m.

10. The integrated circuit of claim 9 wherein the n twists, if n > 0, separate the first and second signal lines of the second signal pair into n+1 segments.

11. The integrated circuit of claim 10 wherein a total length of the first signal line segments and a total length of the second signal line segments of the second signal pair along a signal line path are substantially equal.
12. The integrated circuit of claim 11 wherein the twists are located along the signal line pairs to transform coupling noise between the signal line pairs into common mode noise.

13. The integrated circuit of claim 9 wherein \( n \) is equal to 2 or 3.

14. The integrated circuit of claim 13 wherein the \( n \) twists separate the first and second signal lines of the second signal pair into \( n+1 \) segments.

15. The integrated circuit of claim 14 wherein a total length of the first signal line segments and a total length of the second signal line segments of the first signal pairs along a signal line path are substantially equal.

16. The integrated circuit of claim 15 wherein the twists are located along the signal line pairs to transform coupling noise between the signal line pairs into common mode noise.

17. The integrated circuit of claim 1 wherein the first and second signal pairs comprise first and second bitline
pairs with first and second bitlines along bitline paths on first and second bitline levels.

18. The integrated circuit of claim 17 wherein the twists switch bitline paths of the first and second bitlines within the first bitline pair.

19. The integrated circuit of claim 18 wherein the m twists separate a first and second bitlines of the first bitline pair into m+1 segments.

20. The integrated circuit of claim 19 wherein a total length of the first bitline segments and a total length of the second bitline segments of the first bitline pair along a bitline path are substantially equal.

21. The integrated circuit of claim 20 where m = 1.

22. The integrated circuit of claim 17 wherein the m twists separate a first and second bitlines of the first bitline pair into m+1 segments.

23. The integrated circuit of claim 22 wherein a total length of the first bitline segments and a total length
of the second bitline segments of the first bitline pair along a bitline path are substantially equal.

24. The integrated circuit of claim 23 where m = 1.

25. The integrated circuit of claim 16, 17, 18, 19, 20, 22, 23, or 24 wherein the second bitline pair comprises n twists, where n is a whole number not equal to m.

26. The integrated circuit of claim 25 further comprises a plurality of memory cells coupled to the bitlines.

27. The integrated circuit of claim 26 wherein the n twists, if n > 0, separate the first and second bitlines of the second bitline pair into n+1 segments.

28. The integrated circuit of claim 27 wherein a total length of the first bitline segments and a total length of the second bitline segments of the second bitline pair along a bitline path are substantially equal.

29. The integrated circuit of claim 28 wherein the twists are located along the bitline pairs to transform coupling noise between the bitline pairs into common mode noise.
30. The integrated circuit of claim 29 further comprises a plurality of memory cells coupled to the bitlines.

31. The integrated circuit of claim 25 wherein n is equal to 2 or 3.

32. The integrated circuit of claim 31 wherein the n twists separate the first and second bitlines of the second bitline pair into n+1 segments.

33. The integrated circuit of claim 32 wherein a total length of the first bitline segments and a total length of the second bitline segments of the first bitline pairs along a bitline path are substantially equal.

34. The integrated circuit of claim 33 wherein the twists are located along the bitline pairs to transform coupling noise between the bitline pairs into common mode noise.

35. The integrated circuit of claim 34 further comprises a plurality of memory cells coupled to the bitlines.
Fig. 2
Fig. 3
INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER

IPC 7 H01L23/522 H01L27/108 H01L23/528 G11C11/409

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H01L G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ, WPI Data, INSPEC, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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<td>US 5 144 583 A (TAKASHIMA DAISABURO ET AL) 1 September 1992 (1992-09-01) column 9, line 17-31; figures 13,14</td>
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Patent family members are listed in annex.

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Date of actual completion of the international search

19 December 2000

Date of mailing of the international search report

28/12/2000

Name and mailing address of the ISA

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