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(54) Title: SETTING A DEFAULT READ SIGNAL BASED ON ERROR CORRECTION

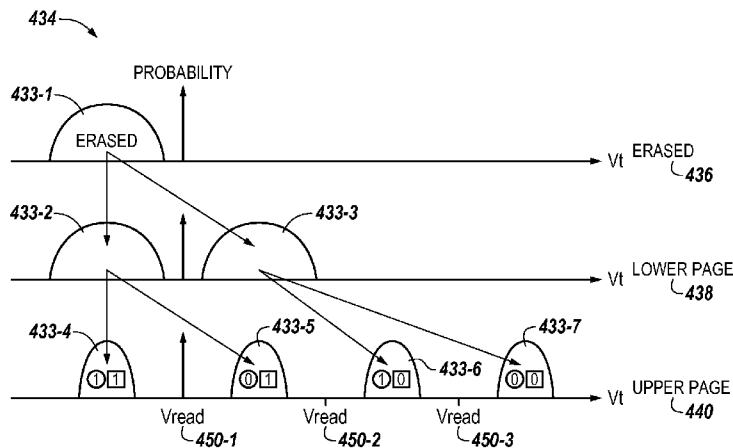


Fig. 4

(57) Abstract: The present disclosure includes apparatuses and methods related to setting a default read signal based on error correction. A number of methods can include reading a page of data from a group of memory cells with a first discrete read signal and error correcting at least one codeword of the page of data as read with the first discrete read signal. Methods can include reading a page of data from the group of memory cells with a second discrete read signal different than the first discrete read signal and error correcting at least one codeword of the page of data as read with the second discrete read signal. One of the first and the second discrete read signals can be set as a default read signal based at least in part on the respective error corrections.

## Setting a Default Read Signal Based on Error Correction

### Technical Field

[0001] The present disclosure relates generally to semiconductor memory and methods, and more particularly, to apparatuses and methods related to setting a default read signal based on error correction.

### Background

[0002] Memory devices are typically provided as internal, semiconductor, integrated circuits in computers or other electronic devices. There are many different types of memory including volatile and non-volatile memory. Volatile memory can require power to maintain its data (e.g., host data, error data, etc.) and includes random-access memory (RAM), dynamic random access memory (DRAM), and synchronous dynamic random access memory (SDRAM), among others. Non-volatile memory can provide persistent data by retaining stored data when not powered and can include NAND flash memory, NOR flash memory, read only memory (ROM), Electrically Erasable Programmable ROM (EEPROM), Erasable Programmable ROM (EPROM), and resistance variable memory such as phase change random access memory (PCRAM), resistive random access memory (RRAM), and magnetoresistive random access memory (MRAM), among others.

[0003] Memory devices can be combined together to form a storage volume of a memory system such as a solid state drive (SSD). A solid state drive can include non-volatile memory (e.g., NAND flash memory and NOR flash memory), and/or can include volatile memory (e.g., DRAM and SRAM), among various other types of non-volatile and volatile memory.

[0004] An SSD can be used to replace hard disk drives as the main storage volume for a computer, as the solid state drive can have advantages over hard drives in terms of performance, size, weight, ruggedness, operating temperature range, and power consumption. For example, SSDs can have superior performance when compared to magnetic disk drives due to their lack of moving parts, which may avoid seek time, latency, and other electro-mechanical delays associated with magnetic disk drives.

[0005] Memory is utilized as volatile and non-volatile data storage for a wide range of electronic applications. Non-volatile memory may be used in portable electronic devices, such as laptop computers, portable memory sticks, digital cameras, cellular telephones, portable music players such as MP3 players, movie players, and other electronic devices. Memory cells can be arranged into arrays, with the arrays being used in memory devices.

#### Brief Description of the Drawings

[0006] Figure 1 is a block diagram of an apparatus in the form of a computing system including at least one memory system in accordance with a number of embodiments of the present disclosure.

[0007] Figure 2 illustrates a schematic diagram of a portion of a non-volatile memory array in accordance with a number of embodiments of the present disclosure.

[0008] Figure 3 illustrates a block diagram of a memory architecture in accordance with a number of embodiments of the present disclosure.

[0009] Figure 4 illustrates a diagram of threshold voltage distributions associated with an example 2-bit memory cell in accordance with a number of embodiments of the present disclosure.

[0010] Figure 5 illustrates a plot of two threshold voltage distributions associated with adjacent data states according to some previous approaches.

[0011] Figure 6 illustrates a plot of a combined threshold voltage distribution and an error probability distribution in accordance with a number of embodiments of the present disclosure.

[0012] Figure 7A illustrates a plot of a number of errors associated with reading a plurality of pages of data with a plurality of discrete read signals in accordance with a number of embodiments of the present disclosure.

[0013] Figure 7B illustrates a plot of a number of errors associated with reading a plurality of pages of data with a plurality of discrete read signals in accordance with a number of embodiments of the present disclosure.

#### Detailed Description

[0014] The present disclosure includes apparatuses and methods related to setting a default read signal based on error correction. A number of methods

can include reading a page of data from a group of memory cells with a first discrete read signal and error correcting at least one codeword of the page of data as read with the first discrete read signal. Methods can include reading a page of data from the group of memory cells with a second discrete read signal different than the first discrete read signal and error correcting at least one codeword of the page of data as read with the second discrete read signal. One of the first and the second discrete read signals can be set as a default read signal based at least in part on the respective error corrections.

**[0015]** In the following detailed description of the present disclosure, reference is made to the accompanying drawings that form a part hereof, and in which is shown by way of illustration how one or more embodiments of the disclosure may be practiced. These embodiments are described in sufficient detail to enable those of ordinary skill in the art to practice the embodiments of this disclosure, and it is to be understood that other embodiments may be utilized and that process, electrical, and/or structural changes may be made without departing from the scope of the present disclosure. As used herein, the designators “B”, “C”, “N”, “M”, and “P”, particularly with respect to reference numerals in the drawings, indicates that a number of the particular feature so designated can be included. As used herein, “a number of” a particular thing can refer to one or more of such things (e.g., a number of memory devices can refer to one or more memory devices).

**[0016]** The figures herein follow a numbering convention in which the first digit or digits correspond to the drawing figure number and the remaining digits identify an element or component in the drawing. Similar elements or components between different figures may be identified by the use of similar digits. For example, 550 may reference element “50” in Figure 5, and a similar element may be referenced as 650 in Figure 6. As will be appreciated, elements shown in the various embodiments herein can be added, exchanged, and/or eliminated so as to provide a number of additional embodiments of the present disclosure. In addition, as will be appreciated, the proportion and the relative scale of the elements provided in the figures are intended to illustrate certain embodiments of the present invention, and should not be taken in a limiting sense.

[0017] Figure 1 is a block diagram of an apparatus in the form of a computing system 101 including at least one memory system 104 in accordance with a number of embodiments of the present disclosure. As used herein, a memory system 104, a controller 108, or a memory device 110 might also be separately considered an “apparatus.” The memory system 104 can be a solid state drive (SSD), for instance, and can include a host interface 106, a controller 108 (e.g., a processor and/or other control circuitry), and a number of memory devices 110-1, . . . , 110-C (e.g., solid state memory devices such as NAND flash devices), which provide a storage volume for the memory system 104. The memory system 104 can be a single memory device.

[0018] As illustrated in Figure 1, the controller 108 can be coupled to the host interface 106 and to the memory devices 110-1, . . . , 110-C via a plurality of channels and can be used to send data between the memory system 104 and a host 102. The interface 106 can be in the form of a standardized interface. For example, when the memory system 104 is used for data storage in a computing system 101, the interface 106 can be a serial advanced technology attachment (SATA), peripheral component interconnect express (PCIe), or a universal serial bus (USB), among other connectors and interfaces. In general, however, interface 106 can provide an interface for passing control, address, data, and other signals between the memory system 104 and a host 102 having compatible receptors for the interface 106.

[0019] Host 102 can be a host system such as a personal laptop computer, a desktop computer, a digital camera, a mobile telephone, or a memory card reader, among various other types of hosts. Host 102 can include a system motherboard and/or backplane and can include a number of memory access devices (e.g., a number of processors). Host 102 can also be a memory controller, such as where memory system 104 is a memory device (e.g., having an on-die controller).

[0020] The controller 108 can communicate with the number of memory devices 110-1, . . . , 110-C (which in some embodiments can be a number of memory arrays on a single die) to control data read, write, and erase operations, among other operations. In some embodiments, the controller 108 can be on the same die or a different die than any or all of the number of memory devices 110.

[0021] Although not specifically illustrated, in some embodiments, the controller 108 can include a discrete memory channel controller for each channel coupling the controller 108 to the memory devices 110-1, . . . , 110-C. The controller 108 can include, for example, a number of components in the form of hardware and/or firmware (e.g., one or more integrated circuits) and/or software for controlling access to the number of memory devices 110-1, . . . , 110-C and/or for facilitating data transfer between the host 102 and memory devices 110-1, . . . , 110-C.

[0022] As illustrated in Figure 1, the controller 108 can include an error correction circuit 112 and an error correction memory 114. For example, the error correction circuit 112 can include an algebraic error correction circuit such as one of the group including a Bose-Chaudhuri-Hocquenghem (BCH) error correction circuit and a Reed Solomon error correction circuit, among other types of error correction circuits. The error correction memory 114 can include volatile (e.g., DRAM, SRAM, etc.) and/or non-volatile (e.g., flash, MRAM, etc.) memory. In a number of embodiments, the error correction memory 114 can be provided by the memory devices 110-1, . . . , 110-C. Each of the error correction circuit 112 and an error correction memory 114 can be discrete components such as an application specific integrated circuit (ASIC) or the components may reflect functionally provided by circuitry within the controller 108 that does not necessarily have a discrete physical form separate from other portions of the controller 108. Although illustrated as components within the controller 108 in Figure 1, each of the error correction circuit 112 and an error correction memory 114 can be external to the controller 108 or have a number of components located within the controller 108 and a number of components located external to the controller 108.

[0023] The error correction circuit 112 can have an error correction capacity number of errors for a page of data. That is, if the page has fewer errors than the error correction capacity number of errors of the error correction circuit 112, then the page of data can be corrected. If the page has more errors, then an uncorrectable error can be reported. The error correction circuit 112 can correct up to a threshold number of bit errors per page of data (or codeword, where a page of data can include one codeword, more than one codeword, or less than a full codeword). A codeword can be an amount of data encoded with error

correction data. The error correction circuit 112 can be configured to operate on a codeword basis. However, depending on the application-specific or device-specific configuration, the error correction circuit can be said to have an error correction capacity for a page of data (depending on the interplay between page length and codeword length in terms of numbers of bits).

**[0024]** The controller 108 can also include a number of trim sets 116. The trim sets 116 can each set a default read signal for the memory devices 110-1, ..., 110-C. For example, trim sets can set a default read signal for pages, blocks, planes, dice, channels, logical units, and/or other units of memory. In a number of embodiments, the controller 108 can be configured to read data from a group of memory cells (e.g., a physical page of memory cells) within one of a plurality of dice with a plurality of discrete read signals. The controller can adjust a trim set 116 to set one of the plurality of read signals as the default read signal for the particular die. The controller 108 can include a trim set 116 for each page, block, plane, die, channel, logical unit and/or other unit of memory or the controller 108 can store a trim set 116 for groups of the units of memory. For example, a first trim set 116 can set a default read signal for a first die while a second trim set 116 can set a default read signal for a second die and a third die. The trim sets 116 for individual units of memory can be adjusted based at least in part on reading and error correcting data read from the individual units of memory, or based at least in part on reading and error correcting data read from other units of memory (e.g., reading and error correcting data from a group of memory cells in a first die can provide a default read signal for a number of groups of memory cells in the first die and a number of groups of memory cells in a second die). The controller 108 can include one trim set 116 for each memory unit (e.g., die) or the controller can include fewer trim sets 116 than the number of memory units.

**[0025]** The number of memory devices 110-1, ..., 110-C can include a number of arrays of memory cells (e.g., non-volatile memory cells). The arrays can be flash arrays with a NAND architecture, for example. However, embodiments are not limited to a particular type of memory array or array architecture. Although floating-gate type flash memory cells in a NAND architecture are generally referred to herein, embodiments are not so limited. The memory cells can be grouped, for instance, into a number of blocks

including a number of physical pages. A number of blocks can be included in a plane of memory cells and an array can include a number of planes. As one example, a memory device may be configured to store 8KB (kilobytes) of user data per page, 128 pages of user data per block, 2048 blocks per plane, and 16 planes per device.

**[0026]** In operation, data can be written to and/or read from memory (e.g., memory devices 110-1, . . . , 110-C of system 104) as a page of data, for example. As such, a page of data can be referred to as a data transfer size of the memory system. Data can be sent to/from a host (e.g., host 102) in data segments referred to as sectors (e.g., host sectors). As such, a sector of data can be referred to as a data transfer size of the host.

**[0027]** According to a number of embodiments of the present disclosure, the controller 108 can be configured to read data from a group of memory cells (e.g., a physical page of memory cells) of a memory array a plurality of times with a respective plurality of discrete read signals each having a different magnitude. The controller 108 (e.g., via error correction circuit 112) can error correct the data read from the group of memory cells with the plurality of discrete read signals and set one of the plurality of discrete read signals as a default read signal based at least in part on the error correction. After each reading and error correction, the controller 108 can store a number of errors corrected for the data read with each respective read signal in the error correction memory 114. In some embodiments, the controller 108 can set as the default, the read signal that results in the fewest errors based at least in part on the error correction results stored in the error correction memory 114. The data read from the group of memory cells can include user data (e.g., as opposed to test data from a known test data pattern). Such embodiments can be beneficial in reducing time used by writing test data and/or reducing wear on the memory 110-1, . . . 110-C from a number of program/erase cycles associated with writing test data. The data can be read, for the purposes of setting a default read signal, as a test operation (although reading user data rather than separately written test data). The test operation can be performed during idle time of the memory apparatus 110-1 . . . 110-C from which the data is read. Idle time can include time during which host operations are not being performed with respect to the memory device 110-1, . . . 110-C.



**[0028]** Figure 2 illustrates a schematic diagram of a portion of a non-volatile memory array in accordance with a number of embodiments of the present disclosure. The embodiment of Figure 2 illustrates a NAND architecture non-volatile memory array. However, embodiments described herein are not limited to this example. As shown in Figure 2, the memory array 200 includes access lines (e.g., word lines 205-1, . . . , 205-N) and intersecting data lines (e.g., local bit lines 207-1, 207-2, 207-3, . . . , 207-M). For ease of addressing in the digital environment, the number of word lines 205-1, . . . , 205-N and the number of local bit lines 207-1, 207-2, 207-3, . . . , 207-M can be some power of two (e.g., 256 word lines by 4,096 bit lines).

**[0029]** Memory array 200 includes NAND strings 209-1, 209-2, 209-3, . . . , 209-M. Each NAND string includes non-volatile memory cells 211-1, . . . , 211-N, each communicatively coupled to a respective word line 205-1, . . . , 205-N. Each NAND string (and its constituent memory cells) is also associated with a local bit line 207-1, 207-2, 207-3, . . . , 207-M. The memory cells 211-1, . . . , 211-N of each NAND string 209-1, 209-2, 209-3, . . . , 209-M are coupled in series source to drain between a source select gate (SGS) (e.g., a field-effect transistor (FET) 213) and a drain select gate (SGD) (e.g., FET 219). Each source select gate 213 is configured to selectively couple a respective NAND string to a common source 223 responsive to a signal on source select line 217, while each drain select gate 219 is configured to selectively couple a respective NAND string to a respective bit line responsive to a signal on drain select line 215.

**[0030]** As shown in the embodiment illustrated in Figure 2, a source of source select gate 213 is coupled to a common source line 223. The drain of source select gate 213 is coupled to the source of the memory cell 211-1 of the corresponding NAND string 209-1. The drain of drain select gate 219 is coupled to bit line 207-1 of the corresponding NAND string 209-1 at drain contact 221-1. The source of drain select gate 219 is coupled to the drain of the last memory cell 211-N (e.g., a floating-gate transistor) of the corresponding NAND string 209-1.

**[0031]** In a number of embodiments, construction of the non-volatile memory cells 211-1, . . . , 211-N includes a source, a drain, a floating gate or other charge storage structure, and a control gate. The memory cells 211-1, . . . ,

211-N have their control gates coupled to a word line, 205-1, . . . , 205-N, respectively. A NOR array architecture would be similarly laid out, except that the string of memory cells would be coupled in parallel between the select gates. Furthermore, a NOR architecture can provide for random access to the memory cells in the array (e.g., as opposed to page-based access as with a NAND architecture).

**[0032]** A number (e.g., a subset or all) of cells coupled to a selected word line (e.g., 205-1, . . . , 205-N) can be written and/or read together as a group. A number of cells written and/or read together can correspond to a page of data. As used herein, examples of high-level operations are referred to as writing or reading operations (e.g., from the perspective of a controller), whereas, with respect to the memory cells, such operations are referred to as programming or sensing. A group of cells coupled to a particular word line and programmed together to respective states can be referred to as a target page. A programming operation can include applying a number of program pulses (e.g., 16V-20V) to a selected word line in order to increase the threshold voltage ( $V_t$ ) of selected cells coupled to that selected word line to a desired program voltage level corresponding to a targeted state.

**[0033]** Read operations can include sensing a voltage and/or current change of a bit line coupled to a selected cell in order to determine the state of the selected cell. The read operation can include precharging a bit line and sensing the discharge when a selected cell begins to conduct. Two different types of read operations are described herein (e.g., those using a ramping read signal versus using a plurality of discrete read signals).

**[0034]** Sensing the state of a selected cell can include providing a ramping read signal (e.g., -2V to +3V) to a selected word line, while providing a signal (e.g., a pass voltage such as 4.5V) to word lines coupled to the unselected cells of the string sufficient to place the unselected cells in a conducting state independent of the charge stored on the unselected cells. Alternatively, sensing the state of a selected cell could include applying discrete read signals (e.g., -.05V, 0.5V, and 2V) to a selected word line, and thus to the control gate of a selected cell. The bit line corresponding to the selected cell being read and/or verified can be sensed to determine whether or not the selected cell conducts in response to the particular read signal applied to the selected word line. For

example, the state of a selected cell can be determined by the word line voltage at which the bit line current reaches a particular reference current associated with a particular state.

**[0035]** According to a number of embodiments of the present disclosure, default read signals can be set based on location within a string of memory cells 209-1, 209-2, 209-3, . . . , 209-M. For example, with respect to Figure 2, those memory cells coupled to word line 205-1 along an edge of the strings 209-1, 209-2, 209-3, . . . , 209-M closer to source select gate 213 may have a different default discrete read signal than those memory cells coupled to word line 205-N along an edge of the strings 209-1, 209-2, 209-3, . . . , 209-M closer to drain select gate 219. Data can be read from a first group of memory cells with a plurality of discrete read signals, where reading the first group of memory cells includes sensing a first memory cell 211-1 from a particular string 209-1 of memory cells. Data can be read from a second group of memory cells with the discrete read signals including sensing a second memory cell 211-N from the particular string 209-1 of memory cells. A first one of the discrete read signals that results in (e.g., returns, generates, etc.) the fewest number of errors during error correction of the data read from the first group of memory cells can be set as a default read signal for with memory cells coupled to a same word line 205-1 as the first memory cell 211-1. A second one of the discrete read signals that results in the fewest number of errors during error correction of the data read from the second group of memory cells can be set as a default read signal for memory cells coupled to a same word line 205-N as the second memory cell 211-N.

**[0036]** Setting a default read signal based on location within a string of memory cells 209-1, 209-2, 209-3, . . . , 209-M can include setting a default read signal for each location (e.g., word line) within the string of memory cells 209-1, 209-2, 209-3, . . . , 209-M or for groups of locations (e.g., more than one word line). For example, a default read signal can be set for memory cells coupled to a particular word line and a number of word lines adjacent thereto. The adjacent word lines can be directly adjacent to the particular word line or within a threshold number of word lines proximal to the particular word line. In a number of embodiments, a first default read signal can be set for a particular location (e.g., word line) within a string 209-1, 209-2, 209-3, . . . , 209-M and a

second default read signal can be set for other locations (e.g., more than one other word line) within the string 209-1, 209-2, 209-3, . . . , 209-M.

**[0037]** Default read signals can be set based on an odd and even page basis. Pages of memory cells can be divided between odd and even numbered memory cells along a word line. In one or more embodiments, an “odd” or “even” page of data can be a logical representation of data where data from half (the “odd” numbered) of the memory cells coupled to a word line are stored in an “odd” page and data from the other half (the “even” numbered) of the memory cells coupled to the word line are stored in an “even” page. For example, memory cells selectively coupled to a particular word line 205-1 and to bit lines 207-1, 207-3, and other odd numbered bit lines may be said to store an odd page of data while memory cells coupled to word line 205-1 and bit lines 207-2, and other even numbered bit lines, and 207-M may be said to store an even page of data. Other examples are provided below with respect to Figure 3. Different default read signals can be set for upper pages of data and lower pages of data.

**[0038]** Data from a first group of memory cells can be read with a plurality of discrete read signals, where reading the data includes sensing a first portion of the plurality of memory cells coupled to a word line. Data from a second group of memory cells can be read with the discrete read signals, where reading the data from the second group of memory cells can include sensing a second portion of the memory cells coupled to the word line. A first one of the discrete read signals that results in the fewest number of errors during error correction of the data read from the first group of memory cells can be set as a default read signal for memory cells coupled to the same bit lines as the first portion of the plurality of memory cells. A second one of the discrete read signals that results in the fewest number of errors during error correction of the data read from the second group of memory cells can be set as a default read signal for memory cells coupled to the same bit lines as the second portion of the plurality of memory cells.

**[0039]** Figure 3 illustrates a block diagram of a memory architecture in accordance with a number of embodiments of the present disclosure. Figure 3 includes two memory dice 318-1 and 318-2 with two planes each, 320-1, 320-2, 320-3 and 320-4. Each plane includes a number of blocks 322-1, 322-2, . . . ,

322-B. As described herein, a block of memory cells can be erased together in one erase operation. Each block includes a number of pages (e.g., pages 324-1, 324-2, . . . , 324-P, included in block 1, 322-1). As described herein, a page of memory cells can be written or read together in one write or read operation. Each plane is in bidirectional communication with a data register 326-1, 326-2, 326-3, 326-4 respectively. Each data register is in bidirectional communication with a cache register 328-1, 328-2, 328-3, 328-4 respectively.

**[0040]** Data can be transferred from a data register 326-1, 326-2, 326-3, 326-4 to a memory plane 320-1, 320-2, 320-3, 320-4 during write operations. Data can be transferred from a memory plane 320-1, 320-2, 320-3, 320-4 to a data register 326-1, 326-2, 326-3, 326-4 during read operations. A cache register 328-1, 328-2, 328-3, 328-4 can output data to input/output (I/O) circuitry at 332 and can receive data from I/O circuitry at 330. Although not specifically illustrated, each cache register can have a separate I/O path. A cache register 328-1, 328-2, 328-3, 328-4 can communicate data with I/O circuitry through a number of data cycles. During non-cache operations, the data registers 326-1, 326-2, 326-3, 326-4 and cache registers 328-1, 328-2, 328-3, 328-4 can operate together as single registers.

**[0041]** During cache operations, data registers 326-1, 326-2, 326-3, 326-4 and cache registers 328-1, 328-2, 328-3, 328-4 can operate separately in a pipelined process. For example, a next sequential access from the array can be pipelined while outputting previously-accessed data. Such a double-buffered technique can allow read access time to be hidden. Data can be first transferred from a memory array to a data register 326-1, 326-2, 326-3, 326-4. If the cache register 328-1, 328-2, 328-3, 328-4 is available (not busy), the data can be moved from the data register 326-1, 326-2, 326-3, 326-4 to the cache register 328-1, 328-2, 328-3, 328-4. Once the data is transferred to the cache register 328-1, 328-2, 328-3, 328-4, the data register 326-1, 326-2, 326-3, 326-4 is available and can start to load the next sequential page from the memory array.

**[0042]** Plane 320-1 can represent half of the blocks on die 318-1, while plane 320-2 can represent the other half. Plane 320-3 can represent half of the blocks on die 318-2, while plane 320-4 can represent the other half. In one or more embodiments, planes can be divided between odd and even numbered blocks. In one or more embodiments, an “odd” or “even” plane of data can be a

logical representation of data where data units from half (the “odd” numbered) of the memory cells coupled to access lines associated with the die are stored in an “odd” plane and data units from the other half (the “even” numbered) of the memory cells coupled to access lines associated with the die are stored in an “even” plane. Embodiments are not limited to a particular plane representing half of the blocks on a given die having more than one plane; other distributions of blocks between planes are possible. Nor are embodiments limited to memory devices with a particular number of blocks, planes, or dice. According to a number of embodiments of the present disclosure, default read signals can be set for a number of dice 318-1, 318-2, a number of planes 320-1, 320-2, 320-3, 320-4, a number of blocks 322-1, 322-2, . . . , 322-B, and/or a number of pages 324-1, 324-2, . . . , 324-P of memory cells.

**[0043]** Figure 4 illustrates a diagram 434 of threshold voltage distributions 433 associated with an example 2-bit memory cell in accordance with a number of embodiments of the present disclosure. Embodiments are not limited to multilevel memory cells being programmed with two bits of data. One or more embodiments of the present disclosure can include a particular memory cell being programmed with more than two bits and/or a fractional number of bits of data.

**[0044]** As part of an erase operation 436, the  $V_t$  of a memory cell can be placed in a  $V_t$  distribution 433-1. As part of a lower page programming operation 438, one or more programming pulses can be applied to memory cells to program the cells to one of a number of intermediate  $V_t$  distributions (e.g.,  $V_t$  distributions 433-2 and 433-3). In this example, those cells whose lower page is to be programmed with data “1” are programmed to intermediate  $V_t$  distribution 433-2 and those cells whose lower page is to be programmed with data “0” are programmed to intermediate  $V_t$  distribution 433-3 during lower page programming operation. Subsequently, as part of an upper page programming operation 440, one or more programming pulses can be applied to the memory cells to program the cells from one of the intermediate  $V_t$  distributions 433-2 and 433-3 to one of  $V_t$  distributions 433-4, 433-5, 433-6, and 433-7, which correspond to data states 11, 01, 10, and 00, respectively. In this example, cells whose lower page is programmed with data “1” are programmed from  $V_t$  distribution 433-2 to one of  $V_t$  distributions 433-4 or 433-5 during upper page

programming 440. Those cells whose lower page is programmed with data “0” are programmed from Vt distribution 433-3 to one of Vt distributions 433-6 or 433-7 during upper page programming 440. In this 2-bit memory cell example, the least significant bit (shown inside squares in Figure 4) of a data state corresponds to the lower page of data and the most significant bit (shown inside circles in Figure 4) of a data state corresponds to the upper page of data. As an example, cells programmed to Vt distribution 433-6 store data “10”, with “0” corresponding to the lower page data and “1” corresponding to the upper page data. However, embodiments are not limited to 2-bit cells or to the particular data values illustrated in Figure 4.

**[0045]** For a particular programming operation, a lower page of data and a corresponding upper page of data are programmed to the same physical memory cells (e.g., the same physical page of memory cells). As will be appreciated, methods for programming multilevel memory cells with a number of bits other than two can be extrapolated from the description herein. For example, a 3-bit memory cell can be programmed with a lower page of data and a number of middle pages of data before being programmed with an upper page of data to a final state. Embodiments described herein with a 2-bit cell are illustrative for purposes of explanation, and do not limit the present disclosure to operation of 2-bit memory cells. Furthermore, the use of “1s” and “0s” and the terms “upper” and “lower” are used herein to illustrate examples and do not limit the present disclosure to a particular notation or data arrangement.

**[0046]** The diagram 434 includes an illustration of a number of read signals (e.g., Vread) 450-1, 450-2, 450-3. Read signal 450-2 can be used as part of a read operation of a lower page to distinguish data states 11 and 01 from data states 10 and 00. For example, if lower page read signal 450-2 is applied and a particular memory cell conducts in response, then the particular memory cell is in one of data states 11 and 01, which indicates that the lower page bit is 1. However, if read signal 450-2 is applied and the particular memory cell does not conduct, then the particular memory cell is in one of data states 10 and 00, which indicates that the lower page bit is 0. First upper page read signal 450-1 can be used to distinguish data state 11 from 01. Second upper page read signal 450-3 can be used to distinguish data state 10 from 00.

[0047] A number of embodiments of the present disclosure can be used to set the magnitude of one or more of the read signals 450-1, 450-2, 450-3. For example, to set the magnitude of lower page read signal 450-2, a group of memory cells can be read with a first plurality of lower page discrete read signals (e.g., where each discrete read signal has a different magnitude in the range of read signal 450-2 as illustrated in Figure 4). Read signals can be in the range of read signal 450-2 by including those magnitudes between data states 01 and 10 and/or potentially including magnitudes that are within portions of data states 01 and 10 in order to set a default magnitude of the read signal 450-2.

[0048] The data read from the group of memory cells using the plurality of lower page discrete read signals, for example at least one codeword, can be error corrected. One of the first plurality of discrete read signals can be set as a default read signal for the lower page of data based at least in part on the error correction. A number of errors corrected during error correction after each reading of the group of memory cells for each of the plurality of discrete read signals can be counted (for those discrete read signals that do not result in an uncorrectable error) and compared to set one of the discrete read signals as a default read signal based at least in part on the comparison (e.g., one of the discrete read signals that results in the fewest number of errors). Such a process can be repeated with different pluralities of discrete read signals to set default read signal magnitudes for each of read signals 450-1 and 450-3. For example, first upper page data from the group of memory cells can be read with each of a second plurality of discrete read signals (e.g., in the range of read signal 450-1). The first upper page data read from the group can be error corrected for each reading thereof and one of the second plurality of discrete read signals can be set as a default for the first upper page based at least in part on the error correction. Second upper page data can be read from the group of memory cells with each of a third plurality of discrete read signals (e.g., in the range of read signal 450-3). Error correction can be performed for each reading thereof and one of the third plurality of discrete read signals can be set as the default for the second upper page of data based at least in part on the error correction.

[0049] Reading the data can entail reading a particular type of page of data such as a lower page, middle page (not specifically illustrated), or upper page of data. Thus, a default read signal can be set for a particular page type.



Although not specifically illustrated, the above-described process can be repeated to set a default read signal for reading a middle page of data. As illustrated in Figure 4, the upper page of data can be read with two discrete read signals 450-1 and 450-3. More than one default read signal can be set for page types that are read with more than one discrete read signal. A different default read signal can be set for upper page data than for lower page data.

**[0050]** Figure 5 illustrates a plot 534 of two threshold voltage distributions associated with adjacent data states according to some previous approaches. The plot 534 includes a first threshold voltage ( $V_t$ ) distribution (e.g., for data state 0) and a second  $V_t$  distribution (e.g., for data state 1). The x-axis of the plot 534 illustrates increasing  $V_t$  and the y-axis illustrates increasing probability (population of the  $V_t$  distribution). Such information can be gathered, for instance, from soft data associated with a read operation. For example, a page of memory cells can be read and soft data can be obtained from the use of a voltage ramp, which can indicate a more exact charge stored on a particular memory cell or from using a more than one discrete read signal for each particular data state to more accurately determine the charge stored on a particular memory cell. This soft data, over the page of memory cells, can result in the solid line 544 on the plot 534. That is, a memory system can determine a distribution of cells with each particular  $V_t$  level, but, from this soft data alone, it may not be clear which cells correspond to which data state. That is, soft data can indicate more exactly, a charge stored on a cell, but not to which data state the cell was supposed to be programmed.

**[0051]** The dashed lines 546-0 and 546-1 illustrate a remainder of the plots of the first data state 0 and the second data state 1 respectively (e.g., if perfect information were available indicating the specific charge stored on each cell and to which data state it was supposed to be programmed). Such perfect information may be available with the use of test data, where the page is programmed with known test data. According to some previous approaches, a read signal may be set based on a valley between  $V_t$  distributions for adjacent data states (here, state 0 and state 1). In Figure 5, this read signal is illustrated at 550, which is set in the valley between state 0 and state 1. The areas 548-0 and 548-1 under the dashed lines 546-0 and 546-1 illustrate the respective errors associated with using read signal 550 to distinguish between data state 0 and data

state 1. Using read signal 550 to distinguish between data state 0 and data state 1 would result in errors for those cells indicated by area 548-0, which were programmed to data state 0, but which would be read as data state 1 and for those cells indicated by area 548-1, which were programmed to data state 1, but which would be read as data state 0. For those instances when the  $V_t$  distributions for adjacent data states are non-symmetric, the errors are also non-symmetric (e.g., there are more errors represented by area 548-0 than by area 548-1). In such instances, using a read signal defined by a valley can result in more errors than would occur with a different read signal.

**[0052]** Rather than setting a default read signal based on a valley between  $V_t$  distributions of adjacent data states, a number of embodiments of the present disclosure can read data from a group of memory cells (e.g., a physical page) with a plurality of discrete read signals, error correct the data read with the plurality of discrete read signals, and set a default read signal based at least in part on the discrete read signal that results in a fewest number of errors. Such embodiments do not require the use of known test data or other knowledge of a correlation between data states and  $V_t$  distributions that could provide information about areas 546-0 and 546-1. Furthermore, soft data sufficient to provide a plot 534 of  $V_t$  distributions as illustrated in Figure 5 does not have to be gathered for such embodiments because they are based at least in part on minimizing errors from multiple discrete hard reads rather than requiring soft data.

**[0053]** Figure 6 illustrates a plot 635 of a combined threshold voltage distribution 637 and an error probability distribution 639 in accordance with a number of embodiments of the present disclosure. The plot 635 includes a  $V_t$  distribution 637 representing a summation of the  $V_t$  distributions for data states 0 and 1 respectively from Figure 5. The plot 635 includes an error probability distribution 639 for a given magnitude of a read signal, where the magnitude is indicated by the x-axis. The x-axis of the plot 635 illustrates increasing  $V_t$  and/or magnitude of a read signal, the left y-axis illustrates increasing probability (population of the  $V_t$  distribution), and the right y-axis illustrates an increasing probability of error.

**[0054]** The plot 635 illustrates a first read level 650-1 and a second read level 650-2. The read levels can correspond to a magnitude of a discrete read

signal. For example, first read level 650-1 can correspond to a magnitude of a first discrete read signal and second read level 650-2 can correspond to a magnitude of a second discrete read signal. The first read level 650-1 represents a read level that could be set according to some previous approaches that set a default read level in a valley between  $V_t$  distributions of adjacent data states. As illustrated, the first read level 650-1 is set at a minimum point in the summation  $V_t$  distribution 637 of adjacent data states 0 and 1. However, the second read level 650-2 represents a read level set according to a number of embodiments of the present disclosure based at least in part on a minimizing a number of errors that result from the read level. Along error probability distribution 639, all other read levels result in more errors, but the read level 650-2 results in a minimum number of errors, resulting in more accurate reads than would otherwise be provided by setting a read level 650-1 in a valley between  $V_t$  distributions of adjacent data states. The error probability distribution 639 can be obtained by sweeping a read level across a plurality of magnitudes, reading data page of memory cells with each read level, error correcting the data read with each read level, counting the number of errors for each read level, and extrapolating therefrom.

**[0055]** Figure 7A illustrates a plot 752A of a number of errors associated with reading a plurality of units of memory with a discrete read signal in accordance with a number of embodiments of the present disclosure. The plot 752A includes distributions of a number of errors versus magnitudes of read signals for each of four memory units (e.g., Page A, Page B, Page C, Page D) and an average of the four memory units (e.g., Pavg). The x-axis of the plot 752A illustrates increasing  $V_t$  and/or magnitude of a read signal, the y-axis illustrates an increasing probability of error. Plot 752A includes distributions for reads associated with a first data state (e.g., data state 00 and/or lower pages). The four memory units can be spatially averaged to result in Pavg. Spatial averaging can minimize noise resulting from sampling (e.g., versus simple averaging and a global minimum function). The four memory units can be topologically distributed throughout an array of memory cells, can be topologically distributed throughout a memory system (e.g., a plurality of dice), can be from a single block, or from different blocks of memory cells. A minimum (e.g., a valley) of any of the four memory units, the average of each of

the minimums or the minimum of  $P_{avg}$  can be set as a magnitude of a default read signal.

[0056] Figure 7B illustrates a plot 752B of a number of errors associated with reading a plurality of units of memory with a discrete read signal in accordance with a number of embodiments of the present disclosure. The plot 752B includes distributions of a number of errors versus magnitudes of read signals for each of four memory units (e.g., Page A, Page B, Page C, Page D) and an average of the four memory units (e.g.,  $P_{avg}$ ). The x-axis of the plot 752B illustrates increasing  $V_t$  and/or magnitude of a read signal, the y-axis illustrates an increasing probability of error. Plot 752B includes distributions for reads associated with a second data state (e.g., data state 01 and/or upper pages). The four memory units can be spatially averaged to result in  $P_{avg}$ . Spatial averaging can minimize noise resulting from sampling (e.g., versus simple averaging and a global minimum function). The four memory units can be topologically distributed throughout an array of memory cells, can be topologically distributed throughout a memory system (e.g., a plurality of dice), can be from a single block, or from different blocks of memory cells. A minimum (e.g., a valley) of any of the four memory units, the average of each of the minimums, or the minimum of  $P_{avg}$  can be set as a magnitude of a default read signal.

[0057] According to a number of embodiments of the present disclosure, reading a group of memory cells with more than one discrete read signal comprises separate hard reads rather than one soft read operation. That is, each data read with a different discrete read signal can be error corrected to determine a number of errors according to the data read with the discrete signal on a macro level (e.g., on a page and/or codeword basis), whereas with a soft read operation, each successive read (for those soft read operations using multiple discrete signals as opposed to a ramping signal) may be used to more accurately determine a particular charge stored on memory cells. Using more than one discrete read, error correcting for each read, and setting a default read signal accordingly does not provide greater detail about a charge stored on any particular memory cell, but rather can provide greater detail about which read level can provide fewer errors over a page of memory cells.

[0058] According to a number of embodiments of the present disclosure, reading a group of memory cells with more than one discrete read signal, error correcting the data read with each of the discrete read signals for each read, and setting a default read signal (e.g., to minimize a number of errors according to the error correction) is different than adjusting a read signal based on an uncorrectable error reported from error correction circuitry. For instance, some previous approaches to setting a read signal may have included incrementally adjusting a read signal that previously resulted in an uncorrectable error being reported from error correction circuitry until such an uncorrectable error is not reported. However, such an approach merely provides a read signal that passes error correction without any knowledge provided as to whether the read signal is better or worse (in terms of number of errors resulting) than any other read signal that passes error correction. Furthermore, such an approach would be likely to yield a read signal that would tend to result in a relatively high number of errors because the incremental adjustments of the read signal would tend to set the read signal distal to a valley in an error probability distribution (see, for example, error probability distribution 639 in Figure 6). In contrast, a number of embodiments of the present disclosure can set a read signal that significantly reduces a resulting number of errors versus simply avoiding an uncorrectable error, or even setting a read level based on a valley between threshold voltage distributions for adjacent data states.

#### Conclusion

[0059] The present disclosure includes apparatuses and methods related to setting a default read signal based on error correction. A number of methods can include reading a page of data from a group of memory cells with a first discrete read signal and error correcting at least one codeword of the page of data as read with the first discrete read signal. Methods can include reading a page of data from the group of memory cells with a second discrete read signal different than the first discrete read signal and error correcting at least one codeword of the page of data as read with the second discrete read signal. One of the first and the second discrete read signals can be set as a default read signal based at least in part on the respective error corrections.

[0060] Although specific embodiments have been illustrated and described herein, those of ordinary skill in the art will appreciate that an arrangement calculated to achieve the same results can be substituted for the specific embodiments shown. This disclosure is intended to cover adaptations or variations of one or more embodiments of the present disclosure. It is to be understood that the above description has been made in an illustrative fashion, and not a restrictive one. Combination of the above embodiments, and other embodiments not specifically described herein will be apparent to those of skill in the art upon reviewing the above description. The scope of the one or more embodiments of the present disclosure includes other applications in which the above structures and methods are used. Therefore, the scope of one or more embodiments of the present disclosure should be determined with reference to the appended claims, along with the full range of equivalents to which such claims are entitled.

[0061] In the foregoing Detailed Description, some features are grouped together in a single embodiment for the purpose of streamlining the disclosure. This method of disclosure is not to be interpreted as reflecting an intention that the disclosed embodiments of the present disclosure have to use more features than are expressly recited in each claim. Rather, as the following claims reflect, inventive subject matter lies in less than all features of a single disclosed embodiment. Thus, the following claims are hereby incorporated into the Detailed Description, with each claim standing on its own as a separate embodiment.

What is claimed is:

1. A method, comprising:
  - reading a page of data from a group of memory cells with a first discrete read signal;
  - error correcting at least one codeword of the page of data as read with the first discrete read signal;
  - reading a page of data from the group of memory cells with a second discrete read signal different than the first discrete read signal;
  - error correcting at least one codeword of the page of data as read with the second discrete read signal;
  - setting one of the first and the second discrete read signals as a default read signal based at least in part on the respective error corrections.
2. The method of claim 1, wherein error correcting the at least one codeword of the page of data comprises correcting within an error correction capacity number of errors in the at least one codeword of the page of data.
3. The method of claim 1, wherein setting one of the first and the second discrete read signals comprises setting one of the first and the second discrete read signals that results in a fewer number of errors according to the error corrections.
4. The method of claim 1, wherein error correcting the at least one codeword of the page of data includes counting a number of errors corrected.
5. The method of claim 1, wherein the second discrete read signal has a different magnitude than the first discrete read signal.
6. The method of any one of claims 1-5, wherein error correcting the at least one codeword of the page of data comprises error correcting all codewords of the page of data.
7. The method of any one of claims 1-5, wherein the method includes:

reading a page of data from the group of memory cells with at least one additional discrete read signal different than the first and the second discrete read signals; and

error correcting at least one codeword of the page of data as read with each of the at least one additional discrete read signal;

wherein setting one of the first and the second discrete read signals as a default read signal comprises setting one of the first, the second, and the at least one additional discrete read signals as the default read signal.

8. The method of any one of claims 1-5, wherein the method includes:
- reading a page of data from the group of memory cells with a third discrete read signal different than the first and the second discrete read signals;
- error correcting at least one codeword of the page of data as read with the third discrete read signal;
- reading a page of data from the group of memory cells with a fourth discrete read signal different than the first, second, and third discrete read signals;
- error correcting at least one codeword of the page of data as read with the fourth discrete read signal; and
- setting one of the third and the fourth discrete read signals as an additional default read signal based at least in part on the respective error corrections.

9. The method of claim 8, wherein the method includes using the default read signal and the additional default read signal as read signals to distinguish different data states.

10. A method, comprising:
- reading data from a group of memory cells with a plurality of discrete read signals;
- counting a number of errors corrected for the data read with each of the plurality of discrete read signals that do not return an uncorrectable error;
- comparing the number of errors for each of the plurality of discrete read signals:



setting one of the plurality of discrete read signals as a default read signal based at least in part on the comparison.

11. The method of claim 10, wherein setting one of the plurality of discrete read signals as the default read signal based at least in part on the comparison comprises setting the one of the plurality of discrete read signals that results in a fewest number of errors as the default read signal.

12. The method of claim 10, wherein reading the data comprises reading a particular type of page of data from the group of memory cells, wherein the particular type of pages of data is selected from the group including a lower page of data, a middle page of data, and an upper page of data.

13. The method of claim 12, wherein comparing the number of errors comprises comparing the number of errors for the particular type of page of data; and

wherein setting one of the plurality of discrete read signals as the default read signal based at least in part on the comparison comprises setting the one of the plurality of discrete read signals that results in a fewest number of errors for the particular type of page of data as the default read signal for the particular type of page of data.

14. The method of claim 10, wherein reading the data with the plurality of discrete read signals comprises reading the data with the plurality of read signals each having a different magnitude.

15. The method of any one of claims 10-14, wherein the method includes error correcting a respective page of data read from the group of memory cells with each of the plurality of discrete read signals.

16. The method of claim 15, wherein counting the number of errors corrected comprises counting the number of errors corrected during error correction after each reading of the group of memory cells with each of the plurality of discrete read signals.

17. The method of claim 10, wherein reading the data comprises reading a page of data from the group of memory cells that includes user data.
18. The method of claim 10, wherein reading the data comprises reading the data with the plurality of discrete read signals as a test operation during idle time of a memory device.
19. The method of any one of claims 10 or 17-18, wherein counting the number of errors corrected comprises counting the number of errors corrected for a particular die;  
wherein comparing the number of errors comprises comparing the number of errors for the particular die; and  
wherein setting one of the plurality of discrete read signals as the default read signal based at least in part on the comparison comprises setting the one of the plurality of discrete read signals that results in a fewest number of errors for the particular die as the default read signal for the particular die.
20. A method, comprising:  
reading a lower page data from a group of memory cells with each of a plurality of lower page discrete read signals;  
error correcting the lower page data read with the plurality of lower page discrete read signals;  
setting one of the plurality of lower page discrete read signals as a default lower page read signal for the group of memory cells based at least in part on the error correction;  
reading upper page data from the group of memory cells with each of a plurality of upper page discrete read signals;  
error correcting the upper page data read with the plurality of upper page discrete read signals; and  
setting one of the plurality of upper page discrete read signals as a default upper page read signal for the group of memory cells based at least in part on the error correction.

21. The method of claim 20, wherein the upper page data comprises first upper page data, wherein the upper page discrete read signals comprises first upper page discrete read signals, and wherein the method includes:

reading second upper page data from the group of memory cells with each of a plurality of second upper page discrete read signals;

error correcting second upper page data read with the plurality of second upper page discrete read signals; and

setting one of the plurality of second upper page discrete read signals as a default second upper page read signal for the group of memory cells based at least in part on the error correction.

22. The method of claim 20, wherein the method includes:

reading middle page data from the group of memory cells with each of a plurality of middle page discrete read signals;

error correcting the middle page data read with the plurality of middle page discrete read signals; and

setting one of the plurality of middle page discrete read signals as a default middle page read signal for the group of memory cells based at least in part on the error correction.

23. The method of any one of claims 20-22, wherein setting one of the plurality of lower page discrete read signals as a default lower page read signal for the group of memory cells comprises setting as the default lower page read signal one of the plurality of lower page discrete read signals that results in a fewest number of errors based at least in part on the error correction.

24. An apparatus, comprising:

a memory array; and

a controller coupled to the memory array, wherein the controller is configured to:

read data from a group of memory cells of the memory array a plurality of times with a respective plurality of discrete read signals each having a different magnitude;

error correct the data read with the plurality of discrete read signals; and

set one of the plurality of discrete read signals as a default read signal based at least in part on the error correction.

25. The apparatus of claim 24, wherein the controller is configured to set the one of the plurality of discrete read signals as the default read signal that results in the fewest number of corrected errors based at least in part on the error correction.

26. The apparatus of claim 24, wherein the apparatus includes a plurality of dice, each including at least one memory array; and

wherein the controller is configured to set the one of the plurality of discrete read signals as the default read signal for a number of the plurality of dice.

27. The apparatus of any one of claims 24-26, wherein the group of memory cells includes a plurality of memory cells coupled by an access line and a plurality of data lines; and

wherein the controller is configured to:

read the data from a portion of the group of memory cells that are coupled to a portion of the plurality of data lines; and

set the one of the plurality of discrete read signals as the default read signal for memory cells coupled to the portion of the plurality of data lines.

28. The apparatus of any one of claims 24-26, wherein the memory array includes a plurality of strings of memory cells, wherein each string of memory cells of the array is coupled to a respective data line; and

wherein the controller being configured to read the data from the group of memory cells comprises the controller being configured to sense at least one memory cell from the group of memory cells; and

wherein the controller being configured to set comprises the controller being configured to set the one of the plurality of discrete read signals as the

default read signal for memory cells coupled to a same access line as the at least one memory cell from the group of memory cells.

29. The apparatus of any one of claims 24-26, wherein the memory array includes a plurality of planes of memory cells; and

wherein the controller being configured to read, error correct, and set comprises the controller being configured to:

read the data from a first plane of the memory array;

set the one of the plurality of discrete read signals as a default read signal for the first plane;

read data from a second plane of the memory array a plurality of times with the respective plurality of discrete read signals;

error correct the data read from the second plane with the plurality of discrete read signals; and

set one of the plurality of discrete read signals as a default read signal for the second plane based at least in part on the error correction.

30. The apparatus of claim 24, wherein the controller is configured to set a different default read signal for reading an upper page of data than for reading a lower page of data.

31. The apparatus of any one of claims 24-26, wherein the memory array includes a plurality of blocks of memory cells; and

wherein the controller being configured to read, error correct, and set comprises the controller being configured to:

read data from each of a portion of the plurality of blocks a plurality of times with the respective plurality of discrete read signals;

error correct the data read from the portion of the plurality of blocks with the plurality of discrete read signals; and

set as the default read signal the one of the plurality of discrete read signals that results in a fewest number of errors averaged across the portion of blocks as the default read signal.

32. The apparatus of claim 31, wherein the portion of blocks are topologically distributed throughout the memory array.
33. An apparatus, comprising:  
a memory comprising units of memory; and  
a controller coupled to the memory;  
wherein the controller includes a plurality of trim sets each setting a default read signal for at least one unit of the memory; and  
wherein the controller is configured to:  
read data from a group of memory cells within one of the units of memory with a plurality of discrete read signals; and  
adjust one of the plurality of trim sets to set one of the plurality of discrete read signals as the default read signal for the one of the units of memory.
34. The apparatus of claim 33, wherein the controller being configured to adjust comprises the controller being configured to adjust the one of the plurality of trim sets to set the one of the plurality of discrete read signals as the default read signal for more than one of the units of memory.
35. The apparatus of any one of claims 33-34, wherein the controller is configured to:  
read data from a group of memory cells within a second one of the units of memory with the plurality of discrete read signals; and  
adjust a second one of the plurality of trim sets to set a second one of the plurality of discrete read signals that results in the fewest number of errors during error correction of the data read from the group of memory cells within the second unit of memory as the default read signal for the second unit of memory.
36. The apparatus of claim 35, wherein the controller being configured to adjust the second one of the plurality of trim sets comprises the controller being configured to adjust the second one of the plurality of trim sets to set the second

one of the plurality of discrete read signals as the default read signal for the second unit of memory and at least one other unit of memory.

37. The apparatus of claim 35, wherein the second one of the plurality of discrete read signals has a same magnitude as the one of the plurality of discrete read signals.

38. The apparatus of claim 35, wherein the second one of the plurality of discrete read signals has a different magnitude than the one of the plurality of discrete read signals.

39. The apparatus of any one of claims 33-34, wherein the plurality of trims sets are fewer than the units of memory.

40. The apparatus of any one of claims 33-34, wherein the plurality of trims sets are equal to the units of memory.

41. The apparatus of any one of claims 33-34, wherein the units of memory comprise one of the group of units of memory including pages, blocks, planes, dice, channels, and logical units.

42. An apparatus, comprising:

a memory array including a plurality of memory cells coupled by an access line; and

a controller coupled to the memory array, wherein the controller is configured to:

read data from a first group of the plurality of memory cells with a plurality of discrete read signals;

read data from a second group of the plurality of memory cells with the plurality of discrete read signals;

set a first one of the plurality of discrete read signals that results in the fewest number of errors during error correction of the data read from the group of the plurality of memory cells as a default read signal for memory cells

coupled to a same plurality of data lines as the first group of the plurality of memory cells; and

set a second one of the plurality of discrete read signals that results in the fewest number of errors during error correction of the second group of the plurality of memory cells as a default read signal for memory cells coupled to a same plurality of data lines as the second group of the plurality of memory cells.

43. The apparatus of claim 42, wherein the default read signal comprises a read signal selected from the group including an upper page read signal and a lower page read signal.

44. An apparatus, comprising:

a memory array including a plurality of strings of memory cells, wherein each string of memory cells in the array is coupled to a respective data line; and

a controller coupled to the memory array, wherein the controller is configured to:

read data from a first memory cell of a particular string of memory cells with a plurality of discrete read signals;

read data from a second memory cell of the particular string of memory cells with the plurality of discrete read signals;

set a first one of the plurality of discrete read signals that results in the fewest number of errors during error correction of the data read from the first memory cell as a default read signal for memory cells coupled to a same access line as the first memory cell; and

set a second one of the plurality of discrete read signals that results in the fewest number of errors during error correction of the data read from the second memory cell as a default read signal for memory cells coupled to a same access line as the second memory cell.

45. The apparatus of claim 44, wherein the controller is configured to set the first one of the plurality of discrete read signals as the default read signal for memory cells coupled to an access line adjacent to the access line coupled to the first memory cell.



46. The apparatus of claim 44, wherein the controller is configured to set the first one of the plurality of discrete read signals as the default read signal for memory cells coupled to a plurality of access lines that are within a threshold number of access lines adjacent to the access line coupled to the first memory cell.

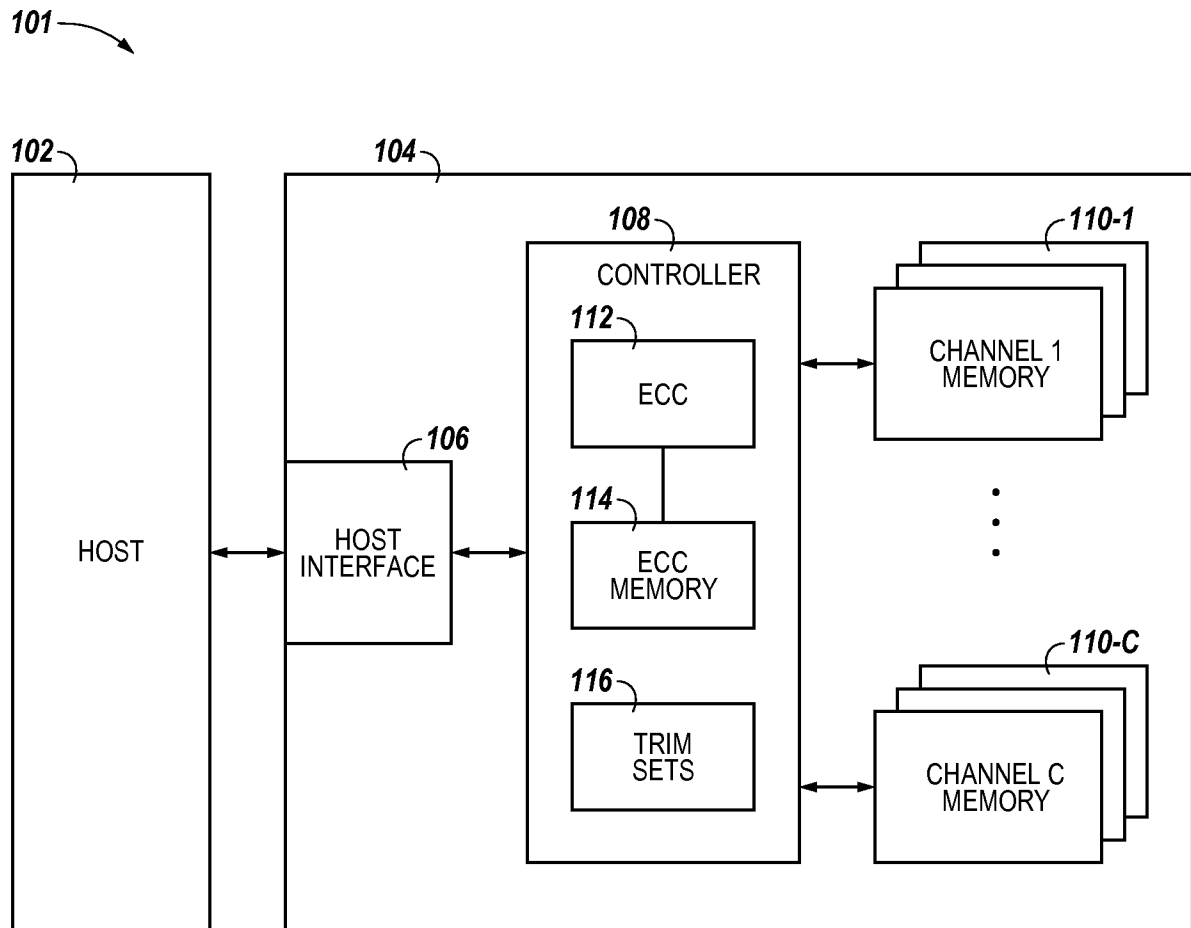
47. The apparatus of claim 46, wherein the controller is configured to set the second one of the plurality of discrete read signals as the default read signal for memory cells coupled to access lines other than the same access line as the first memory cell and the plurality of access lines within the threshold number of access lines adjacent to the access line coupled to the first memory cell.

48. An apparatus, comprising:  
a memory array; and  
an error correction circuit coupled to the memory array, wherein the error correction circuit is configured to error correct data read from a group of memory cells of the memory array a plurality of times with a respective plurality of discrete read signals each having a different magnitude; and  
a trim set coupled to the error correction circuit, wherein the trim set is configured to set one of the plurality of discrete read signals as a default read signal based at least in part on the error correction.

49. The apparatus of claim 48, wherein the apparatus includes an error correction memory coupled to the error correction circuit, wherein the error correction memory is configured to store a number of errors corrected for each respective discrete read signal.

50. The apparatus of claim 49, wherein the trim set is coupled to the error correction memory, and wherein the trim set being configured to set comprises the trim set being configured to set the one of the plurality of discrete read signals as the default read signal based at least in part on the number of errors corrected for each respective discrete read signal.

51. The apparatus of any one of claims 49-50, wherein the apparatus includes a plurality of trim sets coupled to the error correction memory.



*Fig. 1*

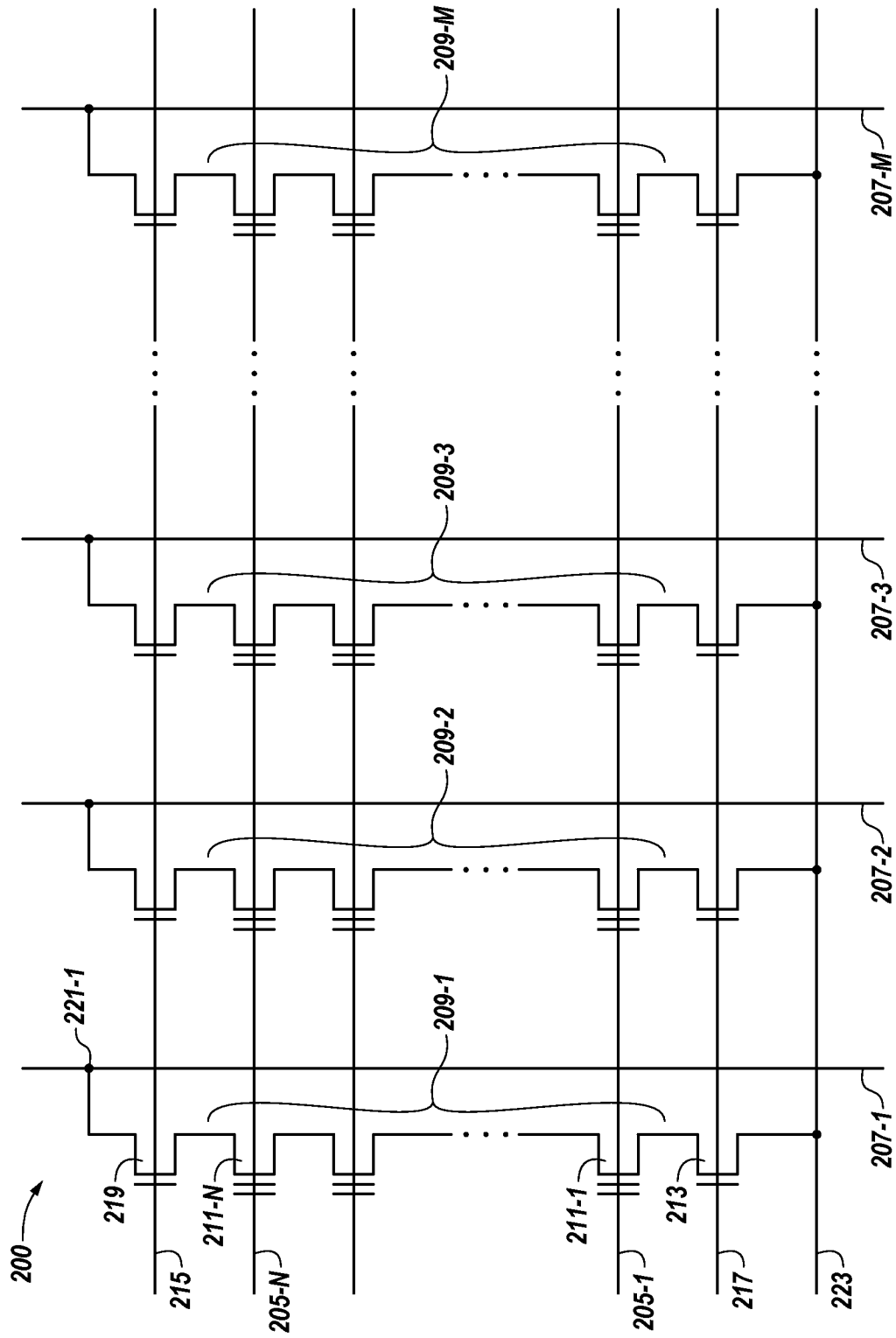


Fig. 2

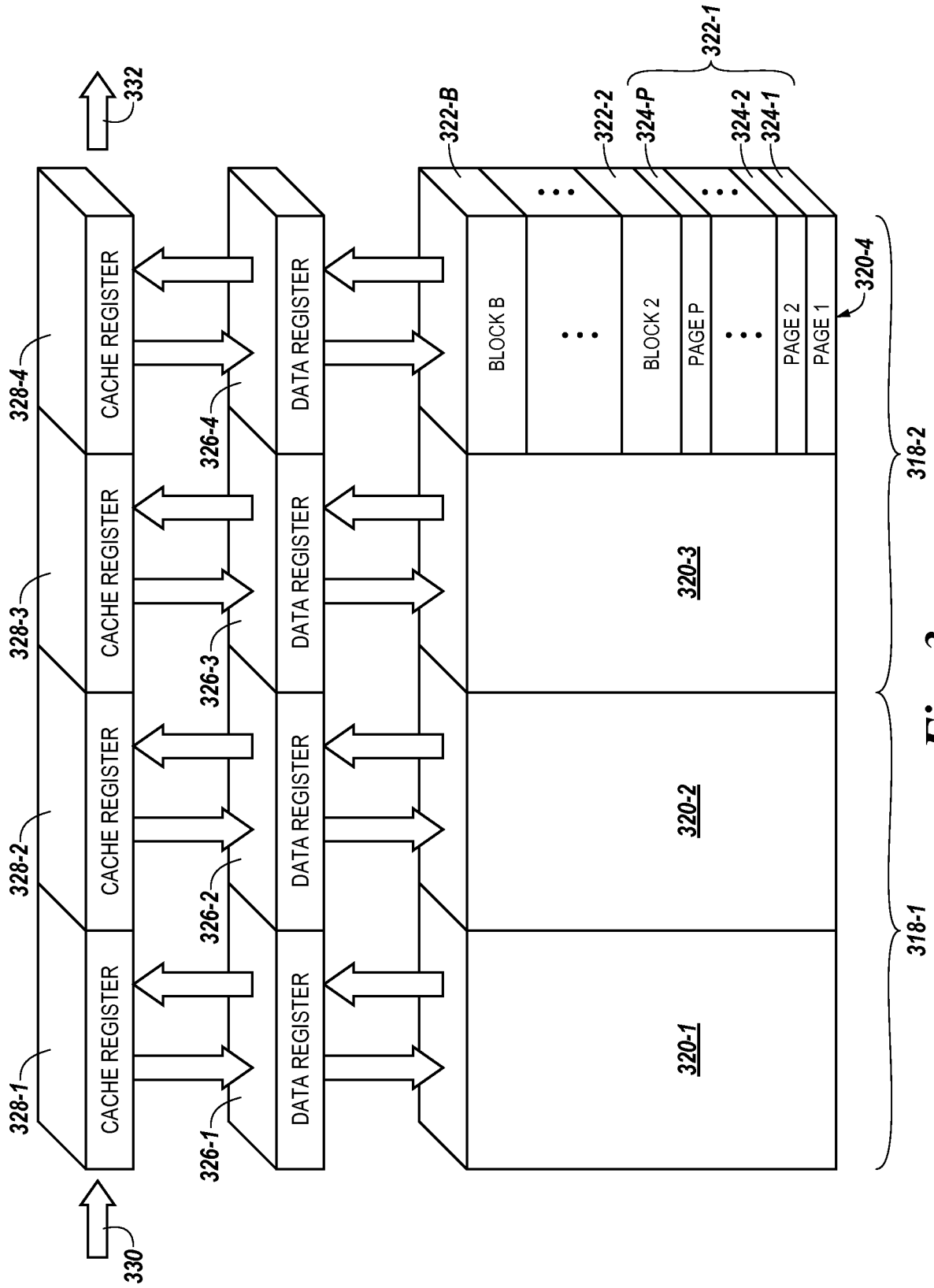
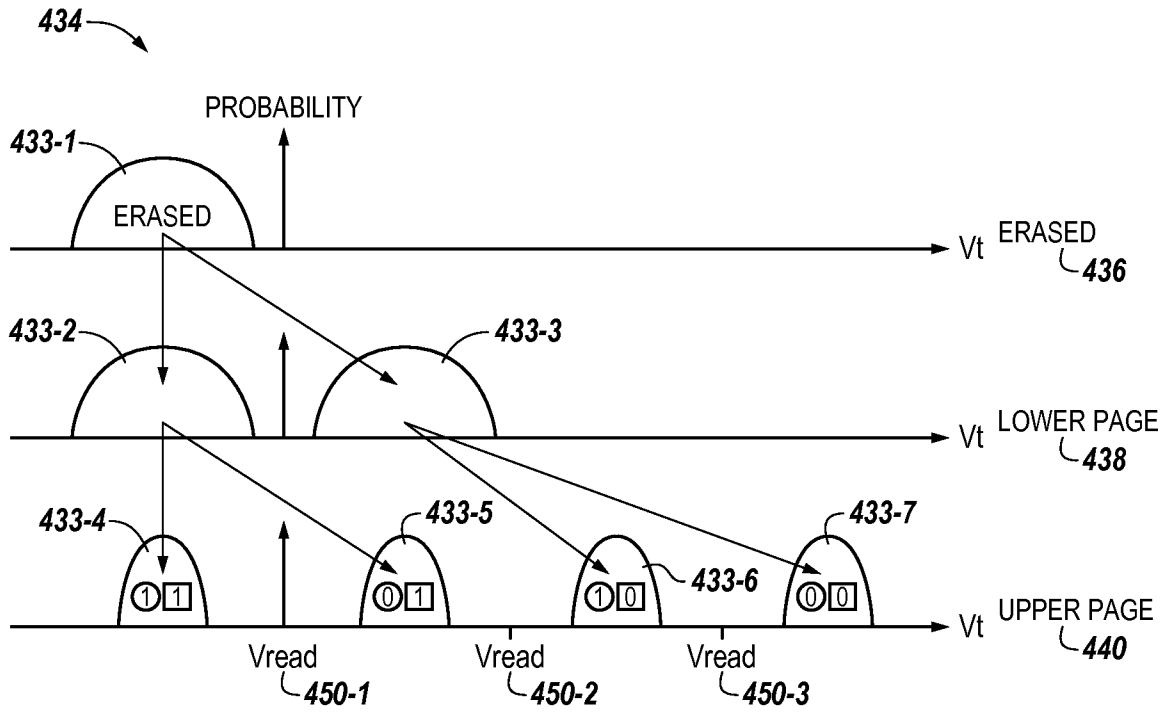
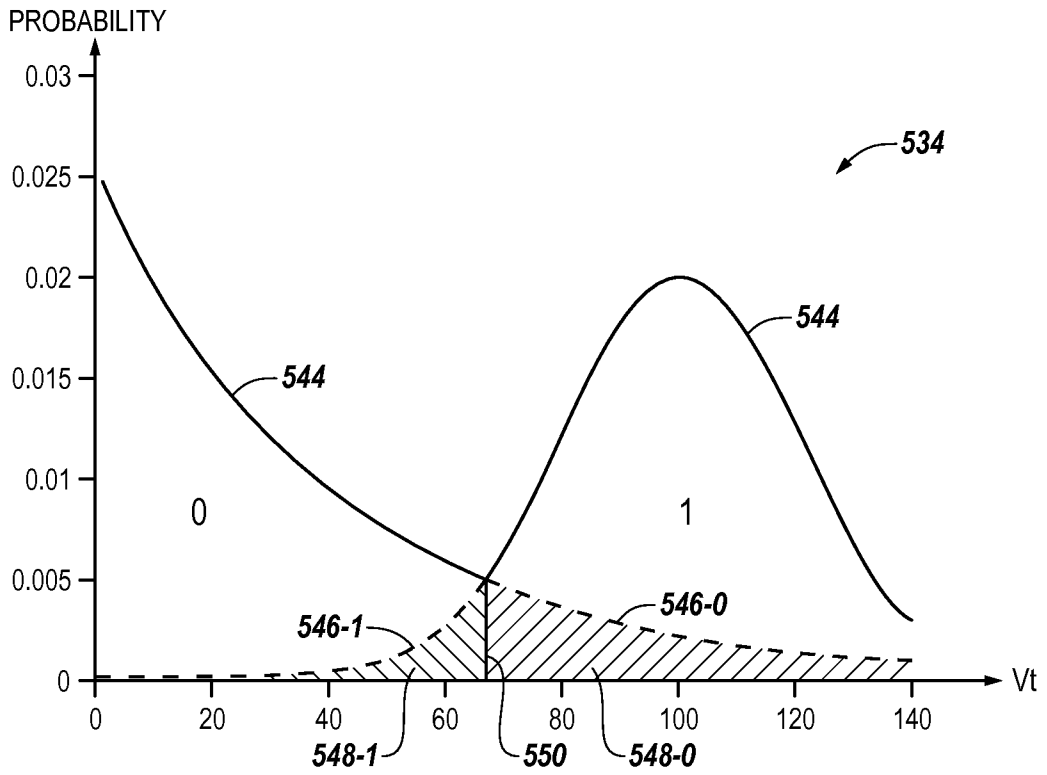


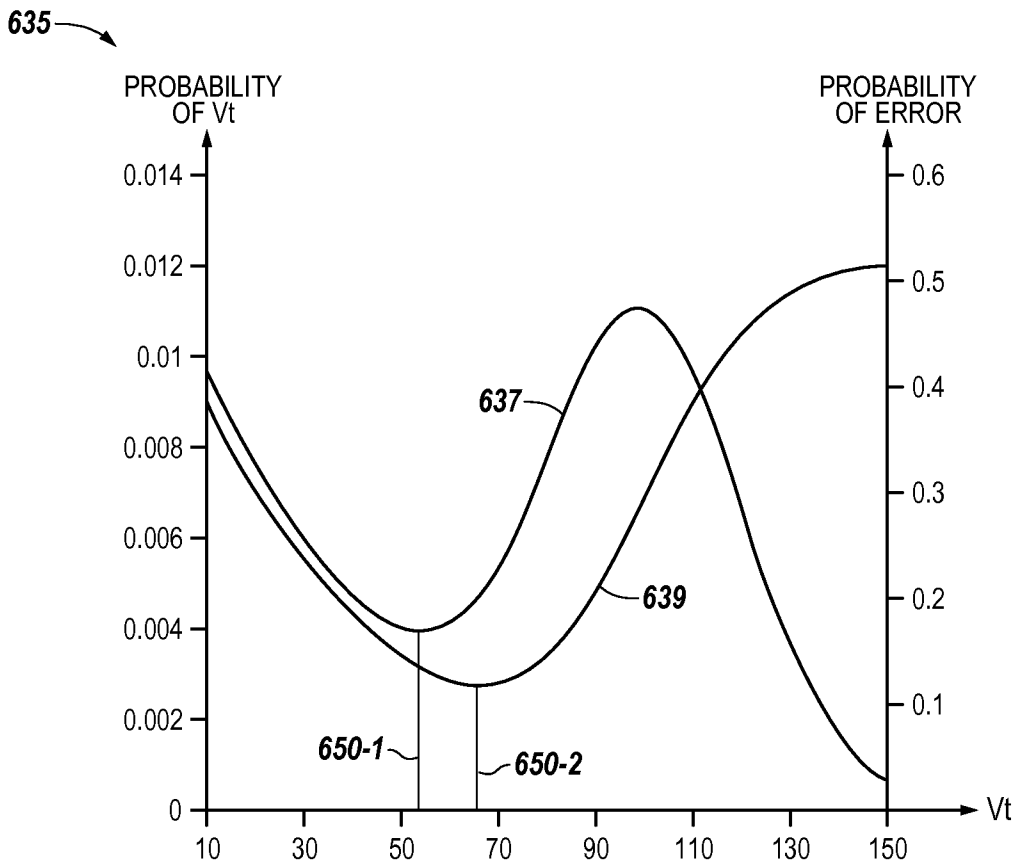
Fig. 3



**Fig. 4**



**Fig. 5 (PRIOR ART)**



**Fig. 6**

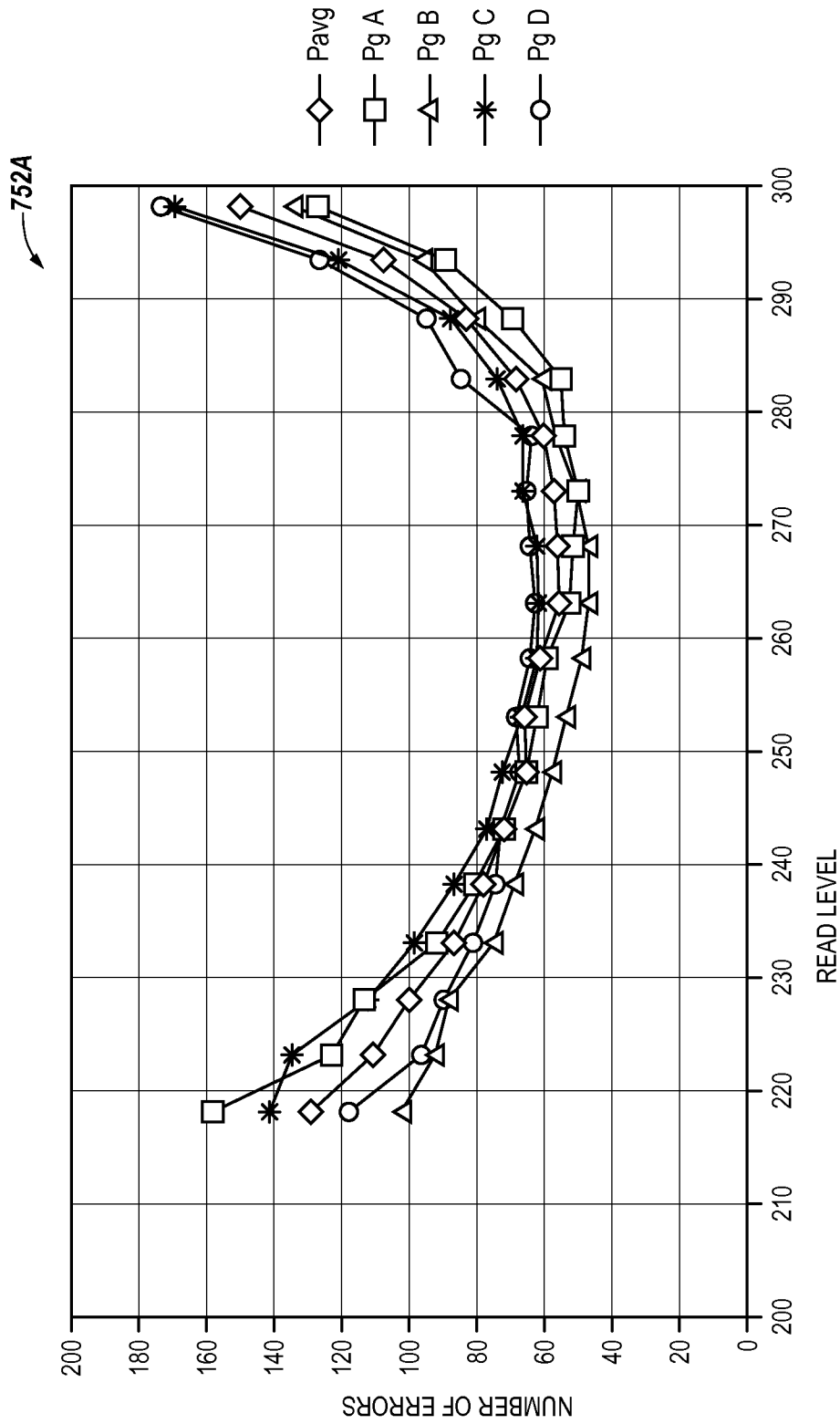


Fig. 7A



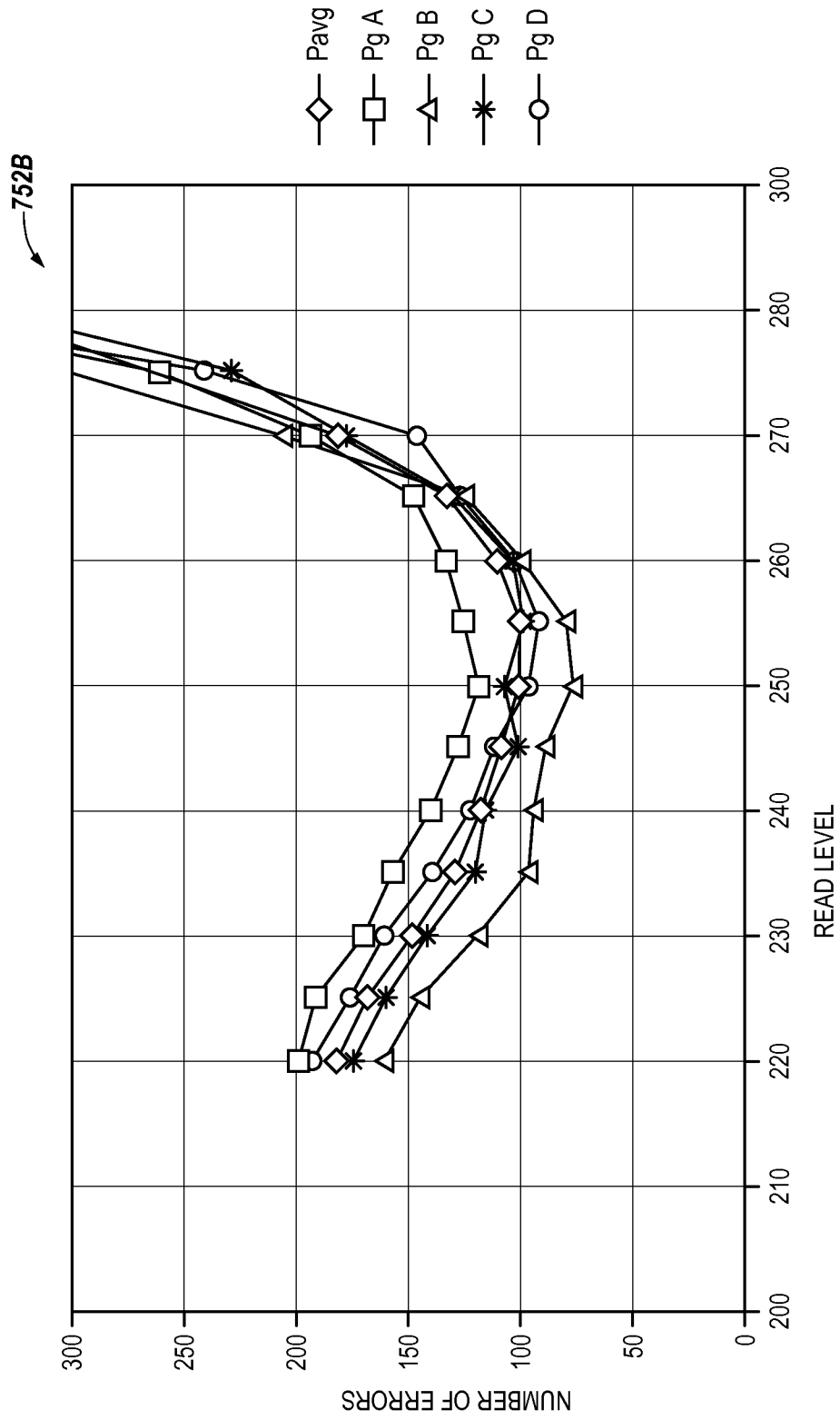


Fig. 7B

## INTERNATIONAL SEARCH REPORT

International application No.  
**PCT/US2013/073348****A. CLASSIFICATION OF SUBJECT MATTER****G11C 29/42(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

G11C 29/42; G06F 12/16; G11C 16/04; G11C 16/02; G06F 11/10; G11C 16/08; G06F 11/08; G11C 16/06

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) &amp; Keywords: read, page, error correct, count, compare, discrete read signal

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 2012-058328 A1 (SANDFORCE, INC.) 03 May 2012 See paragraphs [0013], [0071], [0077], [0079], [0090], [0092], [0094]-[0095], [0098]; and figures 1, 2A.	1-51
A	US 2010-0177564 A1 (PETER S. FEELEY et al.) 15 July 2010 See paragraphs [0027], [0029], [0032]-[0033], [0036], [0042], [0045]; and figures 2-3, 4B-4C.	1-51
A	US 2011-0307758 A1 (JEREMY FILLINGIM) 15 December 2011 See paragraphs [0047]-[0052], [0191]-[0192], [0196]-[0199]; and figures 1, 6.	1-51
A	KR 10-2010-0021497 A (SANDISK IL LTD.) 24 February 2010 See paragraphs [0070]-[0075]; and figures 5a-5b.	1-51
A	JP 2010-237822 A (TOSHIBA CORP) 21 October 2010 See paragraphs [0027]-[0042]; and figure 4.	1-51

 Further documents are listed in the continuation of Box C. See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&amp;" document member of the same patent family

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Date of mailing of the international search report

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## INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

**PCT/US2013/073348**

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