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SPEECH COMPRESSION SYSTEMS

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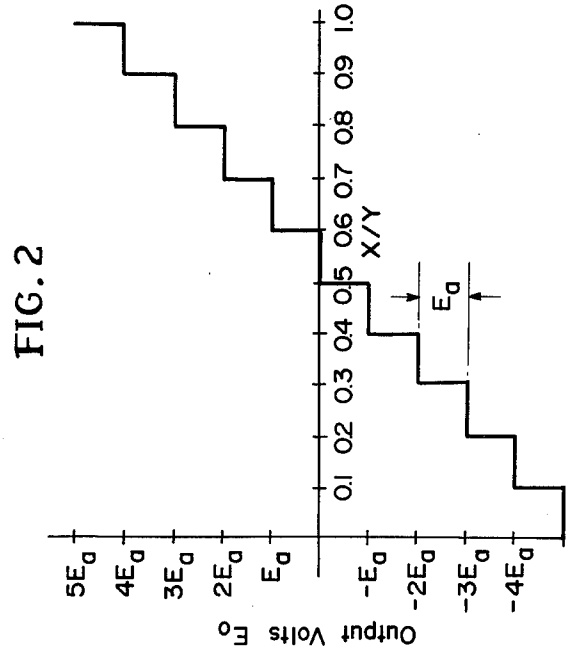


FIG. 2

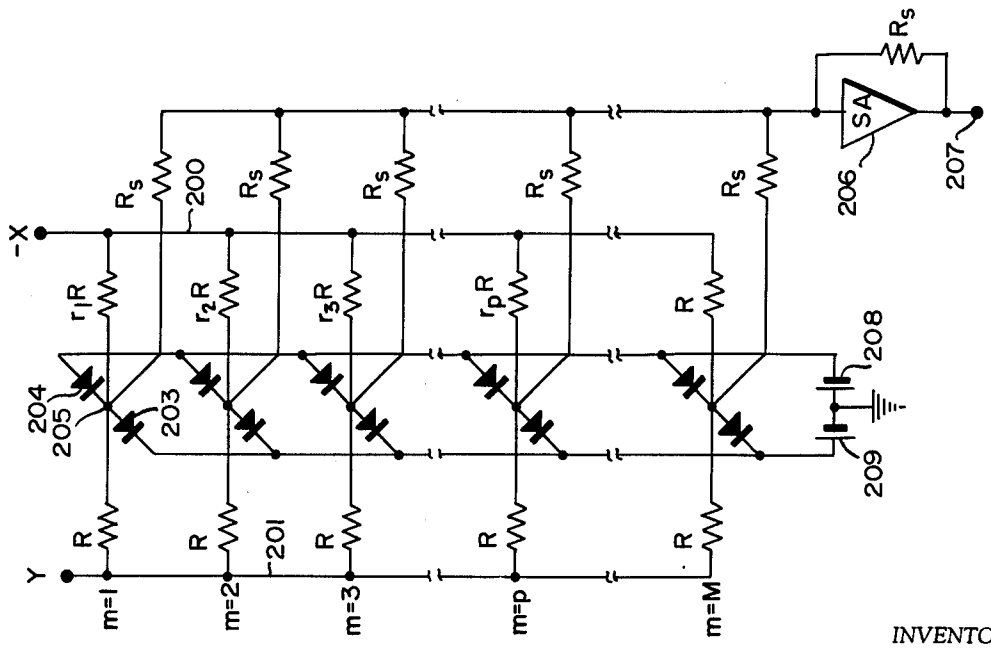


FIG. 1

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SPEECH COMPRESSION SYSTEMS

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Original application July 31, 1958, Ser. No. 752,253, now Patent No. 3,078,345, dated Feb. 19, 1963. Divided and this application Oct. 11, 1962, Ser. No. 243,965

6 Claims. (Cl. 235—196)

This application is a division of our application, Serial No. 752,253, filed July 31, 1958, now Patent No. 3,078,345, and entitled "Speech Compression Systems."

The present invention relates generally to analog computer type circuits and more particularly to a circuit for deriving an output that is a function of two inputs wherein a plurality of clamping type networks is employed to be responsive to the sum of the two inputs and each clamping type network derives a constant amplitude, bipolarity signal.

According to a preferred embodiment of the invention, a division or divider circuit is provided to derive an output in accordance with the ratio of two input variables represented by D.C. signals X and Y, respectively.

Ideally, the output of the divider varies in discrete steps as the input ratio $|X/Y|$ traverses the range of values from zero to unity. For proper operation, the following conditions must be imposed: $X<0, Y>0, |X|\leq|Y|$. This restricts the ratio $|X/Y|$ to the range of values from $0<|X/Y|<1$, a condition which is satisfied by appropriate choice of proportionality constant, "a."

The circuit for a general case of M steps operates in the following manner. To divide the interval from zero to unity into M steps, M resistor pairs are required, each with ratio $r_m=m/M$ where $m=1, 2, 3 \ldots M$. This is achieved in the circuit according to a preferred embodiment of the invention by selecting one of the ratio resistors as R and the other as r_mR. The resistors with value R are all connected to the Y input and those with value r_mR to the X input. For the $M=P$ resistor ratio pair, when $r_p<|X/Y|\leq r_{p+1}$, all the voltages at the resistor pair junction such that $m>p$ are negative, and those such as $m\leq p$ are positive. These voltages can be limited to $\pm E_a/2$ volts by the action of clamp diodes connected to each junction. Hence for the case such that

$$r_p<|X/Y|\leq r_{p+1}$$

the sum of junction voltages (clamped by the diodes) is given by the relation

$$(1)\qquad E_0=\frac{E_a}{2}\sum_{m=0}^{m=M} a_m \qquad \begin{matrix} a_m=1,\ m\leq p \\ a_m=-1,\ {}_m>p \end{matrix}$$

This summation reduces to the following relation by carrying out the indicated summation.

$$(2)\qquad E_0=\frac{E_a}{2}\left[\sum_{m=0}^{m=p} a_m \oplus \sum_{m=p+1}^{-m=M} a_m\right]$$

$$(3)\qquad =\frac{E_a}{2}[2p-M]$$

where $p/M<|X/Y|\leq(p+1)/M$.

It is, accordingly, an object of the present invention to provide a new and improved system for deriving an output that varies in a predetermined manner in accordance with a certain function of two input signals.

Another object of the present invention is to provide a new and improved system for determining if the ratio between two voltages of opposite polarity is in one of a plurality of ranges.

It is still another object of the present invention to provide a new and improved analog computer type ratio computer wherein a plurality of clipping networks are provided to be responsive to two input signals and provide an output of predetermined, fixed value depending upon the relative magnitudes of the two signals applied thereto.

The above and still further objects, features, and advantages of the present invention will become apparent upon consideration of the following detailed description of one specific embodiment thereof, especially when taken in conjunction with the accompanying drawings, wherein:

FIGURE 1 is a functional block diagram of a discrete ratio divider or computer, according to a preferred embodiment of the present invention; and

FIGURE 2 is an output voltage function generated by the divider circuit of FIGURE 1.

A preferred embodiment of the computer employed for obtaining the ratio X/Y, where X and Y are D.C. voltages of opposite polarity, is illustrated schematically in FIGURE 1 of the accompanying drawings. Operation of the circuit requires that $|X|\leq|Y|$, so that the ratio will be less than unity, for all values of the variables.

The X voltage is applied to terminal X, and the Y voltage to terminal Y. The X terminal is connected to a bus **200** and the Y terminal to a bus **201**. Connected between the bus **200** and the bus **201** is a plurality of resistance pairs in parallel, the resistances of each pair being connected in series. These resistance pairs are identified by the nomenclature R and r_mR where m assumes values 0, 1, 2 . . . M, and M is the total number of discrete values desired to be obtained from the computer, and correspondingly with the number of parallel resistance pairs employed. The resistances directly connected with the bus **201** may be all equal and the resistances connected directly to the bus **200** are all weighted, having values r_mR where $m=1, 2, 3 \ldots M$, and $r_m=m/M$. Since the ratio of the resistances of each pair is the controlling factor in the design of the computer, however, the values R need not all be equal, provided the proper ratios are observed.

The junction of two series connected diodes **203, 204** is connected to each junction **205** between a pair of resistances R, r_mR, and all the junctions are connected via summing resistances R_s to the input of a D.C. operational amplifier **206** having an output terminal **207**.

The anodes of diodes **204** are all biased negatively by a voltage source **208**, having a voltage $E_a/2$, while the cathodes of the diodes **203** are positively biased by a source **209** to a value $E_a/2$.

The sets of diodes **203, 204** are clamp diodes, and limit the voltage at each junction **205** to a value $\pm E_a/2$ volts. The polarity of X is always negative and Y always positive, and $|X|>0$ and $|Y|>0$. For this condition the voltage at any junction is for any given value of $m=p$, negative for $m>p$ and positive for $m\leq p$. However, the values of the voltages are limited by the clamp diodes to $\pm E_a/2$ volts. It follows that the sum of the junction voltages, as measured by the summing amplifier **206**, is

$$E_0=\frac{E_a}{2}[2p-M]$$

where p is an integer such that

$$\frac{p}{M}<\frac{X}{Y}<\frac{p+1}{M}$$

This relation is plotted in FIGURE 2, the plot indicating that as $|X/Y|$ varies over the range from zero to unity in 10 steps the junction voltages are all negative when the value $|X/Y|$ is less than $1/M$. When the first junction attains the value 1/M the first junction only reverses po-

larity, and as $|X/Y|$ increases through successive increments of $1/M$, successive junctions reverse polarity until

$$\left|\frac{X}{Y}\right|=1$$

At this point all the junctions are biased positively. The value of output voltage available at terminal 207 accordingly assumes value

$$-\frac{ME_a}{2} \text{ to } \frac{ME_a}{2}$$

in M equal steps as $|X/Y|$ varies from zero to unity.

The operation of the system of FIGURE 1 may be further clarified by considering one junction, and by considering that it joins a fixed resistance R to a variable resistance sR. If $X=-1Y$, the junction is at zero potential, if $s=1$. If s is less than unity, the junction goes positive, while if s is greater than unity, the junction goes negative. If $Y=-2X$, for example, the junction is at zero potential if $s=\frac{1}{2}$ and the junction goes negative if X increases, or Y decreases, from the stated relation.

In summary, any number of parallel test paths may be employed, connected to the Y and X terminals, and these may have values selected to provide selectively $+E_a/2$ or $-E_a/2$, for any desired ratio X/Y. The summation algebraically of the positive and/or negative junction voltages, then, provides a measure of X/Y, in quantized fashion, but the quanta need not be uniform over a range of values of X/Y. Equation 3 is used to plot the relation shown in FIGURE 2 for $M=10$. Physically, the relation indicates that $|X/Y|$ covers the range from zero to unity in M steps. The junction voltages start out all biased in the negative direction when the input voltage is less than $1/M$. When the ratio reaches the value $1/M$, the first junction reverses polarity while all others remain the same as before. This process repeats as the ratio $|X/Y|$ continues to increase through successive increments of $1/M$ until the value of unity is reached. At this point, all of the junctions are biased in the positive direction. Thus, it is seen that the output voltages range from $-ME_a/2$ to $+ME_a/2$ in M equal steps as $|X/Y|$ ranges from zero to unity.

It is to be understood that the input versus output relationship shown in FIGURE 2 is for the ideal case, i.e. when $|X|>>0$ and $|Y|>>0$ for a ten-step divider. This case is referred to as ideal since the slope of the transition between steps is shown to be infinite. In actual operation, of course, this slope is finite and the edges are rounded. Of course, it is also to be understood that the number of divider steps can be greater than or less than 10, as long as a plurality of such steps are employed.

While we have described and illustrated one specific embodiment of our invention, it will be clear that variations of the details of construction which are specifically illustrated and described may be resorted to without departing from the true spirit and scope of the invention as defined in the appended claims.

What we claim is:

1. A discrete ratio computer for dividing two voltages Y and X, whereby to derive the ratio X/Y, where X and Y are of opposite algebraic signs, comprising a plurality of voltage dividers having each a voltage divider output terminal and each a different division ratio, said division ratios assuming an array of equal quantized values corresponding with M, where M is the total number of quantized values and assumes a different one of m values 0, 1, 2 . . . M for each of the dividers, and means for clamping the voltages at said terminals between values $\pm E_a/2$, where E_a is the quantized difference between two adjacent quanta, and means for summing algebraically the voltages at said terminals.

2. In a computer for computing the ratio of two voltages X/Y, M resistor pairs, each pair having a different one of the resistance ratios m/M, where $m=1, 2, 3 \ldots M$,

means for applying said two voltages to all said resistor pairs in parallel in additive relation, each of said resistor pairs having a junction of the resistors thereof, means for limiting the voltages of all said junctions between the same two adjacent values and means for summing the voltages at said junctions.

3. A voltage divider matrix for obtaining the voltage ratio X/Y, where X and Y are voltages of opposite polarities and X is smaller than Y, a plurality of discrete divider units each arranged to detect whether X/Y is above or below a fixed voltage interval and to generate a signal which is selectively of positive constant value or negative constant value according as X/Y is above or below said voltage interval, and means for algebraically adding said signals.

4. A voltage divider matrix for obtaining the voltage ratio X/Y, comprising a plurality of discrete voltage divider elements in said matrix each arranged to detect whether the algebraic sum of X and Y, divided in a series of different discrete ratios, is above or below a predetermined constant level, and means for signaling the difference between the number of divider elements for which said sum is above and for which said sum is below said predetermined level.

5. A system for deriving a function of D.C. signals represented by X and Y, where X and Y are voltages of opposite polarities, comprising a plurality of parallel networks simultaneously responsive to said voltages for determining whether the predetermined function is above or below different predetermined values, each of said networks, comprising: a first resistance having first and second terminals, a second resistance having third and fourth terminals, means directly connecting said second terminal to said third terminal to form a junction, means for connecting one of said voltages to said first terminal, means for connecting the other of said voltages to said fourth terminal, means for clamping the voltage of said junction between fixed voltage values $\pm E_a/2$, and means for measuring the voltage of said junction, whereby said voltage at said junction may be selectively positive or negative according to the values of said resistances and the values of said voltages; and means for linearly combining the signals deriving from said networks.

6. A system for deriving a predetermined function of two input voltages, X and Y, where X and Y are of opposite polarity, comprising a plurality of clamping networks simultaneously responsive to said X and Y voltages, each of said clamping networks including: a pair of diodes connected in series circuit having unlike electrodes connected together to a first junction, a first resistor connected between said first junction and one of said voltage sources, a second resistor connected between said first junction and the other of said voltage sources, and a constant amplitude bias source connected across the series circuit of said pair of diodes tending to back bias said series connected diodes; the second resistors of each of said clamping networks all being of substantially the same value, the first resistors of each of said clamping networks being of different weighted values depending upon said predetermined function, and means for linearly combining the voltages deriving from each of said clamping networks.

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