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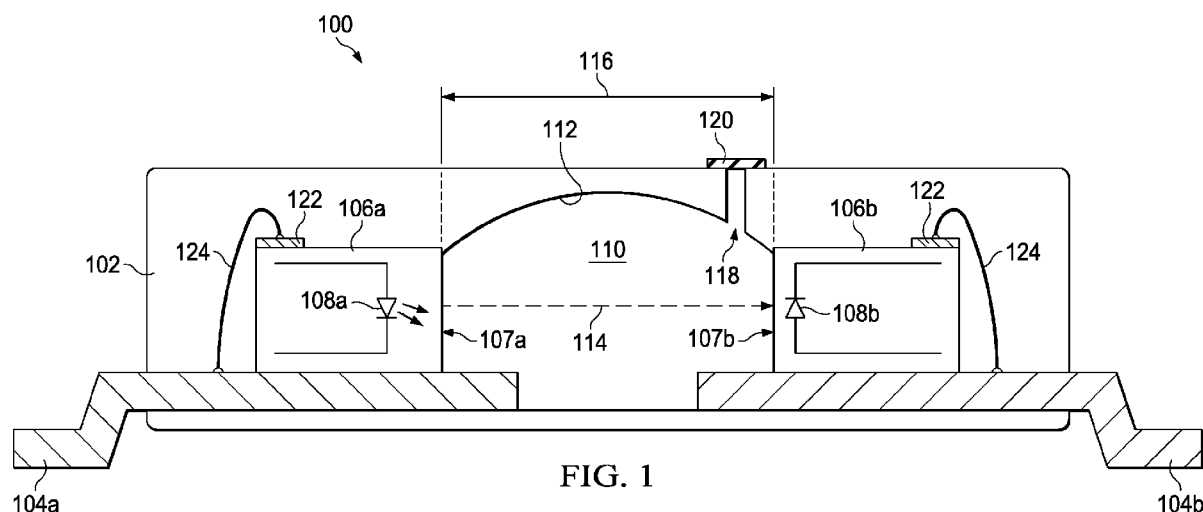


FIG. 1

(57) Abstract: Disclosed examples include integrated circuits (100) with a leadframe structure (104a, 104b), a first circuit structure (106a) including a light source (108a) configured to generate a light signal along an optical path (114), a second circuit structure (106b) including a light sensor (108b) facing the optical path (114) to receive the light signal, and a molded package structure (102) enclosing portions of the leadframe structure (104a, 104b), the molded package structure (102) having a cavity (110) defined by an interior surface of the molded package structure (102), the optical path (114) extending in the cavity (110) between the first and second circuit structures (106a, 106b).

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ISOLATOR INTEGRATED CIRCUITS WITH PACKAGE STRUCTURE CAVITY AND FABRICATION METHODS

BACKGROUND

[0001] Isolation products are used to provide electrical isolation to transfer signals between circuits of different voltage levels and/or between circuits that operate from different supply voltages and ground references. One type of isolator is called an opto-isolator or opto-coupler that provides an optical transmission path to transfer signals between circuits that can be electrically isolated from one another. Opto isolators are used in data communication, power supplies, and other systems where high voltage or high slew-rate common-mode signals appear between the input and output. Opto-isolators are often constructed as a transmitter and a receiver separated by glass and packaged together. Glass provides dc electrical isolation and optical transmission, but suffers from capacitive coupling between the transmitter and receiver and also adds cost to the device. Transformers provide isolation between magnetically coupled primary and secondary coils separated by an insulator to transfer data and/or power between two circuits that are separated by a high voltage or high slew-rate common-mode signal. Some transformers include a magnetic coupling material to enhance the magnetic coupling between the primary and secondary.

SUMMARY

[0002] Disclosed examples include integrated circuits (ICs) with a light source to generate a light signal, a light sensor to receive the light signal, and a molded package structure with a cavity that provides a solid-free optical path between the light source and the light sensor. Further example ICs provide magnetic coupling between first and second coil structures in a package structure cavity. Example IC fabrication methods include mounting a semiconductor die on a leadframe structure, connecting bond wires between the die and the leadframe structure, forming a sacrificial material over a portion of the die, forming a molded package material over the die, the bond wires and over portions of the leadframe structure and the sacrificial material, and sublimating the sacrificial material to create a cavity that includes at least a portion of an isolation barrier between first and second circuits associated with the semiconductor die.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] FIG. 1 is a sectional side elevation view of an optical isolation integrated circuit including an LED light source and a photo receptor diode sensor in spaced semiconductor dies in an internal cavity of a molded package structure providing an optical path for electrical isolation according to an embodiment.

[0004] FIG. 2 is a sectional side elevation view of another optical isolation IC embodiment with an LED light source and a bipolar transistor sensor, including a reflective coating formed on a concave surface of the package cavity.

[0005] FIG. 3 is a top plan view of the optical isolation IC of FIG. 1.

[0006] FIG. 4 is a sectional side elevation view of another optical isolation IC embodiment including horizontal diodes forming an optical sensor circuit.

[0007] FIG. 5 is a partial sectional side elevation view showing optical reception in the embodiment of FIG. 4.

[0008] FIG. 6 is a sectional side elevation view of another optical isolation IC embodiment including vertical diodes forming an optical sensor circuit.

[0009] FIG. 7 is a partial sectional side elevation view showing optical reception in the embodiment of FIG. 6.

[0010] FIG. 8 is a flow diagram of a method to make an integrated circuit according to an embodiment.

[0011] FIG. 9 is a partial sectional side elevation view of a transformer integrated circuit including coil sections extending in an internal cavity of a molded package structure according to another embodiment.

[0012] FIG. 10 is a sectional top plan view of the transformer IC of FIG. 9.

[0013] FIGS. 11-16 are sectional side elevation views of the IC of FIGS. 9 and 10 at various stages of fabrication.

[0014] FIG. 17 is a sectional side elevation view of another transformer IC embodiment including coil sections and a ferrous material extending in an internal cavity of the molded package structure.

[0015] FIG. 18 is a top plan view of the transformer IC embodiment of FIG. 17.

[0016] FIG. 19 is a flow diagram of a method to make an integrated circuit according to another embodiment.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0017] In the drawings, like reference numerals refer to like elements throughout, and the various features are not necessarily drawn to scale. In the following discussion and in the claims, the terms "including", "includes", "having", "has", "with", or variants thereof are intended to be inclusive in a manner similar to the term "comprising", and thus should be interpreted to mean "including, but not limited to..." Also, the terms "couple", "coupled" or "couples" is intended to include indirect or direct electrical or mechanical connection or combinations thereof. For example, if a first device couples to or is coupled with a second device, that connection may be through a direct electrical connection, or through an indirect electrical connection via one or more intervening devices and connections.

[0018] Referring initially to FIGS. 1-3, FIG. 1 shows an example optical isolation integrated circuit (IC) 100, for example, an opto-isolator or opto-coupler device. The IC 100 includes a light source 108a configured to generate a light signal along an optical path 114. In one example, the light source is an LED fabricated in a first semiconductor die or other circuit structure 106a, although lasers or other optical sources can be used in other embodiments. The IC 100 further includes a second device or circuit structure 106b including a light sensor 108a facing the optical path 114 to receive the light signal. In one example, the light sensor 108b is a photo receptor diode sensor as schematically illustrated in FIG. 1. Any suitable light sensor can be used, which receives the light signal from the source 108a. FIG. 2 illustrates another possible implementation, in which the second circuit structure 106b includes a bipolar transistor 109 that senses the received light signal. As shown in FIG. 1, the circuit structures 106a and 106b individually include bond pads 122 connected by bond wires 124 to corresponding electrical conductors 104a, 104b of the lead frame structure. In one example shown in FIG. 3, the first circuit structure 106a includes first and second bond pads 122 individually connected to a pair of corresponding first pair of the electrical conductors 104a-1, 104a-2 of the leadframe structure. The conductors 104a-1 and 104a-2 in one example are IC pins or pads that can be soldered to a host printed circuit board (PCB, not shown). In this example, an external circuit (not shown) provides a signal to the light source 108a via the conductors 104a-1 and 104a-2, and the light source 108a generates the light signal in response. In this example, the second circuit structure 106b also include bond pads 122 that are electrically connected by corresponding bond wires 124 to a second pair of leadframe electrical conductors 104b-1 and 104b-2. The conductors 104b-1 and 104b-2 in the illustrated examples provide pads or

pins of the IC 100 that can be soldered to a host PCB to deliver a signal from the sensor 108b that is isolated from the source signal at the conductors 104a-1 and 104a-2. In this manner, the spacing 116 of the circuit structures 106a and 106b provides electrical isolation, with signal transmission along the path 114 through the cavity 110 of the IC 100.

[0019] The optical source 108a and sensor 108b are spaced from one another in an internal cavity 110 of a molded package structure 102 to provide electrical isolation therebetween according to an embodiment. The cavity 110 provides an optical path 114 that is free of solids (i.e., solid free). The conventional use of glass or other optically transmissive solid structure adds cost to optical isolation devices, and adds to the capacitance of the source/sensor configuration. The capacitance of devices using solid transmission media presents problems, particularly for high speed data communications and high common-mode slew rate rejection, and the manufacturing cost is prohibitive for many applications. In addition, the solid transmission media also presents issues with degradation of optical performance over time. The disclosed opto-coupler IC 100, in contrast, advantageously reduces the coupling capacitance and cost while facilitating any desired level of electrical isolation and high breakdown voltage. In this regard, air has a much lower dielectric constant than glass or other transparent materials, and the disclosed examples reduce capacitive coupling between the optical sensor and transmitter. In addition, the solid-free gap 116 between the source and sensor dies 106a and 106b can be controlled by the structural relative positioning thereof to provide a desired spacing or gap distance 116 for optical transmission along the path 114 with any desired voltage isolation rating. The gap distance 116 can be controlled by the deposited sacrificial sublimation material in one example. The gap 116 in certain examples is controlled by mechanical features on one of the dies 106, such as oxide bumps (not shown) extending between the dies 106 to set the gap distance 116. The gap 116 is controlled in some examples by mixing filler material of a particular size with the sacrificial material. In other embodiments, the sublimation region can be formed as a unique printed shape using inkjet printing technology, and the optical channel can be directly printed.

[0020] The light sensor 108b at least partially faces the light source 108a to receive the light signal. In the examples of FIGS. 1-3, the first circuit structure 106a includes a light source signal output face or side 107a, and the second circuit structure 106b includes a sensor face or side 107b, where the signal output face 107a and the sensor face 107b lie in generally parallel planes, spaced from one another by the distance 116 in the cavity 110. In other possible examples, the faces 107

need not be parallel. Any relative configuration can be used in which the sensor face 107b at least partially faces the light source 108a so as to receive the light signal. The sensor face 107b allows light to enter the structure 106b so as to modify the electrical behavior of the sensor, whether a diode 108b or a transistor 109 or other light sensor structure, to generate a sensor signal to be output or further processed by the second circuit structure 106b. The circuit 106b may include further interface circuitry (not shown) to operate on the sensor signal. As shown in FIGS. 1 and 2, moreover, significant portions of the faces 107a and 107b are exposed within the cavity 110, although not a strict requirement of all possible embodiments.

[0021] The IC 100 in FIGS. 1-3 also includes a molded package structure 102 that encloses portions of the leadframe structure 104 and portions of the circuit structures 106a and 106b. In other examples, the package structure material 102 need not enclose the circuit structures 106a and 106b. The package structure 102 exposes portions of the electrical conductors 104a-1, 104a-2, 104b-1 and 104b-2 to allow external connection to the first and second circuit structures 106a and 106b. In the illustrated implementations, the package structure 102 is a molded material structure that includes the cavity 110, and the optical signal path 114 extends within the cavity 110 between the light source 108a and the light sensor 108b, 109 of the circuit structures 106a, 106b. The cavity 110 thus provides a solid-free optical path 114 for the light signal between the circuit structures 106a and 106b. The illustrated structure further includes a port 118 extending from the cavity 110 to the exterior of the package structure 102, as well as a cover or seal structure 120 that seals the cavity 110 from the IC exterior. The port 118 can be in the upper portion of the cavity 110 as illustrated, or the cavity can be ported through the side, or through the bottom, or combinations thereof.

[0022] The cavity 110 is defined by an interior surface of the package structure 102. The interior surface can be of any suitable shape and profile. In certain examples, the interior surface enhances optical transmission in the cavity. The interior surface of the package structure 102 includes a concave portion in the embodiments of FIGS. 1 and 2. In this example, the concave surface can be provided by forming a sacrificial material during fabrication as a drop or one or more drops, such as using a printing process. This deposited sacrificial material thus forms a partially convex structure, and the material is later sublimated or evaporated after formation of the molded package structure material 102, leaving a convex inner surface.

[0023] In the example of FIG. 2, the concave portion of the interior surface includes a reflective coating 200 that reflects light from the light source 108a toward the light sensor 108b, 109. The reflective coating material 200 in one example is deposited over the convex sacrificial sublimation material prior to the molding process that creates the molded package structure material 102. Sublimation of the sacrificial material layer after the molding process leaves the cavity 110 defined at least part by the concave surface of the remaining reflective material layer 200. Any suitable non-conductive material 200 can be used which facilitates reflection of all or part of the light signal generated by the light source 108a toward the light sensor 108b, 109. As shown in FIG. 2, the light signal from the source 108a can travel through the cavity 110 along the optical path 114 directly to the sensing face 107b of the sensor die 106b, and/or the signal can also travel along a reflected path 202 via the reflective coating 200 on the concave surface.

[0024] In other examples, a concave surface 210, 212 can be formed (shown in dashed line form in FIG. 2) that extends laterally outward to expose top portions of one or both of the source and sensor circuit structures 106a and 106b. In one implementation, the concave surface 212 includes a reflective coating material 210. These embodiments can include an LED or other light source circuit 106a having an emissive upper or top surface that emits light toward the reflective coating material 210 and the light signal reflects one or more times to impart a side and/or top sensing face of the sensor circuit 106b. As used herein, a sensing face of the circuit 106 at least partially faces a light source circuit directly or via one or more reflective surfaces (e.g., surfaces 200, 210) of a concave or flat surface of the cavity 110. In certain embodiments, top and/or side emitting source circuits 106a can be used in combination with top and/or side sensing circuits 106b for transfer of an optical signal directly or with one or more reflections.

[0025] The package structure 102 can be formed by molding or other suitable process, preferably using an electrical insulator material. Disclosed examples use a sublimation process to provide low-cost isolation devices using the cavity 110 that includes at least a portion of the isolation barrier between the source and sensor circuit structures 106a and 106b. The circuit structures 106 are at least partially encapsulated in a deposited sacrificial sublimation material during fabrication, and then further encapsulated by the molded package structure material 102. The structure is then baked to sublime (e.g., evaporate) the sacrificial material, leaving the internal cavity 110 in which the dies 106a and 106b, or at least a portion thereof, are not touching the mold compound 102. The opening 118 in certain examples is drilled or cast into the package

structure 102 such that the sacrificial material can be sublimated, and thereafter the seal structure 120 is provided over the top of the opening 118 to seal the cavity 110. The opening 118 can be cast into the package structure 102 via a mold sprue, or the opening 118 can be incorporated into the package before the molding process via a disposable plug, or drilled into the package 102 after molding using mechanical drilling, laser drilling, etching or other techniques.

[0026] The disclosed structure advantageously facilitates small package size, mitigation of the cost and manufacturing difficulties associated with insertion of glass or other transparent material in the optical path of an optical isolation device. Furthermore, the disclosed examples mitigate the capacitance and aging problems associated with glass or other solid materials in the optical path of an opto-isolator, and thus provide enhanced performance particularly for high speed communications applications. In addition, the disclosed examples can be fabricated using ordinary mainstream manufacturing processing steps and equipment.

[0027] In certain example, the dies 106 individually include a substrate, such as silicon, SOI, or other semiconductor substrate. The light source 108a and the light sensor 108b, 109 and various interface circuitry can be formed on or in the associated substrate using known semiconductor fabrication processes and equipment. The package structure 102 in one example is a molded structure. The package structure 102 can be any suitable molding material that provides electrical insulation and mechanical protection for the dies 106, and can include low modulus of elasticity material to enhance stress immunity. The dies 106, moreover, can be supported in any suitable manner within the cavity 110, such as mounting onto a lead frame structure as shown. Thereafter, sacrificial material is deposited at least partially over the dies 106 prior to molding. Following molding or other formation of the packaging material 102, the assembly is heated to cause sublimation of the sacrificial encapsulant material through the port 118 of the molding material structure 102. Suitable fabrication processes and materials are illustrated and described in US Patent Application No. 15/248,151, filed August 26, 2016, and entitled "Floating Die Package", the entirety of which is hereby incorporated by reference.

[0028] Referring also to FIGS. 4 and 5, FIG. 4 shows another optical isolation IC embodiment 100. In this example, the light sensor 108a includes a plurality of connected diodes, each including N and P doped regions of a substrate. The second circuit structure 108b in this example includes five parallel-connected horizontal diodes in each of two (e.g., lower and upper) substrates or dies 401 and 402, although any number 1 or more such stacked dies can be used. FIG. 5 illustrates

lateral photon absorption along the length of pn junctions in multiple stacked dies 401 and 402. The N and P regions in this embodiment are arranged generally along the optical path 114, with N regions or wells formed in a p doped substrate leaving a p region underlying the N wells to form multiple diodes connected in parallel with one another. In this example, the circuit structure 108b includes a base die 400 with a semiconductor substrate including any desired amplifiers, filters or other interface circuits (not shown). The dies 401 and 402 are back-ground in one example to have a smaller vertical height than the base die 400. As best seen in FIG. 5, the base die 400 also includes a metallization structure with one or more inter-metal dielectric (IMD) structures (e.g., dielectric layers and conductive metal structures for circuit interconnections) and an upper passivation layer, as well as one or more die pads with bond wire connection(s) 124 to the associated leadframe electrical conductor(s) 104b. The individual dies 401 and 402 in this example include a base substrate 500 (e.g., silicon) doped through implantation of corresponding dopants in the illustrated N and P regions, a metallization structure 502 and an upper passivation layer 504. The circuit structure 108b includes any suitable intervening electrical conductor structures (not shown) to interconnect the diodes of the stacked dies 401 and 402 with the circuits and connections of the base die 400 to provide a sensor or receiver output signal to an external circuit via the associated leadframe conductors 104b.

[0029] FIG. 5 shows optical reception in the stacked dies 401 and 402 of FIG. 4. Examples of direct and reflected optical paths 114 and 202 are shown entering the dual horizontal die stack structure 401,402 at the sensing face 107b. The use of stacked PN junctions and extended lateral optical transmission (e.g., left to right in FIG. 5) provides greater opportunity for the light signal to produce an output signal in the diode structure 108b. The disclosed examples thus facilitate high output signal performance in the lateral optically-coupled isolation IC 100, and mitigate low signal shortcomings of conventional opto-isolators. In one example, the individual dies 401 and 402 each generate a voltage signal of approximately 0.5 V, and the stacked dies 401 and 402 can be interconnected in parallel and/or in series via metallization structure interconnections for enhanced output signal strength. In this regard, embodiments having more than 2 stacked dies can be interconnected in any desired series and/or parallel configuration to achieve a desired output signal level in response to the light signal from the light source 108a.

[0030] FIGS. 6 and 7 show another isolation IC example 100 using multiple stacked diodes in the optical sensor 108b. The second circuit structure 106b in FIG. 6 is a multi-die structure with

vertical diodes which form an optical sensor circuit 108b. This circuit structure 106b includes four stacked dies 601, 602, 603 and 604 formed on a base die 600 to provide the circuit structure 106b. FIG. 7 shows further details of the sensor circuit 108b, where the base die 600 includes a semiconductor substrate with any desired amplifiers, filters or other interface circuits (not shown), as well as a metallization structure with one or more IMD structures and an upper passivation layer, and one or more die pads 122 with bond wire connection(s) 124 to the associated leadframe electrical conductor(s) 104b. The individual dies 601-604 include a base substrate 700 (e.g., silicon) with a bottom portion doped with P type dopants (e.g., boron, designated P+ in FIG. 7) and an upper portion 702 doped with N type dopants (e.g., phosphorus, designated N-) to form a vertically oriented diode. The N and P regions of the dies 601-604 in this example are thus arranged normal to the optical path 114. The individual dies 601-604 also include contacts 704 and an IMD/metallization structure 706 with any associated passivation layer. The upper die 604 in this example includes a die pad 708 connected by a bond wire 710 to a die pad 712 of the base die 600. As with the above example, the circuit structure 108b in FIGS. 6 and 7 includes any suitable intervening electrical conductor structures (not shown) to interconnect the diodes of the stacked dies 601-604 with the circuits and connections of the base die 600 to provide an output signal of any desired level. In one example, the individual dies 601-604 each generate a voltage signal of approximately 0.6 V, and the stacked dies 601-604 can be interconnected in any desired series and/or parallel configuration to achieve a desired output signal level in response to the light signal from the light source 108a.

[0031] FIG. 8 illustrates an example method or process 800 which can be used to fabricate an isolation IC, such as the optical isolation devices described above. The method 800 begins at 802 with mounting of the source and sensor dies in a spaced relationship relative to one another on a leadframe. For example, the first and second circuit structures 106a and 106b can be mounted at 802 to the lead frame structure 104 with the source and sensor faces 107a and 107b spaced from one another by the desired gap distance 116 in FIG. 1 above. In the above example, moreover, the second semiconductor die 106b is mounted on the leadframe structure 104b at 802 such that the sensing face 107b of the light sensor 108b at least partially faces the optical path to receive the light signal from the light source 108a. A wire bonding process is performed at 804 in FIG. 8, including connecting bond wires 124 between the die pads 122 and the corresponding lead frame electrical conductors 104a and 104b in FIG. 1. Other necessary bond wires (e.g., 710) can be

attached at 804, for example, from the base dies 400, 600 to one or more stacked dies 401, 402, 601-604 in the examples of FIGS. 4-7 above. Solder balls or other IC connection technologies can also be used instead of or in addition to wire bonds. At 806, a sacrificial material is formed over at least part of the assembly in a prospective optical path between the source and sensor dies. The sacrificial may be formed at least partially over a portion of one or both of the first and second semiconductor dies 106a, 106b in certain examples at 806. In certain implementations, moreover, the sacrificial material SL is formed at 806 as a drop having a convex surface. In one example, a reflective material is formed at 807 in FIG. 8 on the convex surface of the sacrificial material (e.g., reflective material 200 in FIG. 2 above).

[0032] At 808 in FIG. 8, a molding process is performed in order to form a molded package material (e.g., material 102 above) over the semiconductor dies 106, the bond wires 124 and over portions of the leadframe structure 104 and the sacrificial material to create a molded package structure 102. For implementations using a reflective material formed over all or a portion of the sacrificial material layer, the package material is formed at 808 at least partially on the reflective material 200. At 810, the sacrificial material is sublimated to create an internal cavity (e.g., cavity 110 above) defined by an interior surface of the package structure 102. In the above IC examples 100, the sublimation process at 810 provides a structure 102 with a cavity 110 including at least a portion of the optical path 114 to allow transmission of the light signal between the light source 108a and the light sensor 108b. At 812, in certain examples, the cavity 110 is sealed. For example, the seal structure 120 is mounted over the port 118 at 812 in the example of FIG. 1 in order to seal the cavity 110 from the exterior of the IC 100.

[0033] Referring now to FIGS. 9-19, magnetically coupled isolation ICs 900 are provided according to further embodiments. FIGS. 9 and 10 illustrate a transformer IC 900 that includes transformer primary and secondary coil sections 906 and 908 extending in an internal cavity 110 of a molded package structure 102. FIGS. 11-16 illustrate the IC 900 of FIGS. 9 and 10 at various stages of fabrication according to a fabrication process 1900 shown in FIG. 19. FIGS. 17 and 18 illustrate an alternate embodiment that further includes a ferrous material 1700 in the package structure cavity 110. In various possible embodiments, transformer isolation devices are provided including two or more coil structures. The coil structures in some examples are constructed from conventional wire. In other examples, the coils are etched using PC board technology. In further examples, such as shown in FIGS. 9 and 10, the coil structures are printed using suitable targeted

printing deposition techniques. In the illustrated examples, sacrificial sublimation material is used during intermediate fabrication steps, and then sublimated using suitable processes, such as those described above. In certain examples, a powdered ferrite or other core material is included with the sublimation material for enhanced magnetic coupling between the primary and secondary coil structures 906 and 908. Disclosed examples advantageously position the secondary coil field away from the silicon substrate 902 of a semiconductor die structure 901. This reduces eddy-current losses, and the air-core structure resulting from the magnetic coupling in the cavity 110 facilitates reduction in capacitive loss to enhance high-frequency operation and reduce coupling from high slew-rate common-mode signals. As shown in the illustrated examples, moreover, the coil structures 906, 908 can be at least partially mechanically supported by the molded package structure 102 by selective location of the sacrificial material to at least partially overlie the coil structures 906, 908 prior to molding. In other examples, the coil structures are at least partially mechanically supported by spacer materials formed prior to deposition of the sacrificial material.

[0034] The IC 900 in the example of FIG. 9 includes a leadframe structure with electrical conductors 104a and 104b as described above. A transformer primary circuit in this example is formed by a first coil structure 906 electrically connected to a first pair of leadframe electrical conductors 104a-1 and 104a-2. The first coil structure 906 is partially formed on the semiconductor die structure 901 through a printing process, and also extends over the first sacrificial material (not shown in FIGS. 9 and 10) such that a portion of the resulting first coil structure 906 extends within the prospective cavity 110 after the sublimation processing. In the example of FIG. 9, moreover, the first coil structure 906 is formed at least partially over (i.e., in electrical contact with) a die pad or other conductive structure 122 formed in passivated, IMD/metallization structure 904 of the semiconductor die 901. The metallization structure 904 in this example further includes a conductive structure 907 to electrically connect a first end of the first coil structure 906 to an outer die pad 122 that is wire bonded to a corresponding lead frame electrical conductor 104a. A second end of the coil structure 906 is connected by a second conductive structure 907 to a second lead frame electrical conductor 104a. As best shown in the top view of FIG. 10, the first coil structure 906 forms a turn inside the cavity 110 between the first and second ends. Coil structures 906 and 908 may also be spirals with multiple concentric turns.

[0035] The second coil structure 908 in this example forms a transformer secondary circuit having two ends that are electrically connected to a second pair of the leadframe electrical conductors 104b-1 and 104b-2 via metallization structure conductors 909, corresponding die pads 122 and associated bond wires 124. The second coil structure 908 in this example is formed by a printing deposition process, and includes ends that extend partially on the semiconductor die structure 901 to form electrical connection to corresponding die pads 122. Other examples are possible using two die, one for the primary and one for the secondary. The described techniques can also be used in other embodiments to manufacture an isolation transformer with an air dielectric inside an IC package without an IC die to provide a standalone transformer. The second coil structure 908 extends into the cavity 110 and forms a turn extending at least partially over the first coil structure 906 within the cavity 110. By this configuration, the first and second coil structures 906 and 908 are magnetically coupled with one another via the air or other gas within the cavity 110 to constitute an air-core transformer in certain examples. As with the optical isolation device 100 described above, the cavity 110 in the transformer example 900 of FIG. 9 includes a port or opening 118, which is covered by a seal structure 120 in certain examples. The IC 900 includes a package structure 102 as generally described above, that encloses portions of the leadframe structure 104 and the bond wires 124, while exposing portions of the lead frame electrical conductors 104a-1, 104a-2, 104b-1, 104b-2 to allow external connection to the first and second coil structures 906, 908.

[0036] FIGS. 17 and 18 illustrate an alternate transformer IC embodiment 900, including first and second coil sections 906 and 908 as generally described above. The Example of FIGS. 17 and 18 further includes a ferrous material 1700 extending at least partially in the cavity 110. As seen in FIG. 17, the ferrous material 1700 can be formed on the structure 904 of the semiconductor die structure 901, spaced from and below a portion of the first coil structure 906 and the second coil structure 908. In this example, moreover, the ferrous material 1700 extends at least partially in the cavity 110. In operation, the ferrous material 1700 facilitates magnetic coupling of the first and second coil structures 906 and 908. In other possible implementations, a ferrous material 1700 can be formed at different locations, at least partially within the cavity 110. In one possible implementation, a ferrous material structure 1700 can be formed vertically between, and spaced from, the first and second coil structures 906, 908 to further enhance magnetic coupling of the coils. For example, a ferrous material layer 1700 can be formed over a corresponding sacrificial

material layer above the first coil structure 906 prior to formation of the second coil structure 908, and the second coil structure 908 can be formed over a further sacrificial material layer formed on the ferrous material 1700, which further sacrificial material layer exposes at least a portion of the deposited ferrous material structure 1700. In such an example, subsequent molding of the package material 102 and sublimation of the sacrificial material layers leaves a ferrous material structure 1700 at least partially mechanically supported by the molded material 102, and which extends vertically between, and spaced from, the coil structures 906 and 908. Multiple ferrous material layers can also be used at the same or different locations with respect to the coil structures.

[0037] Referring now to FIGS. 11-19, FIG. 19 illustrates a process or method 1900 to make an integrated circuit according to another embodiment. The process 1900 can be used, for example, to fabricate the transformer IC examples 900 of FIGS. 9, 10, 17 and/or 18 as previously described. The method 1900 begins at 1902 with mounting of one or more semiconductor dies on a leadframe structure. For example, the semiconductor die structure 901 in FIG. 9 or FIG. 17 can be mounted to a leadframe structure including leadframe electrical conductors 104, as seen in FIG. 11. At 1904 in FIG. 19, a wire bonding process is performed to connect bond wires 124 between die pads 122 of the semiconductor die structure 901 and the leadframe electrical conductors 104 as shown in FIG. 11. In certain examples, a ferrous material 1700 may be formed at 1905 for a transformer core, over a portion of the semiconductor die 901 prior to forming a first sacrificial material layer (e.g., as shown in FIG. 17). At 1906, a first sacrificial material is formed over a portion of the semiconductor die 901 (e.g., directly or over an intervening ferrous material layer 1700). The first and subsequent sacrificial material layers can be formed by any suitable deposition process. In FIG. 11, the first sacrificial layer is shown as layer SL1. In this example, the first sacrificial material layer SL1 is formed over a middle portion of the upper surface of the die structure 901 at 1906, and the layer SL1 does not cover the illustrated die pads 122 formed in the structure 904.

[0038] At 1908 in FIG. 19, a first coil structure (e.g., 906 above) is formed at least partially on the first sacrificial material layer SL1. In the example of FIG. 11, the coil structure 906 is formed at least partially over a die pad 122 of the semiconductor die structure 9014 electrical connection to the first pair of the electrical conductors 104a-1, 104a-2 of the leadframe structure by the previous wire bonding processing at 1904. In one example, a printing type deposition process is used at 1908 to print the first transformer coil structure 906. At 1910 in FIG. 19, a second sacrificial material layer SL2 is formed over a portion of the first coil structure 906. FIG. 12 shows an

example in which a second material layer SL2 is formed over a portion of the first sacrificial material layer SL1 and over a portion of the previously formed first coil structure 906. At 1912 in FIG. 19, a second coil structure 908 is formed partially on the second sacrificial material layer SL2. As shown in FIG. 13, in one example, the second coil structure 908 is formed using a printing process to extend at least partially over the second sacrificial material layer SL2 and over a corresponding die pad 122 of the semiconductor die structure 9014 electrical connection through bond wires 124 to the second pair of leadframe electrical conductors 104b-1 and 104b-2.

[0039] Continuing at 1914 in FIG. 19, one or more further sacrificial material layers are formed. In the example of FIG. 14, a third sacrificial layer SL3 is formed to define the upper section of the prospective cavity 110 (e.g., FIG. 9), and thereafter a fourth sacrificial material layer SL4 is formed in order to define the prospective port opening 118 (e.g., FIG. 9). More or fewer sacrificial layers can be formed at 1914 in various implementations. At 1916, a molding process is performed to form a package material (e.g., 102 in FIG. 15) over the semiconductor die 901, the bond wires 124 and over portions of the leadframe structure 104 and the sacrificial material layers to create a molded package structure 102. As shown in FIG. 15, moreover, the molded package material 102 is formed in certain examples at least partially over one or both of the coil structures 906 and/or 908 for subsequent structural support thereof after sublimation of the sacrificial material layers. At 1918, the sacrificial material SL is sublimated to create an internal cavity 110 defined by an interior surface of the package structure 102, as shown for example in FIG. 16. The resulting internal cavity 110 includes at least a portion of an electrical isolation barrier between first and second coil structures 906 and 908, and also at least partially provides an air-core to magnetically couple the coil structures 906, 908 in certain examples. In certain examples, moreover, the cavity is sealed at 1920 in FIG. 19, for example by forming the seal structure 120 over the port 118 in the transformer ICs 900 of FIGS. 9, 10, 17 and 18 above.

[0040] The above examples are merely illustrative of several possible embodiments of various aspects of the present disclosure, wherein equivalent alterations and/or modifications will occur to others skilled in the art upon reading and understanding this specification and the annexed drawings. Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

The following is claimed:

1. An integrated circuit (IC), comprising:
 - a leadframe structure, including a plurality of electrical conductors;
 - first circuit structure electrically connected to a first pair of the electrical conductors of the leadframe structure, the first circuit structure including a light source configured to generate a light signal;
 - a second circuit structure spaced from the first circuit structure and electrically connected to a second pair of the electrical conductors of the leadframe structure, the second circuit structure including a light sensor at least partially facing the light source to receive the light signal; and
 - a molded package structure enclosing portions of the leadframe structure, the molded package structure exposing portions of the first and second pairs of the electrical conductors to allow external connection to the first and second circuit structures, the molded package structure including an internal cavity defined by an interior surface of the molded package structure, the cavity providing a solid-free optical path for the light signal between the first and second circuit structures.
2. The IC of claim 1, wherein the cavity is sealed.
3. The IC of claim 1, wherein the interior surface of the molded package structure includes a concave portion, and wherein the concave portion of the interior surface includes a reflective coating to reflect light from the light source toward the light sensor.
4. The IC of claim 1, wherein the light source includes a light emitting diode (LED).
5. The IC of claim 1, wherein the light sensor includes a diode.
6. The IC of claim 5, wherein the light sensor includes a plurality of diodes.
7. The IC of claim 6, wherein the light sensor includes a plurality of connected diodes, the individual diodes including N and P regions of a semiconductor die arranged along the optical path.
8. The IC of claim 6, wherein the light sensor includes a plurality of connected diodes, the individual diodes including N and P regions of a semiconductor die arranged normal to the optical path.
9. The IC of claim 1, wherein the light sensor includes a transistor.

10. The IC of claim 1, wherein the molded package structure encloses portions of the first and second circuit structures.
11. An integrated circuit, comprising:
 - a leadframe structure, including a plurality of electrical conductors;
 - a first coil structure electrically connected to a first pair of the electrical conductors of the leadframe structure, the first coil structure partially formed on a semiconductor die structure;
 - a second coil structure electrically connected to a second pair of the electrical conductors of the leadframe structure, the second coil structure partially formed on the semiconductor die structure; and
 - a molded package structure enclosing portions of the leadframe structure, the molded package structure exposing portions of the first and second pairs of the electrical conductors to allow external connection to the first and second coil structures, the molded package structure including a cavity to magnetically couple portions of the first and second coil structures.
12. The IC of claim 11, wherein the cavity is sealed.
13. The IC of claim 11, wherein portions of the first and second coil structures extend in the cavity.
14. The IC of claim 13, wherein the molded package structure encloses portions of the first and second coil structures.
15. The IC of claim 14, further comprising a ferrous material extending at least partially in the cavity.
16. The IC of claim 11, wherein the molded package structure encloses portions of the first and second coil structures.
17. The IC of claim 11, further comprising a ferrous material extending at least partially in the cavity.
18. The IC of claim 17, wherein the ferrous material is formed on the semiconductor die structure.
19. A method to fabricate an integrated circuit (IC), the method comprising:
 - mounting at least one semiconductor die on a leadframe structure;
 - connecting a plurality of bond wires between bond pads of the semiconductor die and corresponding electrical conductors of the leadframe structure;
 - forming a sacrificial material over a portion of the semiconductor die;

forming a molded package material over the semiconductor die, the bond wires and portions of the leadframe structure and the sacrificial material to create a molded package structure; and

sublimating the sacrificial material to create an internal cavity defined by an interior surface of the molded package structure, the internal cavity including at least a portion of an isolation barrier between first and second circuits associated with the semiconductor die.

20. The method of claim 19, further comprising sealing the internal cavity.

21. The method of claim 19, further comprising:

mounting a first semiconductor die on the leadframe structure, the first semiconductor die including a light source configured to generate a light signal along an optical path;

mounting a second semiconductor die on the leadframe structure, the second semiconductor die including a light sensor at least partially facing the optical path and spaced from the light source of the first semiconductor die to receive the light signal;

connecting die pads of the first semiconductor die to a first pair of the electrical conductors of the leadframe structure;

connecting die pads of the second semiconductor die to a second pair of the electrical conductors of the leadframe structure; and

forming the sacrificial material over a portion of the first and second semiconductor dies at least partially along the optical path;

wherein sublimating the sacrificial material creates the internal cavity including at least a portion of the optical path to allow transmission of the light signal between the light source and the light sensor.

22. The method of claim 21, wherein the sacrificial material is formed as a drop having a convex surface, the method further comprising forming a reflective coating on the convex surface of the sacrificial material, and forming the molded package material on the reflective coating.

23. The method of claim 19, further comprising:

connecting a first pair of die pads of the semiconductor die to a first pair of the electrical conductors of the leadframe structure;

connecting a second pair of die pads of the semiconductor die to a second pair of the electrical conductors of the leadframe structure;

forming a first sacrificial material layer over a portion of the semiconductor die;

forming a first coil structure partially on the first sacrificial material layer, the first coil structure electrically connected to the first pair of the electrical conductors of the leadframe structure;

forming a second sacrificial material layer over a portion of the first coil structure;

forming a second coil structure partially on the second sacrificial material layer, the second coil structure electrically connected to the second pair of the electrical conductors of the leadframe structure;

forming a third sacrificial material layer over a portion of the second coil structure; and

forming the molded package material over the semiconductor die, the bond wires and portions of the leadframe structure, the first and second coil structures, and the sacrificial material layers to create the molded package structure;

wherein sublimating the sacrificial material includes sublimating the sacrificial material layers to create the internal cavity to provide an electrical isolation barrier between portions of the first and second coil structures.

24. The method of claim 23, further comprising:

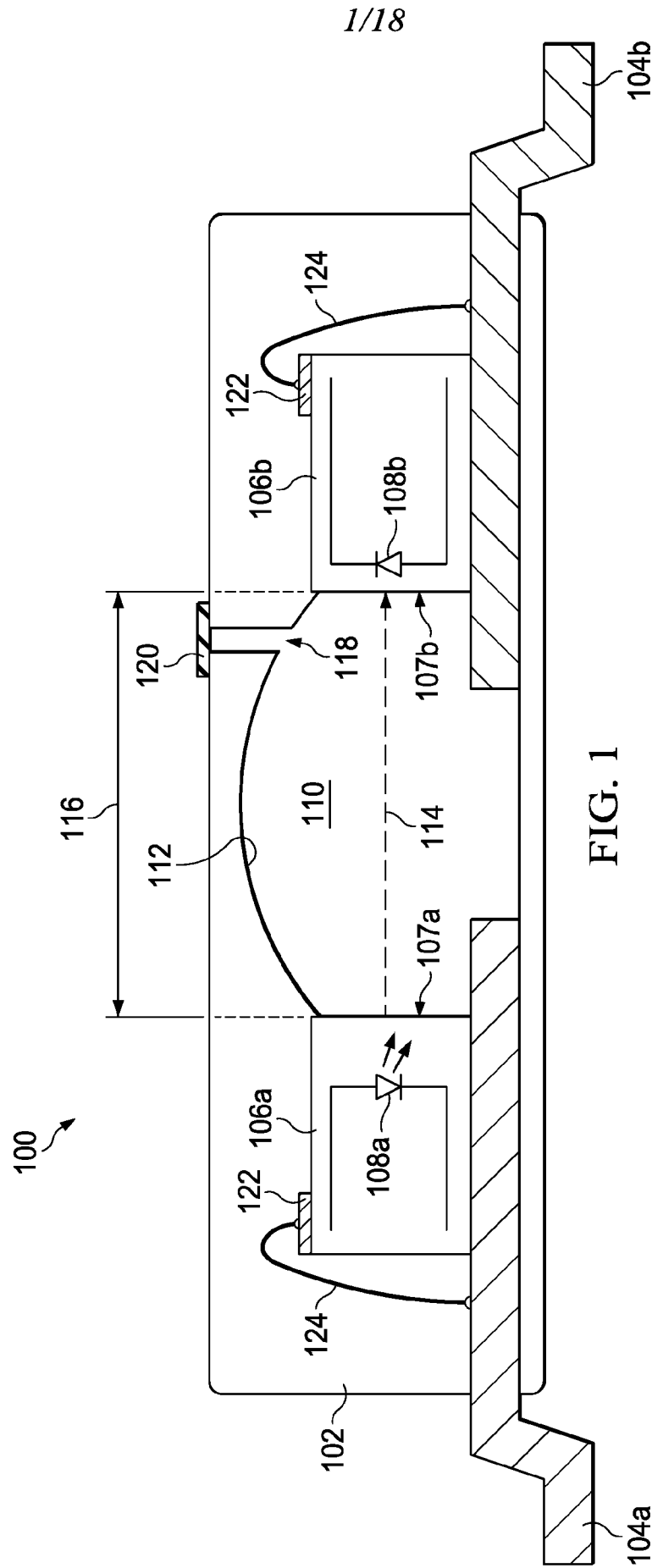
forming a ferrous material layer over a portion of one of the semiconductor die and one of the coil structures prior to forming the molded package material.

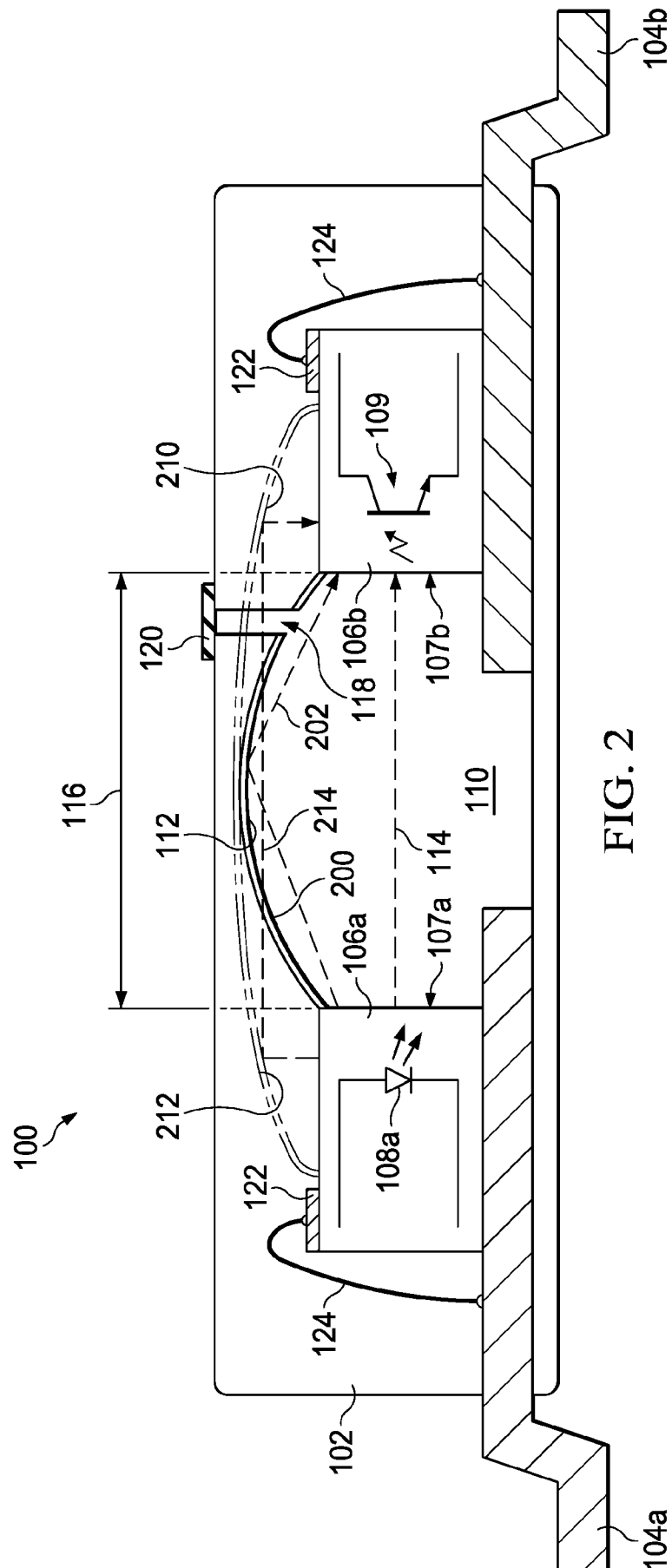
25. The method of claim 23, comprising:

mounting first and second semiconductor dies on the leadframe structure;

forming the first coil structure partially on the first semiconductor die; and

forming the second coil structure partially on the second semiconductor die.





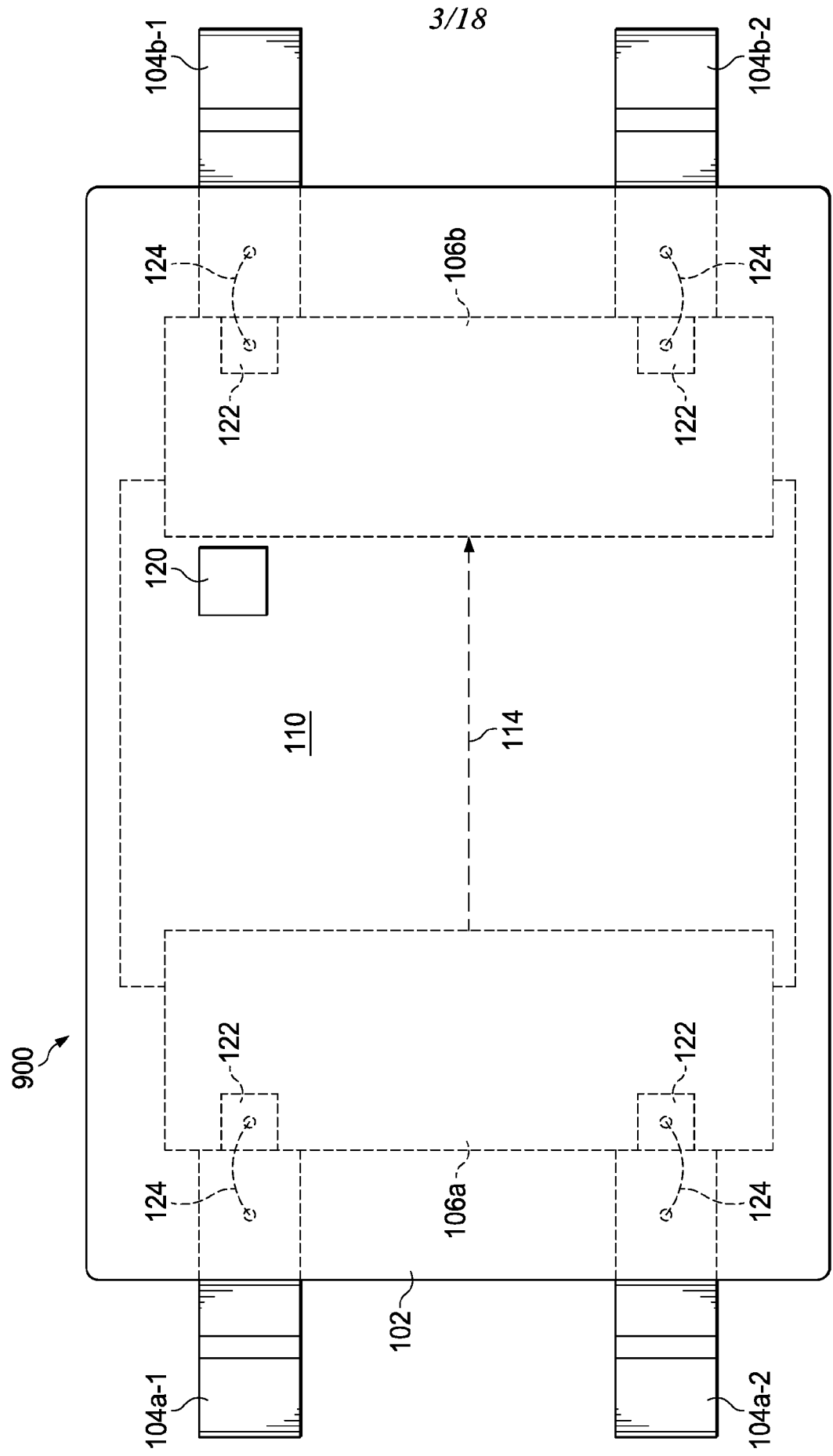
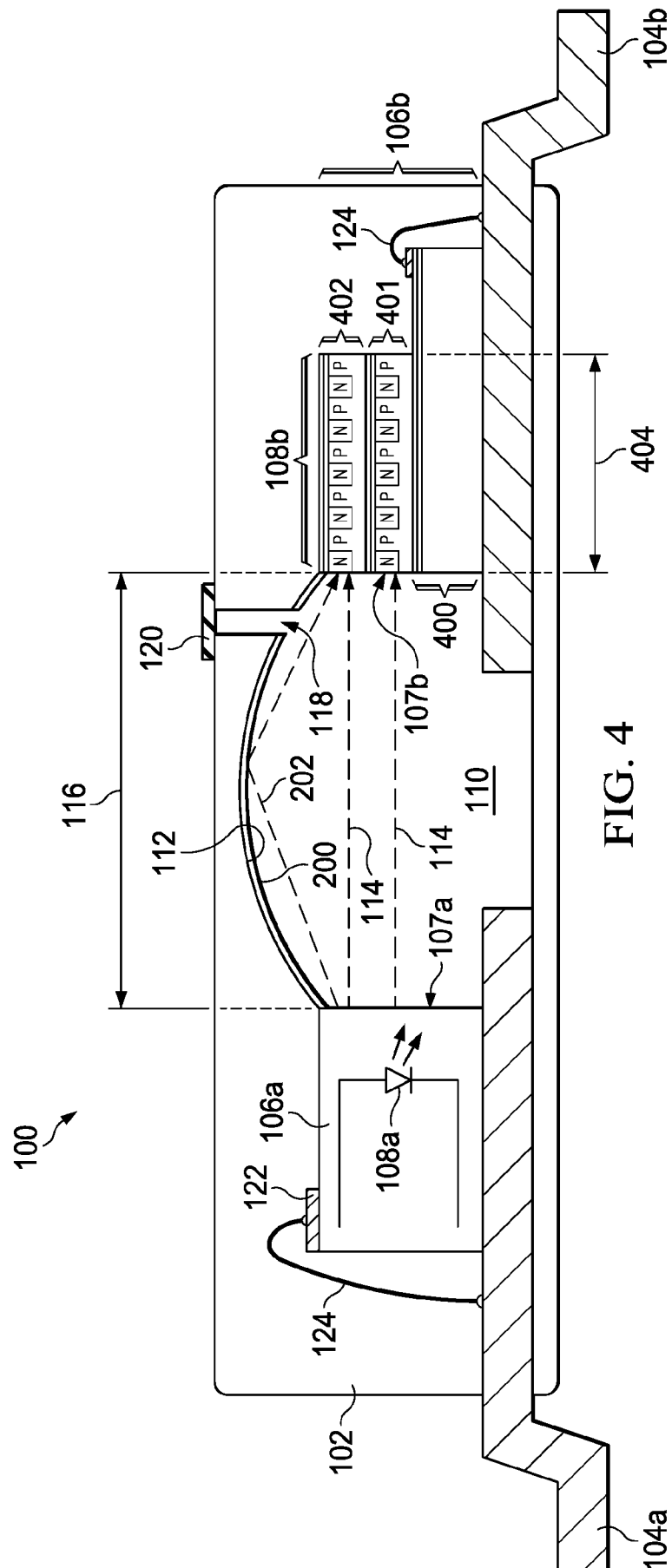


FIG. 3



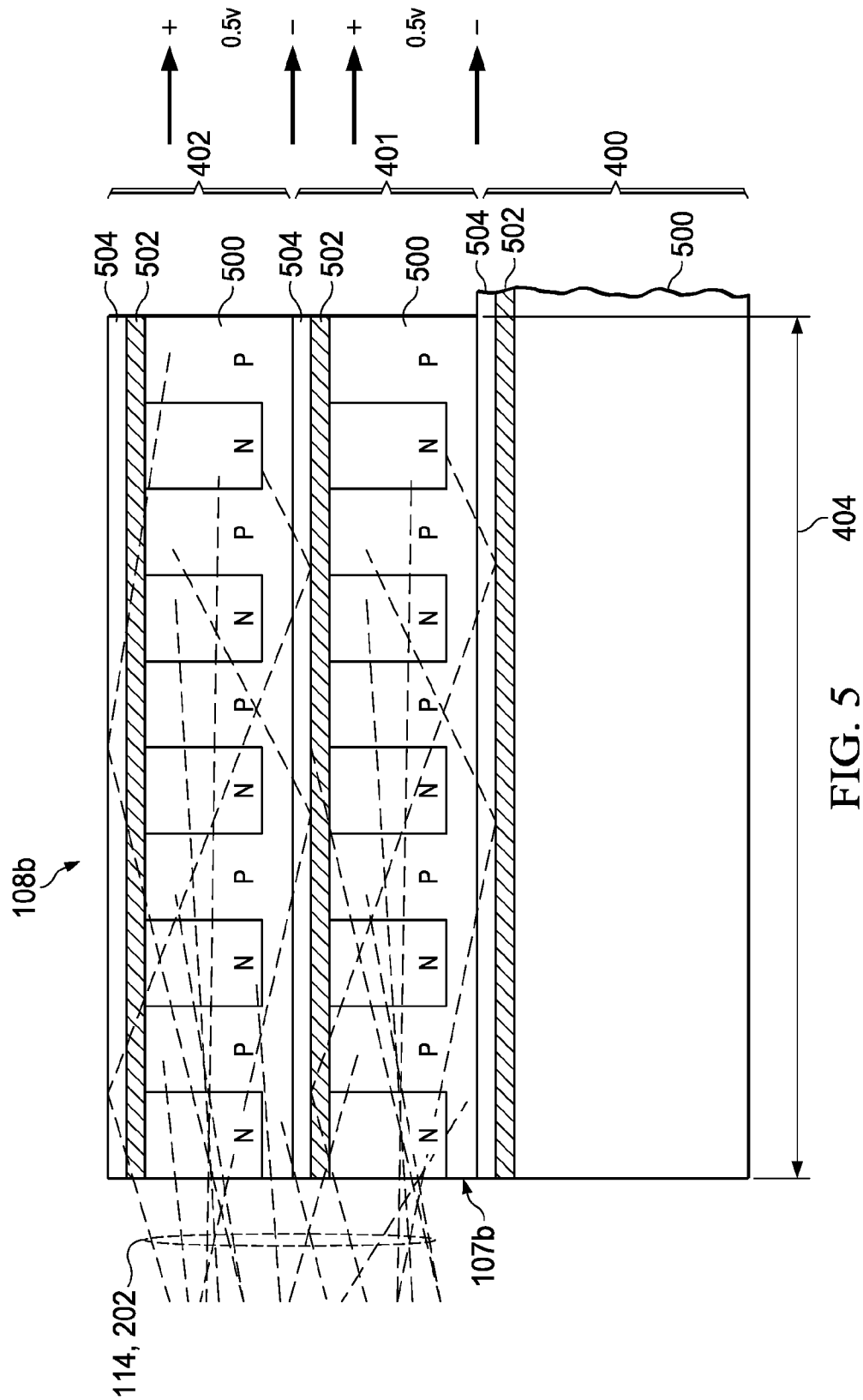


FIG. 5

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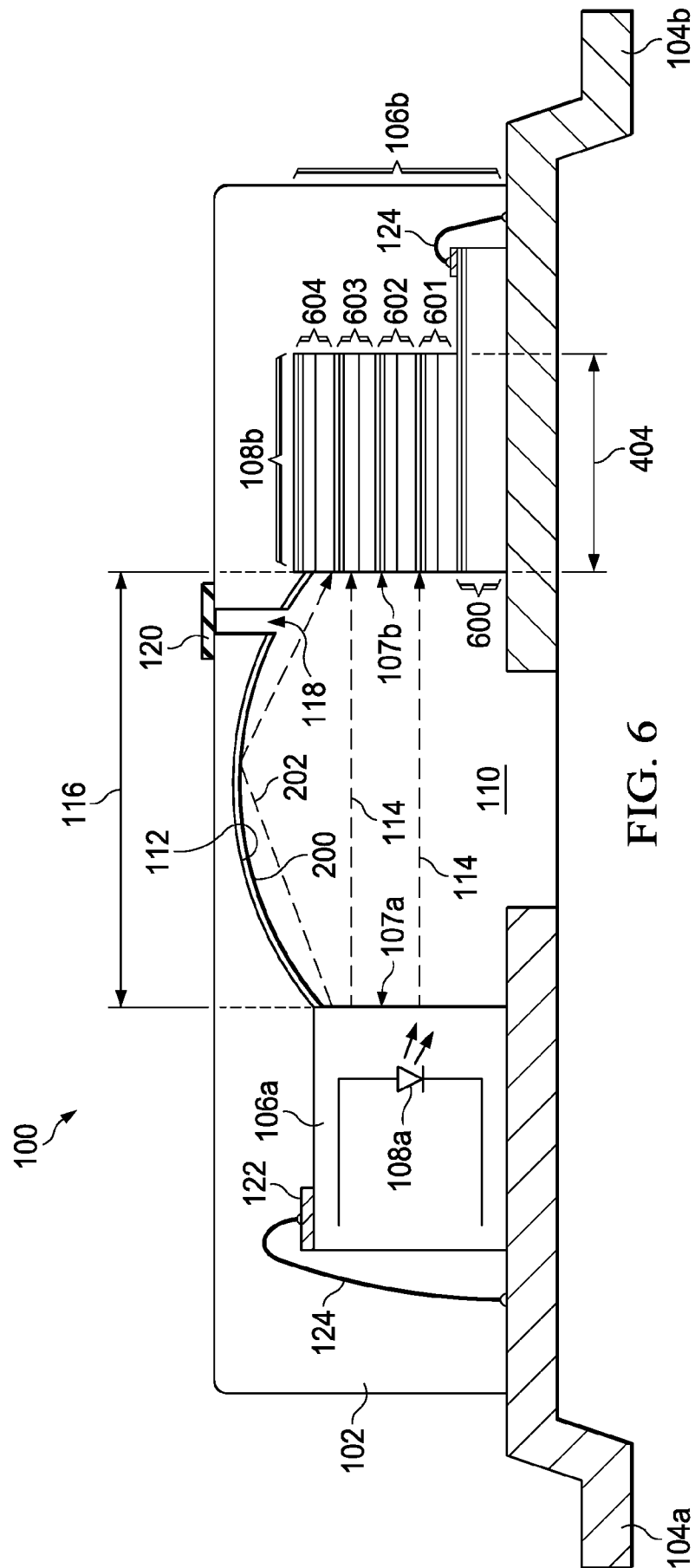


FIG. 6

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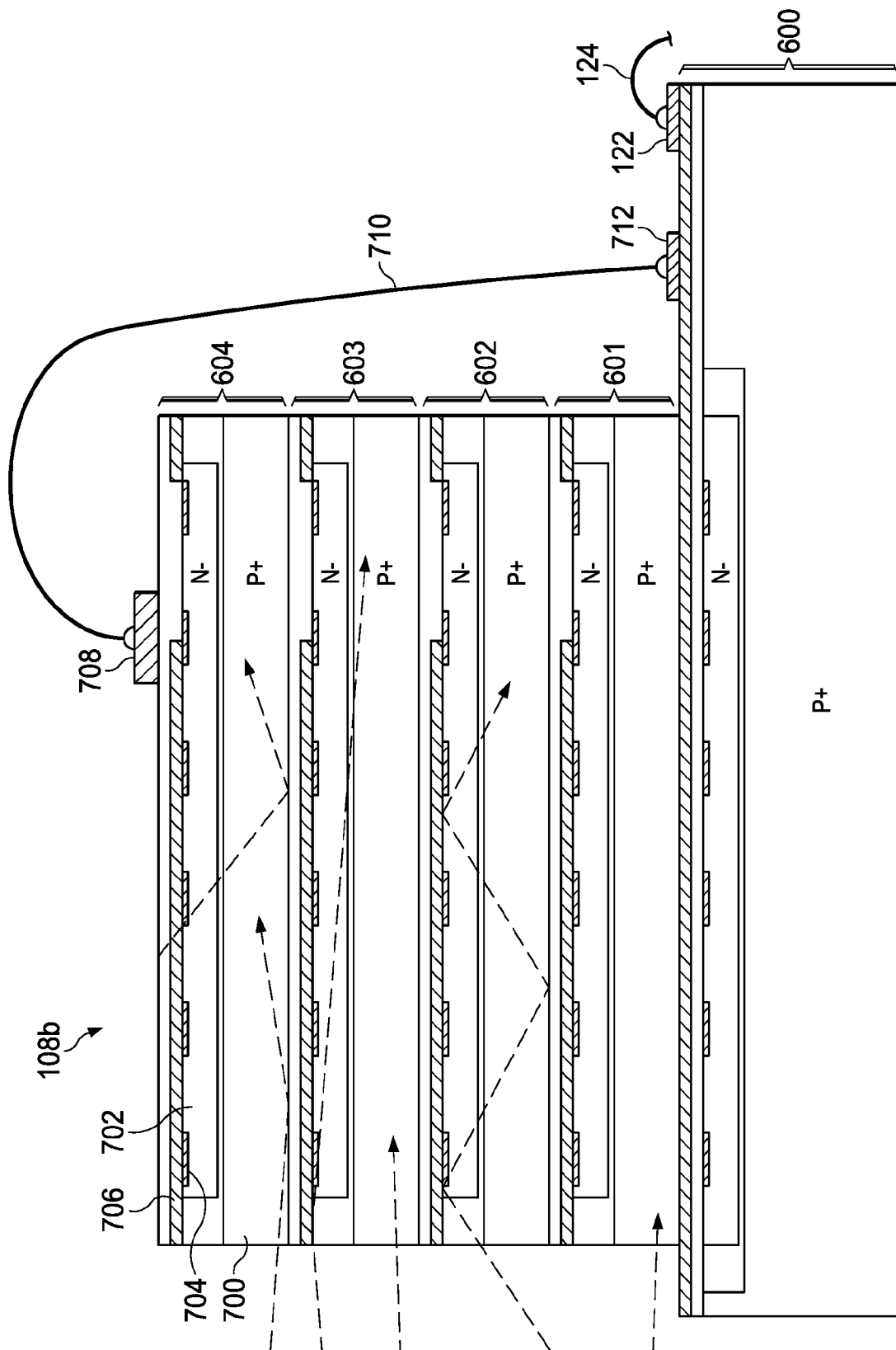


FIG. 7

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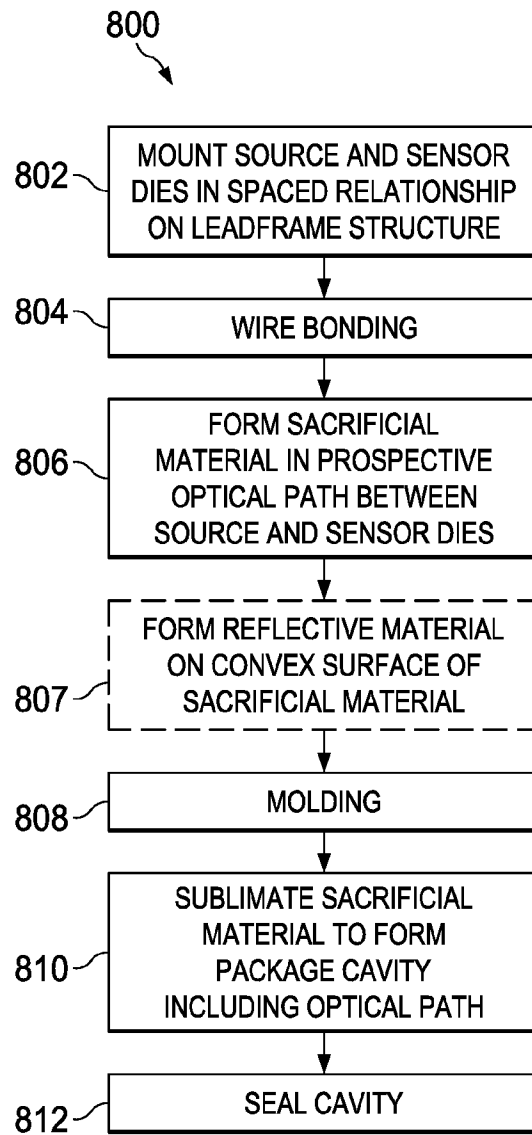


FIG. 8

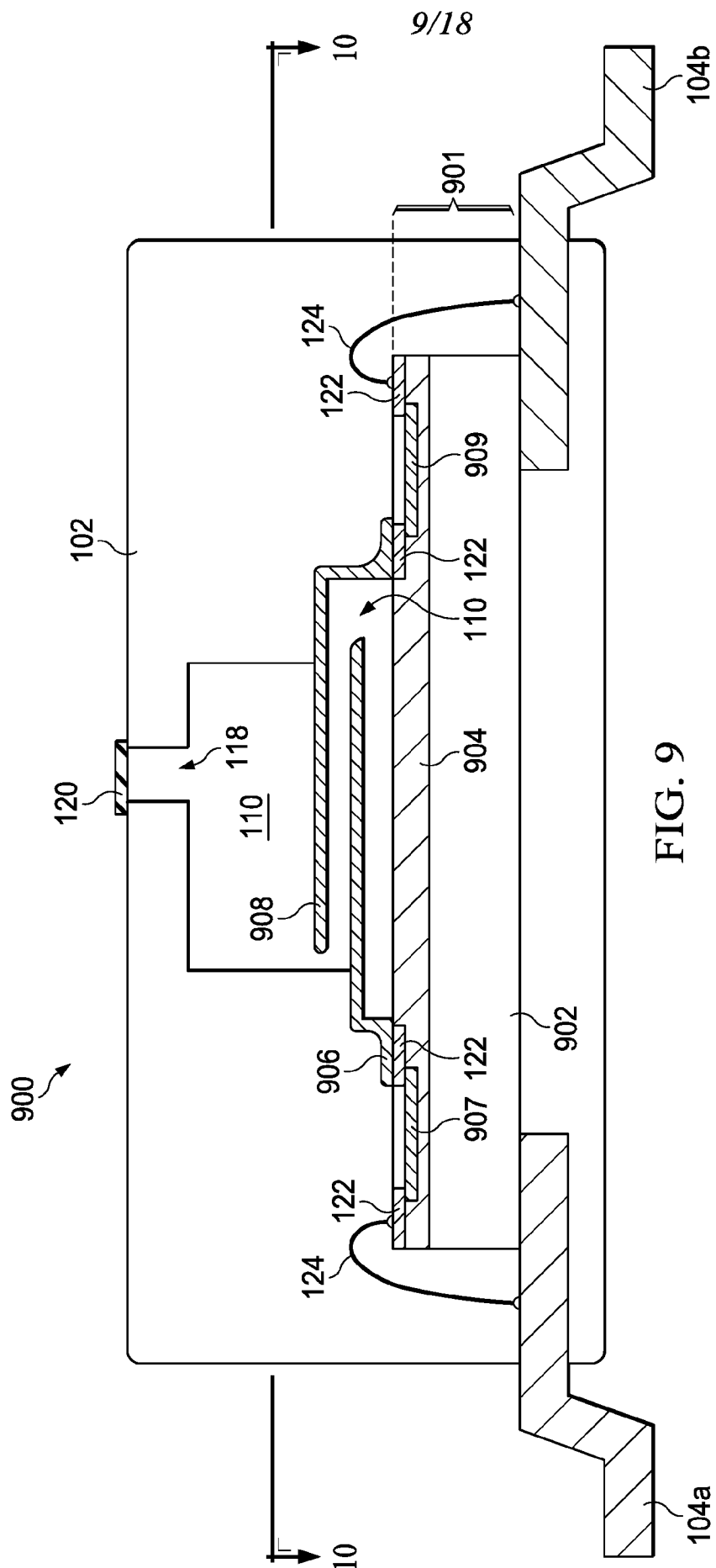


FIG. 9

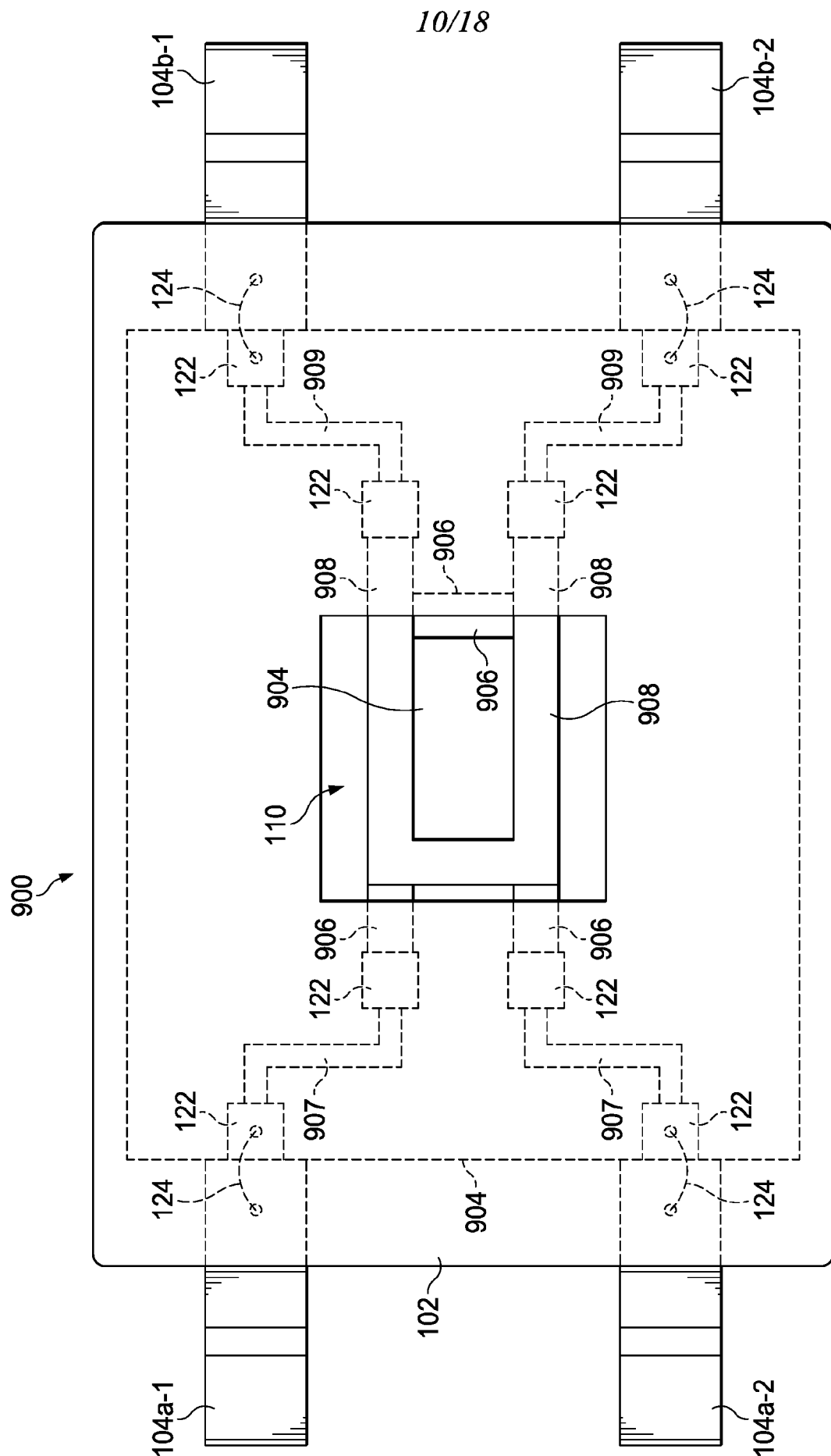


FIG. 10

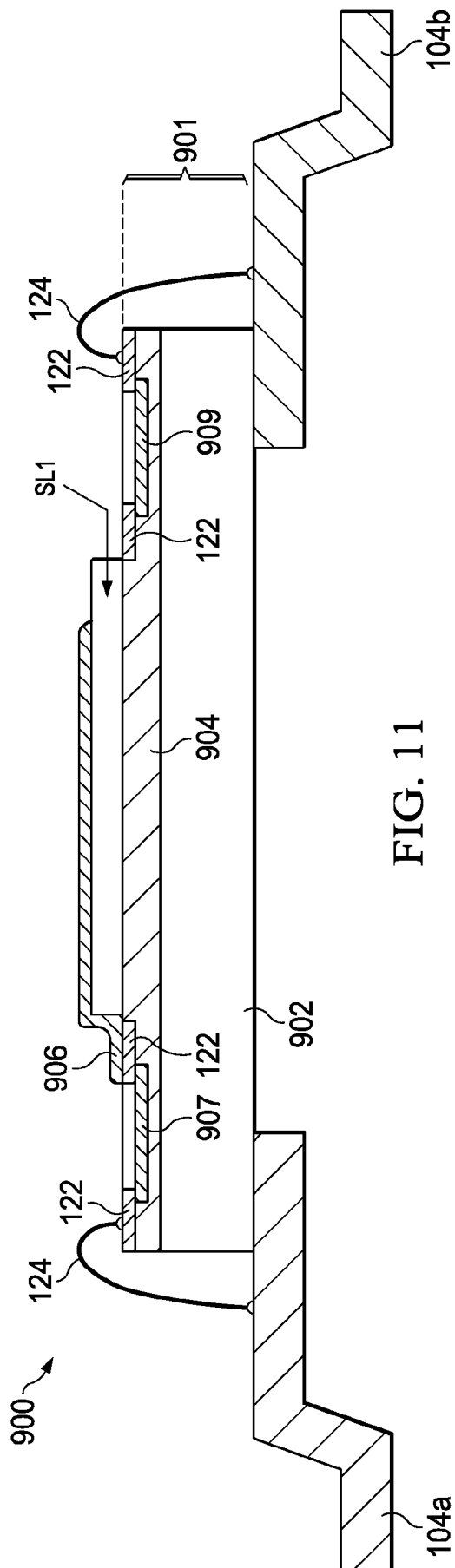


FIG. 11

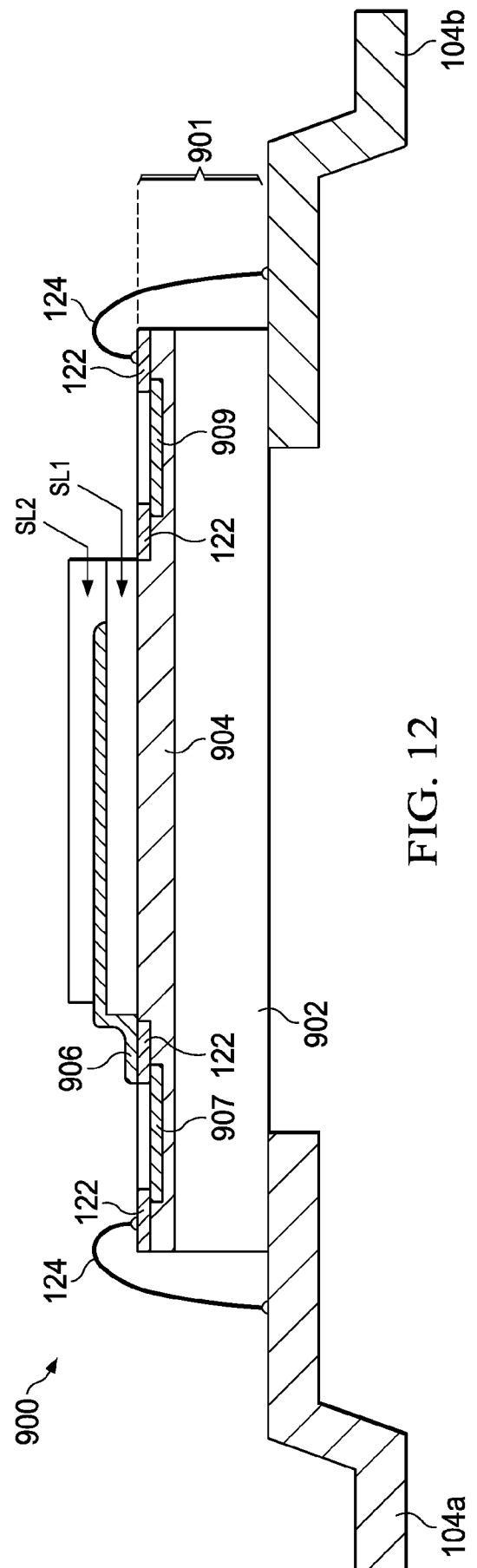


FIG. 12

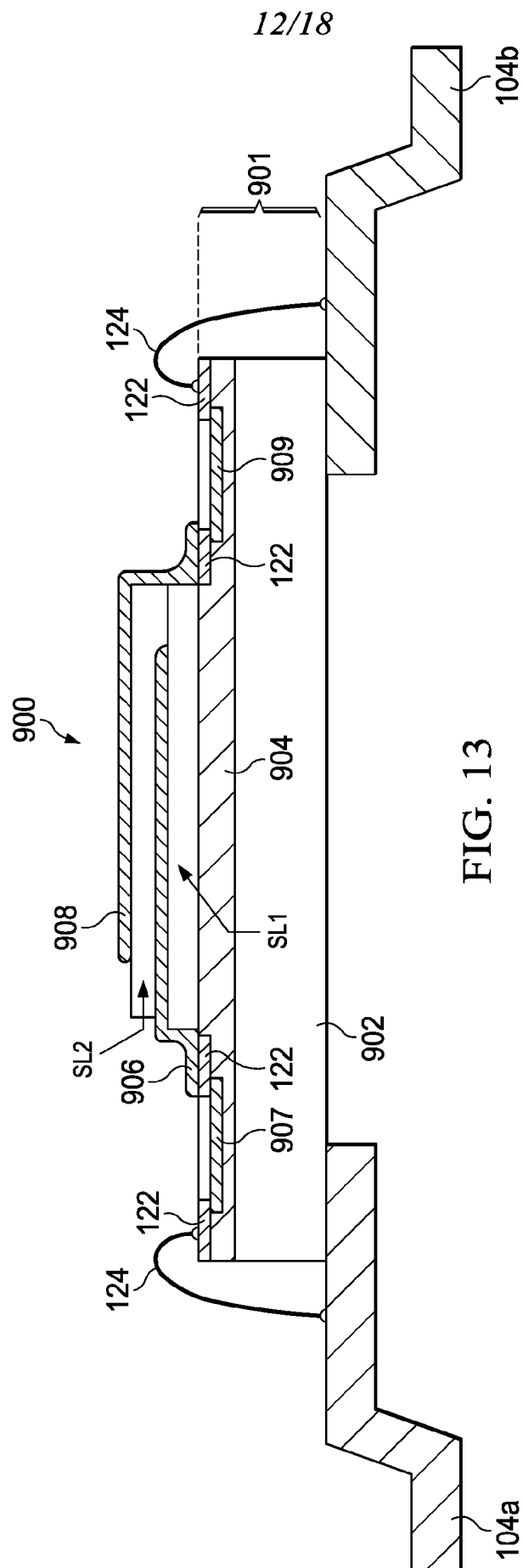


FIG. 13

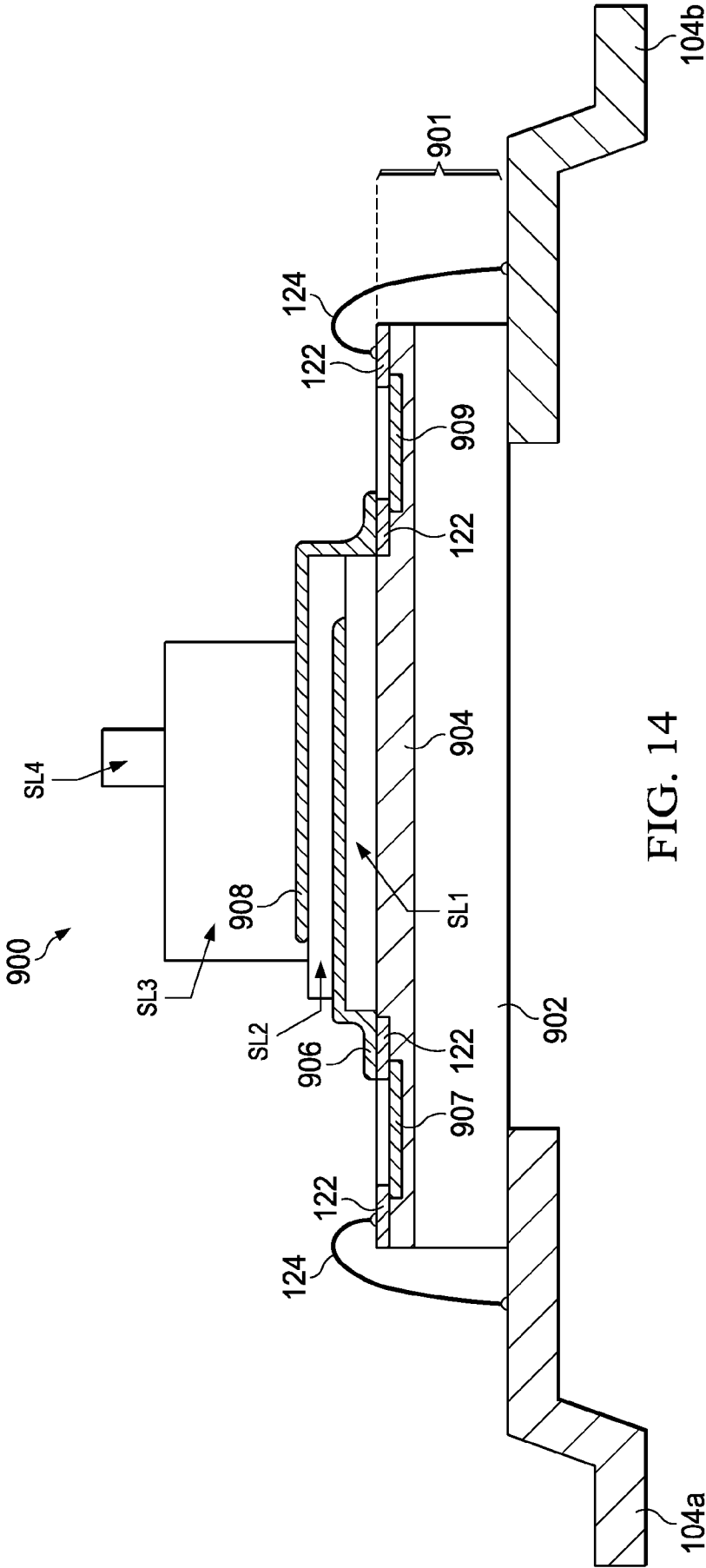
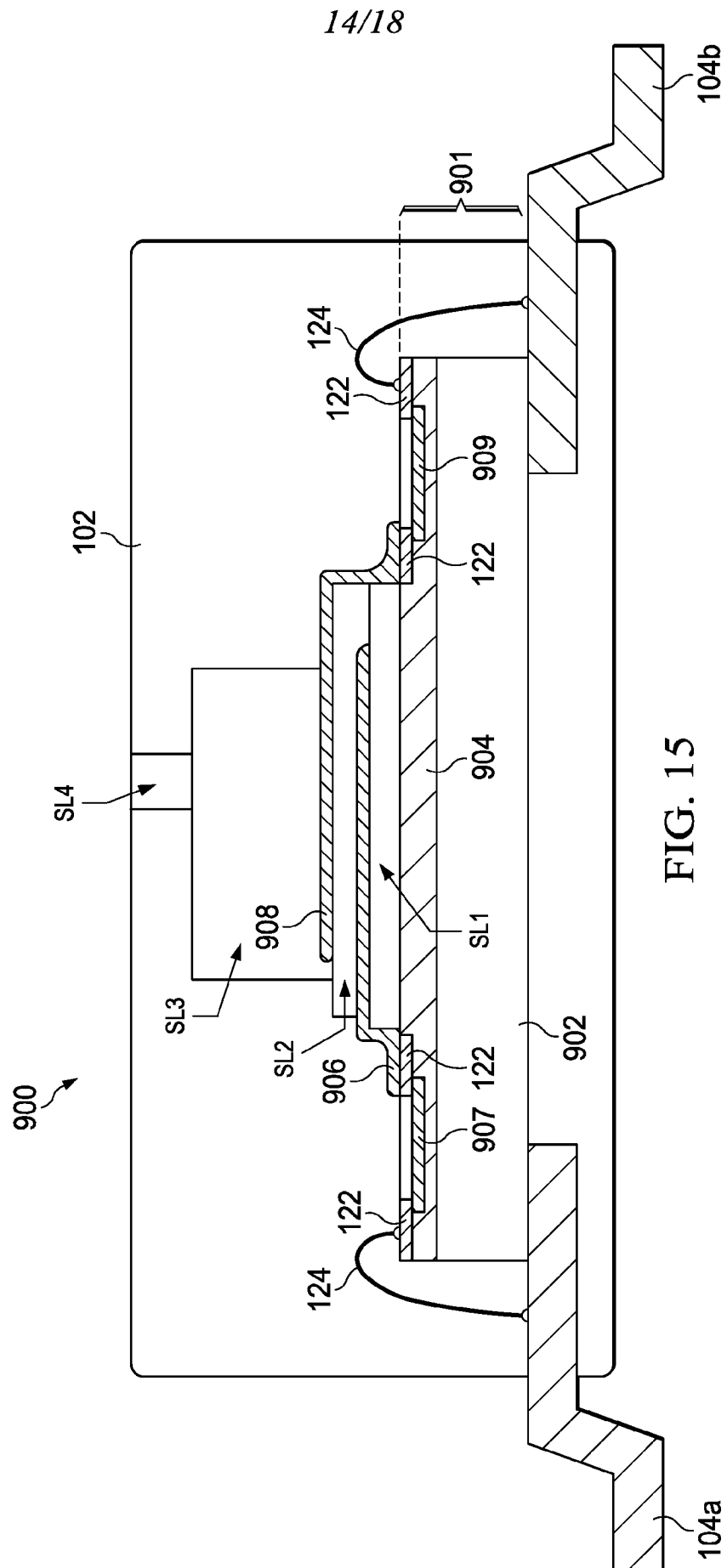
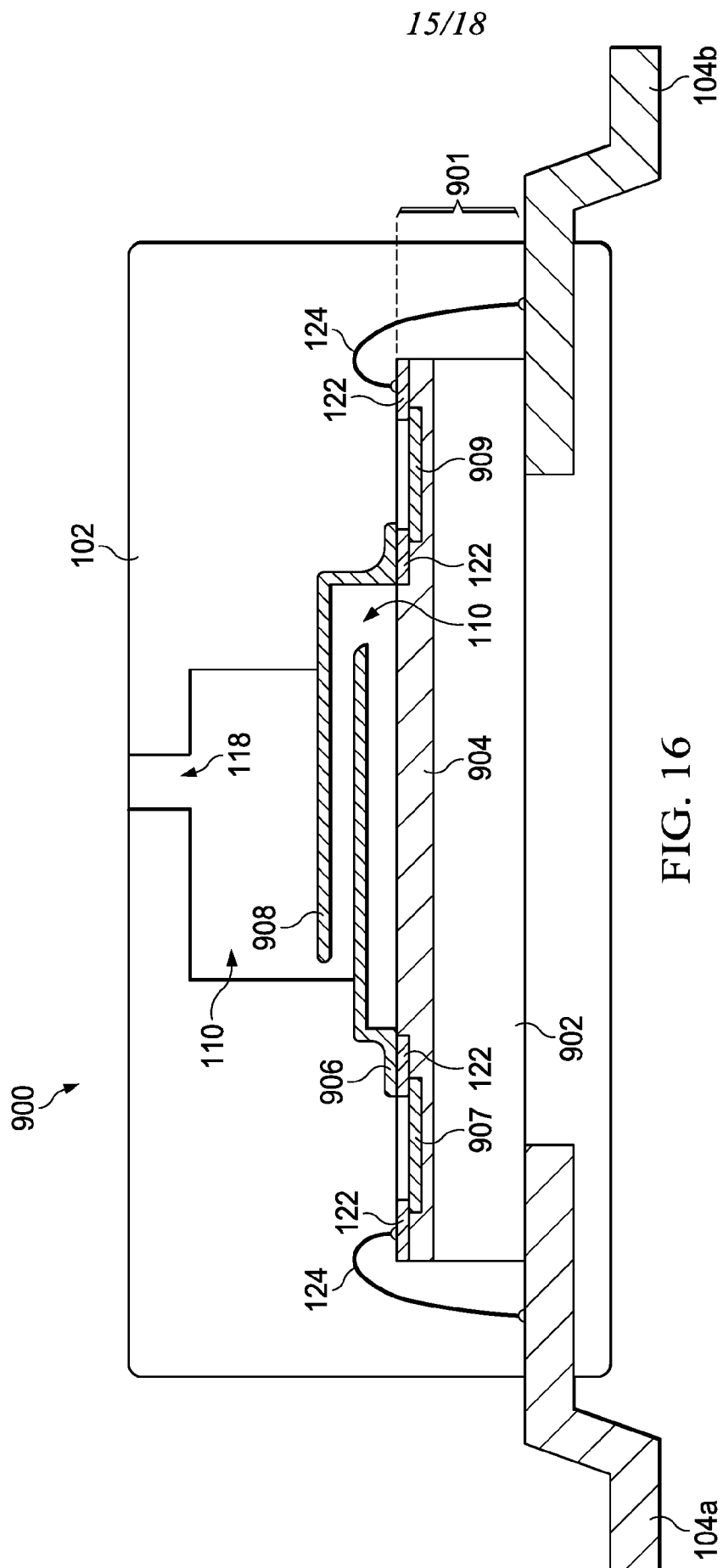
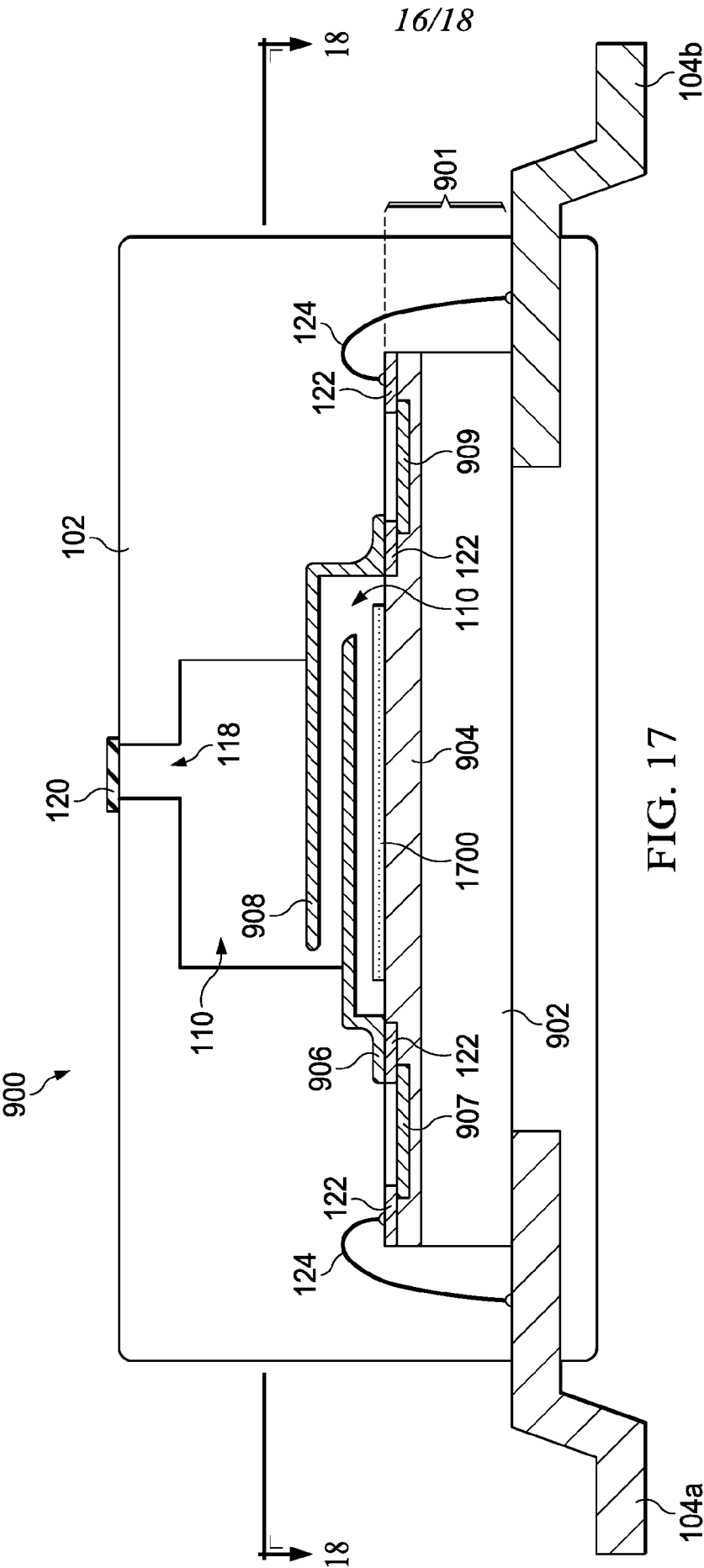


FIG. 14







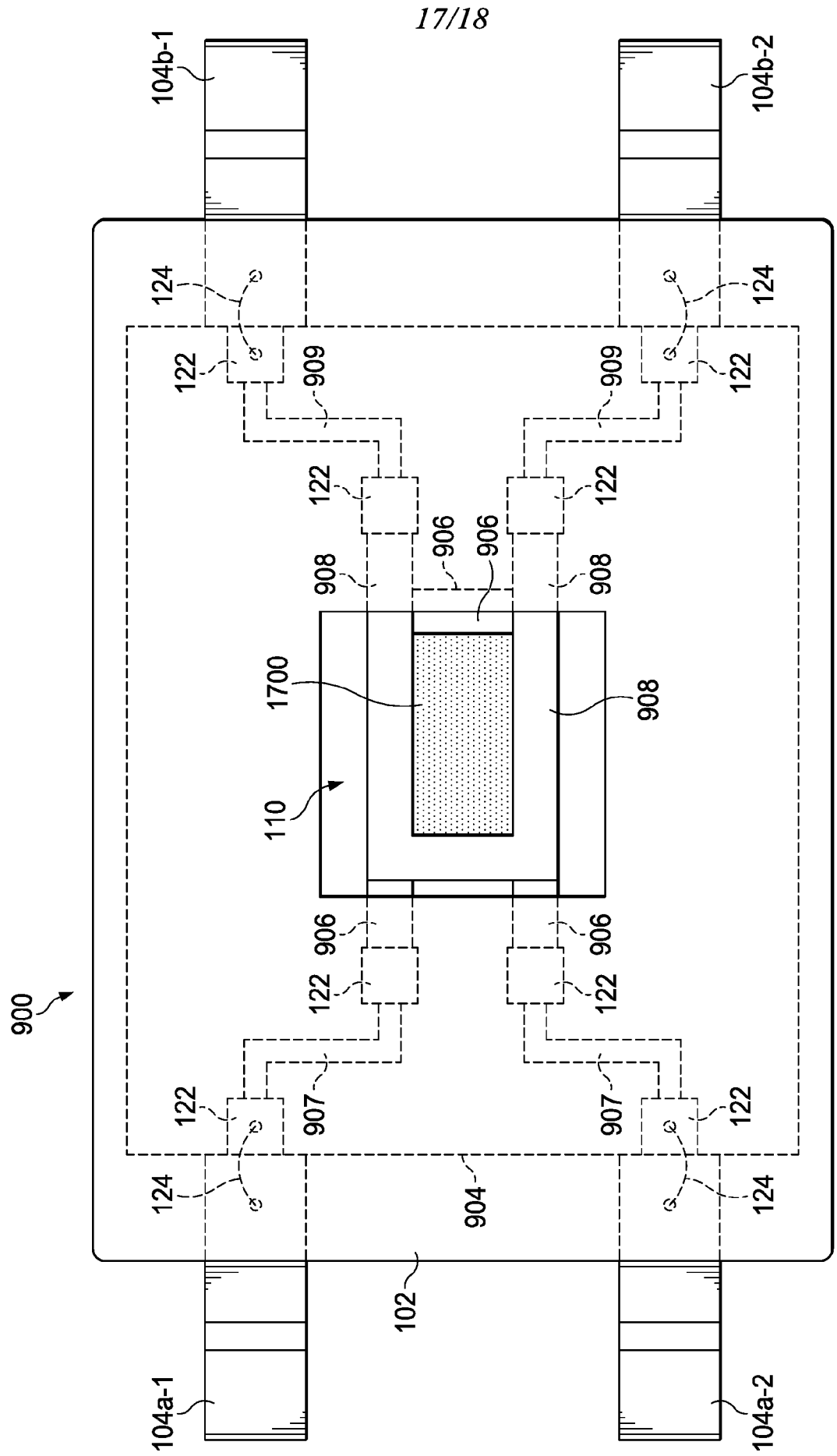


FIG. 18

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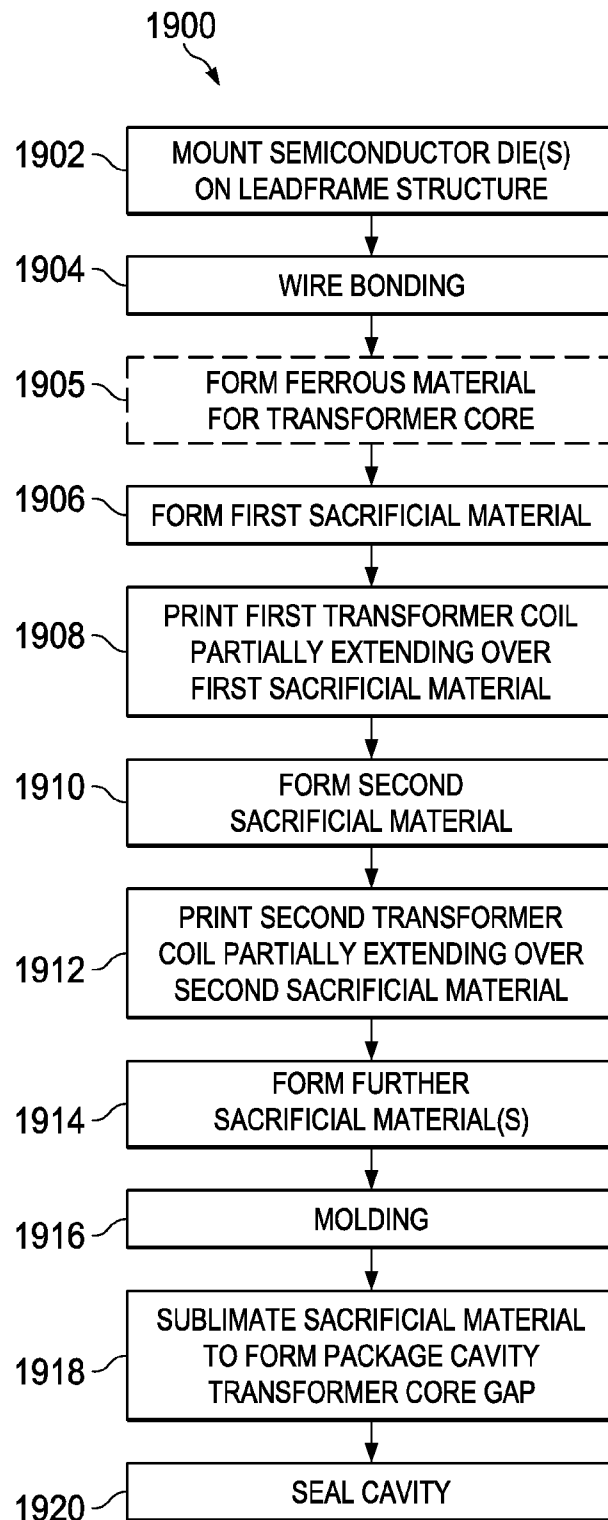


FIG. 19

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2017/068983

A. CLASSIFICATION OF SUBJECT MATTER														
<i>H01L 31/16 (2006.01)</i>														
According to International Patent Classification (IPC) or to both national classification and IPC														
B. FIELDS SEARCHED														
Minimum documentation searched (classification system followed by classification symbols)														
H01L 31/14-31/167														
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched														
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)														
PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, DWPI, EAPATIS, PATENTSCOPE, Information Retrieval System of FIPS														
C. DOCUMENTS CONSIDERED TO BE RELEVANT														
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.												
X	US 6031251 A1 (MOTOROLA INC) 29.02.2000, abstract, fig. 8, 9, col.5, lines 51-65	1-2, 4-8, 10												
Y		3, 9, 11-18												
Y	US 2009/0052214 A1 (FUJI ELECTRIC DEVICE TECHNOLOGY CO., LTD) 26.09.2009, fig.2b, [0124], [0126]	11-18												
Y	RU 2263999 C1 (ZAO "SINTEZ EHLEKTRONNYKH KOMPONENTOV") 10.11.2005, fig.1	3												
☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.														
<table border="0"> <tr> <td>* Special categories of cited documents:</td> <td>"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention</td> </tr> <tr> <td>"A" document defining the general state of the art which is not considered to be of particular relevance</td> <td>"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone</td> </tr> <tr> <td>"E" earlier document but published on or after the international filing date</td> <td>"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art</td> </tr> <tr> <td>"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)</td> <td>"&" document member of the same patent family</td> </tr> <tr> <td>"O" document referring to an oral disclosure, use, exhibition or other means</td> <td></td> </tr> <tr> <td>"P" document published prior to the international filing date but later than the priority date claimed</td> <td></td> </tr> </table>			* Special categories of cited documents:	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention	"A" document defining the general state of the art which is not considered to be of particular relevance	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone	"E" earlier document but published on or after the international filing date	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art	"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&" document member of the same patent family	"O" document referring to an oral disclosure, use, exhibition or other means		"P" document published prior to the international filing date but later than the priority date claimed	
* Special categories of cited documents:	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention													
"A" document defining the general state of the art which is not considered to be of particular relevance	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone													
"E" earlier document but published on or after the international filing date	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art													
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&" document member of the same patent family													
"O" document referring to an oral disclosure, use, exhibition or other means														
"P" document published prior to the international filing date but later than the priority date claimed														
Date of the actual completion of the international search		Date of mailing of the international search report												
26 April 2018 (26.04.2018)		17 May 2018 (17.05.2018)												
Name and mailing address of the ISA/RU: Federal Institute of Industrial Property, Berezhkovskaya nab., 30-1, Moscow, G-59, GSP-3, Russia, 125993 Facsimile No: (8-495) 531-63-18, (8-499) 243-33-37		Authorized officer N. Listvina Telephone No. (499) 240-25-91												

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2017/068983

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2011/0108747 A1 (YONG LIU) 12.05.2011, abstract	9
A	RU 2169962 C2 (SHEN MING-TUNG) 27.06.2011	19-25
A	EP 2490263 A2 (NXP B.V.) 22.08.2012	1-25
A	US 2004/0111881 A1 (HUNG YU YANG et al.) 17.06.2004	1-25