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(54) Title: INTERFACE APPARATUS AND METHOD IN AN ACOUSTIC MICROPHONE SYSTEM

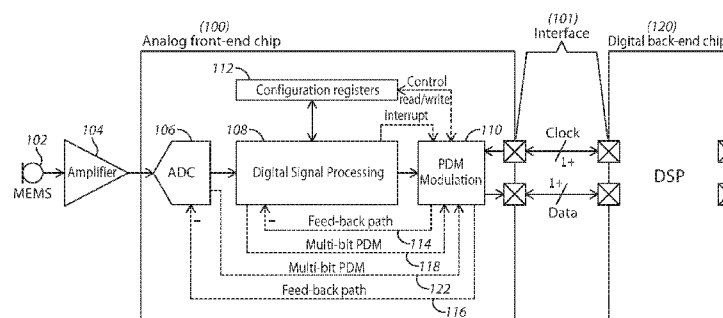


FIG. 1

(57) Abstract: Digital data representing sound energy is received. The digital data is compressed and encoded into compressed and encoded digital data. The compressed and encoded digital data is inserted into a frame structure. The frame structure is transmitted to a digital signal processor over a physical interface, and the physical interface includes one or more data lines and a clock line. The compression is effective to provide sufficient space within the frame structure for control information.

INTERFACE APPARATUS AND METHOD IN AN ACOUSTIC MICROPHONE SYSTEM

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This patent claims benefit under 35 U.S.C. §119(e) to United States Provisional Application No. 62/158,057 entitled “Interface Apparatus and Method in an Acoustic Microphone System” filed May 7, 2015, the content of which is incorporated herein by reference in its entirety.

TECHNICAL FIELD

[0002] This disclosure relates to acoustic systems, and, more specifically to interfaces in microphone systems.

BACKGROUND

[0003] Different types of acoustic devices have been used through the years. One type of device is a microphone and one type of microphone is a microelectromechanical system (MEMS) microphone having a MEMS die that includes a diaphragm and a back plate. In a MEMS microphone, the MEMS die is supported by a substrate and the MEMS die is enclosed by a housing (e.g., a cup or cover with walls). A port may extend through the substrate (for a bottom port device) or through the top of the housing (for a top port device). In any case, sound energy traverses the port, moves the diaphragm relative to the back plate, which creates an electrical signal. Microphones are deployed in various types of devices such as personal computers or cellular phones.

[0004] In microphone systems, there is often a chip that holds different circuits or applications and is connected to a digital signal processor. In these systems, because there is much data moving between the devices, there needs to be multiple data lines and multiple control lines. This in turn increases the area, the cost, and the power used by the system. In fact, these items can also increase noise problems in the systems.

[0005] The problems of previous approaches have resulted in some user dissatisfaction with these previous approaches.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] For a more complete understanding of the disclosure, reference should be made to the following detailed description and accompanying drawings wherein:

[0007] FIG. 1 is a block diagram of an interface between an analog chip and a digital signal processor;

[0008] FIG. 2 is a flow chart for encoding data in the interface;

[0009] FIG. 3 is a flow chart for decoding data in the interface;

[0010] FIGs. 4A, 4B, and 4C are diagrams of framing structures;

[0011] FIG. 5 is a diagram of a physical layer structure used in the interface.

[0012] Those of ordinary skill in the art will appreciate that elements in the figures are illustrated for simplicity and clarity. It will be further appreciated that certain actions and/or steps may be described or depicted in a particular order of occurrence while those of ordinary skill in the art will understand that such specificity with respect to sequence is not actually required. It will also be understood that the terms and expressions used herein have the ordinary meaning as is accorded to such terms and expressions with respect to their corresponding respective areas of inquiry and study except where specific meanings have otherwise been set forth herein.

DETAILED DESCRIPTION

[0013] The present approaches provide for the compression or bunching of data so as to decrease latency and power consumption across an interface between an analog chip and a digital signal processor (DSP). By reducing the amount of data, fewer lines are needed between the analog chip and the DSP, reducing latency and power consumption of the interface. In some examples, two wires (e.g., a clock and data) are used. In other examples, three lines (a clock and two data lines for bidirectional data transfer) are used. As used herein, “latency” means the time delay between an input and a response/output.

[0014] The present approaches provide a point-to-point audio interface between a microphone and a digital signal processor (DSP). In one aspect, a two-wire interface is provided. Simultaneous data and bi-directional command, control and interrupt functionality is also provided. Support for bi-directional and simultaneous audio data between the microphone and the DSP may also be provided, for example, using a three-wire interface. Pulse code modulation (PCM) data is also supported. Support for a low latency, three-level audio stream is provided in one example. This supports enhanced SNR at low audio stream bit rates facilitating low interface power consumption levels. Support for a low latency nine-level pulse density modulation (PDM) audio stream for direct path out of the multi-level chip (e.g., using a three-wire interface) is additionally provided.

[0015] Referring now to FIG. 1, one example of an interface 101 between an analog front end chip 100 and a digital back end chip 120 is described. The analog front end chip 100 is coupled to a MEMS transducer 102, and an amplifier 104, and includes an analog-to-digital converter (ADC) 106, a digital signal processing circuit or module 108, a PDM modulation circuit or module 110, and configuration registers 112.

[0016] By “interface” and as used herein, it is meant (1) the physical interface (e.g., the number of wires, what is carried on the wires); (2) the layers on top of the physical interface (describing how information is transmitted, frame structure, compression functionality); and (3) how the interface operates. Some of this functionality may be implemented at the analog front end chip 100 or the digital back end chip 120.

[0017] The MEMS transducer 102 includes a diaphragm and a back plate. A charge pump (not shown) may also couple to the MEMS transducer 102. Sound moves the diaphragm, which with the back plate creates an electrical signal representative of the sound.

[0018] The amplifier 104 amplifies the signal produced by the MEMS transducer 102. The analog-to-digital converter (ADC) 106 converts the analog signal to PCM or multi-bit PDM.

[0019] The digital signal processing circuit 108 performs processing of the signal received from the ADC 106. For example, the circuit 108 may remove wind noise or perform high pass filtering on the received signal.

[0020] The PDM modulation circuit or module 110 receives data from the module 108, compresses the data, puts the data into frames, and synchronously clocks the data out as a transmission over the physical portions of the interface 101 to the DSP 120. The PDM modulation circuit 110 may be implemented according to any combination of hardware and/or programmed software (e.g., executed on a microprocessor).

[0021] The configuration registers 112 store various parameters used such as identification information or parameters used by various modules of the analog front end chip 100.

[0022] In example of the operation of the system of FIG. 1, analog data representative of sound energy is created by the MEMS microphone 102. As explained above, a change in sound pressure produces an electrical signal from the MEMS transducer 102. The analog electrical signal so-produced is amplified by amplifier 104 and then received by the ADC 106, which converts the analog signal to PCM or multi-bit PDM. This converted signal is sent to the digital signal processing module 108, where some processing of the signal may occur (e.g., removing wind noise, performing high pass filtering). The processed signal is transmitted to the PDM modulation circuit 110, where the data is compressed, put in frames, and clocked out to the DSP 120 via the interface 101. The chip 100 may also include a coupler arrangement or circuit (e.g., pins or wires) that provides an electrical coupling between the PDM modulation circuit 110, and the clock and data lines. The configuration register 112 may have configuration information for the analog front-end chip 100. Feedback lines 114 and 116 increase the accuracy of the determinations made by the Digital Signal processing module 108 and the PDM modulation

circuit 110 and/or increase the overall performance such as improving tolerance for high acoustic inputs (high-SPL levels) or effective higher signal to noise ratio. Multi-bit PDM paths 118 and 122 extend from the ADC 106 and digital signal processing module 108 to the PDM modulation circuit 110. The circuit 110 may be implemented in a variety of different ways including using a microprocessor with programmed instructions, with discrete analog and digital components, or any combination of these elements.

[0023] Referring now to FIG. 2, one example of how the encoding is performed is described. This is the encoding that occurs at the PDM modulation circuit 110, the results of which are sent to the DSP.

[0024] At step 202, PDM symbol values are determined. For encoded $3 \times 1\frac{1}{2}$ -bit PDM, each PDM symbol corresponds to the value:

[0025] $PDM_{symbol} \in \{-1, 0, 1\}$

[0026] in this case and requires three values in a digital representation of $1\frac{1}{2}$ -bit.

[0027] For PDM encoded $3 \times 3\frac{1}{4}$ -bit signals, each PDM symbol is in this case

[0028] $PDM_{symbol} \in \{-4, -3, -2, -1, 0, 1, 2, 3, 4\}$,

[0029] which gives total 9 different values.

[0030] At step 204, the data is encoded. For the encoded $3 \times 1\frac{1}{2}$ -bit PDM case, the data is pooled together with the $\frac{1}{2}$ -bits by grooming together $3 \times 1\frac{1}{2}$ -bits according to this function:

[0031]
$$E = \sum_{i=0}^N 2^i \cdot (PDM_{symbol}[i] + 1)$$

[0032] For the PDM encoded $3 \times 3\frac{1}{4}$ -bit signal case, the encoder becomes:

$$E = \sum_{i=0}^N 9^i \cdot (PDM_{symbol}[i] + 4)$$

[0033] In the first example, E will have three terms (for the PDM symbols with $i=0, 1, 2$) while in the second example each of the three terms represents a PDM symbol $(-4 \dots 4)$ for nine possible values. In the second example, the E value is a 10 bit value, representing three consecutive $3 \frac{1}{4}$ bit samples. This 10-bit value is inserted into the frames and transmitted using two physical data lines. In this way, data is compressed and encoded for transmission over the interface. The compression leaves room for one Frame Control (FC) bit, 432, FIG.4B and one additional spare bit, 436, FIG.4B, that is in this case set to zero. This spare bit could also be used together with the FC bit to provide additional bandwidth for the bi-directional digital control channel. Without this loss less compression, one or more additional bits would not become available and could not be used for a bi-directional digital control channel.

[0034] Referring now to FIG. 3, one example of the decoding of the encoded frames is now described. This operation is performed at the DSP (e.g., DSP 120 of FIG. 1). The DSP receives this information and converts it back to symbols and this is converted to information that can be used by the DSP.

[0035] At step 302, (X) bits (e.g., 10 bits) form the message. This is the E value (computed for example in the approach of FIG. 2) of the message in bit form.

[0036] At step 304, the system converts this value into individual terms of the summation. Reverse operation starting with $PDM_{symbol}[i = 2]$ with weight 3^2 may be used in the first example while reverse operation starting with $PDM_{symbol}[i = 2]$ with a weight of 9^2 may be used in a second example.

[0037] At step 306 and for each of these terms, associate the term with a PDM symbol from the set. For encoded $3 \times 1 \frac{1}{2}$ -bit PDM, each PDM symbol corresponds to one of the values:

[0038] $PDM_{symbol} \in \{-1, 0, 1\}$.

[0039] For PDM encoded $3 \times 3 \frac{1}{4}$ -bit signals, each PDM symbol is in this case one of:

[0040] $PDM_{symbol} \in \{-4, -3, -2, -1, 0, 1, 2, 3, 4\}$,

[0041] which has total 9 different values.

[0042] Once identified, the values can be utilized by a DSP (e.g., the DSP 120 of FIG. 1).

[0043] Referring now to FIG. 4A, one example of the framing structure is described. The frame is six bits long. The first bit 402 is a frame control bit. The remaining bits 404 are encoded 3x1 and 1/2 bit PDM as described above. It will be appreciated that the configurations of FIG. 4A, 4B, and 4C are examples only and that other examples are possible.

[0044] Referring now to FIG. 4B, another example of the framing structure is described. In this example, the frame is twelve bits long, shown in the bottom part. FIG. 4B, the framing structure uses two physical data lines DATA0 and DATA1 as shown in the figure. The first bit 432 is a frame control bit. The 10 bits 434 are encoded 3x3 and 1/4 bit PDM as described above, and the bit 436 is an unused slot bit with a logical value of zero.

[0045] Referring now to FIG. 4C, still another example of the framing structure is described. The frame is twelve bits long. The first bit 432 is a frame control bit. The 10 bits 434 are encoded 3x3 and 1/4 bit PDM as described above, and the bit 436 is an unused slot bit with a logical value of zero. The frame in FIG. 4C is transmitted at double the clock rate of the example of FIG. 4B.

[0046] Referring now to FIG. 5, one example of data clocking (physical structure) is described. A clock line 502 clocks data 504. The data may be in the frame structure of FIG. 4A, FIG. 4B, and FIG. 4C (FIG. 5 shows a small portion of the frames being transmitted).

[0047] Every time a rising or falling edge occurs one bit is transferred. There may be a single data line and a single clock in many examples. The time t_A represents the minimum time in nano seconds to assert the valid voltage potential on the data line to represent the correct binary value of the signal to transmit while the time t_Z represents the maximum time in nano seconds to remove the drive onto the data line.

[0048] The present approaches allow payload data to be in either PCM or PDM form. In one aspect, the payload data sent from the analog back end chip to the DSP is encoded and compacted in multi-bit PDM formatted information. Advantageously, compaction utilizes unused binary value encoding for each sample and requires fewer data lines between the analog back end chip and the DSP. The use of fewer data lines leaves space inside the frame that can be used to embed a digital control channel into the interface. The digital control channel may be

used concurrently to the data streaming and without affecting the data stream as such. Lower latency is also achieved, and the power needed is reduced as compared to previous approaches.

[0049] Preferred embodiments of this disclosure are described herein, including the best mode known to the inventor(s). It should be understood that the illustrated embodiments are exemplary only, and should not be taken as limiting the scope of the appended claims.

WHAT IS CLAIMED IS:

1. An acoustic data processing apparatus comprising:
an analog-to-digital (A/D) converter having an input connectable to an analog signal output of an acoustic sensor, the A/D converter having a digital data output;
a modulation circuit having an input coupled to the digital data output of A/D converter;
the modulation circuit configured to generate a data frame comprising compressed and encoded digital data, the data frame accommodating control information;
an external-device interface having one or more data lines and a clock line coupled to the modulation circuit,
the compressed and encoded data of the data frame provided on the one or more data lines of the external-device interface and a clock signal provided on the clock line,
wherein the compressed and encoded data is synchronized with the clock signal.
2. The apparatus of Claim 1, wherein the data frame includes a bit having a state indicating whether data transfer at the external-device interface is unidirectional or bidirectional.
3. The apparatus of Claim 1, wherein the compressed and encoded digital data includes $3 \times 1\frac{1}{2}$ -bit PDM symbols having three values.
4. The apparatus of Claim 1, wherein the compressed and encoded digital data includes $3 \times 3\frac{1}{4}$ -bit PDM symbols having nine values.
5. The apparatus of Claim 1,
the data frame comprises a plurality of $3 \times 1\frac{1}{2}$ -bit PDM bits and a frame control bit,
wherein the $3 \times 1\frac{1}{2}$ -bit PDM bits and the frame control bit are synchronized with the clock signal when provided on a single data line of the external-device interface.
6. The apparatus of Claim 1,
the data frame comprises a plurality of $3 \times 3\frac{1}{4}$ -bit PDM bits, a frame control bit and an undefined bit having a predetermined state,

wherein the $3 \times 3 \frac{1}{4}$ -bit PDM bits, the frame control bit, and the undefined bit having the predetermined state are synchronized with the clock signal when provided on multiple data lines of the external-device interface.

7. The apparatus of Claim 1,
the data frame comprises a plurality of $3 \times 3 \frac{1}{4}$ -bit PDM bits, a frame control bit, and an undefined bit having a predetermined state,

wherein the $3 \times 3 \frac{1}{4}$ -bit PDM bits, the frame control bit, and the undefined bit having the predetermined state are synchronized with a multiple of the clock signal when provided on a single data line of the external-device interface.

8. The apparatus of Claim 1 is an integrated circuit.

9. A method in an acoustic data processing apparatus, the method comprising:
producing digital data at the apparatus, the digital data produced from an analog signal obtained from an acoustic sensor;
compressing and encoding the digital data at the apparatus;
generating a data frame comprising compressed and encoded digital data at the apparatus, the data frame accommodating control information;
providing compressed and encoded data on one or more data lines of an external-device interface of the apparatus, the compresses and encoded data including
synchronizing the compressed and encoded data provided on the one or more data lines with a clock signal provided on a clock line of the external-device interface.

10. The method of Claim 9, indicating whether data transfer at the external-device interface is unidirectional or bidirectional by selectively setting a bit in the data frame.

11. The method of Claim 9, compressing and encoding the digital data includes encoding the digital data as $3 \times 1 \frac{1}{2}$ -bit PDM symbols having three values.

12. The method of Claim 9, compressing and encoding the digital data includes encoding the digital data as $3 \times 3 \frac{1}{4}$ -bit PDM symbols having nine values.

13. The method of Claim 9,
generating the data frame as a multi-bit frame comprising a plurality of $3 \times 1 \frac{1}{2}$ -bit PDM bits and a frame control bit,
providing the $3 \times 1 \frac{1}{2}$ -bit PDM bits and the frame control bit on a single data line of the external-device interface,
synchronizing the $3 \times 1 \frac{1}{2}$ -bit PDM bits and the frame control bit with the clock signal when providing the $3 \times 1 \frac{1}{2}$ -bit PDM bits and the frame control bit on the single data line of the external-device interface.

14. The method of Claim 9,
generating the data frame as a multi-bit frame comprising a plurality of $3 \times 3 \frac{1}{4}$ -bit PDM bits and a frame control bit,
providing the $3 \times 3 \frac{1}{4}$ -bit PDM bits and the frame control bit on multiple data lines of the external-device interface,
synchronizing the $3 \times 3 \frac{1}{4}$ -bit PDM bits and the frame control bit with the clock signal when providing the $3 \times 1 \frac{1}{2}$ -bit PDM bits and the frame control bit on the multiple data lines of the external-device interface.

15. The method of Claim 9,
generating the data frame as a multi-bit frame comprising a plurality of $3 \times 3 \frac{1}{4}$ -bit PDM bits, a frame control bit, and an undefined bit having a predetermined state,
providing the $3 \times 3 \frac{1}{4}$ -bit PDM bits, the frame control bit, and the undefined bit having the predetermined state on a single data line of the external-device interface,
synchronizing the $3 \times 3 \frac{1}{4}$ -bit PDM bits, the frame control bit, and the undefined bit having the predetermined state with a multiple of the clock signal when providing the $3 \times 1 \frac{1}{2}$ -bit PDM bits, the frame control bit, and the undefined bit having the predetermined state on the single data line of the external-device interface.

16. A microphone apparatus comprising:
an acoustic sensor having an analog signal output;
a front-end circuit including an analog-to-digital (A/D) converter having an input coupled to the analog signal output of the acoustic sensor, the front-end circuit including a modulation circuit having an input coupled to a digital data output of A/D converter, the modulation circuit configured to generate a data frame comprising compressed and encoded digital data, the data frame accommodating control information, the front-end circuit including an external-device interface having one or more data lines and a clock line coupled to the modulation circuit;
a digital back-end circuit including an external-device interface having one or more data lines and a clock line coupled to the modulation circuit, the digital back-end circuit and the front-end circuit coupled via corresponding data lines of the external-device interfaces,
wherein compressed and encoded data provided by the front-end circuit to the digital back-end circuit over the one or more data lines are synchronized with a clock signal on the clock lines.

17. The apparatus of Claim 16, wherein the data frame includes a bit having a state indicating whether data transfer at the external-device interface is unidirectional or bidirectional.

18. The apparatus of Claim 16,
the data frame comprises a plurality of $3 \times 1\frac{1}{2}$ -bit PDM bits and a frame control bit,
wherein the $3 \times 1\frac{1}{2}$ -bit PDM bits and the frame control bit are synchronized with the clock signal when provided on a single data line of the external-device interfaces.

19. The apparatus of Claim 16,
the data frame comprises a plurality of $3 \times 3\frac{1}{4}$ -bit PDM bits, a frame control bit and an undefined bit having a predetermined state,
wherein the $3 \times 3\frac{1}{4}$ -bit PDM bits, the frame control bit, and the undefined bit having the predetermined state are synchronized with the clock signal when provided on multiple data lines of the external-device interfaces.

20. The apparatus of Claim 16,

the data frame comprises a plurality of 3×3 $\frac{1}{4}$ -bit PDM bits, a frame control bit, and an undefined bit having a predetermined state,

wherein the 3×3 $\frac{1}{4}$ -bit PDM bits, the frame control bit, and the undefined bit having the predetermined state are synchronized with a multiple of the clock signal when provided on a single data line of the external-device interfaces.

21. The apparatus of Claim 1, wherein the front-end circuit is an integrated circuit and the digital back-end circuit is an integrated circuit.

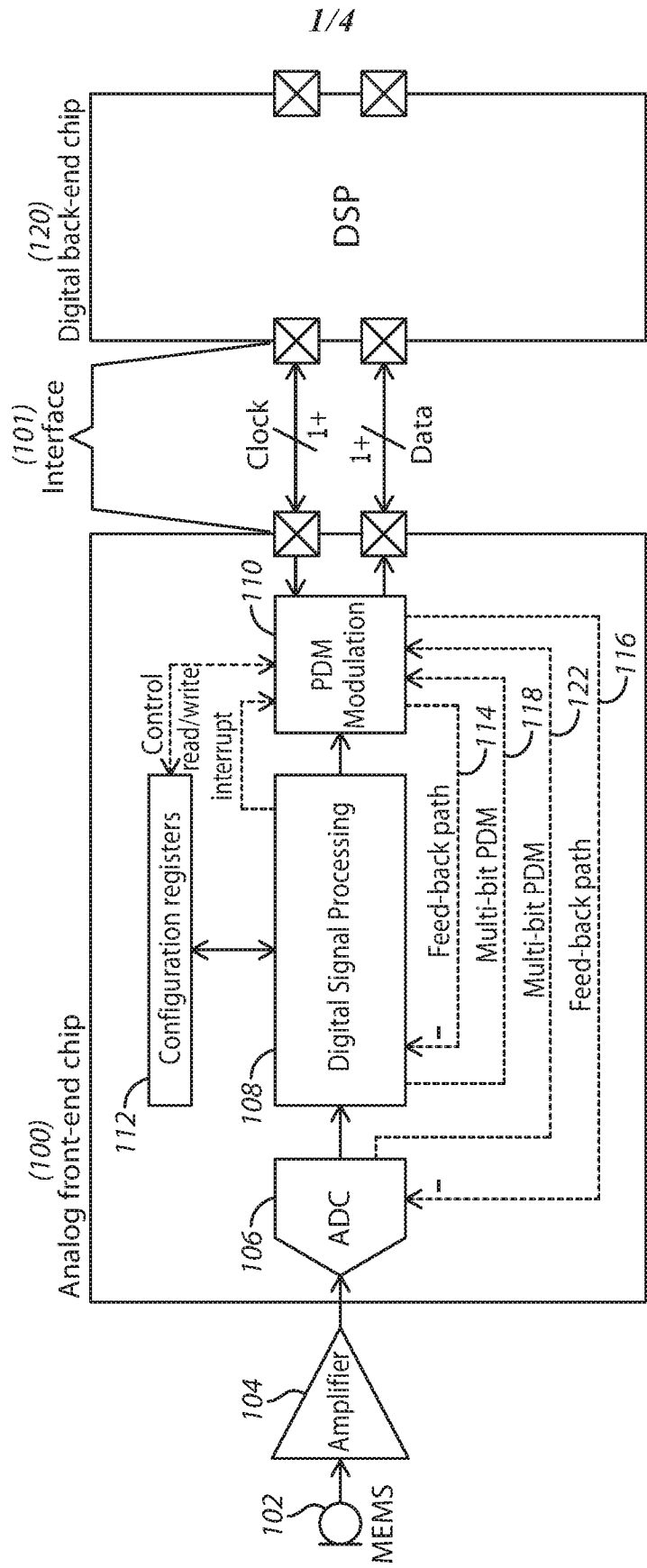
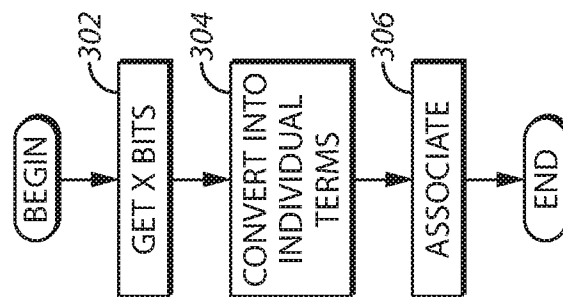
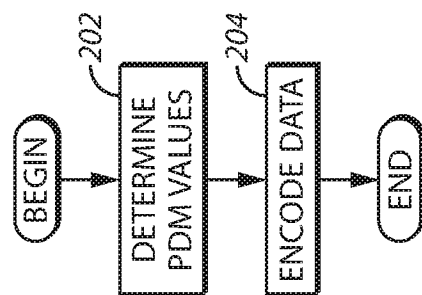


FIG. 1

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**FIG. 3****FIG. 2**

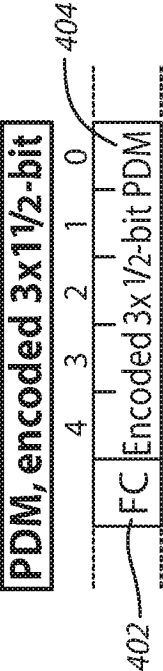


FIG. 4A

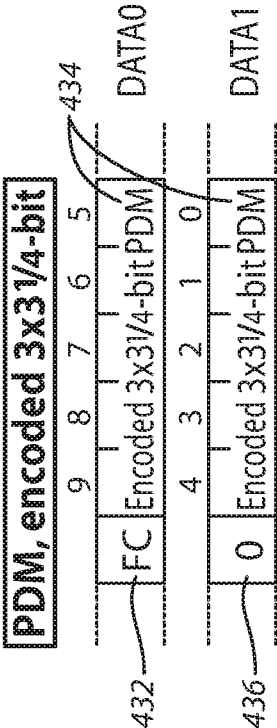


FIG. 4B

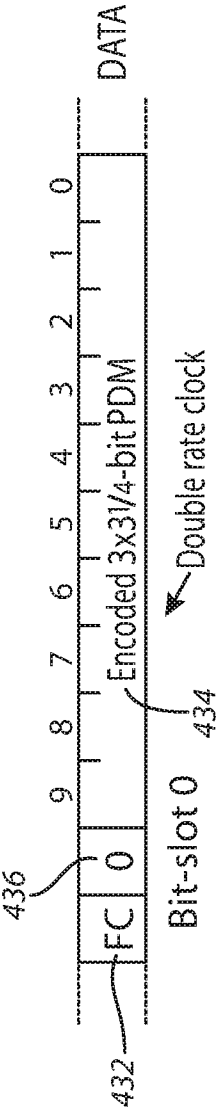


FIG. 4C

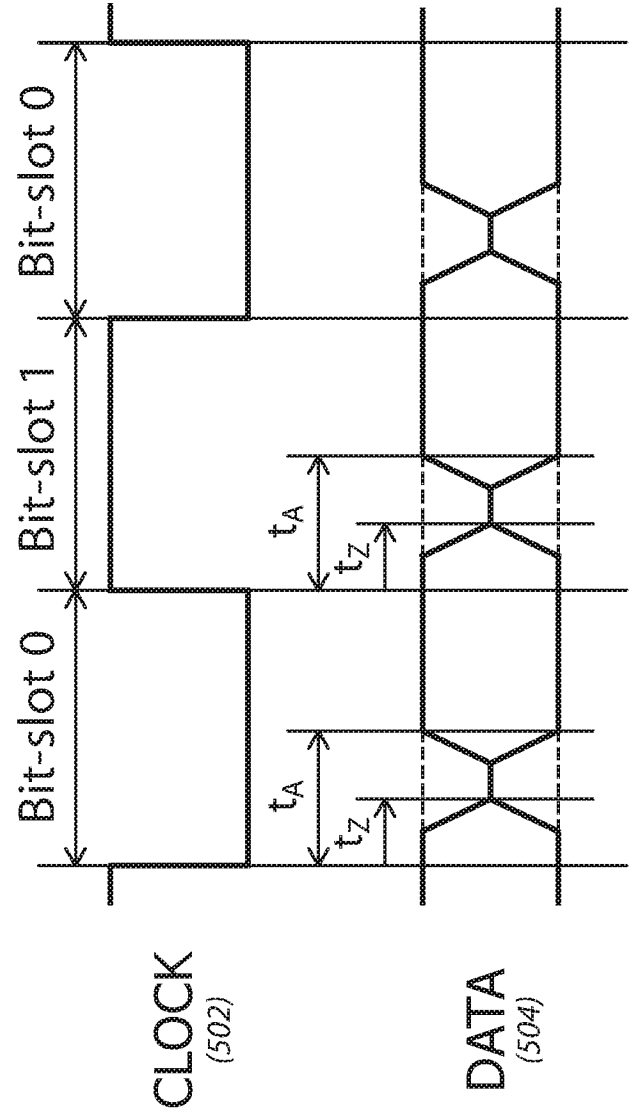


FIG. 5

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2016/030982

A. CLASSIFICATION OF SUBJECT MATTER
INV. H04R1/04 H04R19/00
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04R

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EP0-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2006/034472 A1 (BAZARJANI SEYFOLLAH [US] ET AL) 16 February 2006 (2006-02-16)	1,3-9, 11-16, 18-21
A	paragraphs [0057], [0066] - [0070]; figures 5,6	2,10,17
A	----- EP 2 608 569 A1 (ST ERICSSON SA [CH]) 26 June 2013 (2013-06-26) abstract; figure 2	1-21
A	----- US 5 051 799 A (PAUL JON D [US] ET AL) 24 September 1991 (1991-09-24) column 3, line 55 - column 6, line 60; figure 1	1-21



Further documents are listed in the continuation of Box C.



See patent family annex.

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29 June 2016

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2016/030982

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