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H03L 7/18

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H3A
Selected US specifications from IPC sub-classes H03B H03L

(54) Phase-locked loop systems

(57) A phase-locked loop system comprises a reference-frequency pulse source (22) and a controllable pulse generator (20) switchable between two frequencies one higher and one lower than the frequency of the reference pulse source (22). The controllable generator (20) includes a capacitor (26) and a switch (28) for switching the capacitor (26), into and out of circuit to effect the change in frequencies. A comparator (24) compares the output of the controllable generator with the output of the reference source (22) and switches the switch (28) in a sense to maintain the phase relationship between the two outputs substantially constant. Switching is effected at substantially the same instant during each cycle of the controllable pulse source (22) to effect a smooth transition from one frequency to the other.

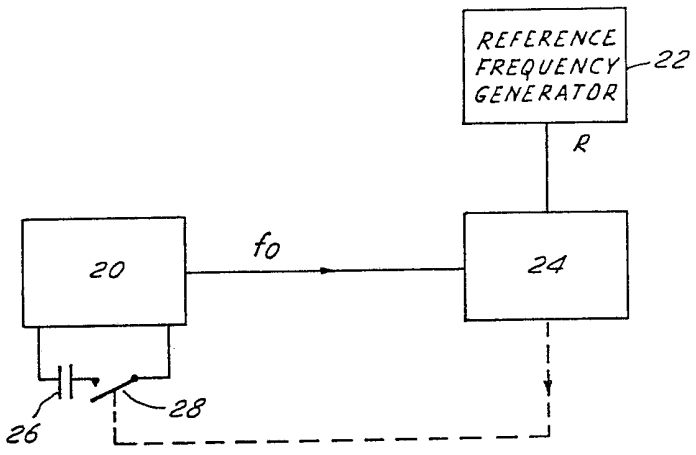

FIG.5

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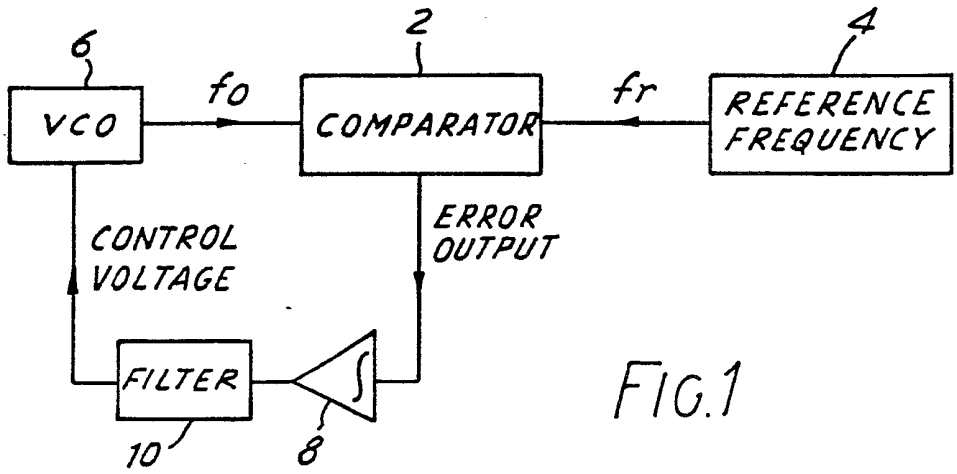

FIG.1

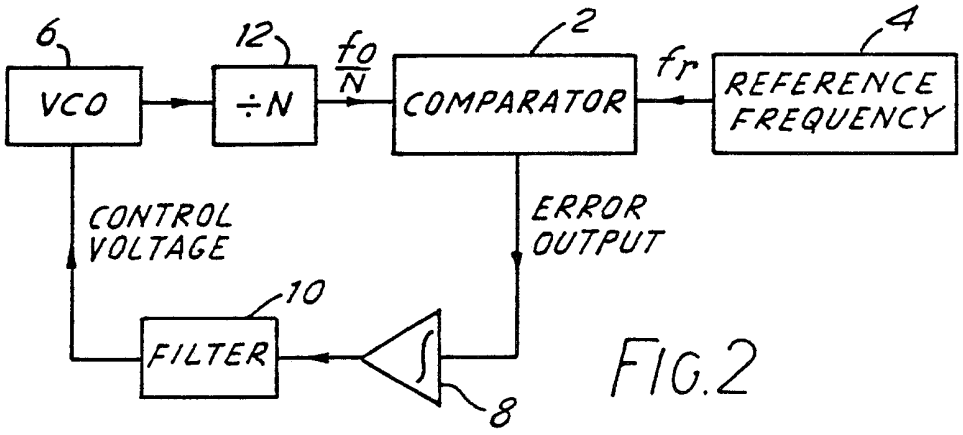

FIG.2

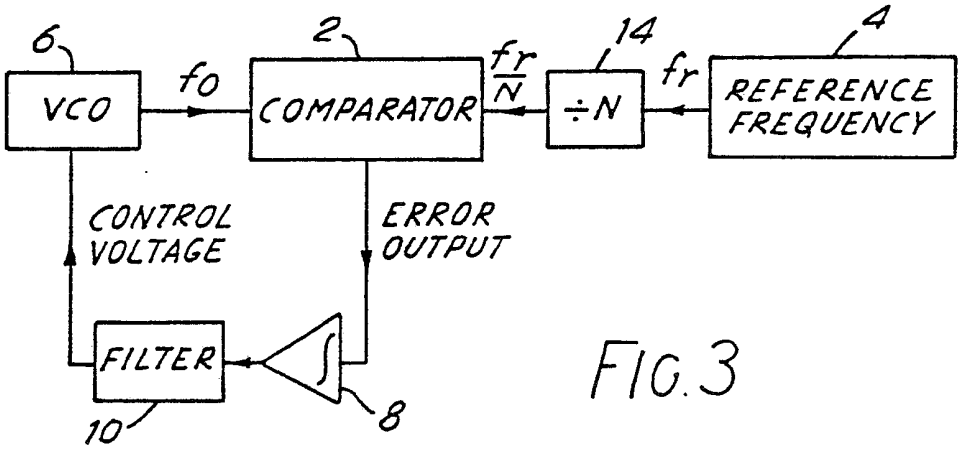

FIG.3

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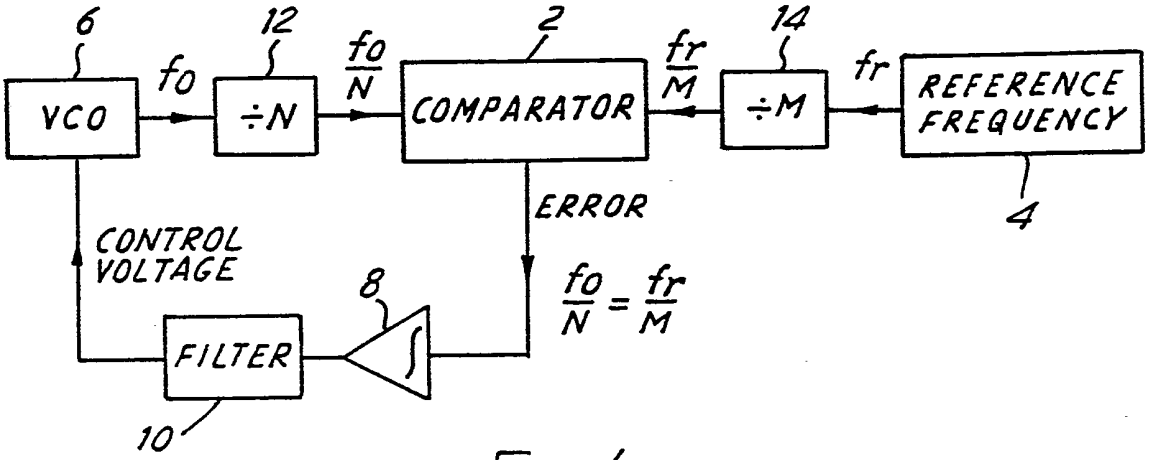


FIG. 4

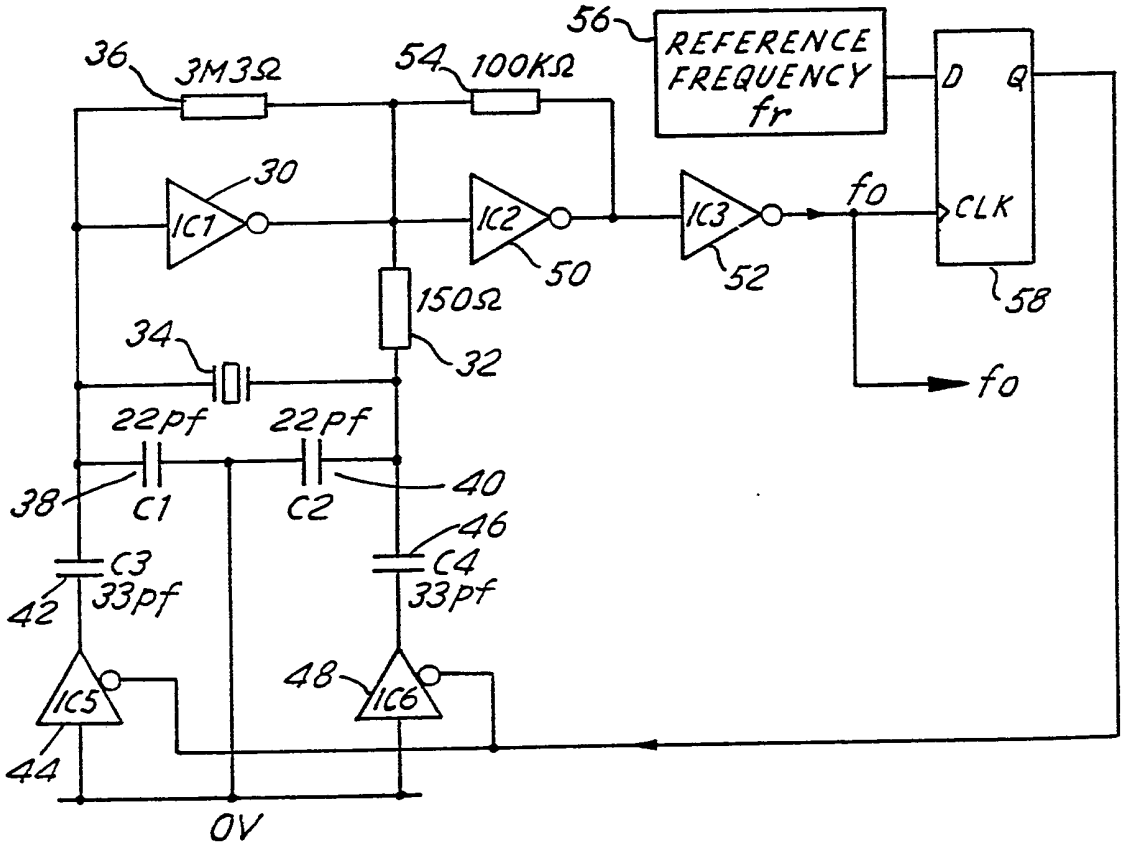


FIG. 7

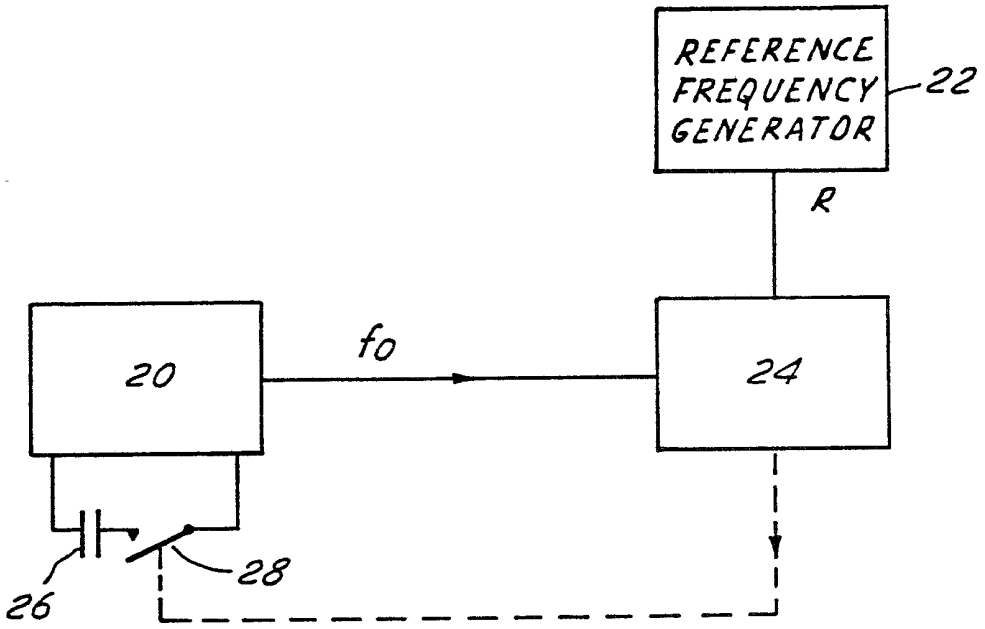

REFERENCE
FREQUENCY
GENERATOR
22
R
20
fo
24
26
28

FIG. 5

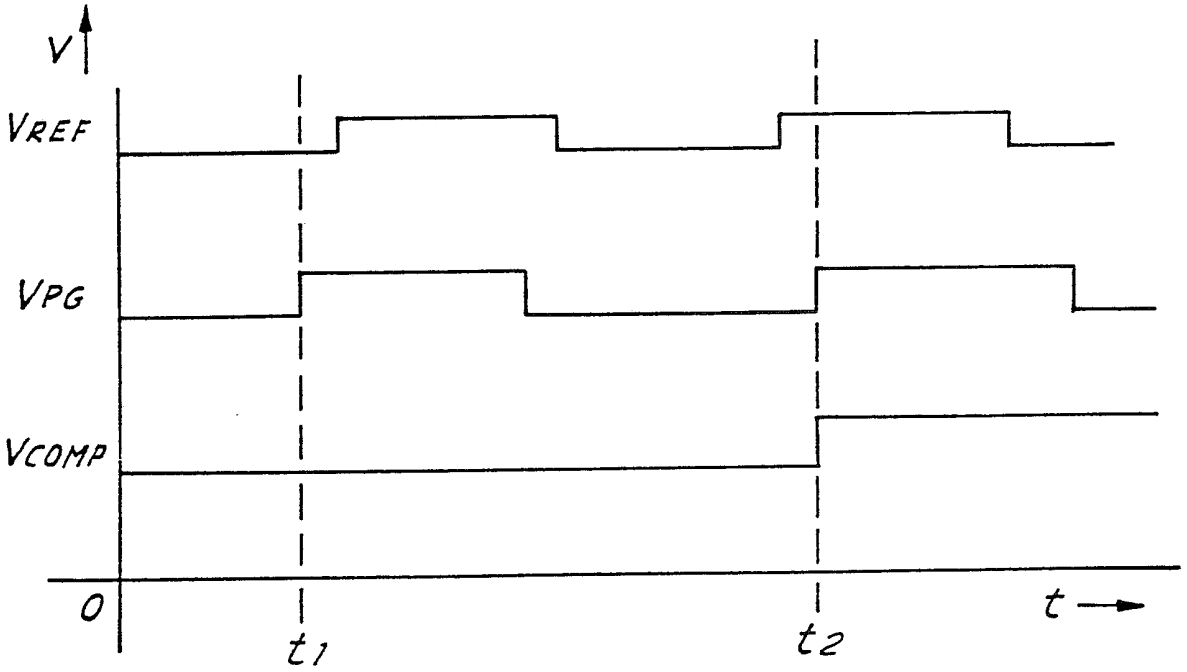
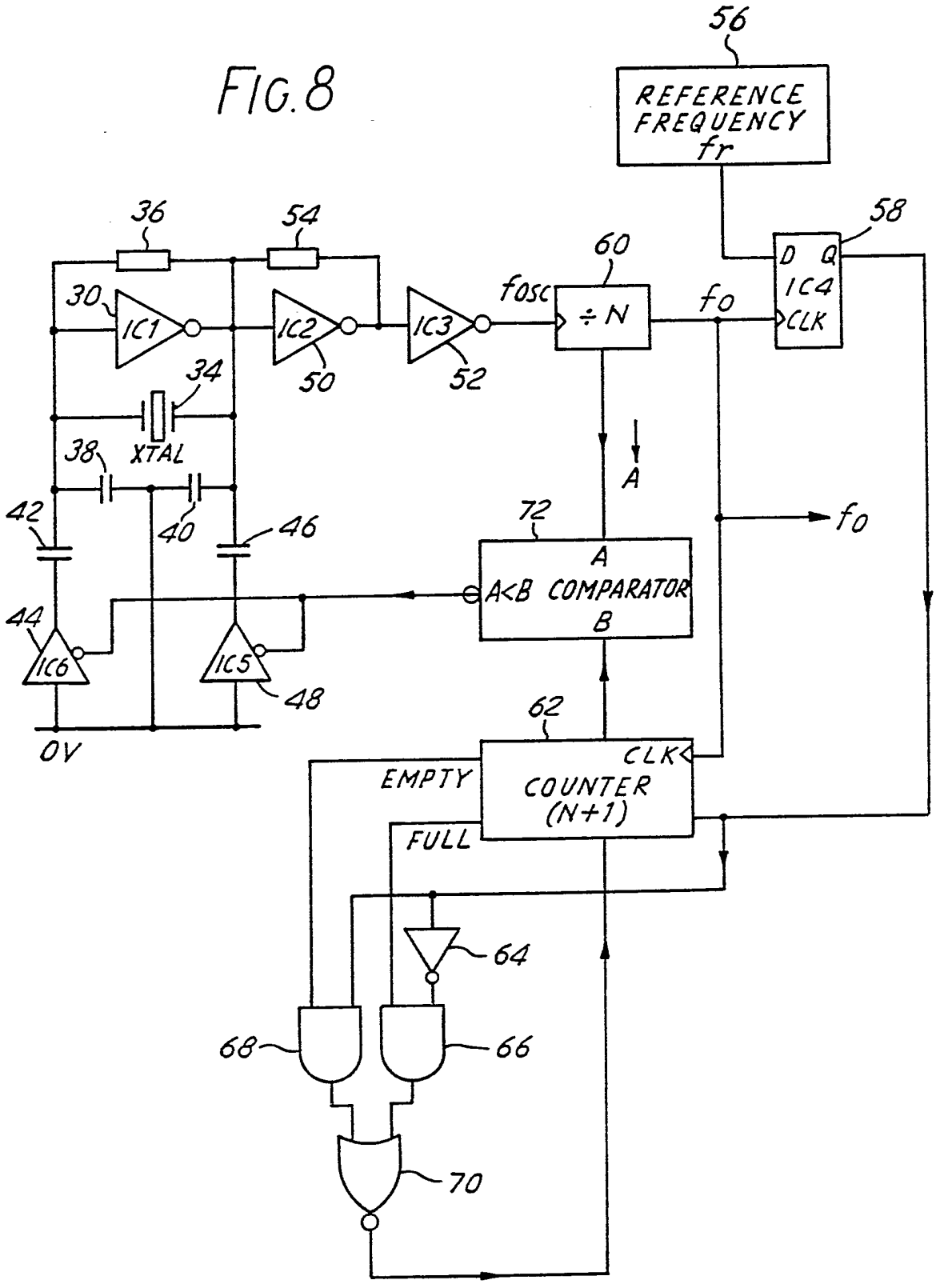

V
VREF
VPG
VCOMP
0
t1
t2
t

FIG. 6

FIG. 8


56
REFERENCE FREQUENCY fr
58
D Q
IC4
CLK
60
fosc
÷ N
fo
36
54
30
IC1
IC2
IC3
50
52
34
XTAL
38
40
42
46
44
IC6
IC5
48
0V
A
72
A
A<B COMPARATOR
B
fo
62
CLK
EMPTY
COUNTER (N+1)
FULL
64
68
66
70

PHASE-LOCKED LOOP SYSTEMS

The present invention relates to phase-locked loop systems and in particular to systems in which the output frequency of a variable frequency generator is locked to a reference frequency.

It is an object of the invention to provide an improved phase-locked loop system.

According to the present invention there is provided a phase locked-loop system comprising a reference frequency generator for generating a signal having a predetermined reference frequency, a controllable generator for producing an output signal which is switchable between first and second predetermined frequencies respectively higher and lower than the reference frequency, and a comparator for comparing the output of the reference generator with the output of the controllable generator and operable to switch the controllable generator between said first and second frequencies when the output of the controllable generator starts to or is about to lead or starts to or is about to lag behind the output of the reference generator, the switching operation taking place at substantially the same point in each cycle of the controllable generator output.

According to the present invention there is further provided a phase-locked loop system comprising a reference-pulse generator for generating a signal having a predetermined reference frequency, a controllable pulse generator having a crystal oscillator, auxiliary capacitive means and switching means for switching the auxiliary capacitive means into and out of circuit with the crystal oscillator to change the frequency generated by the oscillator between a first value which is higher than the frequency of the reference pulse generator and a

second value which is lower than the frequency of the reference pulse generator, a bistable circuit for generating an output signal which only changes at the start of each occasion that the output of the reference generator begins to lead the output of the controllable generator and the start of each occasion that the output of the controllable generator begins to lead the output of the reference generator, the output signal of the bistable circuit controlling the switching means to switch the capacitive means in and out of circuit at a timing such that the switching occurs at substantially the same point in each cycle of the controllable pulse generator output.

Phase-locked loop systems embodying the present invention will now be described, by way of example, with reference to the accompanying diagrammatic drawings, in which:

Figure 1 is a block diagram of one form of a previously proposed phase-locked loop system;

Figures 2 to 4 are block diagrams of further forms of previously proposed phase-locked loop systems;

Figure 5 is a generalised block diagram of a phase-locked loop system embodying the present invention;

Figure 6 is a waveform diagram of the system of Figure 5;

Figure 7 is a block diagram of a specific embodiment of the phase-locked loop system of Figure 6; and

Figure 8 is a block diagram of another specific embodiment of the phase-locked loop system of Figure 6.

The previously proposed phase-locked loop system shown in Figure 1 includes a comparator 2 for

comparing the output frequency fr of a reference-frequency source 4 with the output frequency fo of a voltage-controlled oscillator 6. When the two frequencies fr and fo are equal the output of the comparator 2 is zero. When there is a difference between the two frequencies the output of the comparator 2 will either have a positive or negative value dependent on the direction of the difference. The output of the comparator 2 is fed via an integrator 8 and a filter 10 to the control input of the voltage controlled oscillator 6, and is used to bring the output frequency of the oscillator 6 back into step with the frequency of the reference source.

A particular problem with this arrangement is that it is not always possible or convenient to obtain a reference frequency source having a frequency exactly equal to the required output frequency from the voltage controlled oscillator.

To cope with this problem three possible solutions are shown in Figures 2, 3 and 4. In these Figures parts similar to those in Figure 1 are similarly referenced.

When the reference frequency is lower than the required frequency, a divider 12 is introduced into the system between the voltage-controlled oscillator and the comparator 2 (see Figure 2).

When the reference frequency is lower than the required frequency a divider 14 is introduced into the system between the comparator 2 and the reference frequency source 4 (see Figure 3).

Both the solutions of Figures 2 and 3 depend upon the required frequency having an exact multiple of the reference frequency or vice versa.

Where the exact multiple relationship is

not possible a first divider 12 is introduced between the voltage controlled oscillator 6 and the comparator 2 and a second divider 14 is introduced between the comparator 2 and the reference frequency source 4 (see Figure 4). In this way by appropriately choosing the dividing factor N for the divider 12 and the dividing factor M for the divider 14 virtually any reference-frequency source can be used to control the voltage-controlled oscillator to the required frequency.

The disadvantage of this system is that the response time is relatively long and as a result the system is subject to low frequency jitter, especially when the ratio between the two frequencies in question is low.

A phase-locked loop system embodying the invention is shown in Figure 5. A controllable pulse generator 20 is provided which can be operated at two different frequencies and has a capacitor 26 which can be switched in and out of circuit by a switch 28 to change from one frequency to the other. The two frequencies are selected to lie on opposite sides of the reference frequency of a reference-pulse generator 22. A comparator 24 compares the output frequency of the controllable generator 20 with that of the reference generator 22 and switches the controllable generator 20 to its lower frequency as soon as the output frequency fo starts to exceed the reference frequency, and switches the controlled generator 20 to its higher frequency as soon as the output frequency fo starts to fall behind the reference frequency. By this switching arrangement the output frequency fo is kept in step with the reference frequency fr. In order to ensure a smooth transition in switching between higher and lower

frequencies, the switching operation is controlled to take place at the same point in each cycle. Thus, any charge built up on the capacitor 26 at the instant that the switch 28 is opened is sustained until the switch 28 is again closed at the same point in a subsequent cycle so that charging of the capacitor 26 can be resumed.

The switching operation can be more clearly seen from the waveform diagram shown in Figure 6.

Initially it will be assumed that the output frequency of the controllable generator 20 is at its lower level and that the leading edge of each pulse (see VPG) at time t1, occurs ahead of the leading edge of the reference-source pulse (see VREF). Progressively the leading edge of the reference pulses will overhaul the leading edge of the controllable pulse generator. When at time t2 the comparator 24 detects that the leading edge of pulse VPG occurs after the leading edge of pulse VREP it will generate a switching pulse VCOMP which will operate the switch 28 to change the controlled generator 20 to a higher frequency mode of operation. The switch 28 will remain switched until the leading edge of the pulses VPG creeps ahead of the leading edge of the pulses VREF at which point the switch 28 is again switched to change the controlled pulse generator 20 to its lower frequency mode of operation.

Figure 7 shows a specific embodiment of the generalised block diagram of Figure 5.

The controllable oscillator is based on unbuffered CMOS component in the form of an amplifier 30 having the series combination of a resistor 32 and a 10 MHz crystal 34 connected between the output and the input of the amplifier 30. A feedback resistor

36 is also connected across the output and input of the amplifier 30. A pair of series connected trimming capacitors 38 and 40 are connected in parallel with the crystal 34 and the junction between the capacitors 38 and 40 is connected to the 0 volts line of the system.

The series combination of a capcitor 42 and a switching (tristate buffer) amplifier 44 is connected between one terminal of the crystal 34 and the 0 volts line and the series combination of a capacitor 46 and a switching (tristate buffer) amplifier 48 is connected between the other terminal of the crystal 34 and the 0 volt line.

The output of the amplifier 30 is fed to a pair of series connected buffer amplifiers 50 and 52 which act to shape the leading and trailing edges of the pulses. A feedback resistor 54 is connected between intput and output of the amplifier 50. A reference frequency generator 56 supplies a reference frequency fr. A comparator in the form of a bistable flip-flop 58 has its clock terminal connected to the output terminal of the buffer amplifier 52 and its input terminal D connected to the reference generator 56. The output terminal Q of the flip-flop 58 is connected to the control inputs of the switching amplifiers 44 and 48.

In operation with the switching amplifiers 44 and 48 turned ON the controlled generator operates at a low frequency fl and the resultant pulses suitably shaped (squared) by the buffer amplifiers 50 and 52 are applied to clock the flip-flop 58. If the reference signal fr is at a high logic level when the controlled signal fo rises, the Q output of the flip-flop turns to a logic high and switches the switching amplifiers 44 and 48 OFF. This disconnects the

capacitors 42 and 46 from the controllable generator circuitry and as a result the output frequency rises to a high level fo. The output signal fo slips back until fr is a logical low when the flip flop 58 is clocked. This resets the output Q of the flip flop 58 to a logic low. The switching amplifiers 44 and 48 are again switched ON to bring back the capacitors 42 and 46 into the controllable generator circuit. The controllable generator now operates at a low level fl. The synchronisation between the controllable generator and the reference generator is thus maintained by constantly switching the capacitors 42 and 46 in and out of circuit as the rising edge of the reference voltage fr just follows or just precedes the rising edge of fo. This locks the positive transitions of fo to the positive transition of fr. Any jitter in fo can be reduced by making the values of fh and fl as close as possible. Thus, for example, fh may be set at 10.0005 MHz and fl set at 9.9996 MHz. This in theory would give a capture range of 900 Hz and a per clock jitter of 10 picoseconds. In practice other factors (the set up and hold time of the flip flop) would increase the per clock jitter to an order of 2 nanoseconds. Advantageously fh and fl should be set to be within 0.1 % of fr but preferably they are within 0.01 % as shown above.

By using the signal fo to trigger the clock input of the flip-flop 58 it is ensured that the capacitors 42 and 46 are switched in and out of circuit to precisely the same point in each cycle. Since during their disconnection the capacitors 42 and 43 retain substantially all of the charge, the transition of the controllable generator from one frequency fh to the other fl takes place smoothly and

without any significant disruption.

Trials were conducted with different crystals having different frequencies in the range of from 1 to 20 MHz and satisfactory performances were achieved.

It will be appreciated that as with the systems shown in Figures 2 to 4 a divider can be introduced between the buffer amplifier 52 and the flip-flop 58 and/or between the reference generator 56 and the flip-flop.

In a modification, instead of crystals, ceramic resonators can be used. With ceramic resonators the capture range tends to be increased to several kHz and consequently the jitter increased in proportion.

In the phase-locked loop system of Figure 8 parts similar to those in Figure 7 are similarly referenced. As shown a divider 60 (having a division factor N) is connected between the output of the buffer amplifer 52 and the clock input of the flip-flop 58. A counter 62 that is programmed to count from zero to N+1 has its input connected to the Q output of the flip-flop 58 and its clock input connected to receive the output signal fo from the divider 60. An AND gate 68 has one input connected to the Q output of the flip-flop 58 and its other input connected to an output of the counter 62 which indicates when the counter is empty. A second AND gate 66 has one input connected via an invertor 64 to the Q output of the flip-flop and its other input connected to an output of the counter 62 which indicates when the counter is full.

An OR gate 70 has its two inputs connected to respective outputs of the two AND gates 68 and 66. This output of the OR gate 70 is connected to an

inhibit input for the counter 62 to inhibit the count of the counter 62.

A comparator 72 is connected to compare the contents A of the divider 60 with the contents B of the counter 62. When A B the comparator 72 generates a signal to switch the two switching amplifiers 44 and 48 ON.

The counter 62 is controlled so that it will never overflow or underflow. If the counter 62 is full and the up mode is selected when the clock pulse occurs, the AND gate 66 will open to pass a signal through the OR gate 70 to the inhibit input of the counter 62 and accordingly the counter will remain full. If the counter 62 is empty and the down mode is selected, the AND gate 68 will open to pass a signal through the OR gate 70 to the inhibit input of the counter 62 and accordingly the counter will remain empty.

In operation the divider 60 which is in the form of a counter counts from an empty condition and proceeds sequentially to a full condition at which point it is reset to zero again.

The counter 62 operates so that when phase lock is achieved it will have a count of say M. This value will change to M+1 or M-1 on the next clock signal and back to M again on the following clock.

The comparator 72 compares the instantaneous count A of the divider 60 with the instantaneous count B of the counter 62. As soon as the contents of the divider 60 and counter 62 are equal or the contents of the divider 60 exceeds the contents of the counter 62, the comparator 72 will switch the two switching amplifiers 44 and 48 ON to change the frequency of the controlled generator from fl to fh.

It will be appreciated that with this mode of control there are M low frequency cycles and N-M high frequency cycles out of each succession of N cycles.

To analyse the position more clearly the generator operates in a mode to satisfy the following equation.

$$Po = NxPh + MxD \quad .... \quad (1)$$

where Po is the period of the divider counter cycle; Ph is the period of the generator when operating at high frequency fh; and D is the difference between the periods of the generator when operating at high frequency fh and at low frequency fl.

For any two consecutive divider cycles the value in the up/down counter 62 can only change by 1 (i.e. from M to M+1 or from M to M-1). Let it be assumed that the new value of the counter is (M+1). This means that there will now be M+1 low frequency cycles for every divider cycle. Therefore

$$Po' = NxPh + D(M+1) \quad .... \quad (2)$$

From equations 1 and 2 it will be immediately apparent that the difference between the two divider periods Po - Po' = D.

Therefore, for any given divider counter cycle, only one generator clock cycle out of N will change from low to high frequency if the up/down counter is incremented. This means that the period difference between any two consecutive divider counter cycles is the same as the difference of the periods between the low and the high frequency generator frequencies.

The percentage jitter over two consecutive divider counter cycles is thus reduced by a factor N.

The performance of the circuit can be

further improved by interleaving the high and low frequency generator clock cycles, rather than grouping them either at the beginning or at the end of each divider counter cycle. This helps maintain a uniform charge on capacitors C3 and C4 as these are then switched more frequently in and out of circuit.

If phase lock is achieved when the up/down counter is empty, the generator is operating at its high frequency. If lock is achieved when the up/down counter is full, then the generator is operating at its low frequency. These two limits define the capture range of the phase-locked loop. Therefore the jitter remains constant for any divider counter value.

It will be appreciated that the systems described can be implemented using any mix of analog or digital techniques.

It will also be appreciated that all the components except the crystal and other major capacitive components can be embodied in a single semi-custom chip, making manufacture of the system particularly simple and cheap.

Furthermore the need for voltage controlled oscillators, filters and integrators (all expensive sub-assemblies) as used in the previously proposed systems is avoided.

If the system is implemented as a discrete circuit, the layout of the components is not critical since any external influences (e.g. interference) will have little or no effect on the operation of the system. The switching capacitors are either switched into or out of circuit and any external electric field influences on the charge of the capacitor when in circuit are unlikely to affect the operation of the system in any significant manner.

CLAIMS

1. A phase-locked loop system comprising a reference-frequency generator for generating a signal having a predetermined reference-frequency, a controllable generator for producing an output signal which is switchable between first and second predetermined frequencies, respectively higher and lower than the reference frequency, and a comparator for comparing the output of the reference generator with the output of the controllable generator, and operable to switch the controllable generator between said first and second frequencies when the output of the controllable generator starts to or is about to lead, or starts to or is about to lag behind the output of the reference generator.

2. A system according to Claim 1 wherein the switching operation is controlled to take place at substantially the same point in each cycle of the controllable generator output.

3. A system according to Claim 1 or to Claim 2 wherein the said first and second predetermined frequencies are within the range of $\pm$ 0.1 % of the said reference frequency.

4. A system according to Claim 1 or to Claim 2 wherein said first and second predetermined reference frequencies are within the range of $\pm$ 0.01 % of the said reference frequency.

5. A system according to any one of Claims 2 to 4 wherein said controllable generator comprises an RC oscillating circuit, an auxiliary capacitor, and switch means for switching the auxiliary capacitor in and out of the RC circuit in response to the output of the comparator.

6. A phase locked loop system comprising a reference pulse generator for generating a signal

having a predetermined reference frequency, a controllable pulse generator having a crystal oscillator, auxiliary capacitive means and switching means for switching the auxiliary capacitive means into and out of circuit with the crystal oscillator to change the frequency generated by the oscillator between a first value which is higher than the frequency of the reference-pulse generator and a second value which is lower than the frequency of the reference pulse generator, a bistable circuit for generating an output signal which only changes at the start of each occasion that the output of the reference generator begins to lead the output of the controllable generator and the start of each occasion that the output of the controllable generator begins to lead the output of the reference generator, the output signal of the bistable circuit controlling the switching means to switch the capacitive means in and out of circuit at a timing such that the switching occurs at substantially the same point in each cycle of the controllable pulse generator output.

7. A system according to Claim 6 wherein the crystal oscillator comprises an amplifier, the series combination of a crystal and resistor connecting the output of the amplifier to the input, and a pair of series-connected trimming capacitors connected in parallel with the crystal, the auxiliary capacitive means and switching means comprising the series combination of a first capacitor and a first switchable amplifier connected in parallel with one said trimming capacitor and the series combination of a second capacitor and a second switching amplifier connected in parallel with the other trimming capacitor.

8. A system according to Claim 6 or to Claim 7

wherein the controllable pulse generator includes shaping means for shaping the output of the crystal oscillator.

9. A system according to any one of Claims 6 to 8 including a frequency divider for dividing the output of the controllable oscillator by a factor N before supplying it to the bistable circuit, an N+1 up/down counter connected to count the output of the bistable circuit, means for inhibiting the counter from counting up when full and down when empty, and a comparator for comparing instantaneous count of the up/down counter with the instantaneous count of the divider, and causing the switching means to switch when the count of one of said divider and counter reaches or exceeds the count of the other of said divider or counter.

10. A system according to any preceding claim wherein all the components of the system except for the capacitive components are embodied in a single chip.

11. A phase-locked loop system substantially as hereinbefore described with reference to any one of Figures 5 to 8.

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