

[54] ELECTRONIC MUSICAL INSTRUMENT
EMPLOYING WAVESHAPE MEMORIES

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84/1.13; 84/1.19; 84/1.25; 84/1.26; 84/1.27
[51] Int. Cl. G10h 1/02; G10h 5/02
[58] Field of Search 84/1.01, 1.03, 1.09-1.11,
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Goldsmith & Deschamps

[57] ABSTRACT

In an electronic musical instrument, actuation of each key switch produces a key data signal indicative of the identification name of the key switch. A key address code corresponding to this key data signal is stored in a key address code memory. Frequency data corresponding to the fundamental frequencies of musical tones for the respective key switches are stored beforehand in a frequency information memory. The key address code read from the key address code memory is used to read frequency information corresponding to the key address code from the frequency information memory. The frequency information is thereafter counted cumulatively in a counter to produce a wave-shape address code successively changing with time. Musical tone waveshape memories are provided for storing waveshapes in time-sampled analog representation. The sampled analog values are successively read out in accordance with the changing waveform address code thereby constructing the waveform. Envelope shapes of the musical tones are stored in time-sampled analog representation in envelope memories. Control signals representing depression and release of a key are produced from the key data signal which is produced by the depression and release of the key. A suitable clock pulse is selected by these control signals to read out the envelope shapes. The read out outputs of the envelope memories are applied to the voltage control terminals of the musical tone waveshape memories to determine the instantaneous amplitude thereby causing the musical tone waveshape memories to produce musical tone waveshapes with desired envelopes. In order to enable a simultaneous reproduction of a plurality of musical tones, the instrument is constructed as a dynamic logic system wherein logical circuits as well as the memories and the counters are used in a time sharing manner.

25 Claims, 53 Drawing Figures

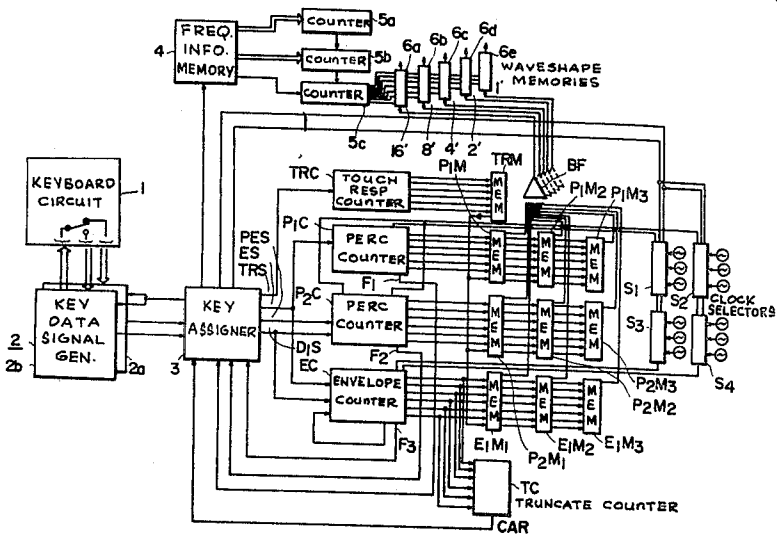


FIG. 2

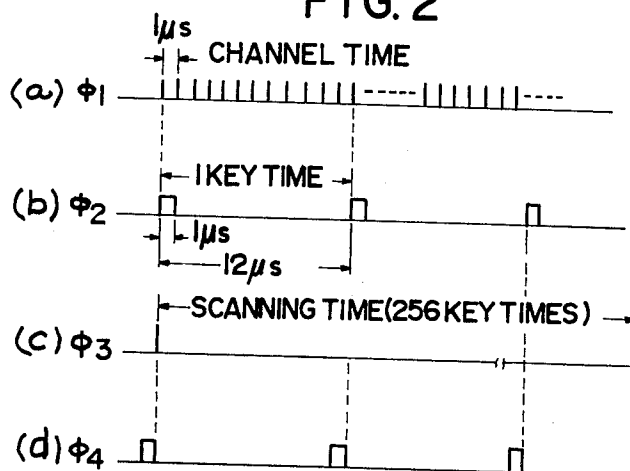


FIG. 6A

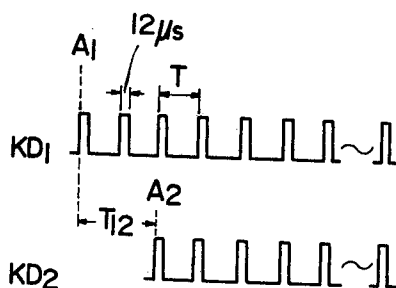


FIG. 6B

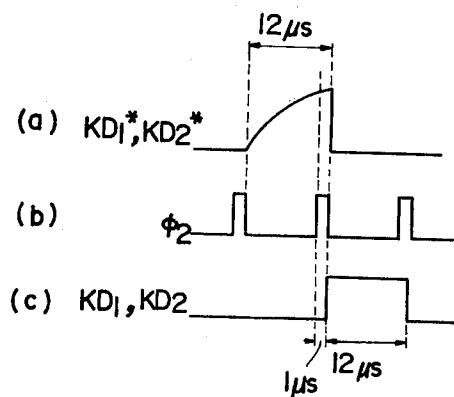


FIG. 3

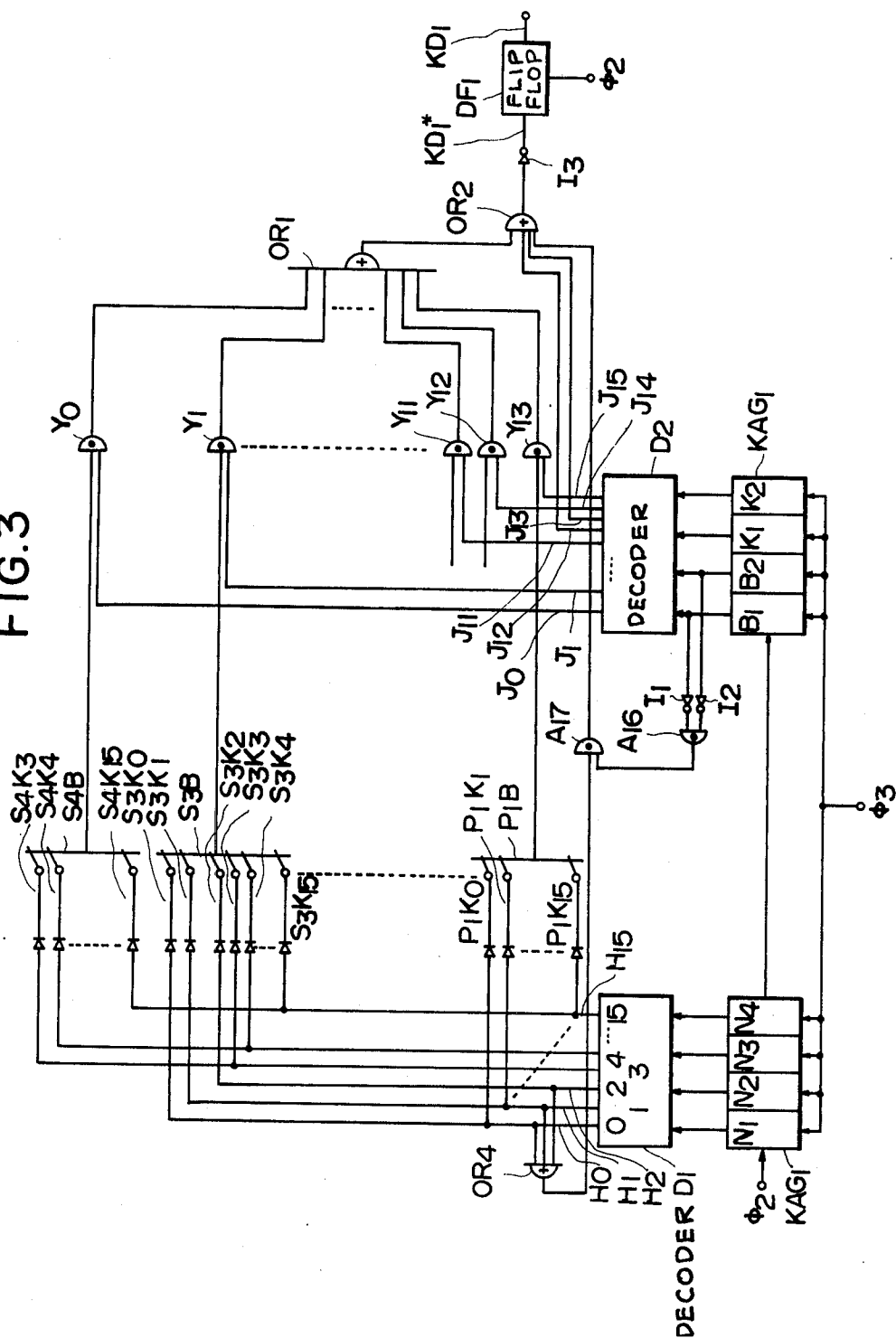


FIG. 4

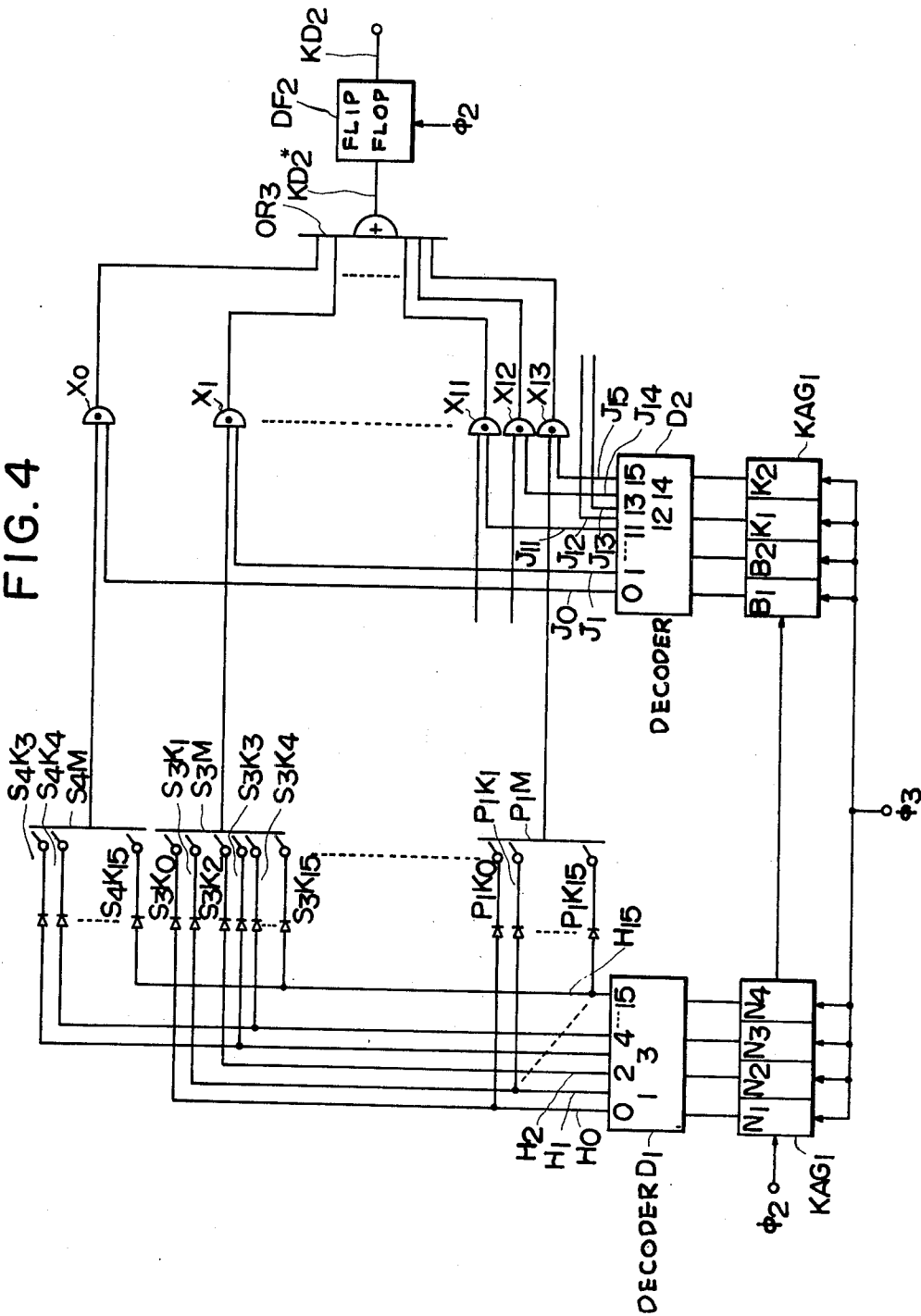
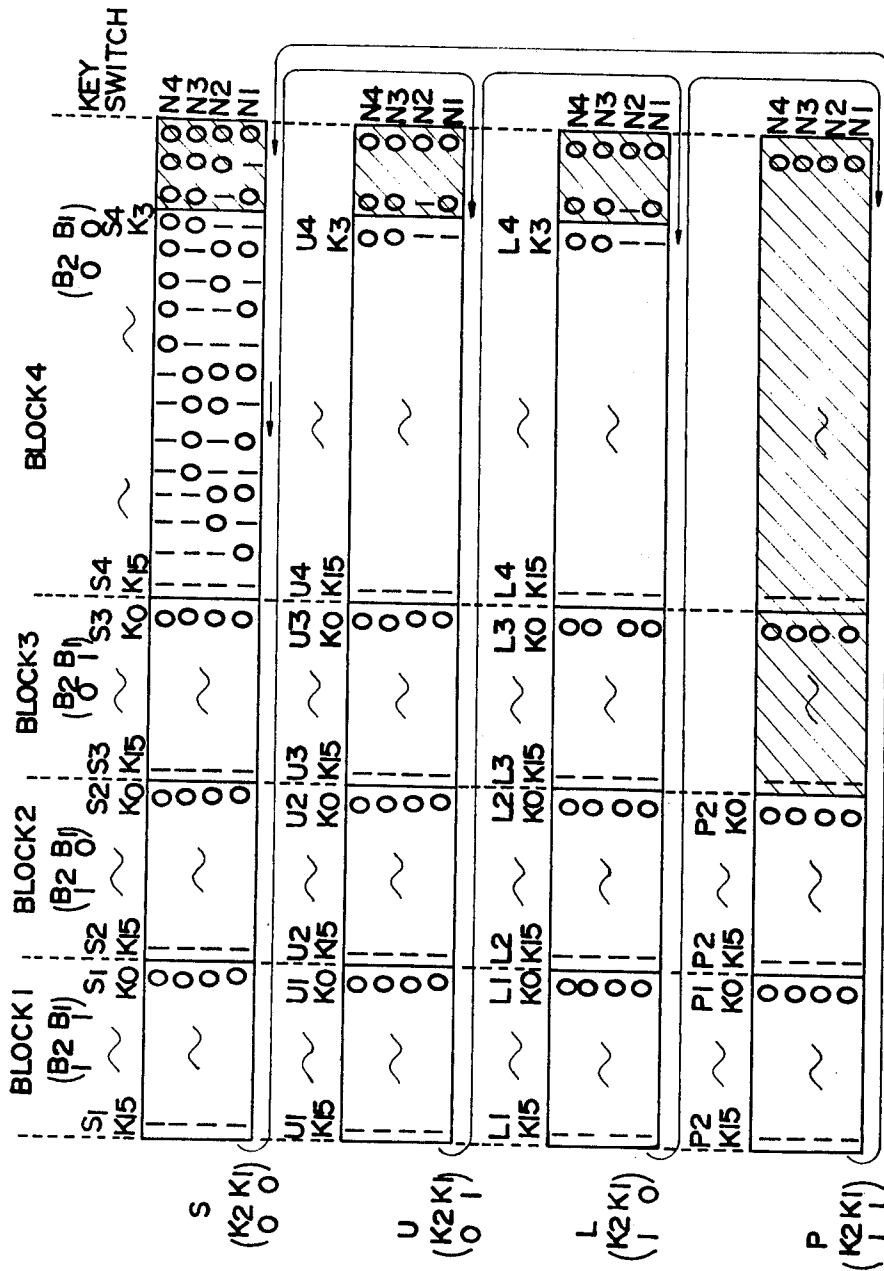


FIG. 5



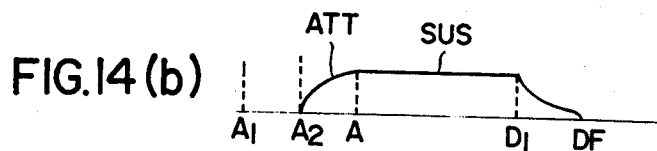
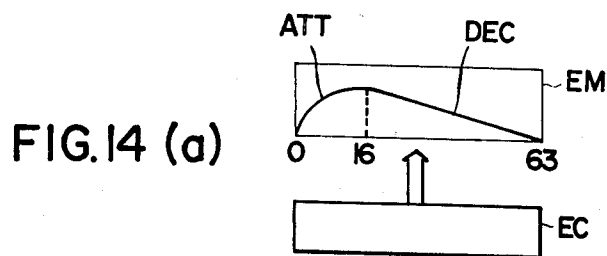
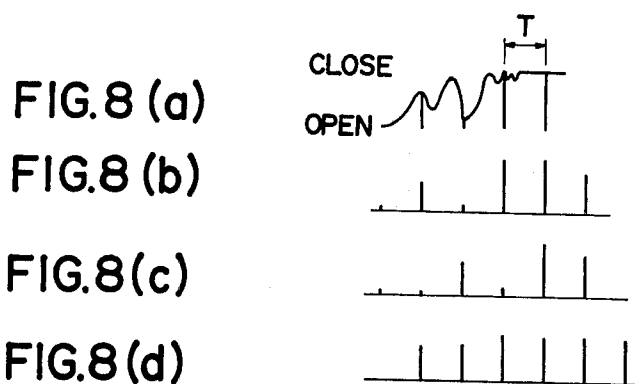
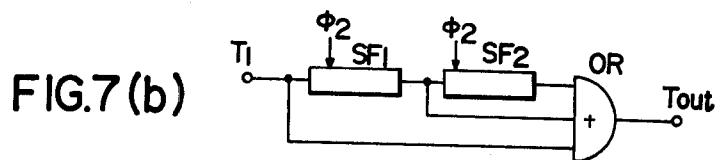
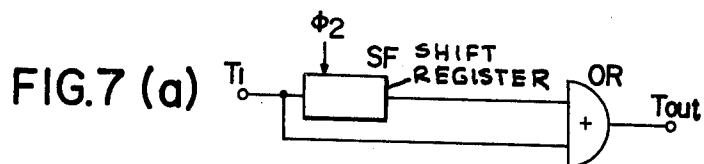


FIG. 9

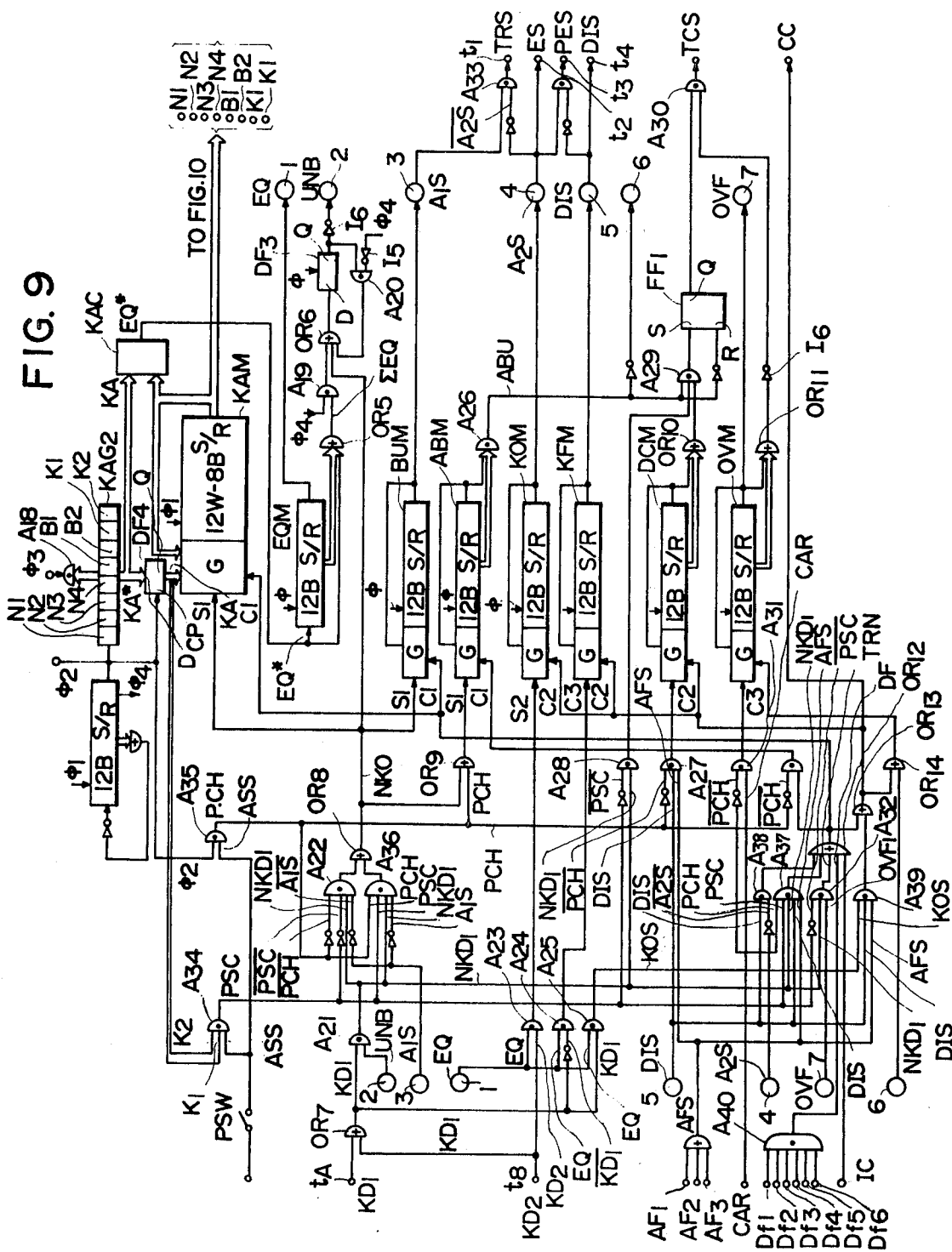
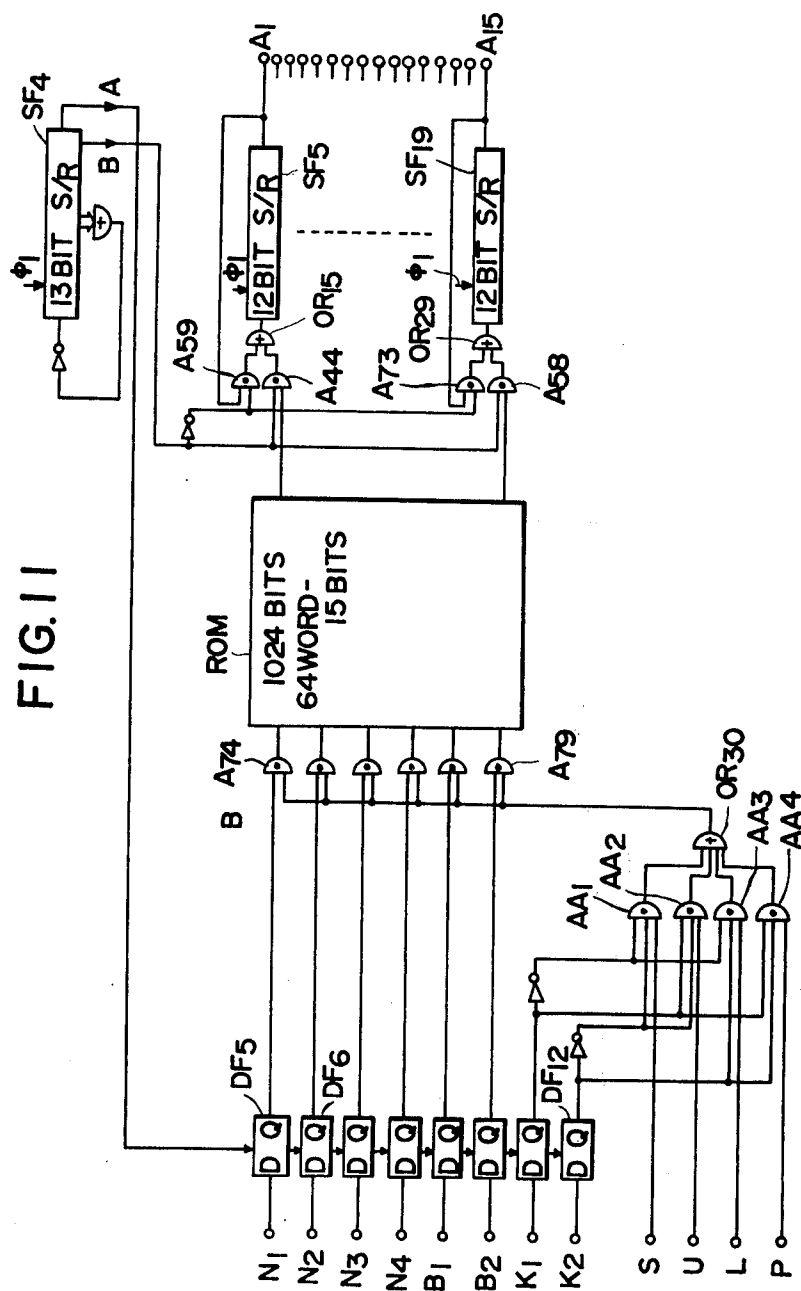


FIG. 11



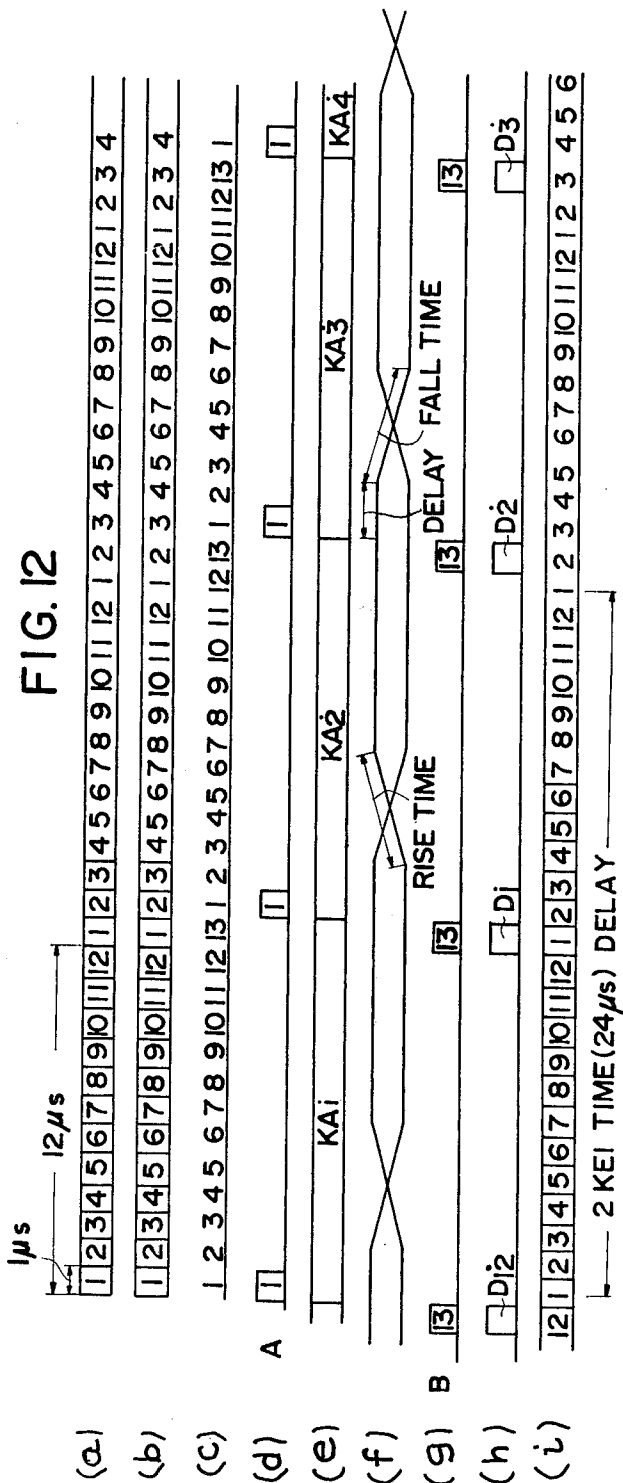


FIG. 13

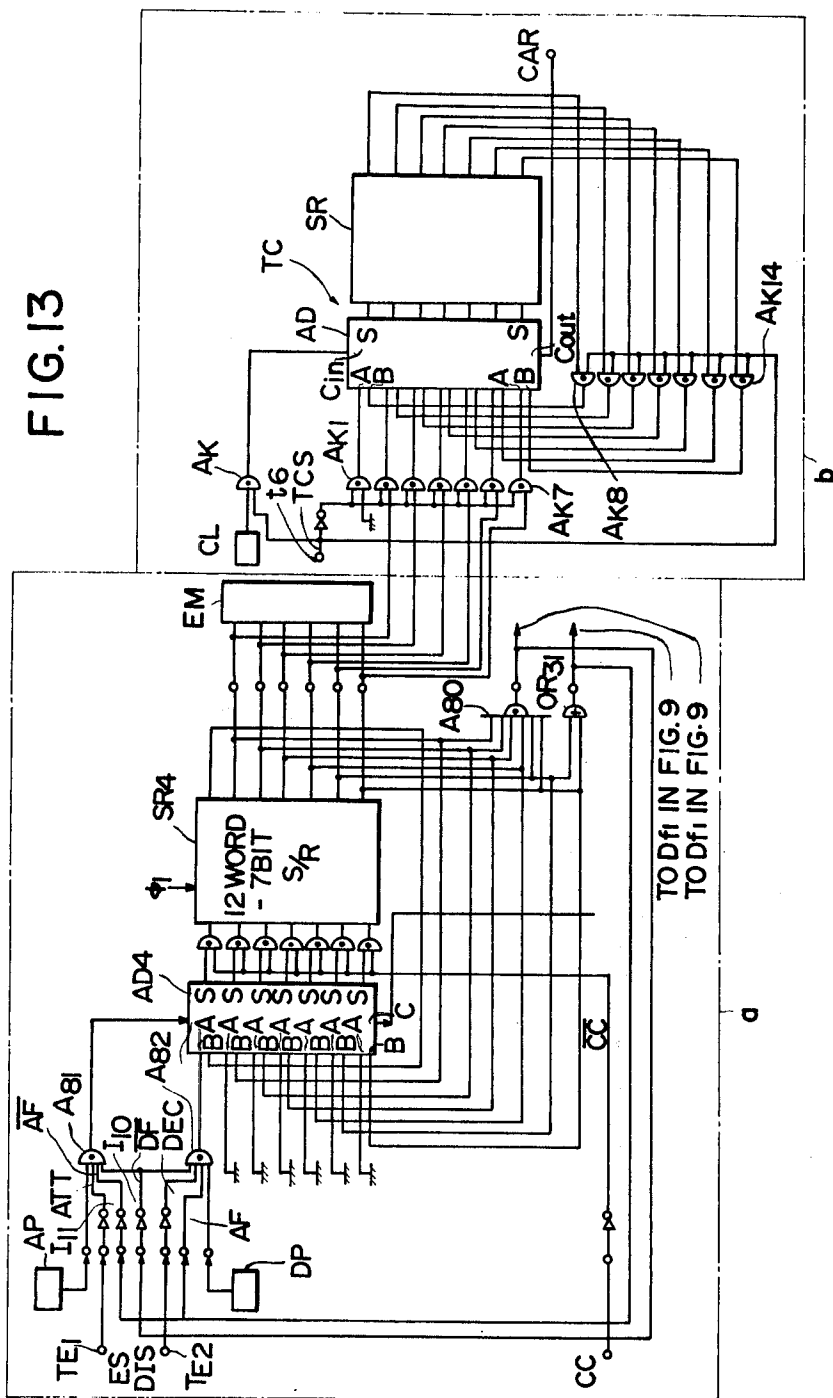
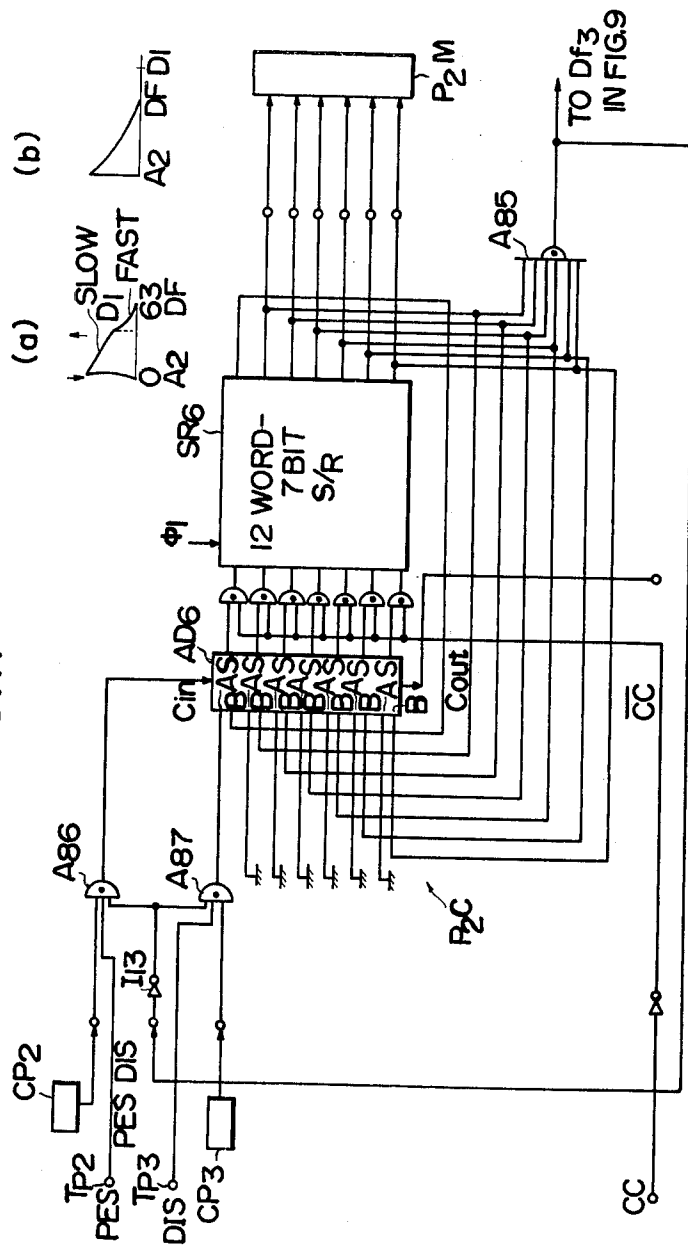


FIG. 17

FIG. 18



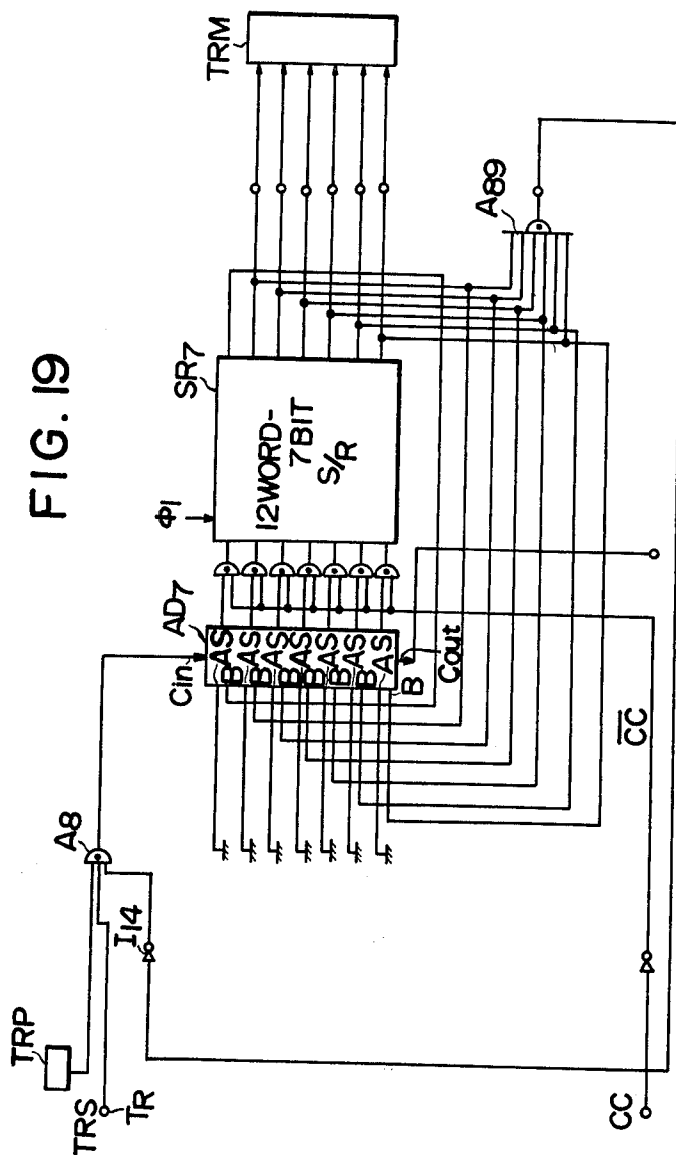


FIG.20

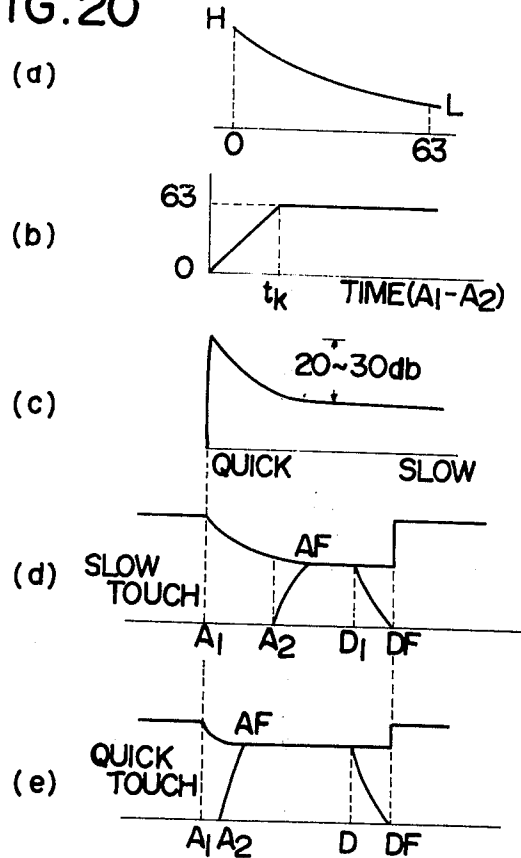


FIG.21

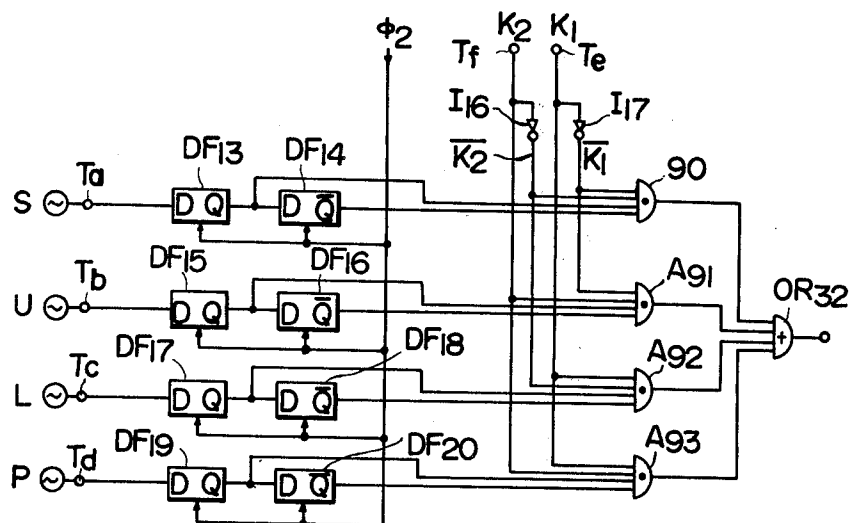


FIG. 22

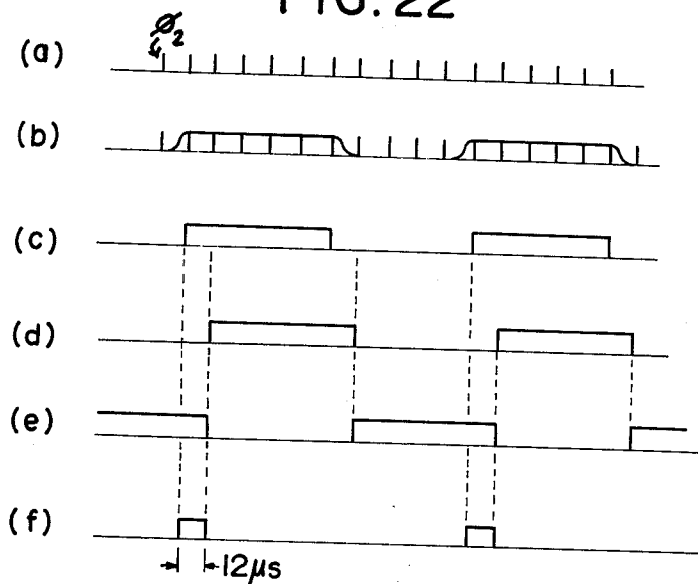


FIG. 23

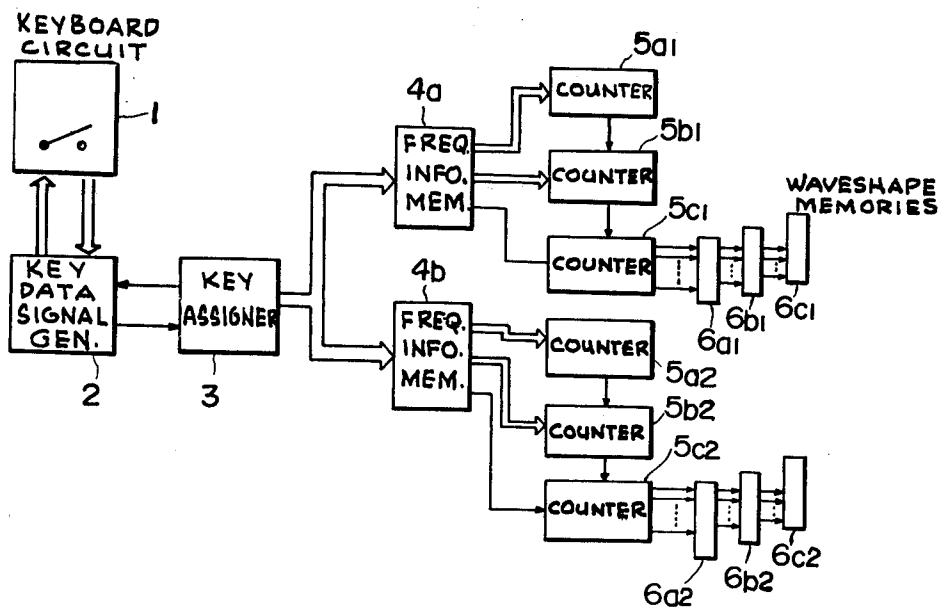


FIG. 24

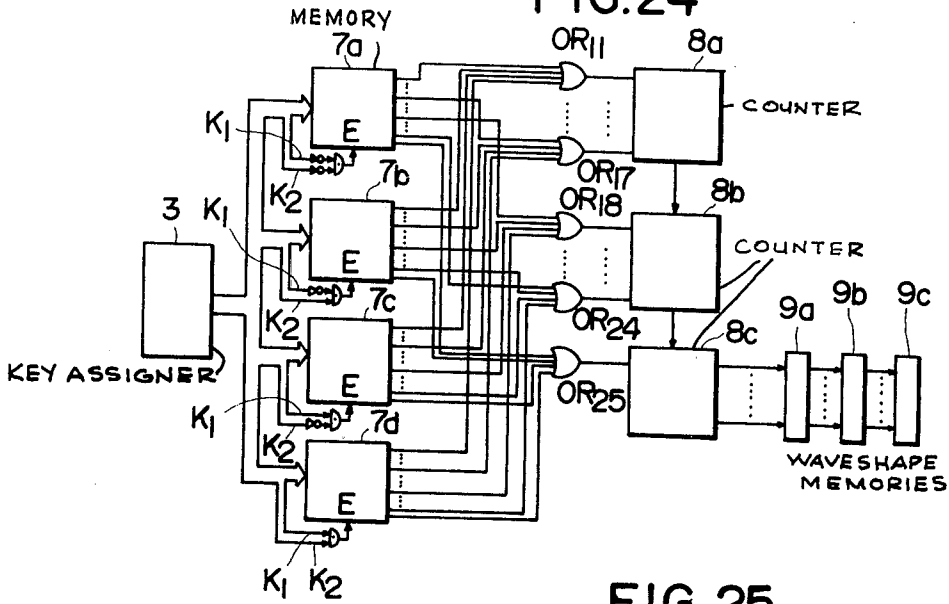


FIG. 25

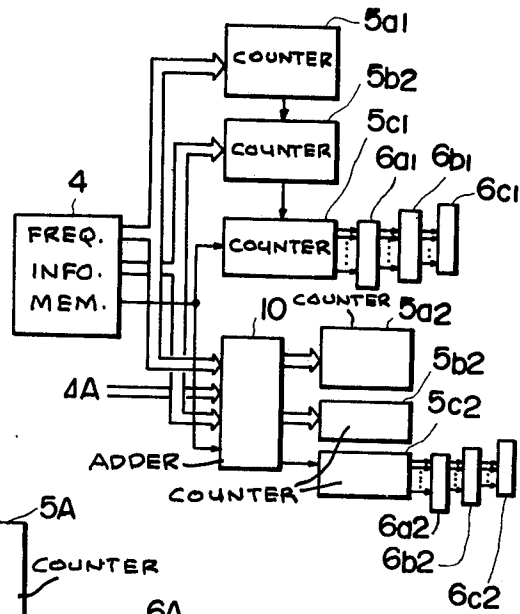
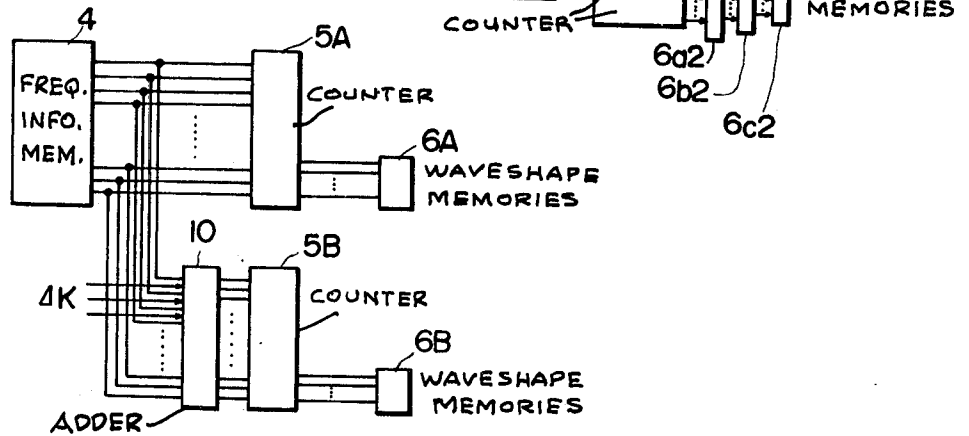


FIG. 26



ELECTRONIC MUSICAL INSTRUMENT EMPLOYING WAVESHAPE MEMORIES

BACKGROUND OF THE INVENTION

This invention relates to an electronic musical instrument and, more particularly, to an electronic musical instrument capable of simultaneously producing a plurality of musical tones respectively having predetermined envelopes. The electronic musical instrument according to the invention comprises memories which store musical tone waveshapes in time-sampled analog representation and memories which store, also in time-sampled analog representation, envelope signals for the respective musical tones and is adapted to process key data signals corresponding in time relation to the notes of depressed keys and key address codes representing the notes of the depressed keys by utilizing a principle of dynamic logic for reading the waveshapes from these memories.

Electronic musical instruments of conventional types employ a plurality of oscillators or frequency dividers for providing sound source signals from their outputs. These sound source signals are supplied to a tone-color circuit through key switches by closing thereof, whereupon desired musical tone signals are obtained. The prior art electronic musical instruments therefore require a large number of oscillators or frequency dividers. Besides, the tone-color circuit has an extremely complicated construction. As a result, the musical instrument generally has a complicated and large system for producing required musical tone signals.

Moreover, it was impossible in the prior art electronic musical instruments to obtain musical tone signals having the same wave shapes as those of natural musical instruments. The musical tones reproduced from the prior art electronic musical instruments therefore only resembled natural musical tones to a degree which was far from being satisfactory.

The prior art electronic musical instruments require a plurality of musical tone signal production systems which make their construction further complicated and large.

Again, in the prior art electronic musical instruments, an envelope of a musical tone signal which determines the shape of the rise portion of the musical tone when a selected key is depressed, the sustain portion of the tone and the fall portion of the tone after the key has been released, is provided by a switching circuit utilizing charging and discharging characteristics of a capacitor.

Thus, a musical tone signal having a predetermined envelope has been obtained from the output terminal of the switching circuit by applying thereto a signal having a predetermined amplitude and operating a switch provided in the charging and discharging circuit in response to the operation of a key switch.

However, the above described instrument which utilizes charging and discharging characteristics of a capacitor for obtaining a musical tone signal is incapable of producing a complicated envelope of a natural musical tone which, for example, rises abruptly, then falls somewhat rapidly to a certain level and maintains this level for a certain length of time and falls gradually thereafter. The envelope characteristic of the musical tone signal obtained by the above described prior art instrument is at best a rough simulation of that of a natural musical tone. Further, the prior art system is inca-

pable of changing at will the duration of the rise portion of the envelope which is formed immediately after depression of a key (hereinafter referred to as "attack") and that of the fall portion which is formed after releasing of the key (hereinafter referred to as "decay").

SUMMARY OF THE INVENTION

The electronic musical instrument constructed according to this invention uses a principle which is entirely different from the one used in the above described prior art electronic musical instrument. According to the invention, a key data signal is produced upon depression of a key. A key address code corresponding to this key data signal is stored in key address code memories provided with a plurality of channels and a musical tone waveshape is read out at a frequency corresponding to the stored key address code. Simultaneously, control signals respectively representing depression and release of the key are produced from the key data signals produced by the depression and the release of the key, and the reading of the envelope memory is controlled by these control signals. A plurality of musical tones respectively having predetermined envelopes can be simultaneously produced by multiplying the envelope shape outputs with the musical tone waveshape outputs. In order to enable the inventive electronic musical instrument to reproduce a plurality of musical tones simultaneously, the instrument is constructed as a dynamic logical circuits system wherein the logics, the counters, the memories etc. are used in a time-sharing manner.

It is an object of this invention to provide an electronic musical instrument of a remarkably simplified circuit construction capable of simultaneously producing a plurality of musical tone signals having accurate waveshapes and envelopes.

It is another object of the invention to provide an electronic musical instrument capable of simultaneously reproducing a plurality of musical tone waveshapes by constructing the counters, logical circuits and memories according to a dynamic logic principle so that these counters etc. may be used in a time-sharing manner.

It is another object of the invention to provide an electronic musical instrument capable of controlling the entire level of a musical tone in response to the speed of depressing the note identification key for that tone.

It is another object of the invention to provide an electronic musical instrument capable of minimizing wiring required for connecting various units which produce musical tones by virtue of utilization of key data signals representing respective keys in time sequence together with key switches.

It is another object of the invention to provide an electronic musical instrument which successfully eliminates adverse effects of chattering of the key switches.

It is another object of the invention to provide an electronic musical instrument capable of accurately producing a plurality of musical tones corresponding to depressed keys up to a maximum number of tones to be reproduced simultaneously.

It is another object of the invention to provide an electronic musical instrument capable of producing a single pedal tone alone regardless of the number of tones to be reproduced simultaneously by operation of the keys of the manual keyboards.

It is another object of the invention to provide an electronic musical instrument in which frequency information representing the notes of the respective keys is stored beforehand in a storage device, frequency information corresponding to the depressed key is read out, and a musical tone waveshape memory is sampled by a waveshape address code signal which is a cumulative counting output obtained by cumulatively counting this frequency information to produce a desired musical tone waveshape signal.

It is another object of the invention to provide an electronic musical instrument capable of varying the sampling frequency of the musical tone waveshape memory in accordance with the pitch (frequency) of the musical tone.

It is another object of the invention to provide an electronic musical instrument capable of reading out a plurality of complicated envelope shapes in a multiplexed form.

It is another object of the invention to provide an electronic musical instrument capable of producing a plurality of musical tones each of which is of a slightly different pitch from the pitch of the note of the corresponding key.

It is still another object of the invention to provide an electronic musical instrument capable of producing musical tones having frequencies which differ slightly from one another depending upon which of several keyboards is used notwithstanding depression of keys for one and the same note.

Other objects and features of the invention will become apparent from the description made hereinbelow with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram showing one preferred embodiment of the electronic musical instrument according to the invention;

FIGS. 2a through 2d are respectively charts showing clock pulses employed in this embodiment of the electronic musical instrument;

FIGS. 3 and 4 are circuit diagrams showing a key data signal generating device employed in the embodiment;

FIG. 5 is a chart showing the correspondence between the key address codes and key switches;

FIGS. 6A and 6B are graphic diagrams illustrative of relations between first and second key data signals and the opening and closing of break and make contacts;

FIGS. 7a and 7b are circuit diagrams showing logical circuits provided for eliminating a chattering effect produced by the key switches;

FIGS. 8a through 8d are graphic diagrams showing key data signals at respective points in the circuit shown in FIGS. 7a and 7b.

FIG. 9 is a circuit diagram showing a detailed logical circuit of a key assigner employed in the embodiment;

FIG. 10 is a block diagram showing fraction and integer counters;

FIG. 11 is a circuit diagram showing one example of a frequency information memory utilizing a (ROM) operated at a low speed;

FIGS. 12a through 12i are charts explanatory of states of signals appearing at certain points of the frequency information memory shown in FIG. 11;

FIG. 13 is a block diagram showing one example of an envelope counter and a truncate counter employed in the inventive electronic musical instrument;

FIGS. 14a and 14b are graphic diagrams illustrating the reading of an envelope waveshape from the envelope memory;

FIG. 15 is a block diagram showing one example of a first percussive counter;

FIG. 16 is a graphic diagram showing a waveshape read from a first percussive memory;

FIG. 17 is a block diagram showing one example of a second percussive counter;

FIGS. 18a and 18b are graphic diagrams showing waveshapes read from the second percussive counter;

FIG. 19 is a block diagram showing one example of a touch response counter;

FIGS. 20a through 20e are graphic diagrams explanatory of a touch response operation operation of the touch response counter shown in FIG. 19;

FIG. 21 is a block diagram showing a clock selector;

FIGS. 22a through 22e are graphic diagrams showing waveshapes appearing at certain points in the clock selector shown in FIG. 21; and

FIGS. 23 through 26 are block diagrams respectively showing other embodiments of the electronic musical instrument according to the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring first to FIG. 1 which shows one preferred embodiment of the inventive electronic musical instrument, a keyboard circuit 1 has key switches corresponding to respective keys. Each of the key switches includes a break contact and a make contact. A key data signal generator 2 comprises a key address code generator which produces key address codes indicative of the notes corresponding to the respective keys successively and repeatedly. The key data signal generator 2 also comprises a first key data signal generating unit 2a which produces a first key data signal when the break contact of a key switch corresponding to a depressed key is opened and a key address code corresponding to the depressed key is produced. The key data signal generator 2 further comprises a second key data signal generating unit 2b which produces a second key data signal when the make contact of the key switch is closed and the key address code corresponding to the depressed key is produced. The first and second key data signals are applied to a key assigner 3. The key assigner 3 comprises a key address code generator which operates in synchronization with the above described key address code generator, a key address code memory which is capable of storing key address codes up to the same number as a maximum number of musical tones to be simultaneously reproduced (e.g. 12 channels as in the present embodiment) and successively and repeatedly outputting these key address codes, a logical circuit which, upon receipt of the first key data signal, applies this first key data signal to the key address code memory for causing it to store the corresponding key address code on the condition that this particular key address code has not been stored in any channel of the memory yet and that one of the channels of the memory is available for storing this key address code, and a logical circuit which generates, upon receipt of the first and second key data signals, a tone response signal TRS, an attack start signal ES, a

percussive signal PES and decay start signal DIS. A touch response counter TRC makes a counting operation during application thereto of the touch response signal TRS, and the output of the touch response counter TRC is applied to a touch response memory TRM as a readout control signal. The output of the touch response memory TRM which corresponds in its level to the time during which the touch response signal is applied to the touch response counter TRC is applied to other memories, i.e., percussive memories and envelope memories for controlling the level of an envelope shape in its entirety. A percussive counter P_1C is adapted to start counting upon receipt of the attack start signal ES. The outputs of the percussive counter P_1C are applied to percussive memories P_1M_1 , P_1M_2 and P_1M_3 as readout control signals. The percussive memories P_1M_1 to P_1M_3 store percussive waveshapes which rise abruptly at the instant when the key is depressed and fall gradually thereafter. It is to be noted that these percussive memories P_1M_1 to P_1M_3 store waveshapes which are different from one another. A percussive counter P_2C is adapted to start counting upon receipt of the percussive signal PES and accelerate the counting operation upon receipt of the decay start signal DIS. The outputs of the percussive counter P_2C are applied to percussive memories P_2M_1 , P_2M_2 and P_2M_3 as a readout control signal. The percussive memories P_2M_1 to P_2M_3 store, as in the percussive memories P_1M_1 to P_1M_3 , percussive waveshapes which rise abruptly and fall gradually thereafter, each waveshape being somewhat different from the others. An envelope counter EC is adapted to start a counting of attack clock pulses upon receipt of the attack start signal ES, stop counting when the count has reached a predetermined value and resume the counting operation upon receipt of the decay start signal DIS. The outputs of the envelope counter EC are applied to envelope memories E_1M_1 , E_1M_2 and E_1M_3 as readout control signals. The envelope memories E_1M_1 to E_1M_3 respectively store, in a time-sampled fashion, attack waveshapes in addresses ranging from 0 to a predetermined address and decay waveshapes in addresses from an address next to the predetermined address to the last address. The memories E_1M_1 to E_1M_3 store waveshapes which are different from one another. Reference characters S_1 to S_4 designate clock selectors provided for applying to each counter clock pulses at a suitable frequency selected in accordance with the kind of the keyboard used. Percussive clock pulses selected by the clock selector S_1 are supplied to the percussive counters P_1C and P_2C . Damping clock pulses selected by the clock selector S_2 are supplied to the percussive counter P_2C . Attack clock pulses selected by the clock selector S_3 and decay clock pulses selected by the clock selector S_4 are both supplied to the envelope counter EC.

The counters P_1C , P_2C and EC respectively apply count finish signals F_1 , F_2 and F_3 which represent the finish of the counting operation to the key assigner 3. When all of the count finish signals have been applied to the key assigner 3, the control signals stored and kept in the key assigner 3 are cleared.

The outputs of the memories $P_1M_1 - P_1M_3$, $P_2M_1 - P_2M_2$ and $E_1M_1 - E_1M_3$ are applied to the control terminals of musical tone waveshape memories 6a to 6e through a buffer circuit BF so as to provide the musical tone waveshapes produced from the musical tone waveshape memories with desired envelopes.

Key address codes produced by the key assigner 3 are also applied to a frequency information memory 4. The frequency information memory 4 stores frequency information corresponding to the respective key address codes and, upon receipt of the key address codes from the key assigner, outputs frequency information corresponding to the respective key address codes. The frequency information consists of a fraction section and an integer section as will be described in detail later, the fraction section being applied to fraction counters 5a and 5b and the integer section to an integer counter 5c.

The fraction counter 5a is adapted to cumulatively count its inputs and apply a carry signal to the next fraction counter 5b when carrying takes place. The counter 5b is constructed in the same principle as the counter 5a and applies a carry signal to the integer counter 5c when carrying takes place.

The integer counter 5c cumulatively counts the carry signals and the integer section information inputs, and delivers out a waveshape address code successively changing with time. The outputs of this counter 5c are applied to a plurality of input terminals provided in each of the waveshape memories 6a to 6e. A musical tone waveshape for one period is sampled at n points and the amplitudes of the sampled waveshape are stored at addresses 0 to $n-1$ of the respective waveshape memories 6a to 6e. The musical tone waveshapes are read from these waveshape memories 6a to 6e by successively reading out the amplitudes at respective time points designated by the waveshape address code from the counter 5c.

For achieving the purpose of reproducing a plurality of musical tones simultaneously, the present electronic musical instrument has a construction based on dynamic logic so that the counters, logical circuits and memories provided therein are used in a time-sharing manner. Accordingly, time relations between clock pulses controlling the operations of these counters etc. are very important factors for the operation of the present electronic musical instrument.

FIGS. 2a to 2d illustrate relations between the various clock pulses used in the present electronic musical instrument. FIG. 2a shows a main clock pulse ϕ_1 which has a pulse period of 1 μ s. This pulse period is hereinafter referred to as "channel time." FIG. 2b shows a clock pulse ϕ_2 having a pulse width of 1 μ s and a pulse period of 12 μ s. This pulse period of 12 μ s is hereinafter referred to as "key time". FIG. 2c shows a key scanning clock pulse ϕ_3 which has a pulse period equivalent to 256 key times. One key time is divided by 12 μ s and each fraction of the divided key time is called first, second . . . 12th channel respectively. FIG. 2d shows a clock pulse ϕ_4 which appears only during the 12th channel in each key time. A channel denotes in this specification a shared portion of time, i.e. a channel time.

Key data signal generator

Each key switch of the present electronic musical instrument has a break contact and a make contact. As a key is depressed, the break contact is initially opened and thereafter the make contact is closed. The key switches are arranged in a plurality of blocks, each block having a plurality of the key switches. A common contact is provided for each block of key switches. FIG.

3 illustrates connections of the break contacts of the key switches and FIG. 4 those of the make contacts.

Referring to FIG. 3, a key address code generator KAG₁ consists of binary counters of eight stages. The clock pulse ϕ_2 with the pulse period of 12 μ s (hereinafter called a key clock pulse) is applied to the input of the key address code generator KAG₁. The key clock pulse applied to the key address code generator KAG₁ changes the code, i.e., the combination of 1 and 0 in each of the binary counter stages.

The highest class of electronic musical instrument typically has a solo keyboard, upper and lower keyboards and a pedal keyboard. The pedal keyboard has 32 keys ranging from C₂ to C₄ and the other keyboards respectively have 61 keys ranging from C₂ to C₇. Thus, this type of electronic musical instrument has 215 keys in all.

According to the present invention, 256 different codes are produced by the key address code generator KAG₁ and 215 codes among them are allotted to the corresponding number of keys. Digits of the key address code generator KAG₁ from the least significant digit up to the most significant digit are represented by reference characters N₁, N₂, N₃, N₄, B₁, B₂, K₁ and K₂ respectively. Among them, K₂ and K₁ constitute a keyboard code representing the kind of keyboard, B₂ and B₁ a block code representing a block in the keyboard and N₁ through N₄ a note code representing a musical note in the block. Each keyboard is divided into four blocks each block including 16 keys. These blocks are designated as block 1, block 2, block 3 and block 4 counting from the lowest note side. The correspondence between the key address codes and the key switches is shown in tabular form in FIG. 5. It is assumed that the key address codes which would correspond to three notes above the actually existing highest key (right side as viewed in FIG. 5) in the solo keyboard S, upper keyboard U and lower keyboard L and the key address codes which would correspond to the blocks 3 and 4 in the pedal keyboard are not allotted to keys in the present embodiment.

The bit outputs of the key address code generator KAG₁ are applied through decoders D₁ and D₂ to the keyboard circuit for sequentially scanning each key. The scanning starts from the block 4 of the solo keyboard S and is performed through the blocks 3, 2, 1 of the solo keyboard S, the blocks 4, 3, 2, 1 of the upper keyboard U, the blocks 4, 3, 2, 1 of the lower keyboard L and the blocks 2, 1 of the pedal keyboard P in the order named as shown by arrows in FIG. 5. One cycle of scanning of all of the keys is thereby completed and this scanning operation is cyclically repeated at an extremely high speed. Scanning time required for 1 cycle of scanning is about 3 ms in the present embodiment in which the above described key clock is used.

The decoder D₁ is a conventional binary-to-one decoder designed as to receive four-digit binary codes consisting of combinations of the digits N₁ to N₄ of the key address code generator KAG₁ and to deliver an output at one of the 16 individual output lines H₀ through H₁₅ successively and sequentially, the binary code in each instance determining a respective output line. The output line H₀ is connected through diodes to the key switches S₃K₀, S₂K₀, S₁K₀, U₃K₀, U₂K₀, U₁K₀, L₃K₀, L₂K₀, L₁K₀, P₂K₀ and P₁K₀ corresponding respectively to the highest note of each block (except the blocks 4) of the respective keyboards. The output line

H₁ is similarly connected to the key switches S₃K₁, . . . P₁K₁ (K₁ keys in the respective blocks) corresponding to the second highest note of each block except the blocks 4. It will be understood that no keys are provided for the three codes on the highest note side in the block 4 of the solo keyboard S, the upper keyboard U and the lower keyboard L and, accordingly, the output lines H₀ to H₂ are not connected in the blocks 4. Output line H₃ and subsequent output lines are connected in a similar manner to the corresponding key switches of each block (also of block 4). The common break contact members S₄B, S₃B . . . P₁B are connected to the inputs of AND circuits Y₀, Y₁ . . . Y₁₃ respectively.

The decoder D₂ is a conventional binary-to-one decoder designed as to receive four-digit binary codes consisting of combinations of the digits B₁, B₂, K₁ and K₂ of the key address code generator KAG₁ and to deliver an output at one of the 16 individual output lines J₀ through J₁₅ successively and sequentially, the binary code in each instance determining a respective output line. The output lines J₀ through J₁₅ (except J₁₂ and J₁₃) are connected to the inputs of the AND circuits Y₀ through Y₁₃ respectively. The outputs of the AND circuits Y₀ through Y₁₃ are connected through an OR circuit OR₁ to one of four input terminals of an OR circuit OR₂. The output lines J₁₂ and J₁₃ are connected to two other input terminals of the OR circuit OR₂ for substituting break contacts of the unused blocks 3 and 4 of the pedal keyboard. The B₁ and B₂ outputs of the key address code generator KAG₁ are connected to the inputs of an AND circuit A₁₆ via inverters I₁ and I₂. The output of the AND circuit A₁₆ is connected to one of the inputs of an AND circuit A₁₇. The output lines H₀, H₁ and H₂ of the decoder D₁ are also connected to the other input of the AND circuit A₁₇ via an OR circuit OR₄. The output of the AND circuit A₁₇ is connected to the remaining input terminal of the OR circuit OR₂ for substituting break contacts of the unused three notes on the highest note side in each block 4. The output of the OR circuit OR₂ is applied to the input of a delay flip-flop circuit DF₁ through an inverter I₃. The output from this circuit DF₁ constitutes a first key data signal.

FIG. 4 illustrates connections of the make contacts. In FIG. 4, the same component parts as those shown in FIG. 3 are denoted by the same reference characters and description thereof is omitted. Common make contact members S₄M to P₁M are connected to the inputs of corresponding AND circuits X₀ to X₁₃. Output lines J₀ to J₁₁, J₁₄ and J₁₅ of a decoder D₂ are also connected to the inputs of the AND circuits X₀ to X₁₃. The outputs of the AND circuits X₀ to X₁₃ are connected to the input of a delay flip-flop DF₂ via an OR circuit OR₃. The output from this delay flip-flop DF₂ constitutes a second key data signal.

The codes produced from the key address code generator KAG₁ change their contacts every time the key clock pulse ϕ_2 is applied.

If a certain key is depressed, the break contact corresponding to the depressed key is opened at the initial stage of the key depressing operation and then the make contact of the depressed key is closed at the last stage of the key depressing operation. When the key address code generator KAG₁ provides a code which corresponds to the depressed key while the break contact is open, an output 0 is produced from one of the AND circuits Y₀ to Y₁₃. This output is applied to

the inverter I_3 via the OR circuits OR_1 and OR_2 . An inverted output 1 from the inverter I_3 is delayed by the delay flip-flop DF_1 and provided therefrom as the first key data signal KD_1 .

The operation by which the first key data signal KD_1 is produced will now be described more in detail. If no key is depressed, all of the break contacts remain closed. Accordingly, the logical output 1 provided on one of the output lines of the decoder D_1 is applied to one of the AND circuits through one of the closed break contacts. Since the output 1 from the decoder D_2 is also applied to the input of the same AND circuit, the AND circuit produces an output 1. This output 1 is applied to the inverter I_3 through the OR circuits OR_1 and OR_2 . Accordingly, the input of the delay flip-flop circuit DF_1 is 0. This state remains unchanged even if the outputs of the decoders D_1 and D_2 change. Thus, the first key data signal is not produced.

The circuit of the present embodiment is so constructed that, with respect to the keys which are not used, the circuit operates in the same manner as in the state wherein the break contact is closed. More specifically, when the key address code generator KAG_1 produces a code which corresponds to one of the unused keys, a signal 1 is applied to the input of the inverter I_3 .

In the present embodiment in which the three keys on the highest note side of the block 4 in each of the solo keyboard S, the upper keyboard U and the lower keyboard L are not actually provided, the circuit is so constructed that a signal 1 is applied to the input of the inverter I_3 when the outputs of the stages B_2 and B_1 are 0 0 and the decoder D_1 produces its output on either one of the output lines H_0 , H_1 and H_2 . The circuit consisting of the OR circuit OR_4 , the inverters I_1 , I_2 and the AND circuits A_{16} , A_{17} is provided for achieving this purpose. Similarly, the output lines J_{12} and J_{13} of the decoder D_2 are connected to the input of the inverter I_3 through the OR circuit OR_2 so as to apply a signal 1 to the inverter I_3 since the blocks 4 and 3 of the pedal keyboard are not used.

Assume that one of the break contacts, for example the break contact of the key switch S_3K_1 , is now opened. When the code of the key address code generator KAG_1 is $K_2 K_1 B_2 B_1 N_4 N_3 N_2 N_1 = 00010001$, i.e., when a signal 1 is produced respectively on the output line H_1 of the decoder D_1 and the output line J_1 of the decoder D_2 , the output 0 is produced from the AND circuit Y_1 and this output 0 is applied to the inverter I_3 . Accordingly, the inverter I_3 produces an output 1 which is delayed in the delay flip-flop DF_1 and is provided therefrom as the first key data signal KD_1 . This key data signal KD_1 represents the opening of the corresponding break contact.

As the above-mentioned particular key is further depressed, the make contact of the key switch S_3K_1 is closed and the second key data signal KD_2 is produced from the delay flip-flop DF_2 . The operation by which this second key data signal is produced will be described hereinbelow.

Assume that one of the make contacts, for example the one of the key switch S_3K_1 , is now closed. When the code of the key address code generator KAG_1 is 00010001, i.e., when a signal 1 is produced respectively on the output line H_1 and the output line J_1 of the decoder D_2 , the output of the AND circuit X_1 is 1. This output is applied to the delay flip-flop DF_2 through the OR circuit OR_3 . The signal delayed in the flip-flop DF_2

is output therefrom as the second key data signal KD_2 .

This second key data signal represents closing of the make contact, i.e., a state in which the key has been fully depressed as well as representing the note of the depressed key by virtue of the time at which the signal is produced.

FIG. 6A graphically illustrates the first and second key data signals KD_1 and KD_2 . In the figure, A_1 represents the time at which the break contact is opened and the first key data signal is produced, whereas A_2 represents time at which the make contact is closed and the second key data signal is produced. The pulse width of each key data signal is the same as the pulse period ($12 \mu s$) of each key clock pulse ϕ_2 . Each key data signal is produced when the code of the key address code generator KAG_1 coincides with the code of the depressed key. The key address code generator KAG_1 is reset by the key scanning clock pulse ϕ_3 upon receipt of 256 key clock pulses ϕ_2 , this operation being repeated by a subsequent counting operation of the key address code generator KAG_1 . Thus, one key data signal is produced at a period of a scanning time $T = 12 \mu s \times 256 = 3.07$ ms as long as the state of the contact of the depressed key remains unchanged. As will be noted from FIG. 6(A) each key data signal is produced during one of 256 periods of time with an equal interval controlled by the outputs of the key address code generator KAG_1 , which one period corresponds to the depressed key. Consequently, a specific key address code, i.e., a specific key depressed at a given time can be known by detecting the time at which the key data signal is produced, by suitable means such, for example, as one detecting a time interval between the time at which the key data signal is produced and the time at which the reset clock pulse ϕ_3 is applied. Furthermore, the speed of depression of the key can be known by detecting by suitable means a time interval T_{12} between the time A_1 at which the first key data signal is produced and the time A_2 at which the second key data signal is produced. This enables adjustment of the level of a tone to be reproduced according to the speed of depression of the key.

In a case where no touch response control to be described later is required, the break contacts and the logical circuit related thereto are not necessary.

The foregoing description is made with regard to a case where only a single key is depressed. In a case where a plurality of keys are simultaneously depressed, the corresponding first and second key data signals KD_1 and KD_2 which respectively consist of a plurality of pulses are likewise produced.

According to the present invention, devices are provided for overcoming various problems which arise from the provision of the key contacts. These devices will be described in detail hereinbelow.

As has previously been described, each key data signal has a pulse width of $12 \mu s$ which is equal to one key time of the key clock pulse ϕ_2 . This is an arrangement designed for utilizing the key data signal in a time-sharing manner by suitably dividing the pulse width of $12 \mu s$ (into 12 in the present embodiment) by means of the main clock pulses which are produced with period of $1 \mu s$ which is defined as a channel time. Accordingly, the key data signal must be a clean rectangular wave pulse which rises abruptly (vertically) and sustains for $12 \mu s$ and then falls abruptly (vertically) as shown in FIG. 6(A). However, the pulse waveshape of

the key data signal actually tends to rise rather gradually because of electrostatic capacity of the key contacts and associated wiring.

In the embodiment shown in FIG. 3 or FIG. 4, electrostatic capacity of the large number of key contacts is relatively large. Besides, electrostatic capacity of the output lines of the decoder D_1 and the input lines of the AND circuits is also large because the key contacts are not necessarily located adjacent to the circuit portion of the instrument. As a result, the pulse waveshape of the key data signals KD_1 and KD_2 applied to the input terminals of the delay flip-flops DF_1 and DF_2 has a gradual rise as shown in FIG. 6B, *a*. This rise portion tends to be misinterpreted as a signal 0 thereby causing a faulty operation of the circuit. With a view to preventing occurrence of such faulty operation, the delay flip-flops DF_1 and DF_2 are provided for shaping the pulse. The key clock pulse ϕ_2 (FIG. 6B, *b*) is applied to the delay flip-flops DF_1 and DF_2 as a synchronizing signal thereby causing the flip-flops to store a sufficiently stable state of the input signal applied thereto. This stable state is held until a next clock pulse ϕ_2 is applied, i.e., for 12 μs , and provided as the key data signal. Thus, the key data signals KD_1 and KD_2 which are delayed for one key time (12 μs) but have a desired pulse waveshape which accurately sustains a 1 state for 12 μs as shown by FIG. 6B, *c* are obtained. Accordingly, the possibility of occurrence of a faulty operation in the post-stage signal processing circuit is totally eliminated.

There is another problem involving an undesirable omission of pulses due to contact chattering. When the key data signals KD_1 and KD_2 are produced by opening of the break contacts and closing of the make contacts respectively, chattering takes place and the opening or closing of the contacts remains in an unstable state for about 10 ms, resulting in an inaccurate production of the key data signals, i.e., an undesired omission of pulses. If chattering such as shown in FIG. 8*a* occurs during the transition from an open state to a closed state of a make contact, omission of the key data signal KD_2 will result as illustrated in FIG. 8*b*. This omission is equivalent an opening of the make contact and clearly causes trouble. Similarly, occurrence of chattering in a transient state from a closed state to an open state of a break contact causes omission of the key data signal KD_1 .

According to the invention, a logical circuit as shown in FIG. 7*a* may be provided for applying the key data signal to an input terminal T_1 and thereby obtaining an accurate key data signal without pulse omission at an output terminal T_{out} . More specifically, this logical circuit comprises a shift register SF (256 bits in this embodiment) operated by the key clock pulse ϕ_2 which is used for delaying the key data signal by one key scanning time T . The key data signal from the terminal T_1 and the output of the shift register SF are applied to an OR circuit OR, and a desired key data signal without pulse omission is produced at the output of the OR circuit OR. When the key data signal shown in FIG. 8*b* is applied to the terminal T_1 , the shift register SF produces an output such as shown in FIG. 8*c* which is delayed by one key scanning time T . Since these key data signals are applied to the OR circuit OR, a key data signal as shown in FIG. 8*d* which has no omitted pulse is obtained at the terminal T_{out} .

It will be understood from the foregoing description that omission of a pulse in the output key data signal is

prevented by the provision of the logical circuit even if there occurs omission of one pulse in the original key data signal. If two shift registers are provided in the logical circuit as shown in FIG. 7*b*, omission of two consecutive pulses can be prevented. It will be apparent that an increase in the number of shift registers will result in the prevention of an omission of a like number of pulses and that such a logical circuit would be applicable to both of the key data signals.

The foregoing description has been made with regard to a case where only one key is depressed. If a plurality of keys are depressed simultaneously, key data signals respectively corresponding to the depressed keys are produced in the same manner and different musical tone wave shapes respectively corresponding to these key data signals are obtained. For convenience of explanation, description will be made hereinbelow about a case where only one key is depressed to obtain one musical tone waveshape.

Generation of a musical tone waveshape

FIG. 9 is a block diagram showing the construction of the key assigner 3 in detail. A key address code memory KAM has memory channels of a number equal to that of the musical tones to be reproduced at the same time, each of these channels storing a key address code representing the musical note being played. The key address code memory KAM is adapted to apply the key address code in a time-sharing manner to the frequency information memory 4 as a frequency designation signal. In the present embodiment, a shift register of 12 words - 8 bits is utilized as the key address code memory KAM. This shift register performs shifting upon receipt of the main clock pulse ϕ_1 produced at an interval of 1 μs . The output from the last stage of this shift register is provided to the frequency information memory and, simultaneously, fed back to its input side through its gate G. Accordingly, each key address code is circulated in the shift register at a cycle of 1 key time (12 μs) unless the code is cleared from its corresponding channel.

The key assigner 3 comprises a key address code generator KAG_2 which produces the key address codes to be stored in the above described key address code memory KAM. This generator KAG_2 is of the same construction as the key address code generator KAG_1 . These two generators KAG_1 and KAG_2 operate in exact synchronization with each other. More specifically, the fact that the respective bits of the key address code generator KAG_2 are all 0 is detected by an AND circuit A_{18} and the detected signal ϕ_3 is applied to the reset terminals of the respective bits of the key address code generator KAG_1 as the key scanning clock signal. This arrangement obviates a plurality of lines which would otherwise be necessary for receiving the key address codes supplied from the code generator KAG_1 .

One of the principal operations of the key assigner 3 is to cause the key address code memory KAM to store a key address code corresponding to the key data signal upon receipt thereof when the following two conditions are satisfied:

Condition (A);

The key address code is not identical with any of the codes already stored in the key address code memory KAM.

Condition (B);

There is a not-busy channel, i.e. a channel in which no code is stored, in the key address code memory KAM.

In order to examine whether the condition (A) is satisfied or not, the key address code memory KAM must be operated for 1 cycle and this operation requires one key time. Likewise, 1 key time is required for examining whether the condition (B) is satisfied or not.

Accordingly, 2 key times are required for examining both of the two conditions (A) and (B). This necessitates a key data signal having a pulse width of 2 key times according to a normally conceivable method. As a result, one scanning period required for scanning all of the key switches in the key data signal generator becomes double, i.e., 6.4 ms which is too long to keep up with the playing speed of the key.

If the key assigner 3 of the present electronic musical instrument, a device is provided for enabling it to examine presence of the above described two conditions (A) and (B) within 1 key time.

Assume now that a key data signal KD_1^* is produced from the inverter I_3 . While this signal is in a state of 1 which lasts for 12 μ s, the key address code KA^* from the key address code generator KAG_2 coincides with the code of the key address code generator KAG_1 and represents the note of the depressed key. The key data signal KD_1^* however, is delayed by the delay flip-flop DF_1 for one key time and has not been applied to the key assigner 3 yet. During this 12 μ s period, the key address code KA^* is applied to a comparison circuit KAC in which the code KA^* is compared with each output of the channels of the key address code memory KAM. Alternatively stated, the key address code KA^* is compared with each code in the memory KAM for detection of coincidence between the two. A coincidence signal EQ^* produced from the comparison circuit KAC is 1 when there is coincidence and 0 when there no coincidence. The coincidence signal EQ^* is applied to a coincidence detection memory EQM and also to one input terminal of an OR circuit OR_5 . This memory EQM is a shift register having a suitable number of bits, e.g. 12 as in this embodiment. The memory EQM successively shifts the signal EQ^* , i.e. delays it by one key time when the signal EQ^* is 1 and thereby produces a coincidence signal $EQ (=1)$. Each of the outputs from the first to eleventh bits of the coincidence detection memory EQM is applied to the OR circuit OR_5 . Accordingly, the OR circuit OR_5 produces an output when either the signal EQ^* from the comparison circuit KAC or one of the outputs from the first to eleventh bits of the shift register EQM is 1. The output signal ΣEQ of the OR circuit OR_5 is applied to one of the input terminals of an AND circuit A_{19} . The AND circuit A_{19} receives a clock pulse ϕ_4 at the other input terminal thereof. Since information stored in the shift register before the first channel is false information, correct information, i.e. information representing the result of the comparison between the key address code KA^* and the codes in the respective channels of the key address code memory KAM is obtained only when the result of the comparison in each of the first to 11 channels is applied to the coincidence detection memory EQM and the result of comparison in the 12th channel is applied directly to the OR circuit OR_5 . This is the reason

why the clock pulse ϕ_4 is applied to the AND circuit A_{19} .

If the signal ΣEQ is 1 when the clock pulse ϕ_4 is applied, the AND circuit A_{19} produces an output 1 which is applied through an OR circuit OR_6 to a delay flip-flop DF_3 . The signal is delayed by this delay flip-flop DF_3 by one channel time and fed back thereto via an AND circuit A_{20} . Thus, the signal 1 is stored during 1 key time until a next clock pulse ϕ_4 is applied to the AND circuit A_{20} through an inverter I_5 . The output 1 of the delay flip-flop DF_3 is inverted by an inverter I_6 and is provided as an unblank signal. This unblank signal indicates that the same code as the key address code KA^* is not stored in the key address code memory KAM when it is 1, and that the same code as the key address code KA^* is stored in the memory KAM when it is 0.

As described in the foregoing, presence of the condition (A) is examined during production of the key data signal KD_1^* and the unblank signal 1 is produced when the condition (A) is satisfied, whereas the unblank signal 0 is produced when this condition is not satisfied. The key data signal KD_1^* is delayed by one key time and applied to one of the input terminals of an AND circuit A_{21} through a terminal t_A and an OR circuit OR_7 of the key assigner 3. In the meantime, the unblank signal UNB produced in the above described manner is applied to the other input terminal of the AND circuit A_{21} . Consequently, the key data signal KD_1 is fed through the AND circuit A_{21} to an AND circuit A_{22} when the signal UNB is 1.

In order for a new key address code to be stored in the key address code memory KAM, one of the twelve channels of the memory must be in a not-busy state, i.e. available for storage. A busy memory BUM is provided to detect whether there is a not-busy channel in key address code the memory. The busy memory BUM consists of a shift register of 12 bits, and is adapted to store 1 when a new key-on signal to be described later is applied thereto from an OR circuit OR_8 . This signal 1 is sequentially and cyclicly shifted in the busy memory BUM. This new key-on signal is simultaneously applied to the key address code memory KAM so as to cause the memory KAM to store the new key address code. Accordingly, the signal 1 is stored in one of the channels of the busy memory BUM corresponding to the busy channel of the key address code memory KAM. Contents of a not-busy channel are 0. Thus, the output of the final stage of the busy memory BUM indicates whether this channel is busy or not. This output is hereinafter referred to as a busy signal A_1S .

This busy signal A_1S is applied to one of the input terminals of the AND circuit A_{22} via an inverter. When a signal A_1S is 1, i.e., a certain channel is not busy, the key data signal is applied to the busy memory BUM as the new key-on signal via the AND circuit A_{22} and the OR circuit OR_8 , thereby causing the busy memory BUM to store 1 in its corresponding channel. Simultaneously, the gate G of the key address code memory KAM is controlled so that the key address code KA from a delay flip-flop DF_4 will be stored in a not-busy channel of the memory KAM.

The delay flip-flop DF_4 is provided for delaying the output KA^* of the key address code memory by one key time so that a key address code corresponding to the key data signal KD_1^* may be stored in synchronization with the key data signal KD_1^* , since the key data

signal KD_1 which is delayed by one key time is applied to the key assigner.

The new key-on signal NKO from the OR circuit OR_8 is applied through the OR circuit OR_6 to the delay flip-flop DF_3 to set the flip-flop. The output of the flip-flop DF_3 is inverted by the inverter I_6 and the unblank signal UNB becomes O . Accordingly, the output of the AND circuit A_{21} becomes O when the unblank signal UNB becomes O thereby changing the new key-on signal NKO to O . This arrangement is provided to ensure storage of the key address code KA in only one, and not two or more, not-busy channel of the key address code memory KAM .

In the above described operation, input signals $\overline{PCH}$ and $\overline{PSC}$ are assumed to be 1 respectively for convenience of explanation. The input signals PCH and PSC will be described in detail later.

It will be understood from the foregoing description that as the key data signal KD_1 is applied to the key assigner, the key address code corresponding to the key data signal KD_1 is stored in the key address memory KAM so long as the above described conditions (A) and (B) are both satisfied.

In this way, 12 kinds of key address codes each consisting of eight digits $K_2K_1B_2B_1N_4N_3N_2N_1$ are stored in the key address code memory KAM , and these address codes are shifted by the main clock pulse ϕ_1 and the outputs of the final stage are successively applied to the frequency information memory 4 and also fed back to the input side of the memory KAM for cyclically producing outputs therefrom, changing at a rate of 1 μs , i.e. the same code appearing once every 12 μs .

The frequency information memory 4 stores information representing a plurality (e.g. 253) of predetermined frequencies corresponding to the respective key address codes and produces the frequency information for a particular key address code when this key address code is applied thereto.

The frequency information for each frequency consists of a suitable number of bits, e.g. 15 as in the present embodiment. One bit of the 15 bits represents an integer section and the rest of the bits, i.e. 14, represent a fraction section. The following Table I illustrates example of the frequency information corresponding to keys C_2 , C_3 , C_4 , C_5 , C_6 , D_6^* , E_6 and C_7 .

tions are separately carried out in time sharing fashion, 12 sets in 12 μs . Now let μs watch the accumulation of one particular set, which will occur once in 12 μs . The 7-digit output from the counter 5c is the integer portion of the cumulative value of the frequency information and is defined as a waveshape address code, which is applied to the musical tone waveshape memories 6a to 6c for designating the address of the waveshape memory to be read. Assume that the waveshape of the musical tone to be reproduced is stored as 64 sampled analog values at 64 sample points and the frequency information is represented by F . If one key time is 12 μs , the number of times per second F is accumulated in the frequency counters 5a to 5c per 1 second is $1/12 \times 10^6$.

Accordingly, the counted value of the frequency counters 5a to 5c after lapse of one second is $1/12 \times 10^6 \times F$. Thus, the frequency f of the musical tone waveshape to be reproduced is

$$f = \frac{10^6}{12} F \times \frac{1}{64}$$

From this equation, the frequency information F stored in the frequency information memory 4 becomes

$$F = 12 \times 64 \times f \times 10^{-6}$$

Accordingly, this value F is stored in the memory 4 in accordance with the frequency f to be obtained. For example, F for the note C_3 is 0.104650 because the frequency of C_3 is 130.313 Hz. The values F for the other notes are determined in a similar manner.

Upon receipt of each of the changing key address codes from the key address code memory KAM , the frequency information memory 4 provides corresponding changing frequency information outputs, each consisting of 15 digits ($n_{15} \dots n_1$).

The frequency information outputs from the least significant digit (n_1) up to the seventh digit (n_7) of the digits are applied from the frequency information memory 4 to the fraction counter 5a, those from the eighth digit (n_8) up to the fourteenth digit (n_{14}) to the fraction counter 5b, and the 15th digit (n_{15}) to the integer counter 5c respectively. The counters 5a - 5c comprise

Table I

	Integer section		Binary fraction section												F-number	
	n_{15}	n_{14}	n_{13}	n_{12}	n_{11}	n_{10}	n_9	n_8	n_7	n_6	n_5	n_4	n_3	n_2	n_1	
key																
C_2	0	0	0	0	0	1	1	0	1	0	1	1	0	0		0.052325
C_3	0	0	0	0	1	1	0	1	0	1	1	0	0	1	0	0.104650
C_4	0	0	0	1	1	0	1	0	1	1	0	0	1	0	1	0.209300
C_5	0	0	1	1	0	1	0	1	1	0	0	1	0	1	0	0.4188600
C_6	0	1	1	0	1	0	1	1	0	0	1	0	1	0	0	0.837200
D_6^*	0	1	1	1	1	1	1	1	0	1	1	1	0	0	0	0.995600
E_6	1	0	0	0	0	1	1	1	0	0	0	0	0	0	1	1.054808
C_7	1	1	0	1	0	1	1	0	0	1	0	1	0	0	1	1.674400

In this table, the first through the fourteenth bits represent the fraction section and the 15th bit represents the integer section. The F represents a number expressed in a decimal notation.

The frequency information changing every 1 μs from the frequency information memory 4 is applied to frequency counters 5a to 5c as shown in FIG. 10 and counted thereby successively and cumulatively once every 1 key time (12 μs). Twelve different accumula-

adders $AD_1 - AD_3$ and shift registers $SR_1 - SR_3$. These shift registers are shown in FIG. 10 as 7×12 BIT shift registers, i.e. they operate with 12 words of 7 bits per word. Each of the adders $AD_1 - AD_3$ adds the output from the frequency information memory 4 and the output from the corresponding one of the shift registers $SR_1 - SR_3$. The shift registers $SR_1 - SR_3$ are adapted to store the 12 kinds of outputs in time sequence from the adders $AD_1 - AD_3$ temporarily and feed them back to

the input side of the adders $AD_1 - AD_3$. The shift registers $SR_1 - SR_3$ respectively have the same number of stages as the maximum number of musical tones to be reproduced simultaneously, e.g. 12 as in the present embodiment. This is an arrangement made for operating the frequency counters in a time-sharing manner, since the frequency information memory 4 receives in time sharing sequence the key address codes stored in the 12 channels (shift register stages) of the key address code memory KAM and produces the frequency information for the respective channels.

Explanation will now be made about this arrangement with respect to the first channel. If the contents of the first channel of the shift register SR_1 of the fraction counter 52 are 0, frequency information signals n_1 through n_7 , i.e. the first 7 bits of the fraction section are initially stored in the first channel of the shift register SR_1 . After lapse A of 1 key time, new frequency information signals n_1 through n_7 are added to the contents already stored in the first channel. This addition is repeated at every key time and the signals n_1 through n_7 are cumulatively added to the stored contents. When a carry takes place in the addition, a carry signal C_1 is applied from the counter 5a to the next counter 5b. The fraction counter 5b consisting of the adder AD_2 and the shift register SR_2 likewise makes cumulative addition of frequency information signals n_8 through n_{14} , i.e. the next 7 bits of the fraction section, and the carry signal C_1 , applying a carry signal C_2 to the adder AD_3 when a carry takes place as a result of the addition. The integer counter 5c consisting of the adder AD_3 and the shift register SR_3 receives the single digit n_{15} , i.e. the integer section, and the carry signal C_2 from the adder AD_2 and makes cumulative addition in the same manner as has been described with respect to the fraction counters 5a and 5b. The integer outputs of 7 bits stored in the first channel of the shift register SR_3 are successively applied to the musical tone waveshape memories 6a to 6c for designating the reading addresses to read.

The output signals S_1 to S_6 among the 7 bit outputs S_1 to S_7 of the shift register SR_3 are applied to a first digit input terminal P_1 through a sixth digit input terminal P_6 of the waveshape memory 6b for an 8' register note. The presence of an AND circuit A_{43} will be disregarded for the moment for convenience of explanation. In the meantime, the output signals S_2 through S_7 are respectively applied to digit input terminals P_1 through P_6 of the waveshape memory 6a for a 16' register note. The first digit input terminal P_2 of the waveshape memory 6c for a 4' register note is grounded and therefore fixed at 0, and the second through sixth digit input terminals $P_2 - P_6$ of the memory 6c receive S_1 through S_5 respectively. Accordingly, if reading from the 8' musical tone waveshape memory 6b is taken as a reference, with the output from the shift register SR_3 being 0, 1, 2, 3, 4, . . . 6, waveshape amplitudes at addresses 0, 1, 2, 3, 4 . . . 6 are read from the waveshape memory 6b. In this case, waveshape amplitudes at addresses 2, 4, 6, 8, 10, 12, 14 . . . are successively read from the waveshape memory 6c since the first digit thereof is fixed to 0 as has previously been described. Thus, a musical tone waveshape at a frequency which is double that of a musical tone waveshape of the waveshape memory 6b is produced from the waveshape memory 6c. As regards the waveshape memory 6a, waveshape amplitudes at addresses 0, 0, 1, 1, 2, 2, 3 . . . are successively read out. Therefore, a musical tone waveshape at a fre-

quency which is half that of the musical tone waveshape of the waveshape memory 6b is produced from the waveshape memory 6a.

In case the waveshape memory 6c for a 2' register note is further provided as shown in FIG. 1, input terminals P_1 and P_2 are likewise fixed to 0 and the signals S_1 through S_4 are applied to input terminals P_3 through P_6 respectively. If the waveshape memory 6e for a 1' register note is further provided, input terminals P_1 , P_2 and P_3 are fixed to 0 and the signals S_1 through S_3 are applied to input terminals P_4 through P_6 respectively.

Assume now that production of the highest tone (e.g. C_7 with its fundamental wave of 2.1 kHz) is desired. Since the sampling number of the waveshape memory 6b is 64, frequency F_1 of a harmonic of the highest degree (a harmonic of a degree at half the sampling number) is

$$f_1 = 2.1 \text{ KHz} \times \frac{64}{2} = 67.2 \text{ KHz.}$$

In the meanwhile, the outputs of the frequency counter 5c are applied to the waveshape memory 6b every 12 μ s for each channel so that a sampling rate f_2 of the waveshape memory 6b is

$$1/12 \times 10^6 \text{ Hz} = 83.3 \text{ kHz.}$$

Accordingly, the signal at the frequency f_1 is sampled by the signal at the frequency f_2 in the waveshape memory 6b with a result that a noise waveshape at a frequency of 16.1 kHz which is equivalent to the difference between the frequency f_1 and the frequency f_2 is produced. Since this frequency is not a harmonic of the fundamental wave frequency of 2.1 kHz, an unpleasant noise is heard.

This frequency is produced according to the sampling theorem when a harmonic frequency of a desired musical tone exceeds half of a sampling rate ($f_1 > f_2/2$). Alternatively stated, this frequency is produced when a product obtained by multiplying the fundamental wave frequency with the sampling number of the memory exceeds the sampling rate, i.e., the information F of the frequency information memory is more than 1 (in case the frequency information memory has an integer output).

According to the present invention, an arrangement has been made to prevent occurrence of the above described frequency. When an integer output of the frequency information memory 4 is 1, this output is inverted by the inverter I_8 and thereafter applied to one of the input terminals of the AND circuit A_{43} as a signal 0. Thus, the input to the input terminal P_1 of the waveshape memory 6b is made 0 whereby the sampling number of the waveshape memory 6b is reduced to 32. The frequency F_1 therefore becomes $F_1 = 2.1 \times 32/2 = 33.6 \text{ kHz}$ which is lower than $F_2/2$ so that occurrence of the noise frequency is avoided.

In the present embodiment, a read only memory (ROM) which produces its outputs at a very high rate (i.e. access time 1 μ s) is used as the frequency information memory 4. The frequency information memory 4 is not limited to this type of ROM but a ROM operating at a lower rate with a longer access time may also be used.

FIG. 11 shows an example of construction of a frequency information storage device using a ROM which operates at a relatively low speed.

Key address codes from the first channel to the twelfth channel are successively and repeatedly applied to the frequency information memory 4 every 1 μ s as shown in FIG. 12b. These key address codes thereafter are respectively applied to delay flip-flops DF₄–DF₁₂. These delay flip-flop DF₅–DF₁₂ store a key address code applied to their input when an output A from the last stage of a 13 bit shift register SF₄ becomes 1 and hold the key address code during 13 μ s until the output from the last stage of the same shift register SF₄ becomes 1 again (FIG. 12(e)). The 13 bit shift register SF₄ receives the main clock pulse ϕ_1 and is shifted every 1 μ s. The shift register SF₄ stores 1 for one channel only. Consequently, the shift register SF₄ produces the pulse A as shown in FIG. 12d when a signal 1 is output from the last stage thereof, and produces a pulse B as shown in FIG. 12g when a next signal 1 is shifted to the last stage thereof. This pulse B is fed to AND circuits provided on the output side of a read only memory ROM.

Assume that the last stage output A of the shift register SF₄ is 1 when a key address code of the first channel (hereinafter referred to as KA1) is applied to the respective delay flip-flops DF₅ through DF₁₂. The delay flip-flops DF₅–DF₁₂ store the key address code KA1. When the shift register SF₄ produces an output 1 as its last stage output A after 1 cycle, a key address code KA2 of the second channel is stored in the respective delay flip-flops DF₅ through DF₁₂ because the key address code applied at this time to the inputs of these delay flip-flops DF₅ through DF₁₂ has elapsed 13 μ s after the preceding code, i.e. 1 μ s over 12 μ s, so that this code corresponds to the second channel. Each key address code of the subsequent channels is successively applied in a similar manner to the delay flip-flops DF₅ through DF₁₂ at every 13 bit time (13 μ s).

The outputs of the delay flip-flops DF₅ through DF₁₂ are applied to the read only memory ROM. Since the read only memory ROM operates at a relatively low speed, several μ s are required before a frequency information (hereinafter also called data D with its suffix number representing a channel number) rises to a stable state from the moment when the key address code is applied as shown in FIG. 12(f). Again, a delay time of 2 to 3 μ s and a fall time of 3 to 4 μ s are required from the moment when the key address code ceases to be applied until the moment when the data D cease to be produced. When a period of 12 μ s has elapsed from the moment when the key address code KAI is applied to the read only memory ROM, the next last stage output B of the shift register SF₄ which is a logical value 1 is applied to AND circuit A₄₄–A₅₈. Since at this time the read only memory ROM produces the data DI, the data DI is applied to 12 bit shift registers SF₅–SF₁₉ through the AND circuits A₄₄–A₅₈ and OR circuits OR₁₅–OR₂₉. The shift registers SF₅–SF₁₉ effect shifting operation upon receipt of the main clock pulses ϕ_1 . The last stage outputs of these shift registers SF₅–SF₁₉ are fed back to the first stages thereof via AND circuits A₅₉–A₇₃ and the OR circuits OR₁₅–OR₂₉ whereby the data circulate through these shift registers. Consequently, the data DI are output from the shift registers SF₅–SF₁₉ 12 μ s after it is applied thereto (FIG. 12h).

Thus, the data DI are provided from the output of the frequency storage device as shown in FIG. 11 with delay of 24 μ s after it has been applied thereto (FIG. 12i). As regards the key address codes of the other channels, corresponding data are likewise produced with delay of 24 μ s.

The key address codes K₁ and K₂ function to selectively operate either one of the frequency information storage devices provided respectively for the sole keyboard, upper keyboard, lower keyboard and pedal keyboard for storing frequency information which differs from one another so as to produce a variety of musical tone waveshapes which are peculiar to the respective keyboards and differ slightly from one another. If, for example, the storage device shown in FIG. 11 is for the upper keyboard and a signal 1 is being applied to its terminal U, the key address code representing the upper keyboard, i.e. when K₁ is 1 and K₂ is 0, causes an AND circuit AA₂ to produce an output 1. This output is applied to the respective AND circuit A₇₄–A₇₉ through an OR circuit OR₃₀ and causes these AND circuits A₇₄–A₇₉ to gate out the signals from the delay flip-flops DF₅–DF₁₂ which signals thereafter are applied to the read only memory ROM. It will be apparent that at this time no key address codes representing the other keyboards pass the AND circuits A₇₄–A₇₉.

Envelope control for musical tone waveshapes

Assume with reference to FIG. 9 that a new key address code is stored in the first channel of the key address code memory KAM and a signal 1 is stored in the first channel of the busy memory BUM. As the busy memory BUM performs shifting operation and produces an output for the first channel, this output is applied to one of the inputs of the AND circuit A₃₃. At this time, no key data signal KD₂ has yet been applied to the first channel of the key-on memory KOM so that an output signal 0 is produced from the key-on memory KOM. This output 0 is inverted by an inverter A₂₅ and thereafter is applied to the other input terminal of the AND circuit A₃₃. The AND circuit A₃₃, therefore, produces an output 1. This output 1 of the AND circuit A₃₃ is transmitted as a touch response signal TRS to a terminal t₁.

As the key data signal KD₂ is then applied to one of the input terminals of the AND circuit A₂₃, the AND circuit A₂₃ passes this key data signal KD₂ during a period of time corresponding to the first channel only, for the coincidence memory EOM already has a signal 1 stored in its first channel and provides this signal to the other input terminal of the AND circuit A₂₃. The key data signal KD₂ gated out of the AND circuit A₂₃ is applied to the first channel of the key-on memory KOM thereby causing the key-on memory KOM to store 1. The storage of 1 in the key-on memory KOM stands for a state in which the make contact of the key switch is closed (hereinafter called "key-on"). The signal 1 of the first channel produced from the key-on memory KOM is inverted by an inverter and a signal 0 is applied to the AND circuit A₃₃. Consequently, the touch response signal TRS ceases to be produced. It will be understood from this that the period of time during which the touch response signal TRS is produced is equal to the period of time from the opening of the break contact till the closing of the make contact. Accordingly, the length of time during which the touch re-

sponse signal is produced depends upon the speed of depression of the key.

The signal 1 of the first channel of the key-on memory KOM is also supplied to a terminal t_2 as an attack start signal ES. This attack start signal ES is continuously produced until the signal 1 of the first channel of the key-on memory KOM is reset as will be described later.

When the break contact is closed upon release of the key, the first key data signal ceases to be produced. This causes a signal 1 produced through an inverter to be applied to one of the input terminals of AND circuit A_{24} . The coincidence signal EQ is still being applied to the other input terminal of the AND circuit A_{24} . Accordingly, a signal 1 is stored in the first channel of a key-off memory KFM. The contents of the first channel are successively shifted in the key-off memory KFM and are output from the last stage thereof as a signal 1. This signal 1 which is applied to a terminal t_4 represents a key-off state and hereinafter is called a decay start signal DIS.

While the signal 1 is stored in the first channel of the key-on memory KOM and the signal 1 is not stored in the key-off memory KFM, an AND circuit A_{41} receives a signal 1 in its respective inputs with respect to the first channel and produces a signal 1 which is applied as a percussive signal PES to a terminal t_3 . When the signal 1 is stored in the first channel of the key-off memory KFM and output therefrom, an inverted output 0 is applied to the AND circuit 41 and, accordingly, the percussive signal PES is not produced.

The output terminal of an AND circuit A_{40} is connected to the respective memories of the key assigner via OR circuits OR_{12} , OR_{13} and OR_{14} so as to clear the contents of these memories by applying to the input terminals of the AND circuit A_{40} counting termination signals from all envelope counters to be described later when reading of envelope waveshapes from all of the envelope counters has been completed. The output of the AND circuit A_{40} is also utilized as a clear signal CC for clearing each counter. One input IC to the OR circuit OR_{12} is an input for resetting the respective memories and counters to their initial conditions upon turning-on of the power.

The circuit portion a shown by a chain line in FIG. 13 illustrates one example of the envelope counter. The envelope counter comprises an adder AD_4 and a 12 word 7 bit shift register SR_4 , the result of addition on the adder AD_4 being supplied every 1 key time to corresponding channels of the shift register SR_4 . More specifically, the adder AD_4 adds the output of the shift register SR_4 and the clock pulse and provides a result S to the input terminal of the shift register SR_4 thereby causing the envelope counter to successively effect a cumulative counting with respect to each of the channels.

An output representing a counted value is applied from this envelope counter to an envelope memory EM and a waveshape amplitude stored at an address corresponding to the counted value is successively read from this memory EM. The envelope memory EM stores an attack waveform at addresses starting from 0 to a predetermined address, e.g. 16, and a decay waveform at addresses from the next address to the last one, e.g. 63.

The counting operation of the envelope counter will now be described with respect to the first channel assuming that the counted value of the first channel is initially 0.

When the attack start signal ES is applied to a terminal TE_1 , an AND circuit A_{81} which has already received signals 1 obtained by inverting outputs 0 of an AND circuit A_{80} and an OR circuit OR_{31} respectively by inverter I_{10} and I_{11} gates out an attack clock pulse AP to the adder AD_4 . The adder AD_4 and the shift register SR_4 successively count the attack clock pulse thereby reading out the attack waveshape of the envelope memory EM. When the counted value has reached 16, an output 1 is produced from the OR circuit OR_{31} and, accordingly, the attack clock pulse AP ceases to pass through the AND circuit A_{81} . The attack clock pulse AP remains prevented from passing the AND circuit A_{81} with respect to subsequent counts. Consequently, counting is once stopped and the amplitude stored at address 16 of the envelope memory EM continues to be read out. Thus, a sustain state is maintained.

In this state, an AND circuit A_{82} receives a signal 1 from the OR circuit OR_{31} and also a signal 1 which is obtained by inverting the output 0 of the AND circuit A_{80} by the inverter I_{10} . When the decay start signal DIS is applied to a terminal TE_2 , a decay clock pulse DP passes through the AND circuit A_{82} and is applied to the adder AD_4 . This causes the envelope counter to resume the counting operation for counted values after 16 and the decay waveshape is read from the envelope memory EM. When the counted value has reached 63, all of the inputs to the AND circuit A_{80} become 1 so that the AND circuit A_{80} produces an output 1. Accordingly, the AND circuit A_{82} ceases to gate out the decay clock pulse DP and the counting operation is stopped. Thus, the reading of the envelope waveshape has been completed.

In the above example, the decay start signal DIS is applied at a counted value after 16. In a case wherein the decay start signal is applied before reading of the attack waveshape is completed, i.e., when the key is released immediately after depression thereof, the AND circuit A_{82} does not pass the decay clock pulse DP because the output 0 from the OR circuit OR_{31} is applied to the AND circuit A_{82} . The decay waveshape therefore is never read out before the reading of the attack waveshape is completed, but is read out immediately upon completion of the reading of the attack waveshape.

FIG. 15 shows one preferred example of the first percussive counter P_1C . The first percussive counter P_1C comprises an adder AD_5 and a 12 word - 7 bit shift register SR_5 which effect a counting operation with respect to each of the channels in the same manner as the envelope counter shown in FIG. 13. The counting output of this counter is applied to the percussive memory P_1M so as to read out amplitudes stored at addresses corresponding to the counted values. The percussive memory P_1M stores at its addresses 0 to 63 a waveshape which, as shown in FIG. 16, rises abruptly and thereafter falls gradually until it becomes 0 at the address 63.

The following description is made on the assumption that the counted value of the first channel is initially 0. When the attack start signal ES is applied to a terminal TP_1 , an AND circuit A_{84} passes a percussive clock pulse CP_1 because at this time a signal 1 which is obtained by inverting the output 0 of an AND circuit A_{83} by an inverter I_{12} has been applied to the AND circuit A_{84} . The percussive clock pulse CP_1 thereafter is applied to the adder AD_5 . The adder AD_5 and the shift register SR_5 perform successive counting of the percussive clock pulse CP_1 thereby to read out a percussive waveshape

of the percussive memory P_1M . When the counting has reached the last counted value of 63, all of the inputs to the AND circuit A_{83} become 1 and the AND circuit A_{83} produces an output 1. This output 1 is inverted to 0 by the inverter I_{12} and thereafter is applied to the AND circuit A_{84} . Accordingly, the AND circuit A_{84} ceases to gate out the percussive clock pulse CP_1 and the counting is stopped.

FIG. 17 illustrates one preferred example of the second percussive counter P_2C . The second percussive counter P_2C comprises, as in the above described first percussive counter P_1C , an adder AD_6 and a 12 word 7 bit shift register SR_6 . The counting output of the shift register SR_6 is applied to a percussive waveshape memory P_2M . This memory P_2M stores a waveshape similar to the one stored in the memory P_1M at its addresses 0 to 63. It is assumed again that the counted value of the first channel is initially 0. When the percussive signal PES is applied to a terminal TP_2 , an AND circuit A_{86} gates out a percussive clock pulse CP_2 since it has already received a signal 1 which is obtained by inverting the output 0 of an AND circuit A_{85} by an inverter I_{13} . Thus, a successive counting of the percussive clock pulse CP_2 is performed and the percussive waveshape is read from the memory P_2M . This reading of the percussive waveshape is continued until the moment when the key is released and the decay start signal DIS is applied to a terminal T_{p3} .

As was previously described, the percussive signal PES ceases to be produced in the key assigner when the decay signal DIS is produced. Accordingly, as the decay start pulse DIS is applied to the terminal T_{p3} , the percussive signal PES is no longer applied to the terminal T_{p2} . The AND circuit A_{86} therefore does not gate out the percussive clock CP_2 and, instead, a damping clock pulse CP_3 is applied through an AND circuit A_{87} to the adder AD_6 . Since this damping clock pulse CP_3 is of a higher frequency than the percussive clock pulse CP_2 , counting is performed at a higher speed. As a result, the waveshape read from the memory P_2M falls sharply after a key-off time D_1 as shown in FIG. 18a. When the counted value of the counter has reached 63, the output of the AND circuit A_{85} becomes 1 and the inverted signal 0 is applied to the AND circuit A_{87} . This causes the AND circuit A_{87} to stop its gating-out of the damping clock pulse CP_3 thereby stopping the counting operation.

The foregoing description has been made with respect to a case wherein the decay start signal DIS is applied upon release of the key before the counted value has reached 63. If the decay start signal DIS is applied after the counting has been completed, counting is no longer made and the waveshape read from the memory P_2M is as shown in FIG. 18b.

FIG. 19 shows one preferred example of the touch response counter TRC. The touch response counter comprises an adder AD_7 and a 12 word - 7 bit shift register SR_7 which perform a counting operation in the same manner as the above described counters. A touch response waveshape memory TRM stores a waveshape which attenuates from a high level H at an address 0 to a low level L at an address 63 as shown in FIG. 20a.

Assume that the counted value of the first channel is initially 0. The time during which the touch response signal TRS is applied is, as was previously described, the time difference between the opening of the break contact and the closing of the make contact (hereinafter

referred to as "touch time"). Accordingly, when the touch response signal TRS is applied to a terminal T_R , a touch response clock pulse TRP is applied to the adder AD_7 via an AND circuit A_{88} . Thus, counting is successively performed by the adder AD_7 and the shift register SR_7 . FIG. 20b shows relation between the touch time and counts of the touch response counter TRC. It will be apparent from this figure that the counts of the counter increase in proportion to the touch time. If, however, the touch time is so long that the counter counts 63, the output of an AND circuit A_{88} becomes 1 and this output 1 is inverted to 0 by an inverter I_{14} . Accordingly, the clock pulse TRP does not pass through the AND circuit A_{88} and counting is stopped. If the touch time is within a range of $0 - t_k$, the supply of clock pulse is stopped when the touch response signal ceases to be applied. Accordingly, the count in the counter TRC remains at a value corresponding to the touch time and an amplitude at a level corresponding to this count is read from the touch response waveshape memory TRM. This level varies with the length of the touch time. FIG. 20c illustrates the outputs of the memory ranging from a quick touch to a slow one. The output of the memory TRM is applied to the envelope memory EM to control the level of the envelope as a whole waveshape. As shown in FIG. 20d, the level of the envelope as a whole becomes low if the touch time is long and the level becomes high if the touch time is short.

Truncate Control Operation

According to the present electronic musical instrument, if a 13th key is depressed while all of the 12 notes are being reproduced, one of the 12 notes which has attenuated, i.e. decayed or fallen in level, to the furthest degree is detected and the reproduction of this detected note is stopped in order to reproduce the 13th note. This control operation is hereinafter called truncate control operation.

The truncate control operation can be effected if and when the following conditions are satisfied:

1. all of the 12 notes are being reproduced,
2. one of the notes is attenuating, and
3. the 13th key is depressed.

In order to examine whether condition (1) is satisfied or not, a new key data signal from the OR circuit OR_8 (FIG. 9) is applied through the OR circuit OR_9 to an all-busy memory ABM and stored therein. While all of the twelve notes are being played, all of the channels of the all-busy memory ABM are 1. An AND circuit A_{26} receives all of the bit outputs of the all-busy memory ABM and produces an all-busy signal ABU as its output. This signal ABU indicates that at least one of the channels is not busy when it is 0 and that all of the channels are busy when it is 1.

As to condition (2), the output DIS of the key-off memory KFM is applied to one of the inputs of an AND circuit A_{27} , for the key-off memory KFM stores 1 in either one of its channels corresponding to the channel which is in a key-off state. The AND circuit A_{27} receives at the other input terminal thereof the attack finish signal AFS from the envelope counter. When the signals DIS and AFS are both 1, this indicates that the sound of this channel is attenuating. In the event that the break contact is opened by depression of the key but closed by release of the key before the make contact is closed, the signal DIS is 1. In this case, how-

ever, the sound is not actually attenuating and this state should be distinguished from a state in which the sound is actually attenuating. For this reason, the signal AFS is applied to the AND circuit A₂₇.

When one of the channels is in decay, the output 1 of the AND circuit A₂₇ is applied to a decay memory DCM and stored therein. The storage of 1 in either one of the channels of the decay memory DCM causes an OR circuit OR₁₀ to produce an output 1, thereby enabling detection of the condition (2). This output is hereinafter called "any decay signal".

An explanation will now be given regarding the detection of condition (3). When the thirteenth key is depressed, the key data signal KD₁ is applied to one of the inputs of the AND circuit A₂₁. In the meantime, the unblank signal applied to the other terminal of the AND circuit A₂₁ is 1 because the key data signal KD₁ applied to the AND circuit A₂₁ is a key data signal corresponding to a new key address code which is not stored in the key address memory. Accordingly, the AND circuit A₂₁ produces a new key data signal NKD₁. This signal NKD₁ is applied through an AND circuit A₂₈ to an AND circuit A₂₉. This output represents the depression of the thirteenth key.

When conditions (1), (2) and (3) are all satisfied in the foregoing manner, all of the inputs to the AND circuit A₂₉ become 1 and thereby cause the AND circuit A₂₉ to produce an output 1 which is applied to a flip-flop FF₁ to set it. The set output of the flip-flop FF₁ is provided to a terminal t₅ via an AND circuit A₃₀ as a signal TCS for starting the operation of the truncate counter connected to the terminal t₅. In the truncate counter shown as the circuit portion b in FIG. 13, counting contents of each channel of the envelope counter are sequentially transmitted to each channel of a 12 word - 7 bit shift register SR and stored therein. When the above described signal TCS is applied to a terminal t₆, AND gates AK₁ - AK₇ are closed and AND gates AK₈ - AK₁₄ are opened thereby forming a feed back loop. Accordingly, the truncate counter is separated from the envelope counter and the counting in each channel is accelerated by applying a high rate clock pulse CL through AND circuit A_k to the adder AD.

If the note of a certain channel has attenuated to the furthest degree, the corresponding channel of the truncate counter produces a carry signal CAR.

This signal 1 is stored in a corresponding channel of an overflow memory OVM in the key assigner 3. This memory OVM consists of a 12 word - 1 bit shift register and the output from the last stage of the shift register is fed back to the input thereof. When the signal 1 is stored in any channel of the overflow memory OVM, the output from an OR circuit OR₁₁ becomes 1 because the OR circuit OR₁₁ receives all the bit outputs of the overflow memory OVM. This output 1 of the OR circuit OR₁₁ is a signal indicating that a carry, i.e. overflow, is produced in either one of the channels of the truncate counter and hereinafter is called "any overflow signal." This any overflow signal is inverted by an inverter I₇ and applied to an AND circuit A₃₀. This causes the AND circuit A₃₀ to produce an output 0 and thereby stops the accelerated counting operation of the truncate counter TC.

When the signal 1 is produced from the overflow memory OVM, this signal is applied to one of the inputs of an AND circuit A₃₂. If the new key data signal NKD₁

described above is applied to the other input of the AND circuit A₃₂ at this time, the AND circuit A₃₂ produces a truncate signal TRN. This signal is applied to the key address code memory KAM and the busy memory BUM via the OR circuit OR₁₂ and clears the contents of the corresponding channels in these memories. The truncate signal TRN is also applied to the key-on memory KOM, the key-off memory KFM and the decay memory DCM via the OR circuit OR₁₃ and clears the contents of the corresponding channels of these memories. Further, the truncate signal TRN is applied to the overflow memory OVM via the OR circuit OR₁₄ and clears the contents of the corresponding channel of this memory. Thus, the sounding of this channel is stopped and the new 13th note starts to be played upon storage of the information corresponding to the 13th note.

When the all-busy signal ABU is reset to 0, a reversed signal is applied to the overflow memory OVM through the OR circuit OR₁₄ and clears this memory OVM.

Pedal Monophonic System

A pedal tone is in most cases used for a monophonic performance and two or more pedal tones are very seldom reproduced simultaneously. It is, therefore, desirable that only one pedal tone should be reproduced when a pedal key is depressed. If, however, all of the channels are used for manual tones as has previously been described, a pedal tone cannot be reproduced when desired. In the present electronic musical instrument, one channel is always reserved for a pedal tone so that pedal tone may be reproduced whenever a pedal key is depressed.

More specifically, the instrument is constructed in such a manner that information concerning pedal tones is received in the first channel whereas information concerning tones other than the pedal tones is received in the second to 12th channels and never in the first channel.

Referring to FIG. 9, a pedal channel designation switch PSW is closed for using the first channel exclusively for pedal tones. As the switch PSW is closed, a signal ASS which is 1 is applied to AND circuits A₃₄ and A₃₅. The AND circuit A₃₄ also receives key address codes K₂ and K₁ from the key address codes KA provided by the delay flip-flop DF₄. When both of key address codes K₂ and K₁ are 1, this represents scanning of the pedal keyboard as has already been described with respect to the key data signal generator. Accordingly, the key data signal applied to the key assigner when a signal PSC from the AND circuit A₃₄ is 1 is identified to be the one for the pedal key. The AND circuit A₃₅ also receives the clock pulse ϕ_2 . This clock pulse ϕ_2 synchronizes with the first channel. Accordingly, when the output PCH is 1, the storage device, memories and counters are synchronized at the time corresponding to the first channel, i.e. the channel for the pedal keys.

1. Distinction of the new key-on signal

The new key-on signal is divided into a new key-on signal for the pedal keys and a new key-on signal for the manual keys. When each of the pedal channel signal PCH, pedal scanning signal PSC, new key data signal NKD₁ and the signal A₇S obtained by inverting the busy signal which are applied to an AND circuit A₃₆ is 1, that is, when it is the time for the first channel, the pedal keyboard is being scanned, a new key data signal is

being applied and the first channel is not busy, the new key-on signal for the pedal keys is produced from the AND circuit A_{36} . It is to be noted that the new key data signal applied to the AND circuit A_{36} corresponds to the pedal keys when it is 1. Accordingly, if all of the above described conditions are satisfied, the new key-on signal for the pedal keys produced from the AND circuit A_{36} is applied to the key address code memory KAM and a corresponding key address code is stored in the first channel of the key address code memory KAM. Simultaneously, a signal 1 is stored in the first channel of the busy memory BUM. During the time corresponding to the second to twelfth channels, the pedal channel signal PCH is 0, so that no new key-on signal for the pedal keys is produced from the AND circuit A_{36} . Consequently, no key address code for the pedal keys is stored in the second to 12th channels of the key address code memory KAM.

On the other hand, a signal $\overline{PCH}$ obtained by inverting the pedal channel signal PCH, a signal $\overline{PSC}$ obtained by inverting the pedal scanning signal PSC, the new key data signal NKD₁, and the signal $\overline{A_1S}$ obtained by inverting the busy signal are applied to the AND circuit A_{22} . When these input signals are all 1, i.e. when it is not the time for the first channel, the pedal keyboard is not being scanned, the new key data signal is being applied and at least one of the second to 12th channels are not busy, the new key-on signal for the manual keys is produced from the AND circuit A_{22} . The New key data signal applied to the AND circuit A_{22} corresponds to the manual keys when the signal $\overline{PSC}$ is 1. Accordingly, when the above described conditions are satisfied, the new key-on signal for the manual keys is produced from the AND circuit A_{22} and applied to the key address code memory KAM. Thus, a corresponding key address code is stored in one of the second to twelfth channels of the key address code memory KAM and a signal 1 is stored in a corresponding channel of the busy memory BUM. During the time corresponding to the first channel, the signal $\overline{PCH}$ is 0, so that no new key-on signal for the manual keys is produced from the AND circuit A_{22} . Consequently, no key address code for the manual keys is stored in the first channel of the memory KAM during this time.

2. Truncate control operation

According to the present invention, when a new manual key is depressed while eleven manual tones are being reproduced the reproduction of the manual tone which has attenuated to the furthest degree is cut short and a reproduction of the new manual tone is started. This is the truncate operation for the manual keys. As to the pedal tones, no two or more pedal tones are reproduced at the same time. Accordingly when a new pedal key is depressed while another pedal tone is reproduced, the old pedal tone is cancelled and the new pedal tone is played only if the old pedal tone is attenuating.

The truncate operation for the manual tones will first be described. Detection of an all-busy state for this purpose is related to detection of sounding of tones in the second to 12th channels. However, the AND circuit A_{28} receives outputs of all stages of the all-busy memory ABM and, accordingly, an all-busy state is not detected if a pedal tone is not being reproduced. The memory ABM is therefore constructed to store 1 in its first channel regardless of the reproduction of a pedal

tone. This is done by causing the pedal channel signal PCH to be stored in the first channel of the memory ABM via the OR circuit OR_9 when the signal PCH is 1.

The AND circuit A_{29} receives at one of its inputs new key data signals concerning manual tones only. This is made possible by constructing the circuit so that the AND circuit A_{28} receives a new key data signal from the AND circuit A_{21} at one of its inputs and the signal $\overline{PSC}$ at the other input thereof. If the new key data signal is one for a pedal tone, the AND circuit A_{28} does not pass it, whereas if the new key data signal is one for a manual tone, it is gated out of the AND circuit A_{28} and applied to the AND circuit A_{29} .

The decay memory DCM is constructed not to store a signal 1 which represents a decaying state in its first channel when a decaying tone is a pedal tone. More specifically, since the signal PCH is applied to one of the inputs of the AND circuit A_{27} , a signal 1 is not stored in the first channel of the decay memory DCM even when the pedal tone is decaying and the signals DIS and AFS are respectively 1. Accordingly, it is only when one of the manual tones is decaying that a signal 1 is produced from the OR circuit OR_{10} .

If the pedal tone is extremely attenuated when the truncate counter TC is brought into operation, a carry signal CAR is produced from the first channel of the counter. An arrangement has been made, however, to prevent the carry signal from entering the first channel of the overflow memory OVM, for this carry signal CAR is irrelevant to the truncate operation for the manual tones. For this purpose, the signal $\overline{PCH}$ is applied to one of the inputs of the AND circuit A_{31} . Since the signal $\overline{PCH}$ is 0, the AND circuit A_{31} does not pass the carry signal CAR of the first channel and the first channel of the overflow memory OVM always remains in a 0 state. Accordingly, an output 1 from the OR circuit OR_{11} represents production of a carry signal CAR from either one of the second to 12th channels of the truncate counter TC. This output 1 causes the truncate counter TC to stop its truncate operation with respect to the manual tones only.

The AND circuit A_{32} receives the new key data signal NKD₁ and the signal PSC besides the overflow signal OVF from the overflow memory OVM. Consequently, the AND circuit A_{32} does not gate out a clear signal even when the overflow signal OVF is applied from the overflow memory OVM unless the manual key data signal is applied to the AND circuit A_{32} .

When the clear signal is provided through the OR circuit OR_{12} , the key address code memory KAM and the other memories are cleared with respect to their channel in which the overflow output is produced and reproduction of the new manual tone is started upon application of the new manual key data signal.

Next to be described is the truncate operation for the pedal tones. When the signals AFS, D₁S and PCH are 1 respectively, decay of a pedal tone is detected. Again, when the new key data signal NKD₁ and the signal PSC are 1, this indicates that the new key data signal for the pedal tone has been applied. When, accordingly, all of the inputs to the AND circuit A_{37} are 1, a pedal tone clear signal is produced from the AND circuit A_{37} and applied through the OR circuit OR_{12} to the key address code memory KAM and the other memories to clear these memories with respect to their first channel. Thus, preparation for reproduction of the new pedal

tone upon application of the new pedal key data signal is completed.

Operations in Event a Key is Insufficiently Depressed or the Same Key is Depressed Twice

According to the invention, in the event a break contact of a key is opened by depression of the key but it is closed upon release of the key before the corresponding make contact is closed because the depression of the key is insufficient, the musical tone corresponding to the depressed key is not reproduced but the information stored therefor in the key assigner is cleared at the time when the break contact is closed. When the break contact is opened, a key address code corresponding to the key is stored in the key address code memory KAM and a signal 1 is stored in the busy memory BUM, as previously described. Then, the closing of the break contact causes the key-off signal 1 to be stored in the key-off memory KFM. In this case, however, no signal A_2S is produced because the make contact remains open and, accordingly, the musical tone is not reproduced. When the signal DIS is produced from the key-off memory KFM, both of the input signals DIS and $\overline{A_2S}$ of the AND circuit A_{38} become 1. The AND circuit A_{38} therefore produces an output 1 which is applied to the key address code memory KAM and the other memories through the OR circuit OR_{12} to clear these memories.

According to the invention, if a tone corresponding to a certain key is being reproduced and the same key is depressed again, the old tone is cancelled and reproduction of the same tone is restarted only if the old tone is decaying. The AND circuit A_{25} receives the key data signal KD_1 and the coincidence signal EQ and when both of these signals are 1, i.e., the key data signal corresponding to the key address code stored in the key address code memory KAM is applied thereto, the AND circuit A_{25} produces a key-on signal KOS which is applied to one of the inputs of an AND circuit A_{39} . The decay signal DIS indicating that the reproduced tone has started to decay and the attack finish signal AFS are applied to the rest of the inputs of the AND circuit A_{39} .

Accordingly, the AND circuit A_{39} produces an output 1 when the reproduced tone is decaying. This output 1 is applied to the key-on memory KOM, key-off memory KFM, decay memory DCM and overflow memory OVM through the OR circuit OR_{13} to clear these memories. It is to be noted that the key address code KAM memory and the busy memory BUM are not cleared because these memories are used to reproduce the same tone again.

An AND circuit A_{40} is connected to each of the memories of the key assigner via the OR circuit OR_{12} so as to clear these memories upon completion of reading of the waveshapes therefrom by application to the inputs of the AND circuit A_{40} of the count finish signals $Df_1 - Df_6$ ($Df_4 - Df_6$ are signals produced in case three additional envelope counters are provided) which indicate that the counting in the respective envelope counters (percussive counters) has finished. The output of the AND circuit A_{40} is also used as a clear signal CC to clear the respective counters. The other input IC to the OR circuit OR_{12} is an input for resetting the respective memories and counters to their initial condition upon turning-on of the power.

The foregoing description of the operations of the respective counters has been made with respect to the first channel only. It will be understood, however, that with respect to the other channels also a similar counting operation is performed and the waveshapes of the respective memories are read out.

FIG. 21 shows an example of a clock pulse selector provided for generating clock pulses to be applied to the respective counters and selecting and providing a clock pulse having a frequency corresponding to the kind of the keyboard. Only one selector is illustrated in the figure but a plurality of such selectors may of course be provided if desired.

Input terminals Ta - Td of the clock pulse selector respectively receive signals of a sinusoidal wave at frequencies respectively selected for the solo keyboard S, the upper keyboard U, the lower keyboard L and the pedal keyboard P. The terminal Ta for the solo keyboard S is connected to a terminal D of a delay flip-flop DF_{13} . The output of the delay flip-flop DF_{13} is connected to a terminal D of a delay flip-flop DF_{14} and also to one of input terminals of an AND circuit A_{90} . The output of the delay flip-flop DF_{14} is connected to the other input terminal of the AND circuit A_{90} . The key clock pulse ϕ_2 is applied to each of flip-flops $DF_{13} - DF_{20}$. A circuit of the same construction as the one described above is provided for each of the other keyboards. The key address code signal K_1 from the key address code memory KAM of the key assigner is applied to a terminal Te and the key address code signal K_2 from the memory KAM to a terminal Tf. The signal K_1 is applied directly to inputs of an AND circuit A_{92} and A_{93} . A signal $\overline{K_1}$ which is obtained by inverting the signal K_1 through an inverter I_{17} is applied to the AND circuit A_{90} and A_{91} . The signal K_2 is applied directly to the AND circuits A_{91} and A_{93} , whereas a signal $\overline{K_2}$ which is obtained by inverting the signal K_2 through an inverter I_{16} is applied to the AND circuits A_{90} and A_{92} .

Operation of the clock pulse selector will now be described with respect to the solo keyboard on the assumption that the signals K_2 and K_1 are both 0.

FIG. 22a shows the key clock pulse ϕ_2 . When a signal such as shown in FIG. 22b is applied to the terminal Ta, the output of the delay flip-flop DF_{13} becomes a rectangular wave signal as shown in FIG. 22c. This signal thereafter is applied to the delay flip-flop DF_{14} and delayed for one key time (FIG. 22d) and inverted in its polarity (FIG. 22e) through this flip-flop DF_{14} . Accordingly, the signals shown in FIG. 22c and e are applied to the AND circuit A_{90} . Since the signals K_2 and K_1 are both 0, and AND circuit A_{90} receives signals $\overline{K_1} = 1$ and $\overline{K_2} = 1$ and, consequently, produces as its output a clock pulse having a pulse width of 1 key time and the same frequency as the input signal as shown in FIG. 22f.

With regard to the other keyboards, a similar operation is performed and a clock pulse is produced from an AND circuit corresponding to the signals K_1 and K_2 .

Each of these clock pulses is applied through the OR circuit OR_{32} to a corresponding one of the previously described envelope counters as a clock input so that a predetermined speed of a ttrack, decay or percussive operation which differs with the keyboards may be selected.

In the embodiment described above, a musical tone waveshape obtained is one of a single pitch for a desired note. The present electronic musical instrument

may, however, be so constructed that it may simultaneously produce a plurality of musical tone waveshapes having pitches which are slightly different from one another for one desired note. The instrument may also be constructed so that one not may have a plurality of pitches which differ from one another dependent upon the keyboard or the key group.

FIG. 23 is a block diagram showing one example of a musical tone waveshape generator capable of simultaneously generating a plurality of musical tone waveshapes of pitches which are slightly different from one another for a single predetermined note so as to produce a compound sound effect. This waveshape generator is different from the waveshape generator shown in FIG. 1 in that it is provided with a plurality of frequency information memories (e.g. 4a, 4b) and also a plurality of counters and waveshape memories corresponding to these frequency information memories. The frequency information memories 4a and 4b respectively store frequency data which are slightly different from each other for one and the same key address code. Frequency counters 5a₁ - 5c₁, 5a₂ - 5c₂ which are of the same construction as the frequency counters 5a - 5c shown in FIG. 1 cumulatively add the frequency data. Musical tone waveshape memories 6a₁ - 6c₁, 6a₂ - 6c₂ respectively store, like the musical tone waveshape memories 6a - 6c shown in FIG. 1, waveshapes for one cycle of a musical tone to be reproduced.

When a key address code corresponding to a depressed key is applied to the frequency information memories 4a and 4b, the frequency counters 5a₁ - 5c₁ receive frequency information which is slightly different from that given to the frequency counters 5a₂ - 5c₂. Accordingly, as cumulative counting in the respective series of counters proceeds, an integer output from the counter 5c₂ becomes a value which is slightly different from that of an integer output from the counter 5c₁, resulting in the occurrence of a difference in the addresses obtained for reading waveshapes from the musical tone waveshape memories 6a₂ - 6c₂. Thus, musical tone waveshapes which are slightly different in pitch from each other are simultaneously produced from the waveshape memories 6a₁ - 6c₁ and 6a₂ - 6c₂ for one and the same note. The musical tone waveshapes thus produced are simultaneously reproduced through suitable means and a natural and rich musical tone thereby is obtained.

FIG. 24 shows an example of a musical tone waveshape generator capable of producing a compound sound effect from all of the keyboards. In this waveshape generator, a keyboard circuit 1, a key data generator 2 and a key assigner 3 are of the same construction as the corresponding component parts shown in FIG. 1 so that the keyboard 1 and the key data generator 2 are not shown in the figure.

As in the example of FIG. 23, the key address code generated in the key assigner 3 is supplied to a plurality of frequency information memories. Since the example of FIG. 24 is designed to produce a compound sound effect from the respective keyboards, the key address code is supplied to frequency information memories corresponding in number to the keyboards provided in the instrument.

A frequency information memory 7a corresponds to the solo keyboard, a memory 7b to the upper keyboard, a memory 7c to the lower keyboard and a memory 7d to the pedal keyboard. Accordingly, the key address

code is divided into four systems and applied to the memories 7a - 7d for reading corresponding waveshapes from these memories. The frequency data stored according to the memories 7a - 7d is composed in substantially the same principle as was described with respect to the frequency information memory 4a.

It is to be noted, however, that the frequency information memories 7a - 7d store frequency data which are not the same but slightly different from one another for one and the same key address code.

In this musical tone waveshape generator, the codes K₁, K₂ which represent the kind of keyboard in the key address code applied to the frequency information memories 7a - 7d are used as instruction signals for selectively operating these memories 7a - 7d. More specifically, frequency information is read from the memory 7a when the codes K₂, K₁ are 00, from the memory 7b when the codes K₂, K₁ are 01, from the memory 7c when the codes K₂, K₁ are 10, and from the memory 7d when the codes K₂, K₁ are 11 respectively.

If the keys for the note C₃ in the respective keyboards are simultaneously depressed, key address codes representing these key are produced in a time-sharing manner in the key assigner 3. Thus key address codes are applied to the corresponding memories 7a - 7d for reading of the frequency information for the note C₃ of the respective keyboards. The frequency data stored in these memories are slightly different from one another for one and the same note. The frequency information is applied digit by digit to OR circuit OR₁₁ - OR₂₅ (The first digit to the OR circuit OR₁₁, the second digit to the OR circuit OR₁₂ and so on). The first digit to the seventh digit of the frequency information (the outputs of the OR circuits OR₁₁ - OR₁₇) are applied to a decimal counter 8a, the eighth digit to the 14 digit (the outputs of the OR circuit OR₁₈ - OR₂₄) to a decimal counter 8b and the 15 digit (the output of the OR circuit OR₂₅) to an integer counter 8c. The frequency counters 8a - 8c and musical tone waveshape memories 9a - 9c connected to the counter 8c operate in the same manner as the frequency counters 5a₁ - 5c₁ and the musical tone waveshape memories 6a₁ - 6c₁ shown in FIG. 6.

Thus, the musical tone waveshapes of the note C₃ in the respective keyboards are respectively read in a time-sharing manner from the waveshape memories 9a - 9c.

Since the frequency information of the note C₃ slightly differs for the respective keyboards, the integer outputs of the counter 8c vary according to the kind of keyboard as the cumulative counting in the counters 8a - 8c proceed. Accordingly, the addresses for reading waveshapes from the waveshape memories 9a - 9c also vary.

It will be understood from the foregoing explanation that musical tone waveshapes having pitches which are slightly different from one another are produced for the respective keyboards notwithstanding the fact that one and the same note is played in each keyboard. For convenience of explanation, the foregoing description has been made with respect to a case wherein the keys of the same note are simultaneously played in the respective keyboards. In an actual musical performance, this seldom happens and, instead, the keys of the same note are played at different times. It will be appreciated, however, that even in this case the musical tone waveshapes having pitches which are slightly different from one another are produced for the respective keyboards.

This invention will prove very effective when, for example, a melody is played on the solo keyboard and a chord on the upper keyboard simultaneously. If one key is depressed on the solo keyboard and another key of the same note is depressed on the upper keyboard, the melody tone of the solo keyboard and the chord tone of the upper keyboard are reproduced as two tones having pitches which are subtly different from each other. Again, in case a key for the note C₃ is depressed on the solo keyboard and a key for the note C₄ on the upper keyboard, the two tones are reproduced not as tones which are in a precise octave relation but as tones which are in a pitch relation which is slightly deviated from one octave. Thus, an accurate simulation to a natural musical sound can be produced from the present electronic musical instrument.

In the above described embodiment of FIG. 24, the special musical tone waveshape generating system for producing a compound sound effect is provided in all of the keyboards. It will be apparent to persons skilled in the art to provide such waveshape generating system in a specific keyboard only to produce a similar effect in this specific keyboard.

FIG. 25 shows one example of a the waveshape generating system for producing a compound sound effect. This example comprises one frequency information memory and two waveshape generating systems which produce musical tone waveshapes in accordance with frequency information applied to these systems. In one of the waveshape generating systems, frequency information is directly applied to frequency counters 5a₁ - 5c₁ as in the device shown in FIG. 1. to read waveshapes from musical tone waveshape memories 6a₁ - 6c₁ In the other system, an adder 10 is provided for slightly changing the frequency information provided by the frequency information memory 4. The modified frequency information is cumulatively added in frequency counters 5a₂ - 5c₂ in the same manner as in the counters 5a₁ - 5c₁ for reading waveshapes from musical tone waveshape memories 6a₂ - 6c₂. Thus, waveshapes having frequencies which are slightly different from those of the waveshapes read from the memories 6a₁ - 6c₁ are read from the memories 6a₂ - 6c₂. The adder 10 receives the frequency information from the frequency information memory 4. The adder 10 also receives at several of its less significant digits a digit inputs signal $\Delta A = \text{frequency information} \times 2^{-n}$ which is obtained by shifting the frequency information by *n* digits toward the less significant digits. Therefore, the frequency information produced from the adder 10 is of a value which is slightly different from the frequency information output from the memory 4.

Taking the note of C₃ as an example, the operation of the adder 10 will be described in detail. The adder 10 receives frequency information 000011010110010 counted from the most significant digit and information which is obtained by shifting this frequency information by 9 digits. Accordingly, a modified frequency information from the adder 10 becomes 000011010110101. By applying this output of the adder 10 to the fraction counters 5a₂ and 5b₂ and the integer counter 5c₂ which are of the same construction as the counters shown in FIG. 1, musical tone waveshapes having frequencies which are slightly different from those of the waveshapes of the memories 6a₁ - 6c₁ are read from the memories 6a₂ - 6c₂. If the frequency of the waveshape produced, for example from the

memory 6a₁ is represented as *f*₁ and the frequency of the waveshape produced from the memory 6a₂ as *f*₂, frequencies of these exemplary notes are as shown in the following Table II.

Table II

	<i>f</i> ₁	<i>f</i> ₂
	Hz	Hz
C ₇	2093	2113.93
A ₄	440	444.40
C ₂	65	65.65

If a key for the note C₇ is depressed, a musical tone waveshape at a frequency of 2093 Hz and a musical tone waveshape at a frequency of 2113.93 Hz are simultaneously produced. It will be noted that since percentage of the deviation in frequency is constant, a sufficient compound sound effect is produced.

FIG. 26 shows another example of a musical tone waveshape generating device. This example is different from the foregoing example in that constant frequency data is added to the frequency information in the adder 10. More specifically, the adder 10 receives as one of its inputs the frequency information from a frequency information memory 4 and, as the other input, a constant digital signal *K* (e.g. *K* = 011) at several of its less significant digit inputs, thereby producing slightly modified frequency information upon adding these two inputs.

The modified frequency information is applied, as in the device shown in FIG. 1, to a frequency counter 5B comprising fraction counters and an integer counter and a musical tone waveshape having a frequency which is slightly different from that of a waveshape read from a waveshape memory 6A is read from a memory 6B. A frequency counter 5A is of the same construction as the counter 5B.

Table III shows frequencies of three notes obtained according to this example.

Table III

	<i>f</i> ₁	<i>f</i> ₂
	Hz	Hz
C ₇	2093	2093.8
A ₄	440	440.8
C ₂	62	65.8

It will be noted from the foregoing description of FIG. 26 that by virtue of the provision of this device, a plurality of musical tones having pitches which are slightly different from one another are produced upon depression of a desired key. Thus, the present electronic musical instrument is capable of producing a rich compound sound effect which gives to audience an impression of the expounded of sound which would be produced by a simultaneous performance of a plurality of musical instruments.

What is claimed is:

1. An electronic musical instrument comprising a key data signal generator which produces, in response to depression and release of a key, a key data signal corresponding to said key in a given key time period of a cyclically repeating plurality of key time periods, a key assigner including means which produce, upon receipt of said key data signal, a key address code corresponding to said key and means which concomitantly pro-

duce control signals indicating the depression and release of said key during said given key time period with respect to each of a number of channels which are portions of said time period shared by a maximum number of tones to be reproduced simultaneously, a musical tone waveshape generator means which produce a musical tone waveshape corresponding to the key address code produced from said key assigner, envelope waveshape generator means which produce an envelope waveshape upon receipt of the control signals from said key assigner and means for imparting said envelope waveshape to said musical tone waveshape, said key assigner, musical tone waveshape generating means and envelope waveshape generator means including shift registers having a number of stages corresponding to said number of channels for time-sharing processing of information in said channels and being driven in synchronization with each other.

2. An electronic musical instrument as defined in claim 1 wherein said key data signal generator produces a first key data signal in response to the opening of a break contact of the depressed key and a second key data signal in response to the closing of a make contact of the depressed key, and wherein said key assigner further comprises means for producing a touch response signal indicating the elapsed time between opening of the break contact and closing of the make contact in response to said first and second key data signals, means for producing an output at a level dependent upon said elapsed time in response to said touch response signal and means for multiplying said level output with said envelope waveshape, whereby a musical tone waveshape accompanied by an envelope at a level corresponding to the touch time of the key is obtained.

3. An electronic musical instrument as defined in claim 2 wherein said means for producing an output at a level dependent upon said elapsed time comprises a touch response memory storing a waveshape which falls from a first level to a second level and sustains this second level thereafter and a counter which is connected to said touch response memory and which counts a clock pulse upon receipt of said touch response signal and reads said waveshape from said touch response memory by the counting output thereof.

4. An electronic musical instrument as defined in claim 1 wherein said key data signal generator comprises a key address code generator which receives as its input a clock pulse from a clock oscillator and produces a key address code consisting of a note code representing a note in a block of notes, a block code representing said block of notes and a keyboard code representing a keyboard having the key corresponding to said note, a first decoder which produces, upon receipt of said note code, its output sequentially on a plurality of output lines, a second decoder which produces, upon receipt of said block code and said keyboard code, its output sequentially on a plurality of output lines, a respective key switch operable by each key of said keyboard and having a make contact, the make contacts of the key switches for the keys corresponding to notes in each block of notes being connected in common to a respective AND circuit having two, the output of said first decoder to one of the inputs of said AND circuit of the block to which the depressed key belongs through the make contact provide for the key switch of said block when a key address code corresponding to

the key is produced from said key address code generator and, the output of said second decoder the other input of said AND circuit so as to produce an output from said AND circuit, whereby a key data signal representing in time relation the closing of the make contact of the depressed key is produced.

5. An electronic musical instrument as defined in claim 4 wherein said key switches further comprise respective break contacts, the break contacts of the key switches for the keys corresponding to notes in each block of notes being connected in common by respective common break contact members, a plurality of AND circuits each having two input terminals each and circuit being provided for one of the blocks of the key switch with one input terminal thereof being connected to the common break contact member of its corresponding key switch and the other input terminal thereof being connected to its corresponding output line of said second decoder, means for producing an output of a logical state O from one of said AND circuits corresponding to the common break contact member to which the key switch of the depressed key belongs by interrupting the output from said first decoder upon opening of the break contact corresponding to the depressed key when a key address code corresponding to the depressed key is produced from said key address code generator and an inverter for inverting the output of a logical state O, whereby a key data signal representing in time relation the opening of the break contact corresponding to the depressed key is produced.

6. An electronic musical instrument as defined in claim 4 wherein said key data signal generator further comprises a delay circuit for delaying the key data signal for one key scanning time and an OR circuit which receives the key data signal and the output of said delay circuit, whereby a key data signal free from a chattering effect of the key switches is produced.

7. An electronic musical instrument as defined in claim 1 wherein said key assigner comprises a key address code memory which stores key address codes in channels of a number equal to a maximum number of tones to be reproduced simultaneously, a key address code generator for successively producing key address codes corresponding to the respective keys, first detection means for examining whether there is coincidence of the key address code produced from said key address code generator with the key address code already stored in said key address memory, second detection means for examining whether there is an unused channel in the channels of said key address code memory, a memory for storing the detection output of said second detection means, a logical circuit which, upon receipt of the key data signal, produces a new key data signal when no key address code corresponding to the key data signal is stored in said key address code memory and produces a new key-on signal from said new key data signal only when there is an unused channel in the channels of said key address code memory, and gating means controlled by the new key-on-signal for causing the key address code from said key address code generator to be stored in the unused channel of said key address code memory.

8. An electronic musical instrument as defined in claim 7 wherein said key assigner means further comprises a first delay circuit for delaying the key data signal from said key data signal generator for one said

given key time period before it is applied to said logical circuit and a second delay circuit for delaying the key address code from said key address code generator for one said given key time period before it is applied to the gate of said key address code memory, said first detection means examining whether the same key address code as the one corresponding to said key data signal has already been stored in said key address code memory during the one key time period during which the key data signal is produced from said key data signal generator and said second detection means examining whether there is an unused channel during the next one key time period during which the delayed key data signal is applied to said key address code memory.

9. An electronic musical instrument as defined in claim 7 wherein said key assigner further comprises means for applying a key data signal indicating opening of the break contact to said logical circuit, means for producing a key-on signal upon receipt of the key data signal indicating closing of the make contact when the key address code corresponding to this key data signal is stored in said key address code memory by the key data signal indicating opening of the break contact, a key-on memory for storing this key-on signal and a logical circuit for producing a touch response signal having a duration which is equal to the interval between the opening of the break contact and the closing of the make contact in response to the outputs of said busy memory and said key-on memory.

10. An electronic musical instrument as defined in Claim 7 wherein said key assigner further comprises means for producing a key-off signal when the depressed key is released, a key-off memory for storing the key-off signal, means for detecting a state in which key address codes are stored in all of the channels of said key address code memory and producing an all-busy signal when said state is detected, means for producing, upon receipt of the key data signal relating to the make contact, a key-on signal when the key address code corresponding to this key data signal is stored in said key address code memory, a key-on memory for storing said key-on signal, a decay memory for storing a decay signal indicating a state of decay upon receipt of the key-off signal and an attack finish signal indicating completion of reading of an attack waveshape from an envelope counter which starts counting in response to the key-on signal from said key-on memory, means for detecting storage of the decay signal in any channel of said decay memory and producing an any decay signal when said storage is detected, a logical circuit for producing a truncate counter counting start signal which causes a truncate counter provided for said envelope counters to start counting upon receipt of the all-busy signal, the any decay signal and the new key data signal, means for storing a carry signal from said truncate counter indicating overflow of the computer and producing an any overflow signal upon detection of storage of the carry signal in any channel of said carry signal storing means and means for clearing contents stored in said channel of the key address code memory and the other said memories in response to said any overflow signal.

11. An electronic musical instrument as defined in claim 7 wherein said key assigner further comprises means for producing a pedal scanning signal when the key address code relates to the pedal keyboard and means for producing a pedal channel signal represent-

ing a specific channel assigned for the pedal keyboard, said key address code memory being caused to store the key address code relating to the pedal keyboard in said specific channel upon receipt of the pedal scanning signal and the pedal channel signal while storing key address codes relating to the manual keyboards in the channels other than said specific channel.

12. An electronic musical instrument as defined in claim 1 wherein each of said musical tone waveshape generator means comprises a frequency information memory which stores frequency data respectively corresponding to the notes of the keys and, upon receipt of the key address code corresponding to the depressed key from said key assigner means, produces frequency data corresponding to said key address code, counters which receive said frequency data and cumulatively count the same and musical tone waveshape memories which store musical tone waveshapes and have these waveshapes read out by the output of said counters.

13. An electronic musical instrument as defined in claim 12 wherein said frequency information memory comprises a read only memory having an access time of the order of 1 microsecond.

14. An electronic musical instrument as defined in claim 12 which further comprises at least one additional frequency information memory producing modified frequency data which is slightly different for each note from that of the first mentioned frequency information memory, counters provided for said additional frequency information memory for cumulatively counting the modified frequency data and musical tone waveshape memories which store musical tone waveshapes and have these waveshapes read out by the output of said counters, whereby at least two musical tones having frequencies which are slightly different from each other are simultaneously produced upon depression of a single key.

15. An electronic musical instrument as defined in claim 14 wherein said additional frequency information memory is an adder which adds together a digital data output from said first mentioned frequency information memory and information digital data obtained by shifting said first mentioned toward digital data output toward less significant digits thereof.

16. An electronic musical instrument as defined in claim 14 wherein said additional frequency information memory is an adder which adds together said frequency information and a digital signal representing a constant frequency value.

17. An electronic musical instrument as defined in claim 1 wherein said musical tone waveshape generator means comprises frequency information memories each being provided for respective keyboards and storing frequency information with respect to the corresponding keyboard which is approximately the same as the frequency information for the other keyboards for one and the same note, means for selectively operating these frequency information memories in accordance with the keyboard to which the depressed key belongs, counters provided on the output side of the respective frequency information memories and cumulatively counting the read out frequency information and musical tone waveshape memories storing musical tone waveshapes and have these waveshapes read out by the output of said counters, whereby musical tones having pitches which correspond to the respective keyboards

and are slightly different from one another for said one and the same note are obtained.

18. An electronic musical instrument as defined in claim 12 wherein said frequency information memory comprises memory means for holding the key address code from said key address code memory in storage for a period of time which is at least one channel period longer than said given key time period, a read only memory having an access time greater than 1 microsecond for reading frequency information corresponding to the notes of the respective keys and producing, upon receipt of the key address code from said memory means, frequency information corresponding to said key address code, and means for obtaining and storing the frequency information from said read only memory at a time which is one key time after application of the key address code to said memory means and outputting this key address code one key time later.

19. An electronic musical instrument as defined in claim 12 wherein said musical tone waveshape generator means further comprises logical circuitry for preventing the first digit output among the outputs of said counters from being applied to said waveshape memory when an integer output of frequency information is produced from said frequency information memory, whereby the sampling frequency of said musical tone waveshape memory is reduced to $\frac{1}{2}$.

20. An electronic musical instrument as defined in claim 1 wherein each of said envelope waveshape generator means comprises an envelope counter for counting a predetermined clock pulse in response to a control signal fed from the key assigner and an envelope memory storing a predetermined envelope waveshape and having this envelope waveshape read out by the counting output from said envelope counter.

21. An electronic musical instrument as defined in claim 20 wherein said envelope counter comprises means which, upon receipt of a first control signal representing depression of a key from said key assigner, provides an attack clock pulse to said envelope counter until the count in said counter has reached a predetermined value and means which, upon receipt of a second control signal representing release of the key from said key assigner, provides a decay clock pulse to said counter until to said counter when the count in said

counter has reached a final value, whereby an envelope waveshape which rises after lapse of a predetermined period of time from the time when the key is depressed, sustains a constant amplitude thereafter, and falls from the time when the key is released.

22. An electronic musical instrument as defined in claim 20 wherein said envelope memory stores a waveshape which rises instantaneously and decays gradually thereafter and said envelope counter successively counts the predetermined clock pulse upon receipt of said first control signal to read the waveshape from said envelope memory, the counting being stopped upon completion of the reading of said memory.

23. An electronic musical instrument as defined in claim 20 wherein said envelope memory stores a waveshape which rises instantaneously and decays gradually thereafter and said envelope counter means counts a first clock pulse upon receipt of a first control signal until a second control signal is applied thereto and counts, upon receipt of said second control signal, a second clock pulse having a higher frequency than said first clock pulse, whereby an envelope waveshape which rises abruptly upon depression of the key, decays gradually thereafter and falls sharply upon release of the key is obtained.

24. An electronic musical instrument as defined in claim 20 wherein said envelope counter means repeatedly counts a key clock pulse during application thereto of said first control signal in such a manner that it resumes counting from the beginning after it has counted the last count so as to repeatedly produce an envelope waveshape which rises instantaneously, then decays sharply and rises instantaneously again while the key is depressed.

25. An electronic musical instrument as defined in claim 20 wherein said envelope waveshape generator means further comprises a clock selector adapted to produce a plurality of clock pulses which have frequencies respectively corresponding to frequencies of signals selected for the respective keyboards and which are commonly used by to all of the channels, whereby a clock pulse at a frequency corresponding to the kind of keyboard is obtained.

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 3,882,751
DATED : May 13, 1975
INVENTOR(S) : Norio TOMISAWA, Yasuji UCHIYAMA, Takatoshi OKUMURA
and Toshio TAKEDA

It is certified that error appears in the above—identified patent and that said Letters Patent is hereby corrected as shown below:

On the title page, column 1, fourth line of [75] Inventors, "Takea"
should read --Takeda--;

first line under [30] Foreign Application
Priority Data, "July 6, 1973" should read --Dec. 14, 1972-- and
"48-125513" should read --47-125513--.

Signed and Sealed this

Eighth Day of December 1981

[SEAL]

Attest:

GERALD J. MOSSINGHOFF

Attesting Officer

Commissioner of Patents and Trademarks

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[SEAL]

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