

[54] **DIGITAL SLOPE LIMITER**

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[56] **References Cited**

UNITED STATES PATENTS

3,548,325 12/1970 Salter et al. 307/263 X
3,432,674 3/1969 Hobrough 250/220 SP

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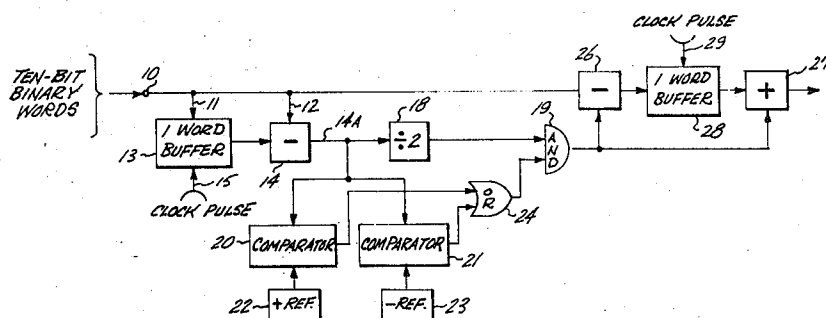
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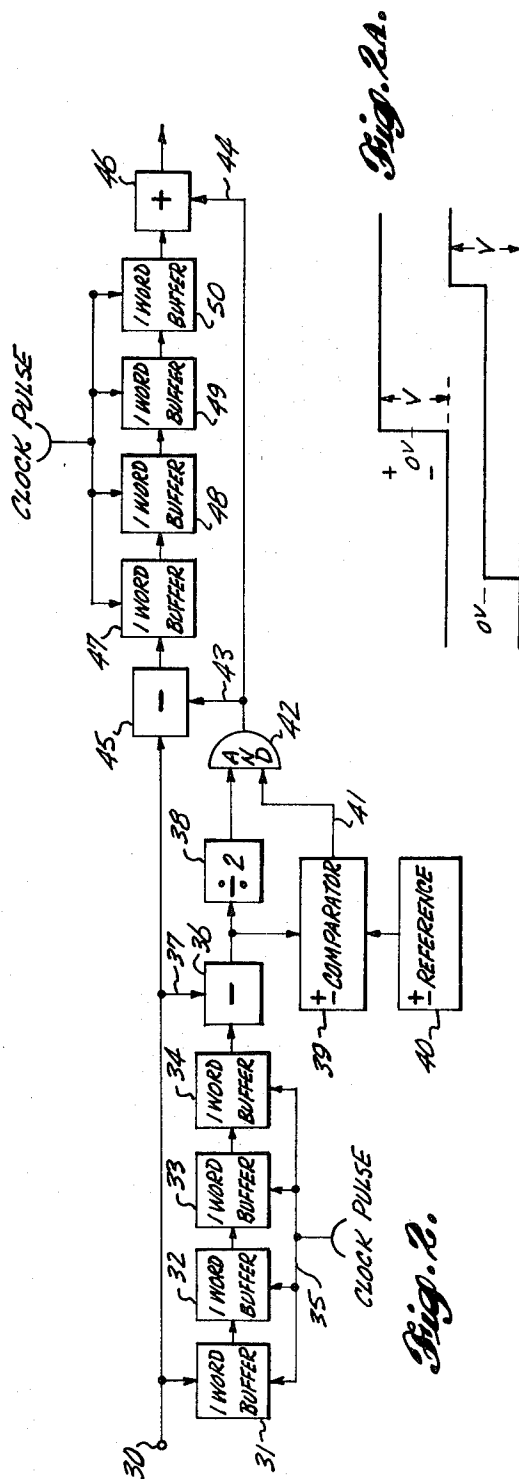
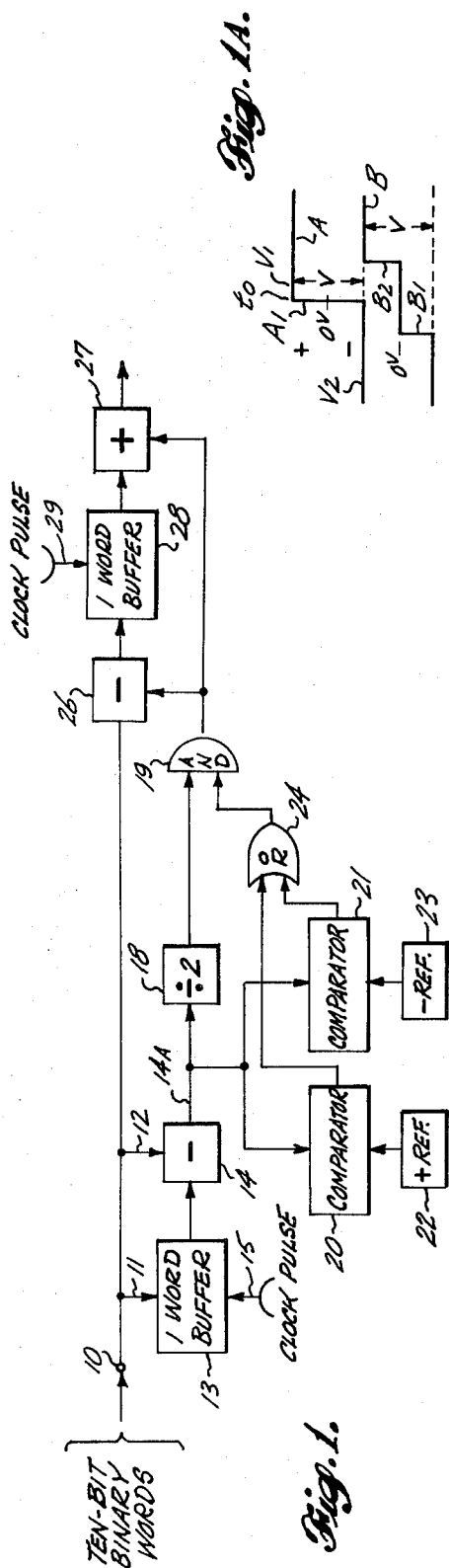
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ABSTRACT

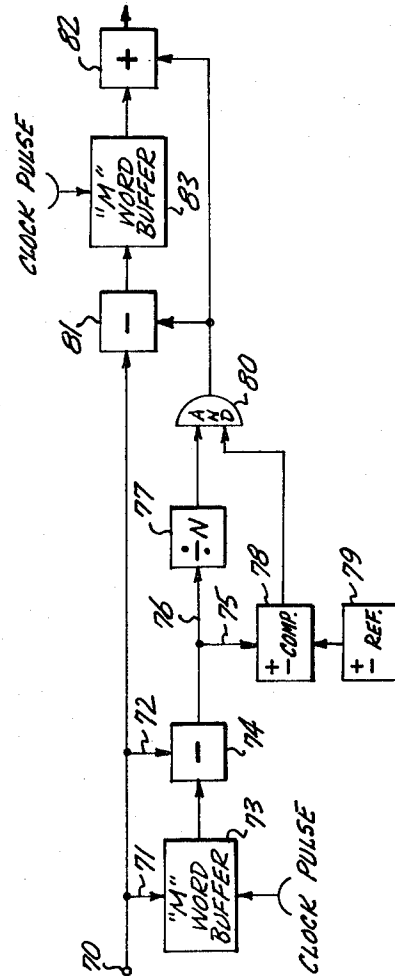
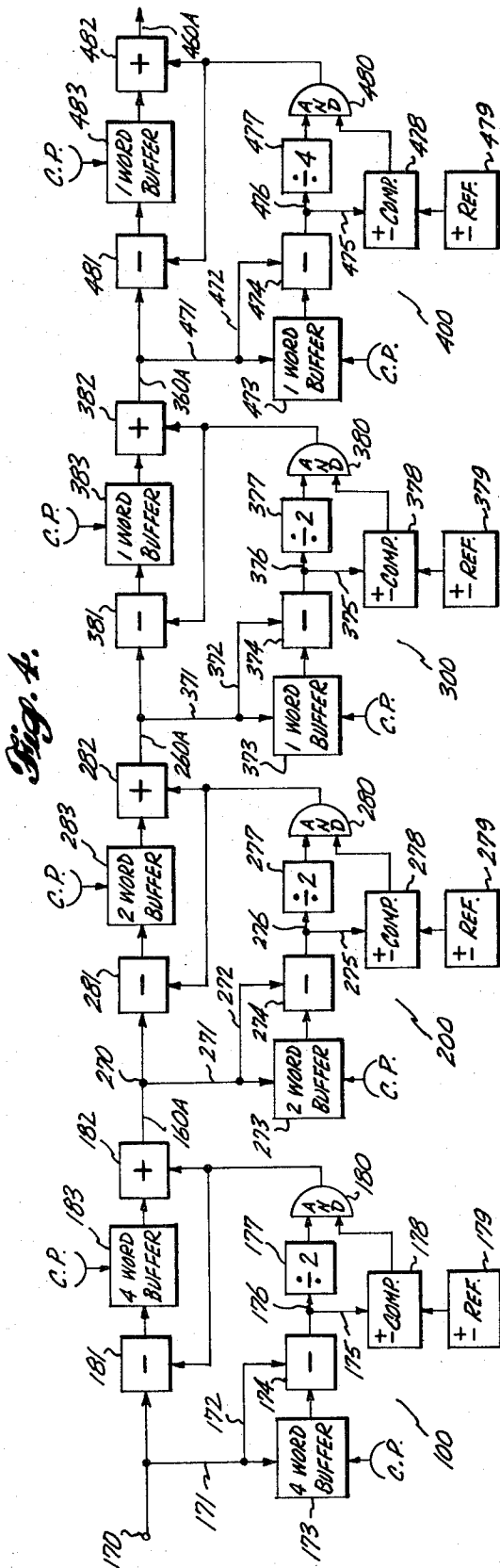
A digital circuit and system are described for detecting and smoothing step-functions or discontinuities in the signal representing height information in a photomapping system. The circuit is called a slope limiter. A threshold detection circuit provides a signal when the discontinuity exceeds predetermined values. Signal dividing circuitry then operates to divide the discontinuity signal (which is represented digitally) by a selected factor N. The divided value is then added and subtracted, respectively, to and from the trailing and leading signal values which are on opposite sides of the discontinuity. The result is that the original step-function signal is changed to a staircase signal of multiple steps. The disclosure includes a plurality of slope limiters in tandem so that the steps of a preceding limiter are acted on by a subsequent limiter. Repeated circulation of the digital signals in a circulating system permits repeated division of the steps in a manner which provides a desired degree of slope limiting. The height signal is thus smoothed through the time domain where the discontinuity existed.

14 Claims, 7 Drawing Figures





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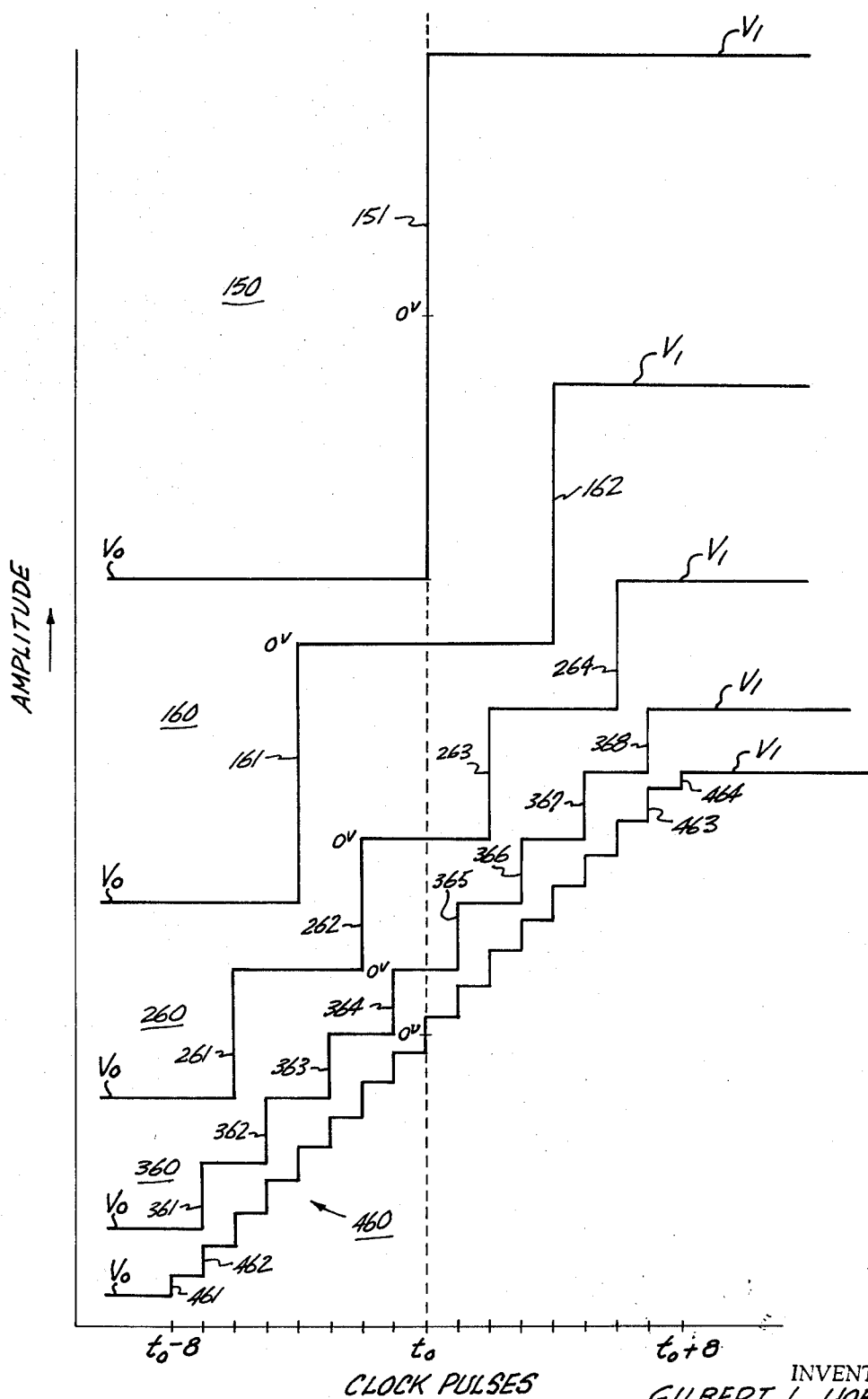


Fig. 4A.

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DIGITAL SLOPE LIMITER

Various types of systems are presently available for obtaining accurate terrain data from pairs of stereo photographs taken from a flying aircraft. One such system is disclosed in my co-pending application, Ser. No. 760,435 titled, "AUTOMATIC ORTHOPHOTO PRINTER," filed on Sept. 18, 1968. Another system is disclosed in U.S. Pat. No. 3,432,674 issued to me on Mar. 11, 1969. In one such system video signals representing left and right photographic data are converted to digital form and then processed by digital circuitry to determine the existence and degree of parallax between the left and right signals. When the terrain contains discontinuities, noise signals create discontinuities, or the photographs contain blank spots, the signal representing height undergoes a step-function change that is difficult to accommodate. It would be advantageous to have the ability to accommodate such discontinuities so that a smoothing function would occur and serve to fill-in the discontinuity encountered by the scanning system or generated by noise.

It is therefore an object of the present invention to provide a digital slope limiter.

Another object of the present invention is to provide a system for processing digital data representing height information and adapted to provide a smoothing function when step-functions of a predetermined magnitude occur in the information signal.

Another object of the present invention is to provide a digital slope limiter having particular advantage in the orthophotomapping art.

In accordance with the teachings of the present invention video signals representing image information in stereo photographs are converted to digital form by analog-to-digital converters. This digital data is processed to obtain height data and is then applied to a threshold circuit which serves to detect the existence of a step-function greater than a predetermined amplitude. When such a step-function is recognized, the signal is divided digitally by a selected factor. The signal value resulting from such division is then added to a leading portion of the discontinuity and is subtracted from the trailing portion of the discontinuity. Thus the slope limiting is done in a manner which maintains symmetry of the smoothed signal about the original point of discontinuity. The signal is processed in series by a plurality of slope limiters and can also be passed through the system a plurality of times in closed loop operation.

The above and additional advantages and objects of the invention will be more clearly understood from the following description when read with reference to the accompanying drawings.

FIG. 1 is a block diagram illustrating a one word-two term embodiment of the present invention, and FIG. 1A is an analog representation of an input signal and an output signal from the circuit of FIG. 1 (however, throughout the system digital signals are processed).

FIG. 2 is a block diagram of an embodiment of the invention similar to that of FIG. 1 but employing a four word-two term system, and FIG. 2A shows the input and output signals for the system of FIG. 2.

FIG. 3 is a generic block diagram of the invention.

FIG. 4 is a block diagram of a preferred system using four separate slope limiters connected in series to provide rapid limiting of an input signal in a single pass through the system.

FIG. 4A is a wave form diagram showing the results achieved using the system illustrated in FIG. 4.

The system illustrated in FIG. 1 is adapted for processing digital information signals identified as "words." The words are received in serial sequence. For purposes of illustration, the input signal information is shown as words of ten-bit parallel binary data plus one bit which is used to identify the algebraic sign of the value. The sign bit is carried through the slope limiter, as will be described below. In practice the words would be derived from processing the left and right video information signals through analog-to-digital converters and parallax discriminating circuitry such as disclosed in my above-referred to application to derive height data.

The input signals are applied to the input circuit 10 and from thence via circuits 11 and 12 to the one word buffer unit 13 and to the subtraction circuit 14. The buffer unit 13 is clocked at the system clock rate by clock pulse signals on clock terminal 15. The one word buffer 13 comprises ten binary signal storage devices such as bistable circuits connected in parallel for the receipt and storage of individual bits making up a word plus one section for sign bit.

The subtraction circuit 14 performs a subtraction operation between an input word on line 10 and the word which existed on line 10 prior to the occurrence of the preceding clock pulse and presently stored in buffer 13. In FIG. 1A the voltage "V" corresponding to the difference between voltages V_1 and V_2 would be represented by the digital signal on the subtraction output circuit 14A. The input signal "A" of FIG. 1A is shown as having undergone a change which is of sufficient magnitude to render the slope limiting circuit operable.

The difference signal obtained from subtraction circuit 14 is applied to the digital division circuit 18 where it is divided by a divisor of two. The output signal from division circuit 18 serves as one of the input signals to AND circuit 19.

The other input signal required to open the AND circuit 19 is present only when the absolute value of the signal from subtraction circuit 14 exceeds a predetermined magnitude. The output circuit 14A of subtract circuit 14 is applied to the comparator circuits 20 and 21 which respectively have the plus and minus reference values applied thereto by the reference sources 22 and 23. The reference sources 22 and 23 provide binary signals to the binary comparator circuits 20 and 21. These values from the reference sources 22 and 23 represent in digital form the value of the voltages which must be exceeded in order to cause slope limiting to occur. When this predetermined magnitude is detected, the AND gate 19 receives a signal via the OR gate 24. The AND gate then is opened so that one half of the value of the signal provided by subtract circuit 14 is applied to subtract circuit 26 and to the add circuit 27. Circuits 26 and 27 will be seen to be connected respectively to the input and output circuits of the word buffer 28. The subtract circuit 26 is also directly connected to the input terminal 10.

It will be seen that the circuitry described thus far acts to subtract from an existing word the value of a preceding word, to divide the difference by two, and then add and subtract one half of the difference to the leading and trailing sides of the step change in input

signal value. It should be noted that the addition and subtraction of signals includes algebraic sign so that in the case of a step-function decrease in the input signals applied to terminal 10 the add circuit 27 would be adding a negative quantity obtained from division circuit 18. In the exemplary wave form A of FIG. 1A the input signal has undergone a voltage increase. The wave form B in FIG. 1A represents the output signal on the output terminal 29. It will be seen that output signal has two steps with the amplitude of each step B_1 and B_2 being one half of the amplitude of the step A_1 of the input signal. It should also be noted that the steps B_1 and B_2 are symmetrically located relative to the step A_1 .

Referring now to FIG. 2 a system operating in accordance with the teachings of FIG. 1 but incorporating a longer delay of the input words will be described. In FIG. 2 the parallel binary signals representing a single word plus the algebraic sign signal are applied to terminal 30 which is connected to the one word buffer 31. Three additional one word buffer units 32, 33 and 34 are connected in serial arrangement downstream from the first buffer unit 31. Each of the four buffer units 30-34 are clocked by clock pulse signals applied via circuit 35. The output circuit of the one word buffer unit 34 is connected to the subtraction circuit 36, which is also coupled by lead 37 to the input terminal 30. The subtract circuit 36 serves to subtract from an existing word the value of the word which occurred four clock pulse intervals earlier. The difference signal is divided by two in the division circuit 38 and is also compared in the absolute value comparator 39 which has both plus and minus digital reference values applied thereto from the reference number source 40. In practice pre-established digital values can be obtained from a pair of reference sources representing the plus and minus voltage values with the two sources being alternately connected to the comparator at double the frequency of the clock pulses being applied to the buffer units.

The comparator 39 is coupled by circuit 41 to the AND gate 42. One half of the difference determined by the subtraction circuit 36 is applied via circuits 43 and 44 to the subtract and add circuits 45 and 46 respectively. The four one word buffer units 47, 48, 49 and 50 are connected in serial arrangement between the subtract circuit 45 and the add circuit 46. These single word buffers are the same as the single word buffers 31-34 and in practice can be flip-flop circuits.

As seen in FIG. 2A the input signal A has undergone a step increase in value A_1 equal to $V_1 - V_2$. The output signal B has two vertical portions B_1 and B_2 which are located four clock pulse intervals on either side of the single step A_1 .

FIG. 3 is a circuit arrangement which generically describes the systems of FIGS. 1 and 2. Thus in FIG. 3 the input circuit 70 is connected by leads 71 and 72 to the "M" word buffer unit 73 and to the subtract circuit 74. The difference between the word on line 72 and the word in the last stage of the buffer unit 73 is applied from subtract circuit 74 via leads 75 and 76 to the division circuit 77 and to the comparison circuit 78. The circuit 77 serves to divide the difference by a division of "N." Reference numbers for comparator 78 are provided by the adjustable reference source 79. The AND circuit 80 provides output signals from the division cir-

cuit 77 to the subtract and add circuits 81 and 82 connected on either side of the "M" word buffer 83. Buffer units 73 and 83 are clocked from the same source and thus provide the same amount of signal delay. From the preceding descriptions it will be seen that the difference signal provided by circuit 74 is divided in circuit 77 by a divisor of "N" with $1/N$ of the difference value being subtracted and added to the output signal train at the appropriate times.

From the above it will be seen that the input signal in the form of a step-function is smoothed by being converted from a single step to a plurality of smaller steps. The output signal can be applied to the input for similar action of the circuitry on each of the new steps. This process can be continued by repeated passes through a single circuit until the desired degree of smoothing has been achieved. A number of similar slope limiters can also be cascaded to obtain rapid smoothing of the signal, as for example using the system shown in FIG. 4.

In the arrangement of FIG. 4 there are four slope limiting circuits 100, 200, 300 and 400. Each has circuitry corresponding in general to that shown in FIG. 3. For convenience of description such similar components bear the reference numbers of FIG. 3 but increased respectively by 100, 200, 300 and 400.

The circuit 100 has four word buffer units 173 and 183 and a division circuit 177 having a divisor of two. It can be described as a four word-two term slope limiter. Similarly the circuit 200 may be called a two word-two term slope limiter. The circuit 300 is a one word-two term slope limiter. The circuit 400 is a one word-three term slope limiter, the "three term" description being based on the fact that adding and subtracting one fourth of the difference signal results in three vertical steps in the output signal from circuit 400 in response to an input signal having a single step.

It is of importance to note that each of the slope limiting circuits of the system of FIG. 4 has a separate comparison circuit 178, 278, 378, 478 and separate reference number sources 179, 279, 379, 479 which can be separately adjusted. In practice the slope limiting circuits can be adjusted to respond to difference signals from their subtraction circuits 174, 274, 374, 474 which are each of different magnitudes.

The results achieved using the system arrangement of FIG. 4 will be evident by reference to the wave form diagrams of FIG. 4A. Therein it will be seen that an input signal 150 has a step-function increase in value of a given magnitude giving rise to the step 151 at clock pulse time T_0 . This step in the input signal is shown as representing a voltage difference of $V_1 - V_0$. The voltages are shown as being referenced about the zero voltage line, the voltages V_1 and V_0 being represented in the system by 10-bit binary words plus algebraic sign. After the input signal has been passed through the first slope limiting circuit 100 the signal 160 is provided on the output circuit 160A of the adder 182. It will be seen that the signal 160 has the steps 161 and 162 which together add up to the value of the step 151 associated with the input signal 150. It is also of importance to note that the vertical steps 161 and 162 are symmetrically located on opposite sides of clock pulse time T_0 .

Each of the steps 161 and 162 are processed by the second slope limiter 200, the signal 260 being provided on the output circuit 260A of the circuit 200. It will be

seen that the step 161 has been divided into the steps 261 and 262 and that the step 162 has been divided into the steps 263 and 264. It will also be seen that the sum of the values represented by the steps 261-264 equals the value of the step 151.

In a similar manner the third slope limiting circuit 300 causes the four steps in signal 260 to be further divided into the signal 360 on circuit 360A. It will be seen that signal 360 has eight vertical steps 361-368.

The last slope limiting circuit 400 operates on each of the eight steps 361-368 giving rise to the output signal 460 on the output circuit 460A. It should be observed that the first step 461 of signal 460 is only one half as great as the vertical step 462. Similarly the last step 464 is only one half as large as the adjacent step 463. This results from the fact that the divisor of division circuit 477 is four. This means that one fourth of the difference signal from subtract circuit 474 is added to and subtracted from the signal existing one clock pulse time preceding and one clock pulse time succeeding the step 368. This means that one half of the step 368 remains as the step 463 in signal 460.

There has been described an improved slope limiting circuit and a system employing a plurality of such circuits connected in series. The invention makes possible symmetrical slope limiting by converting a single step of the input signal into a plurality of steps spread over a selected time base. The slope limiting occurs in a manner which is symmetrical with respect to the occurrence of the original step, which is of practical importance in the photogrammetry field. While the invention has been disclosed by reference to preferred embodiments, it is evident that changes can be made in the detailed systems shown which do not deviate from the spirit of the invention. For example, the input signals could be divided before being applied to the buffer 13 and subtract circuit 14 of FIG. 1, instead of having the division occur following the subtraction operation. In FIG. 4 this would mean that the division circuits 177, 277, 377, and 477 would be in lines 171, 271, 371 and 471. The delayed and undelayed signals could likewise first be divided and then applied to the subtraction circuit.

What is claimed is:

1. A slope limiter comprising in combination: a signal input circuit; first circuit means including a first signal delay circuit and a subtraction circuit connected to said signal input circuit and adapted to provide a difference signal representing the difference in amplitude between first and second input signals; second circuit means connected to said first circuit means for receipt of said difference signal and including division circuit means adapted to provide a signal which is a fractional part of said difference signal; and third circuit means connected to said input circuit and to said second circuit means and including means for adding the output signal of said division circuit means to said first input signal, and subtracting said output signal from said second input signal.

2. The apparatus of claim 1 wherein said third circuit means includes a second delay circuit connected between an addition circuit and a second subtraction circuit, said addition circuit and said second subtraction circuit each being connected to said division circuit means.

3. The apparatus of claim 1 and including fourth circuit means connected to said third and second circuit means, said fourth circuit means including means to inhibit output signals from said division circuit means to said third circuit means unless said difference signal is of a predetermined magnitude.

4. The apparatus of claim 3 wherein said fourth circuit means includes a reference signal generator and a comparator connected to receive said difference signal and compare it to a reference signal, and a gate circuit connected to said division circuit and to said comparator.

5. A slope limiter comprising in combination: first signal storage circuit means, first subtraction circuit means, and division circuit means connected in series circuit and operative to provide a first signal which is a fraction of the difference between a first input signal applied to and stored in said storage circuit means and a second input signal applied directly to said subtraction circuit means; addition circuit means and second subtraction circuit means each connected to said division circuit means; second signal storage circuit means connected between said addition circuit means and said second subtraction circuit means; signal output circuit means connected to said addition circuit means; and signal input circuit means connected to said first signal storage circuit means and to each of said subtraction circuit means.

6. Apparatus as defined in claim 5 and including threshold circuit means connected to said first subtraction circuit means, and signal gating circuit means connected to said division circuit means and to said threshold circuit means.

7. Apparatus as defined in claim 5 wherein each of said signal storage circuit means are digital signal buffer units each adapted to receive and store at least one parallel bit binary word.

8. The apparatus of claim 5 wherein each of said signal storage means comprises a plurality of binary signal buffer units connected in series circuit with each buffer unit adapted to store a parallel bit binary word, and means for applying clock pulse signals to the buffer units.

9. A slope limiter as defined in claim 5 and further including: third signal storage circuit means, third subtraction circuit means, and second division circuit means connected in series circuit with said output circuit means being connected to said third storage circuit means and to said third subtraction circuit means; second addition circuit means and fourth subtraction circuit means each connected to said second division circuit means; means connecting said fourth subtraction circuit means to said output circuit means; fourth signal storage circuit means connected between said second addition circuit means and said fourth subtraction circuit means; and a second signal output circuit connected to said second addition circuit means.

10. A system as defined in claim 9 wherein said first and second signal storage means comprise digital buffer units each adapted to store in serial sequence the same number of parallel bit binary words, and said third and fourth signal storage means comprise digital buffer units each adapted to store in serial sequence the same number of parallel bit binary words.

11. The system of claim 10 wherein said first and second division circuits have different divisors.

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12. The system of claim 11 wherein the number of words stored in said first buffer unit is different from the number of words stored in said third buffer unit.

13. A slope limiter comprising in combination: a signal input circuit; first circuit means connected to said input circuit and including a first signal delay circuit, a subtraction circuit, and a division circuit operatively interconnected to provide a difference signal representing a fraction of the difference in amplitude between first and second input signals; and second circuit means connected to said input circuit and to said

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first circuit means and including means for adding an output signal from said first circuit means to said first input signal, and for subtracting said output signal from said second input signal.

14. The apparatus of claim 13 wherein said second circuit means includes an addition circuit, a second subtraction circuit, and a second delay circuit connected between said addition circuit and said second subtraction circuit.

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