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(54) **INTERLOCKING EMI SHIELD**

EMI-VERRIEGELABSCHIRMUNG

ELÉMENT DE PROTECTION CONTRE LES INTERFÉRENCES ÉLECTROMAGNÉTIQUES À VERROUILLAGE

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Description

Background of the Invention

[0001] This invention is directed to an interlocking electromagnetic interference (EMI) shield system for use in an electronic device.

[0002] Many electronic devices include various electronic components that emit electromagnetic radiation. To prevent disturbances of the electronic components, EMI shields may be provided in the electronic device. For example, the electronic device components may be placed in a conductive box (e.g., a metallic box) that prevents radiation from escaping the box. As another example, the enclosure in which the electronic components are placed may be coated with a metallic or conductive paint. Another example of an EMI shield array is known from EP-A-1 061 789.

[0003] Although these solutions for reducing electromagnetic interferences may be effective, they may take up significant space, especially in view of the size of particular electronic components. For example, a lot of space is used to surround a small electrical circuit on all sides with a metallic box. When several electronic components of an electronic device need to be individually shielded, even more space is used to surround each component with individual conductive boxes. There is a need, therefore, for an EMI shielding system that takes up little space while providing sufficient and effective EMI shielding.

Summary of the Invention

[0004] An interlocking EMI shield system for protecting components of an electronic device from electromagnetic interferences is provided.

[0005] An interlocking EMI shield is provided. Each EMI shield may be constructed from a frame that is coupled to a circuit board or other electronic device structural component, and a cover that is placed over the frame. The frame may be coupled to the circuit board using any suitable approach, including for example soldering, a mechanical fastener, an adhesive, or a snapping mechanism. The frame may include walls extending around the periphery the shield, and a lip extending from the top edge of the walls towards the center of the shield (e.g., to provide additional structural support). The walls may include one or more snaps, tabs, apertures or indentations for receiving a corresponding element from the cover.

[0006] Each cover may include a substantially flat surface operative to be placed over the frame. To couple the cover to the frame, the cover may include several snaps extending vertically from the cover surface towards the circuit board to which the frame is coupled. The snaps may be biased towards the walls of the frame such that the snaps are operative to engage the walls upon coupling of the cover to the frame. In some embodiments, the snaps may include one or more tabs, prongs, or other elements to engage a counterpoint in the wall of the frame.

[0007] Each cover may include any suitable number of snaps. For example, each cover may include several snaps, each separated by a particular distance (e.g., at least by the width of a snap). The snaps may have the same or different sizes, and be distributed evenly or unevenly along the periphery of the cover. To reduce the space taken by the shields, the snaps of shields placed adjacent in the electronic device (e.g., having edges placed almost in contact) may be offset or staggered such that a snap of a first EMI shield may extend into an indentation of the second EMI shield (e.g., in between two snaps extending from the second EMI shield), while a snap of the second EMI shield may extend into an indentation of the first EMI shield (e.g., in between two snaps extending from the first EMI shield). Using this staggered approach, space of at least the thickness of one snap may be saved for other components of the electronic device, or to further reduce the size of the electronic device.

Brief Description of the Drawings

[0008] The above and other features of the present invention, its nature and various advantages will be more apparent upon consideration of the following detailed description, taken in conjunction with the accompanying drawings in which:

FIG. 1 is an exploded perspective view of an illustrative EMI shield in accordance with one embodiment of the invention;

FIG. 2 is a top perspective view of an exploded EMI shield assembly in accordance with one embodiment of the invention;

FIG. 3 is a perspective view of an EMI shield assembly coupled to a circuit board in accordance with one embodiment of the invention;

FIG. 4 is a perspective view of a detail of the EMI shield assembly of FIG. 3 along the boundary between the EMI shields in accordance with one embodiment of the invention;

FIG. 5 is a top view of a detail of the EMI shield assembly of FIG. 3 along the boundary between the EMI shields in accordance with one embodiment of the invention;

FIGS. 6A-6D are top views of a detail of an EMI shield assembly along the boundary between EMI shields in accordance with one embodiment of the invention; and

FIG. 7 is a top view of a detail of an EMI shield assembly along the boundary between EMI shields in accordance with one embodiment of the invention.

Detailed Description

[0009] FIG. 1 is an exploded perspective view of an

illustrative EMI shield assembly in accordance with one embodiment of the invention. EMI shield assembly 100 is formed from first EMI shield 108 that includes frame 110 and cover 120, and second EMI shield 138 that includes frame 140 and cover 150. Each of frames 110 and 140 includes side walls 112 and 142, and upper lip or returns 114 and 144, respectively. Side walls 112 and 142 are operative to be coupled to circuit board 130 of an electronic device to form the side walls of box, for example surrounding electronic components. Side walls 112 and 142 may be coupled to circuit board 130 using any suitable approach. For example, side walls 112 and 142 may be soldered into circuit board 130, snapped or clipped into a structural element of circuit board 130 (e.g., snaps extending in apertures in the circuit board, or snaps coupling to a receiving element incorporated in the circuit board), coupled using an adhesive or tape, or using any other suitable approach. In some embodiments, frames 110 and 140 may be combined into a single frame having a separating wall (e.g., along boundary 115) onto which distinct covers 120 and 150 may be attached.

[0010] Frames 110 and 140 may be placed on any suitable portion of circuit board 130. For example, frames 110 and 140 may be placed to surround specific electronic device components 132 incorporated in circuit board 130. In particular, frames 110 and 140 may be placed around different components 132 that emit electromagnetic radiation, or that are susceptible to electromagnetic radiation. If circuit board 130 includes two different components 132, both emitting electromagnetic radiation, and both susceptible to each other's emissions, each may be surrounded by one of frames 110 and 140 to prevent or reduce electromagnetic interferences to the operation of components 132. In addition, using two separate EMI shields 108 and 138 with separate covers 120 and 150 that can be individually removed may allow for access to particular components 132 (e.g., for repair) without disturbing other components that may be sensitive to interferences from the exposed components.

[0011] To prevent radiation from escaping over the end of side wall 112 and 142, respectively, covers 120 and 150 are placed over frames 110 and 140, respectively. Once the covers are placed over the frames, components 132 are enclosed in all directions by the cover, side walls and circuit board, thus preventing interfering radiation from escaping and damaging other components 132. Covers 120 and 150 may include a substantially flat surface 122 and 152 operative to be placed over each of frames 110 and 140. Covers 120 and 150 may have any suitable boundaries, including for example boundaries that substantially follow side walls 112 and 142, respectively. By providing covers that do not extend past, or minimally extend past side walls 110 and 140, the space required in the electronic device for covers 120 and 150 may be minimized.

[0012] Covers 120 and 150 may be coupled to frames 110 and 140 using any suitable approach. In some embodiments, covers 120 and 150 may include snaps 124 and 154 extending from flat surfaces 122 and 152. For example, snaps 124 and 154 may extend orthogonally (e.g., vertically) from surfaces 122, and be located at the periphery of surfaces 122 and 154. By being located at the periphery, snaps 124 and 154 may be substantially aligned with side walls 112 and 142, respectively, such that the snaps may engage a portion of the side walls. Snaps 124 and 154 may include one or more mechanisms for engaging side walls 112 and 142. For example, snaps 124 and 154 may be elastically biased towards side walls 112 and 142 such that snaps 124 and 154 may deflect when they are placed over frames 110 and 140, respectively, thus creating an interference or frictional fit. As another example, snaps 124 and 154 may include a tab or protrusion 126 and 156, respectively, operative to engage a corresponding indentation or tab 116 and 146, respectively, in the side wall. As still another example, a tape, adhesive or mechanical fastener (e.g., a screw passing through snaps 124 and 154 and engaging side walls 112 and 142, respectively) may be used to secure snaps 124 and 154 to frames 110 and 140, respectively.

[0013] Each cover 120 and 150 may include any suitable number of snaps 124 and 154. For example, a cover may include snaps 124 and 154 offset at distances larger than the width of a snap. In some embodiments, different snaps 124 and 154 may have different sizes, for example based on the component 132 lying adjacent the snap on circuit board 130, or based on the position of snap relative frame 110 or 140 (e.g., a snap adjacent a corner may be wider than a snap in the middle of a wall). The snaps may also be distributed along the periphery of the cover using any suitable approach, including for example evenly, or based on the EMI shielding or structural requirements of the shield.

[0014] Frames 110 and 140, and covers 120 and 150 may be manufactured from any suitable material operative to shield the components of contained within EMI shield 100 from electro-magnetic interference (e.g., from other components of the electronic device). In some embodiments, shield 100 may be constructed from an electrically conductive material such as, for example, metal (e.g., copper, silver, aluminum, steel), graphite, plasma, or any other conductive material. Frames 110 and 140, and covers 120 and 150 may include unbroken surfaces, or materials with a mesh or holes (e.g., so long as the holes are smaller than the wavelength of the radiation being kept out).

[0015] Because two frames 110 and 140, and two covers 120 and 150 may be used in the same electronic device, space may be lost between each EMI shield (e.g., along boundary 115). To reduce the space required between adjacent EMI shields 108 and 138, shields 108 and 138 may interlock along boundary 115. FIG. 2 is a top perspective view of an exploded EMI shield assembly in accordance with one embodiment of the invention. EMI shield 208 and 238 may include some or all of the features of EMI shields 108 and 138 (FIG. 1) described above. Frames 210 and 240 may be coupled to circuit board 130

using any suitable approach. Covers 220 and 250 may then be placed over frames 210 and 240, respectively, such that the electronic device components within the boundary of each frame 210 and 240 are fully enclosed.

[0016] Using some approaches, EMI shields 208 and 238 may be placed adjacent, and brought together until covers 220 and 250, which form the external-most layer of the EMI shields (e.g., because tabs extending from the covers are positioned outside the side walls of the frames), are in near contact (e.g., along boundary 215). To save even more space, however, covers 220 and 250 may be designed to interlock.

[0017] FIG. 3 is a perspective view of an assembled EMI shield assembly in accordance with one embodiment of the invention. EMI shield assembly 300 may include first EMI shield 308 and second EMI shield 338 that are coupled to circuit board 330. EMI shields 308 and 338 may include some or all of the features of any of the EMI shields described above in connection with FIGS. 1 and 2. First EMI shield 308 may include frame 310 to which cover 320 may be coupled, and second EMI shield 338 may include frame 340 to which cover 350 may be coupled. Covers 320 and 350 may include snaps 324 and 354, respectively, for engaging frames 310 and 340, respectively. To save space between EMI shields 308 and 338 along boundary 315, snaps 324 and 354 of covers 320 and 350, respectively, may be arranged such that snaps 324 and 354 may interlock.

[0018] FIG. 4 is a perspective view of a detail of the EMI shield assembly of FIG. 3 along the boundary between the EMI shields in accordance with one embodiment of the invention. FIG. 5 is a top view of a detail of the EMI shield assembly of FIG. 3 along the boundary between the EMI shields in accordance with one embodiment of the invention. By the manner in which snaps 324 and 354 are constructed, snaps 324 and 354 extend beyond the respective peripheries 321 and 351 of covers 320 and 350, creating respective voids 326 and 356 between adjacent snaps 324 and 354, respectively. Voids 326 and 356 may be defined, for example, by the side wall of the underlying frame, and by the width of adjacent snaps 324 or 354.

[0019] By sizing and distributing snaps 324 and 354 and voids 326 and 356 judiciously, a snap 324 may extend into a void 356, and a corresponding snap 354 may extend into a void 324 along boundary 315 (e.g., where covers 320 and 350 engage). In addition, if snaps 324 and 354 have the same width (e.g., which would likely be the case if the same material is used for both covers 320 and 350), the depth of each void 326 and 356 would match the width of each snap 324 and 356 operative to engage or extend into the void. Thus, the space required between adjacent covers 320 and 350 may be reduced from the width of snap 324, plus the width of snap 354, plus a clearance factor to only the width of one of snaps 324 and 354, plus a clearance factor. This allows the space between adjacent EMI shields 308 and 338 to be reduced up to by half (e.g., by the thickness of the material, for example sheet metal plus any additional distance required to clear the snaps). For example, if the width of each snap 224 or 254 is in the range of 0.12 to 0.2 mm, the savings may be for example 0.15 mm.

[0020] Using this approach, in a top view, it may appear as though the snaps of both covers form a single layer placed between the frames of the two EMI shields (e.g., snaps of adjacent shields are substantially aligned). For example, a single plane may include the inner surface of snap 324 and the outer surface of an adjacent snap 354.

[0021] In some embodiments, covers 320 and 350 may have different heights. For example, cover 320 may be higher than cover 350 (e.g., when coupled to frame 310). To allow covers 320 and 350 to engage, snaps 324 and 354 may be offset in the vertical dimension (e.g., along the height of covers 320 and 350). For example, snaps 324 may be located above snaps 354 when covers 320 and 350 engage because cover 320 is located above cover 350. Thus, the void used to place snap 354 near frame 310 may not be adjacent snap 324 (e.g., at a different point on the periphery of cover 320), but rather underneath a snap 324 (e.g., between the bottom edge of snap 324 and circuit board 330).

[0022] Any suitable approach may be used to ensure that adjacent covers 320 and 350 engage properly. For example, covers 320 and 350 may be shaped such that only one possible engagement of covers 320 and 350 is possible. As shown clearly in FIGS. 3-5, boundary 315 includes angled segment 316. Each of covers 320 and 350 may include corresponding angled portions 321 and 351, respectively. The size and shape of angled portions 321 and 351 may render any engagement of covers 320 and 350 that does not engage angled portions 321 and 351 impossible (e.g., covers 320 and 350 cannot engage properly, and save space unless angled segment 316 is properly created). This may ensure that covers 320 and 350 are properly placed on their respective frames, and that EMI shields 308 and 338 are properly mounted.

[0023] Other suitable shapes may be used instead of or in addition to angled segment 316. FIGS. 6A-6D are top views of a detail of an EMI shield assembly along the boundary between EMI shields in accordance with one embodiment of the invention. EMI shields 608 and 638 may include covers 620 and 650, respectively. Cover 620 may include tabs 624 and voids 626, and cover 650 may include tabs 654 and voids 656. Boundary 615 between EMI shields 608 and 638 may have any suitable, non-linear shape that allows only one reasonable engagement configuration. For example, boundary 615A includes a curved shape, boundary 615B includes several curved shapes, boundary 615C includes a single angle, and boundary 615D includes a protrusion. Tabs from each cover 620 and 650 may engage along any suitable surface, including several surfaces if boundary 615 includes several surfaces (e.g., boundary 615C includes engaging tabs along two surfaces of covers 620 and 650). It will be understood, however, that any other suitable shape may be used for boundary 615.

[0024] As another example, snaps 324 and 354, and corresponding voids 326 and 356 may be distributed along the periphery of each cover 320 and 350 such that, along the periphery that forms boundary 315, at least one snap and void in each cover is sized or located such that only one possible engagement of the covers is possible. FIG. 7 is a top view of a detail of an EMI shield assembly along the boundary between EMI shields in accordance with one embodiment of the invention. EMI shields 708 and 738 may include covers 720 and 750, respectively. Cover 720 may include first tabs 724, and second tab 725 that is different from first tabs 724. Conversely, cover 750 may include first voids 756 that is different from second void 757. When covers 720 and 750 are placed adjacent and engaged, the sizes of tabs 724 and 725, and of voids 756 and 757 may be such that the only possible engagement of covers 720 and 750 is with tab 724 engaging void 756, and tab 725 engaging void 757.

[0025] In some embodiments, more than two adjacent EMI shields installed on a circuit board may include tabs operative to engage to save space. For example, a two-dimensional array of interlocking EMI shields may be provided, such that different sides of a particular EMI shield may engage sides of different EMI shields (e.g., every side of the center EMI shield of a 3x3 array may engage another EMI shield). This may allow more components to be individually shielded while limiting the amount of space required for each shield.

[0026] The above described embodiments of the present invention are presented for purposes of illustration and not of limitation, and the present invention is limited only by the claims which follow.

Claims

1. An electromagnetic interference shield array (108, 138), comprising:

   a first frame (110); and
   a first cover (120) operative to be placed over the first frame, the first cover comprising at least a first snap (124) operative to engage a portion of the first frame;
   a second frame (140) placed adjacent to the first frame, wherein the first and second frames each comprise a wall (112, 142) coupled to a circuit board (130); and
   a second cover (150) operative to be placed over the second frame, the second cover comprising at least a second snap (154) operative to engage a portion of the second frame, **characterised in that** the second snap is offset from the first snap such that the first and second snaps are aligned to form a single layer between the first and second frames.

2. The electromagnetic interference shield array of claim 1, wherein the second cover (150) comprises at least two snaps (154), and wherein the first snap (124) extends between the at least two snaps.

3. The electromagnetic interference shield array of claim 1, wherein the first (124) and second (154) snaps are substantially in the same plane.

4. The electromagnetic interference shield array of claim 1, wherein a side of the first frame (110) adjacent to the second frame (140) is not straight.

5. The electromagnetic interference shield array of claim 4, wherein the side of the first frame comprises at least one angle (321, 351).

6. The electromagnetic interference shield array of claim 1, wherein the first (110) and second (140) frames comprise a return.

7. The electromagnetic interference shield array of claim 1, wherein the first snap (124) comprises an engagement feature for coupling the first cover (120) to the first frame (110).

8. The electromagnetic interference shield array of claim 1, wherein space between adjacent edges of the first (110) and second (140) frames is substantially equal to the width of a single snap.

9. A method for assembling an electromagnetic shield array, comprising:

   coupling a wall (112) of a first frame (110) and a wall (142) of a second frame (140) to a circuit board (130), wherein the first frame (110) is positioned adjacent to the second frame (140);
   engaging a first snap (124) of a first cover (120) with a portion of the first frame; and
   engaging a second snap (154) of a second cover (150) with a portion of the second frame, wherein the second snap is offset from the first snap such that the first and second snaps are aligned to form a single layer between the first and second frames.

Patentansprüche

1. Elektromagnetische Interferenz-Abschirmungsanordnung (108, 38), umfassend:

   einen ersten Rahmen (110); und
   eine erste Abdeckung (120), die operativ ist, um über den ersten Rahmen angeordnet zu werden, wobei die erste Abdeckung zumindest eine erste Einrastung (124) umfasst, die operativ ist, um mit einem Abschnitt des ersten Rahmens

einzurasten;
einen zweiten Rahmen (140), der zum ersten Rahmen benachbart angeordnet ist, wobei der erste und zweite Rahmen je eine Wandung (112, 142) umfassen, die mit einer Leiterplatte (130) gekoppelt ist; und
eine zweite Abdeckung (150), die operativ ist, um über den zweiten Rahmen angeordnet zu werden, wobei die zweite Abdeckung zumindest eine zweite Einrastung (154) umfasst, die operativ ist, um mit einem Abschnitt des zweiten Rahmens einzurasten, **dadurch gekennzeichnet, dass** die zweite Einrastung von der ersten Einrastung so versetzt ist, dass die erste und zweite Einrastung ausgerichtet sind, um eine einzige Schicht zwischen dem ersten und zweiten Rahmen zu bilden.

2. Elektromagnetische Interferenz-Abschirmungsanordnung nach Anspruch 1, bei welcher die zweite Abdeckung (150) zumindest zwei Einrastungen (154) umfasst, und wobei die erste Einrastung (124) sich zwischen den zumindest zwei Einrastungen erstreckt.

3. Elektromagnetische Interferenz-Abschirmungsanordnung nach Anspruch 1, bei welcher die erste (124) und zweite (154) Einrastung im Wesentlichen in derselben Ebene sind.

4. Elektromagnetische Interferenz-Abschirmungsanordnung nach Anspruch 1, bei welcher eine Seite des ersten Rahmens (110), der zum zweiten Rahmen (140) benachbart ist, nicht gerade ist.

5. Elektromagnetische Interferenz-Abschirmungsanordnung nach Anspruch 4, bei welcher die Seite des ersten Rahmens zumindest einen Winkel (321, 351) umfasst.

6. Elektromagnetische Interferenz-Abschirmungsanordnung nach Anspruch 1, bei welcher der erste (110) und zweite (140) Rahmen einen Rückteil umfasst.

7. Elektromagnetische Interferenz-Abschirmungsanordnung nach Anspruch 1, bei welcher die erste Einrastung (124) ein Einrastungsmerkmal zum Koppeln der ersten Abdeckung (120) mit dem ersten Rahmen (110) umfasst.

8. Elektromagnetische Interferenz-Abschirmungsanordnung nach Anspruch 1, bei welcher Raum zwischen benachbarten Kanten des ersten (110) und zweiten (140) Rahmens im Wesentlichen gleich zur Breite einer einzigen Einrastung ist.

9. Verfahren zum Zusammenbauen einer elektromagnetischen Abschirmungsanordnung, umfassend:

Koppeln einer Wandung (112) eines ersten Rahmens (110) und einer Wandung (142) eines zweiten Rahmens (140) mit einer Leiterplatte (130), wobei der erste Rahmen (110) benachbart zum zweiten Rahmen (140) positioniert wird;
Einrasten einer ersten Einrastung (124) einer ersten Abdeckung (120) mit einem Abschnitt des ersten Rahmens; und
Einrasten einer zweiten Einrastung (154) einer zweiten Abdeckung (150) mit einem Abschnitt des zweiten Rahmens, wobei die zweite Einrastung von der ersten Einrastung so versetzt ist, dass die erste und zweite Einrastung ausgerichtet sind, um eine einzige Schicht zwischen dem ersten und zweiten Rahmen zu bilden.

Revendications

1. Un réseau de blindage contre les interférences électromagnétiques (108, 138), comprenant :

un premier châssis (110) ; et
un premier couvercle (120) utilisable pour être placé sur le premier châssis, le premier couvercle comprenant au moins un premier encliquetage (124) utilisable pour être en prise avec une partie du premier châssis ;
un second châssis (140) placé adjacent au premier châssis, le premier et le second châssis comprenant chacun une paroi (112, 142) couplée à une carte de circuit (130) ; et
un second couvercle (150) utilisable pour être placé au-dessus du second châssis, le second couvercle comprenant au moins un second encliquetage (154) utilisable pour venir en prise avec une partie du second châssis,
caractérisé en ce que le second encliquetage est décalé par rapport au premier encliquetage de telle sorte que le premier et le second encliquetage soient alignés pour former une couche unique entre le premier et le second châssis.

2. Le réseau de blindage contre les interférences électromagnétiques de la revendication 1, dans lequel le second couvercle (150) comprend au moins deux encliquetages (154), et dans lequel le premier encliquetage (124) s'étend entre les au moins deux encliquetages.

3. Le réseau de blindage contre les interférences électromagnétiques de la revendication 1, dans lequel le premier (124) et le second (154) encliquetage sont substantiellement dans le même plan.

4. Le réseau de blindage contre les interférences électromagnétiques de la revendication 1, dans lequel un côté du premier châssis (110) adjacent au second châssis (140) n'est pas rectiligne.

5. Le réseau de blindage contre les interférences électromagnétiques de la revendication 4, dans lequel le côté du premier châssis comprend au moins un angle (321, 351).

6. Le réseau de blindage contre les interférences électromagnétiques de la revendication 1, dans lequel le premier (110) et le second (140) châssis comprennent un retour.

7. Le réseau de blindage contre les interférences électromagnétiques de la revendication 1, dans lequel le premier encliquetage comprend un élément de venue en prise pour coupler le premier couvercle (120) au premier châssis (110).

8. Le réseau de blindage contre les interférences électromagnétiques de la revendication 1, dans lequel l'espace compris entre les bords adjacents du premier (110) et du second (140) châssis est substantiellement égal à la largeur d'un encliquetage unique.

9. Un procédé d'assemblage d'un réseau de blindage contre les interférences électromagnétiques, comprenant :

le couplage d'une paroi (112) d'un premier châssis (110) et d'une paroi (142) d'un second châssis (140) à une carte de circuit (130), le premier châssis (110) étant positionné adjacent au second châssis (140) ;
la venue en prise d'un premier encliquetage (124) d'un premier couvercle (120) avec une partie du premier châssis ; et
la venue en prise d'un second encliquetage (154) d'un second couvercle (150) avec une partie du second châssis,
le second encliquetage étant décalé du premier encliquetage de telle sorte que les premier et second encliquetages soient alignés pour former une couche unique entre le premier et le second châssis.

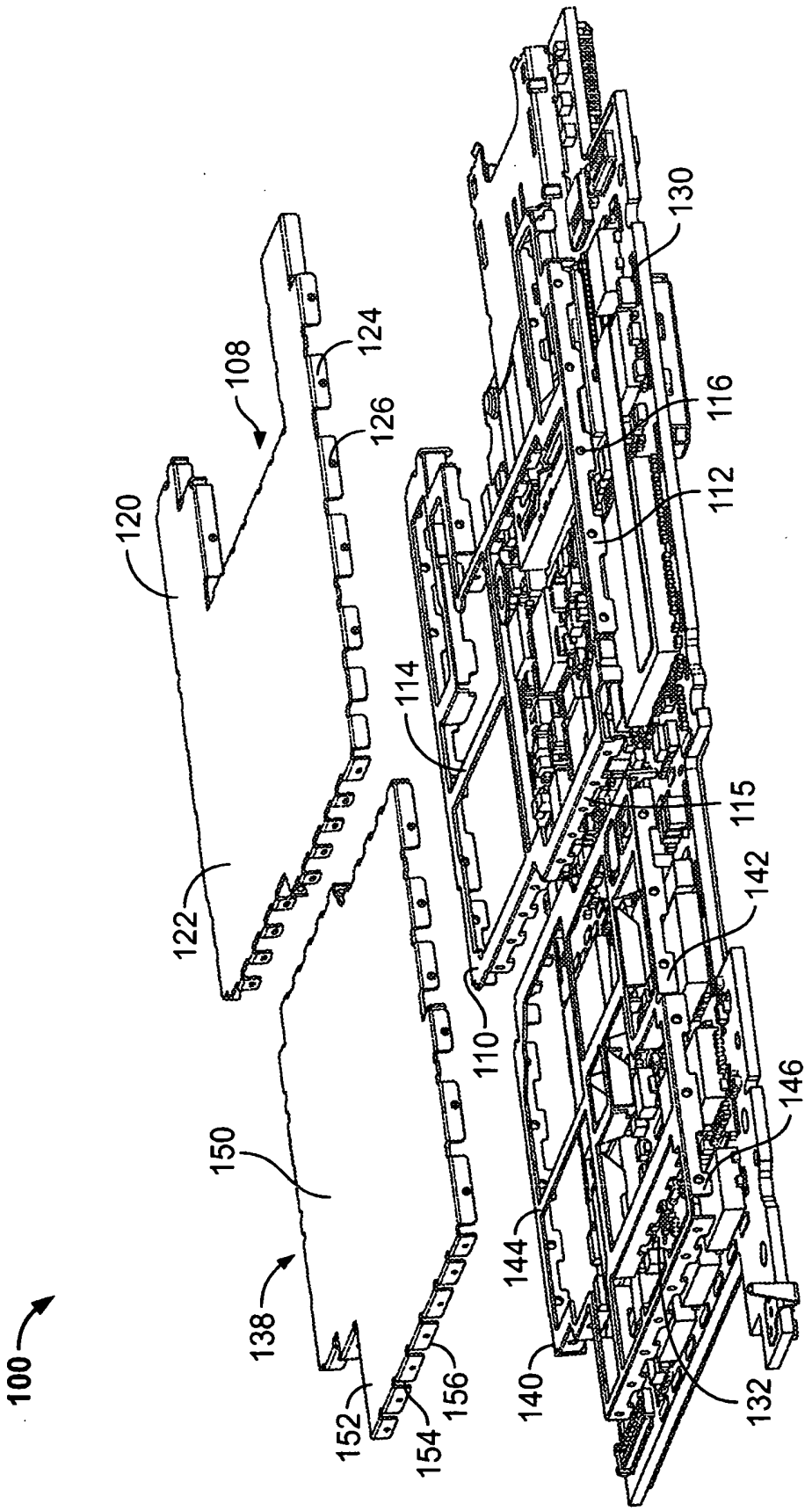
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FIG. 1

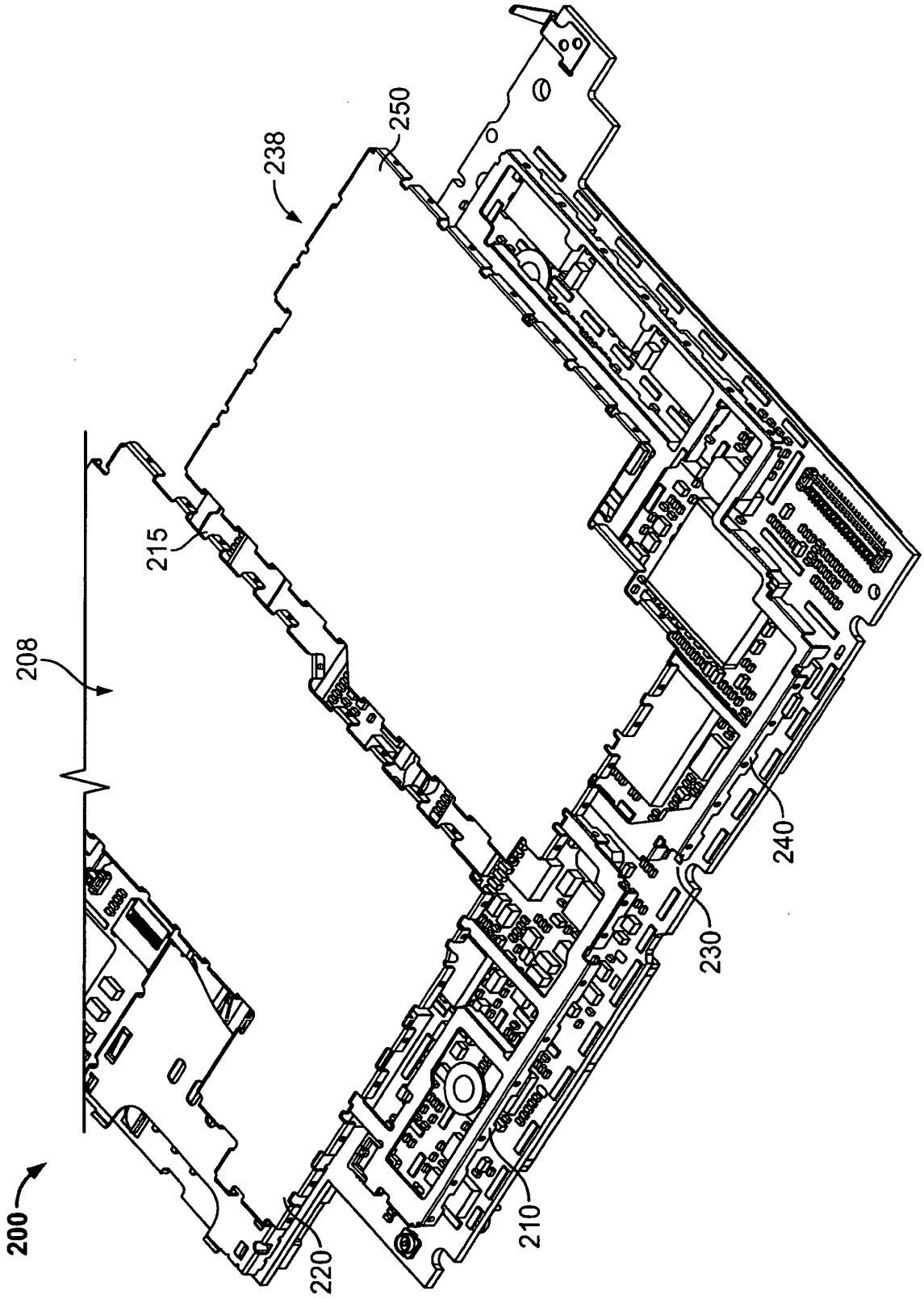

FIG. 2

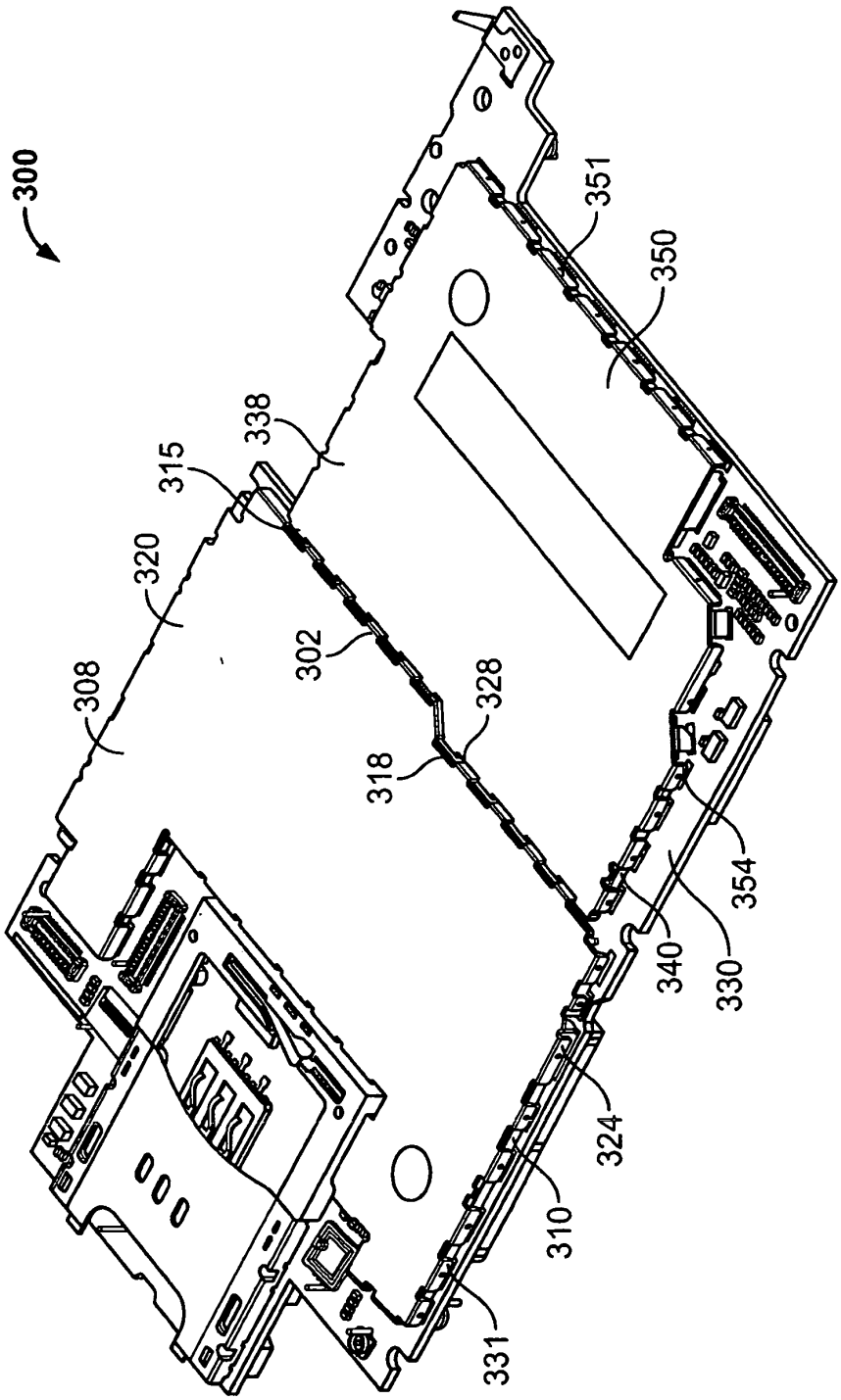

FIG. 3

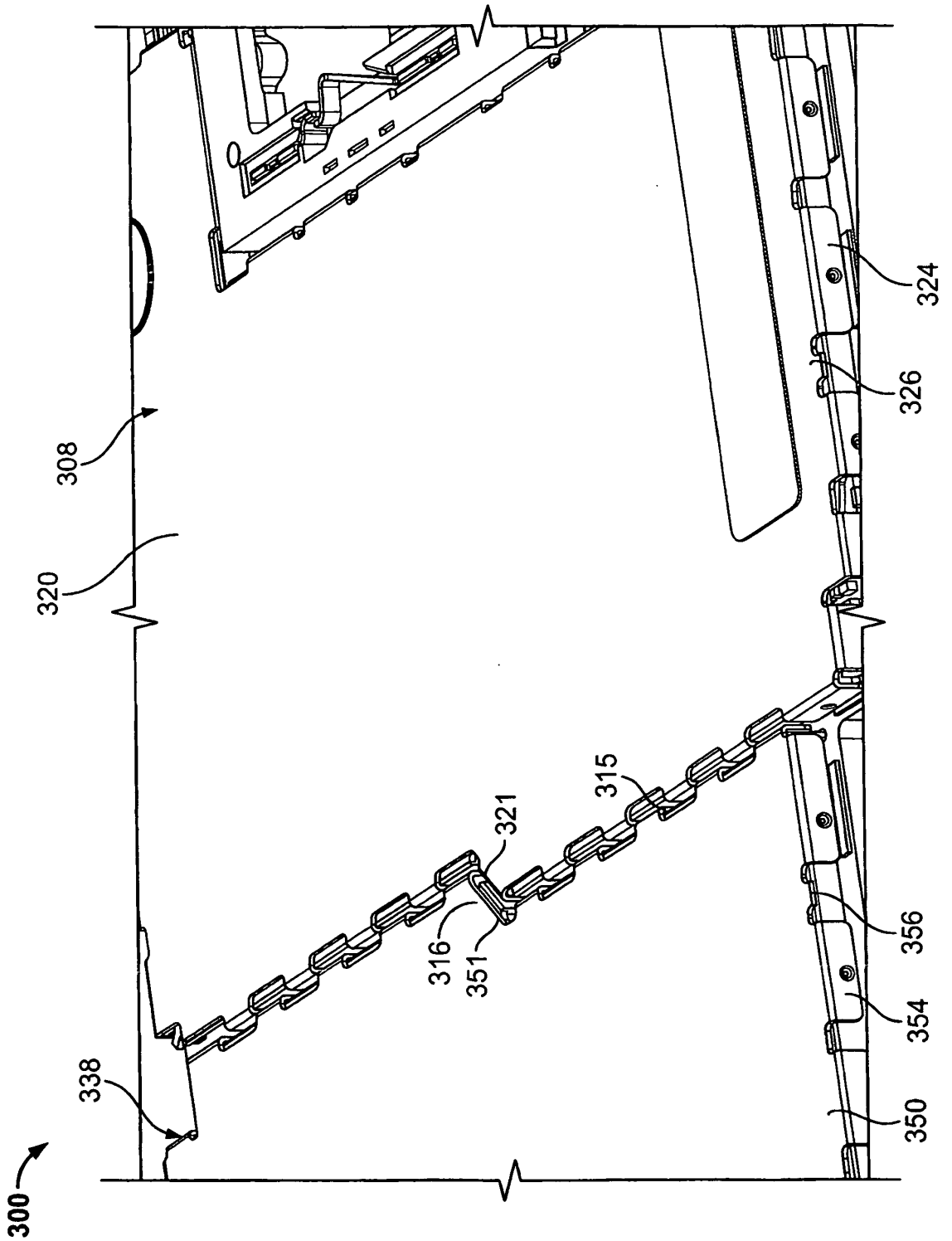

FIG. 4

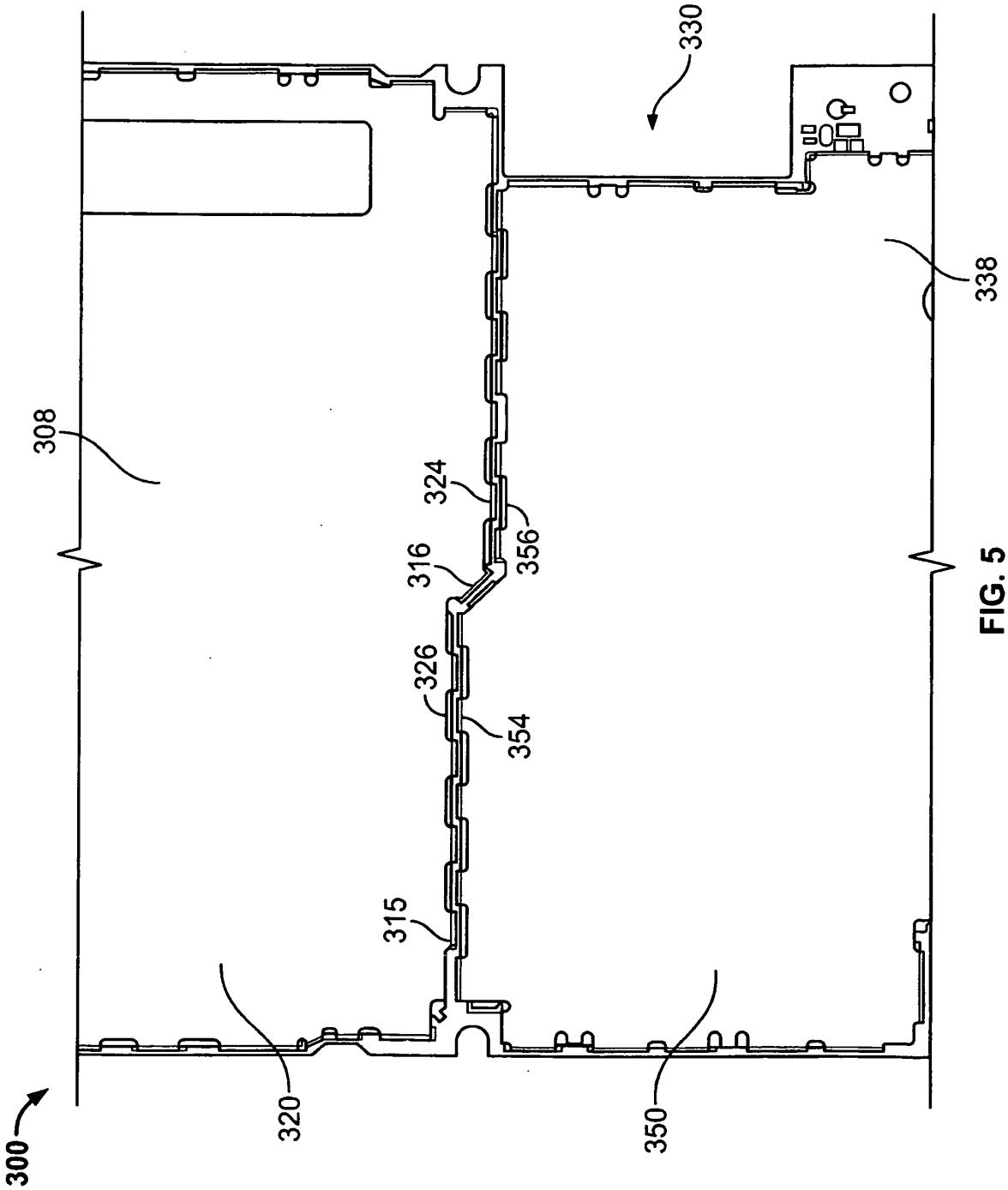

FIG. 5

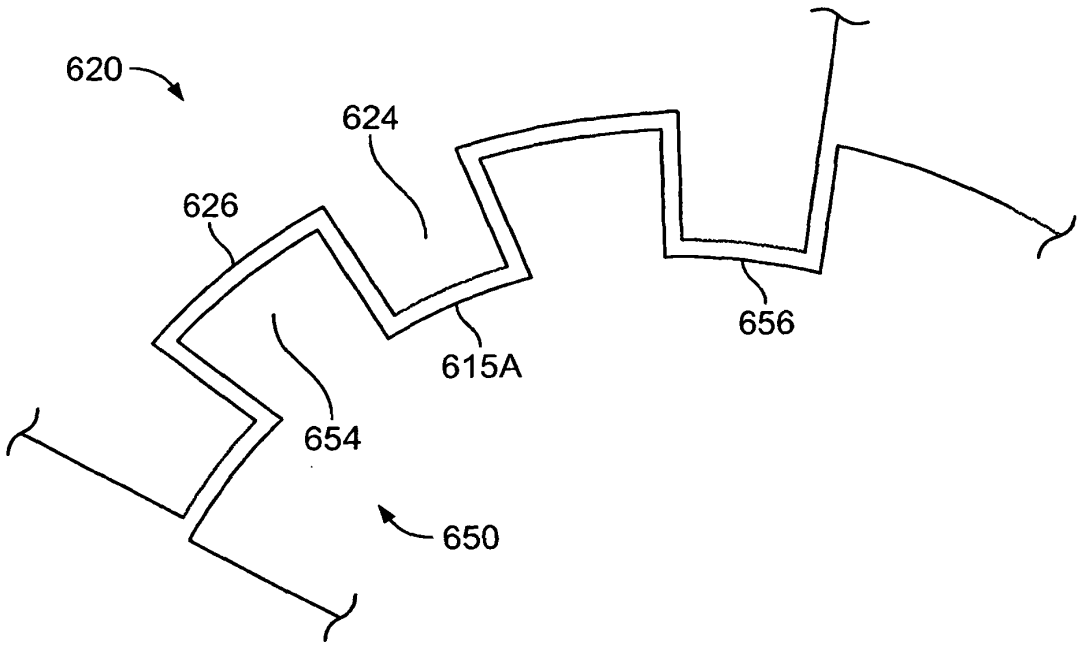

FIG. 6A

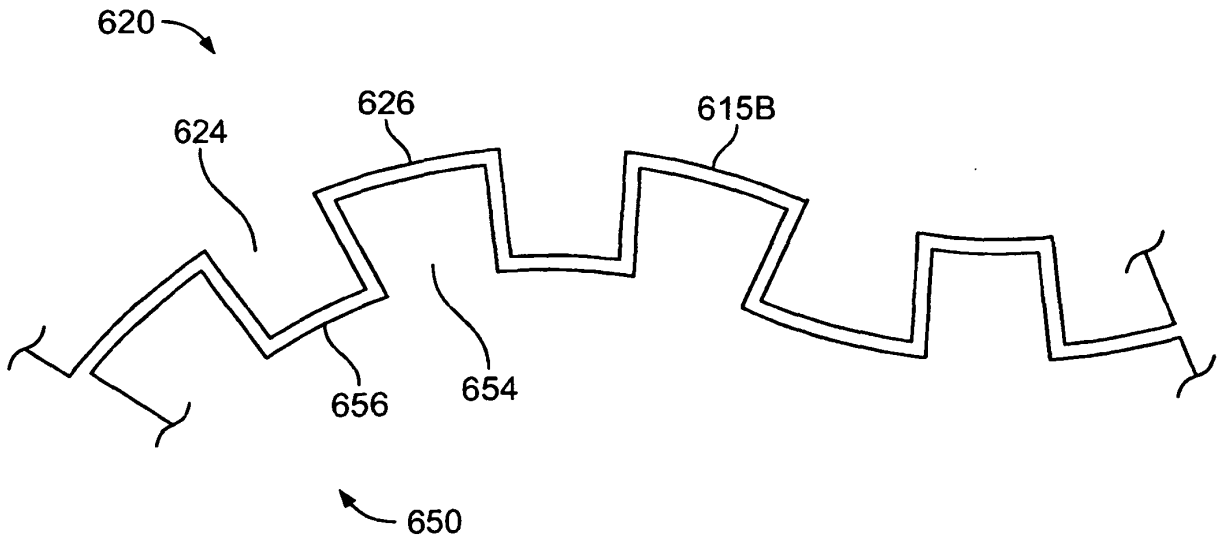

FIG. 6B

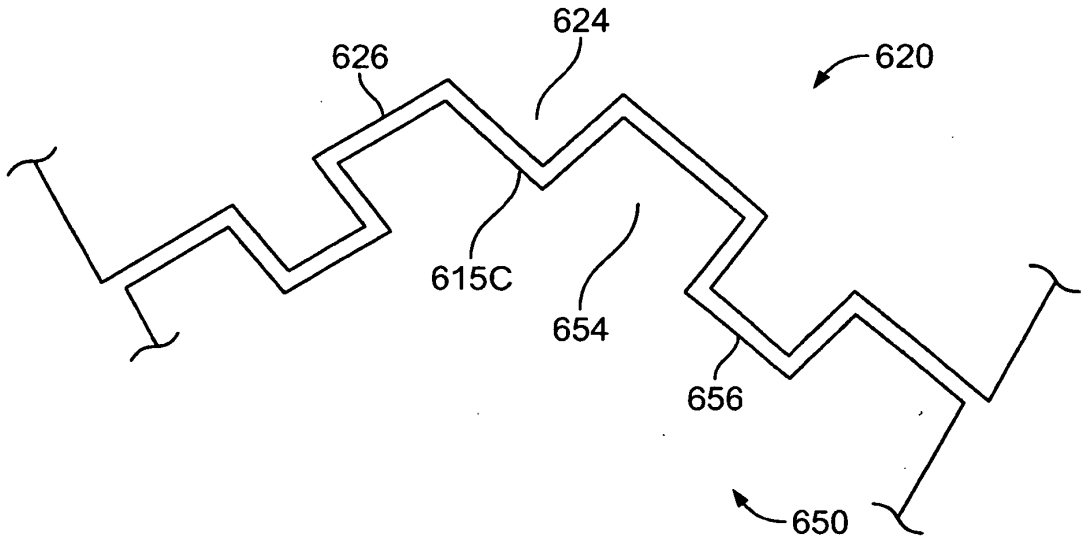

FIG. 6C

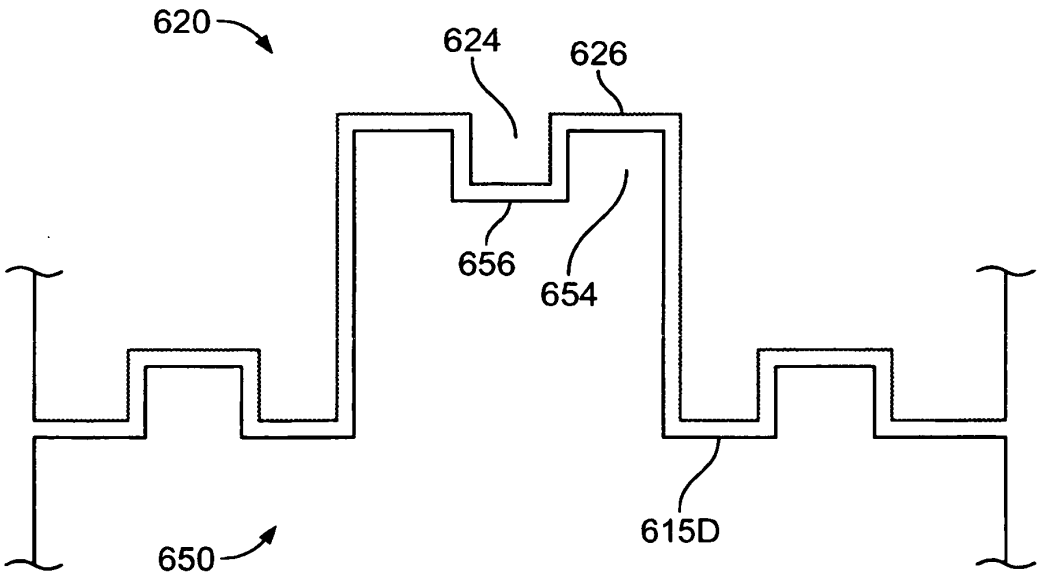

FIG. 6D

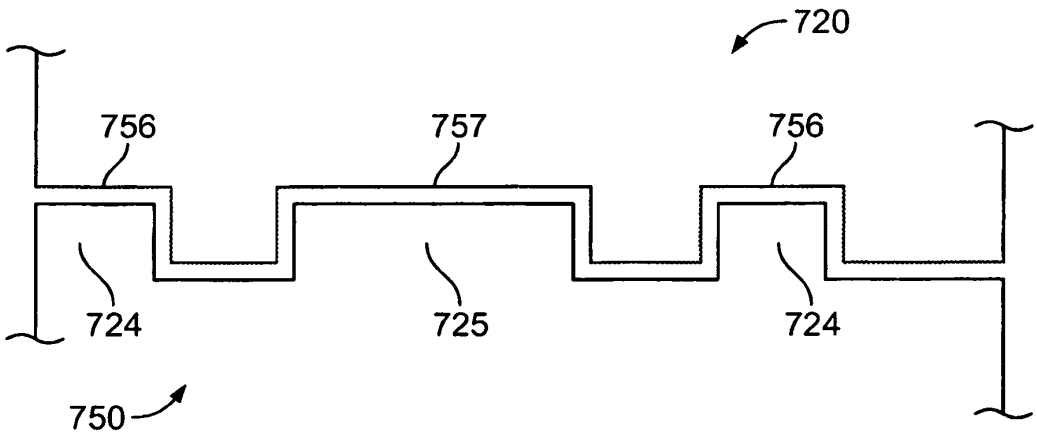

FIG. 7

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

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