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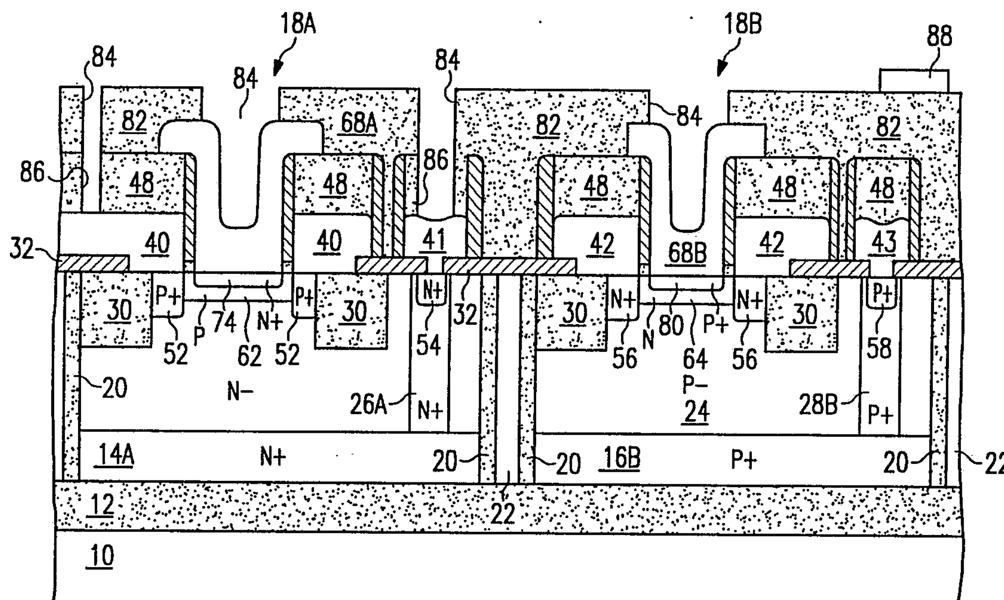

(57) Abstract

Complementary bipolar transistors and a process for fabrication on a dielectrically isolated substrate. Both the NPNs and PNPs have an emitter (74, 80) diffused from an emitter polysilicon contact (68A, 68B) and an extrinsic base (52, 56) diffused from a base polysilicon contact (40, 42) with the emitter polysilicon contact separated from the base polysilicon contact by sidewall oxide/nitride. This provides shallow emitters and a small emitter-to-extrinsic base distance and high performance.

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COMPLEMENTARY BIPOLAR TRANSISTORS HAVING HIGH EARLY VOLTAGE, HIGH FREQUENCY PERFORMANCE AND HIGH BREAKDOWN VOLTAGE CHARACTERISTICS AND METHOD OF MAKING SAME

BACKGROUND AND SUMMARY OF THE INVENTION

The present invention relates generally to the manufacture of integrated circuits and more specifically to complementary bipolar transistors having high Early voltage, high frequency performance, and high breakdown voltage characteristics. Evolution of these analog products parallels the industry trend for higher speed semiconductor devices and higher levels of functional integration. Historically, device architectures have been characterized by deep device junctions and have not minimized lateral device geometries. Furthermore, the limited variety of device types which can be fabricated with a given process has, in turn, limited the integration of analog and digital functions.

U.S. Patent 4,665,425 to Piotrowski teaches the fabrication of vertical complementary bipolar transistors in dielectrically isolated islands. By forming vertical NPN and PNP transistors frequencies above 1 GHz have become achievable.

In order to attain higher frequency performance, it is necessary to decrease junction depths and lateral device dimensions. Junction depths can be reduced with self-aligned polysilicon emitters and the emitter-to-extrinsic base spacing can be reduced with an interposing dielectric spacer. A further advantage of polysilicon emitters is that they allow favorable trade-offs between current gain and Early voltage. U.S. Patent 4,908,691 to Silvestri, et al. discloses an

exemplary high frequency BiCMOS process. Vertical complementary bipolar transistors are formed in an integrated circuit having lateral dielectric isolation and junction bottom isolation.

It is an object of the present invention to provide a method of fabricating complementary bipolar transistors of still higher frequency.

Another object of the invention is to provide complementary bipolar transistors for high frequency *analog applications characterized by increased current gain and Early voltage characteristics.

Still another object is to provide a method for manufacturing integrated circuits incorporating these higher performance complementary bipolar transistors.

According to a preferred embodiment of the invention there is now provided an integrated circuit with complementary bipolar transistors formed in electrically isolated islands having an Early voltage of at least 40 volts; a collector to base breakdown voltage of at least 12 volts; and a frequency response of at least 3 Ghz. Preferably, the transistors exhibit a current gain of at least 100 and a collector to emitter breakdown voltage of at least 12 volts. The base region should have a net peak dopant concentration at least 50 times larger than the net dopant concentration in the collector, and the collector width should be in the range of 0.7 to 1.5 microns. The net peak dopant concentration in the

base region should be in the range of $4x10^{17}$ cm^{-3} to $2.0x10^{18}cm^{-3}$. The process also enables provision of field effect transistors having a frequency response of at least 4 Ghz.

An integrated circuit can be configured with these transistors to provide a feedback amplifier having a bandwidth of at least 45 Mhz and a slew rate of at least 2,000 volts per micro second. The amplifier will operate at a maximum supply current of 25 milliamps and may be connected in the voltage feedback or current feedback mode.

Sample and hold circuits made with these amplifiers in a voltage feedback configuration will exhibit typical acquisition times on the order of 50 ns, to be compared with prior art 500 ns times for 12 bit resolution. In a current feedback configuration a typical 15 ns acquisition time is achievable at 12 bits of resolution with 200 MHz bandwidth. Typical slew rates of 150 volts per microsecond and 500 volts per microsecond are achievable for voltage and current feedback configurations, respectively. A digital to analog converter comprising transistors of the present invention will exhibit a typical settling time of less than 30 nanoseconds to one-half LSB with at least 11 bit resolution. Switches comprising these transistors will exhibit a rise and fall time of less than one nanosecond. When used with programmable current sources, the switches will produce a program current non-linearity of less than one percent.

The process forms complementary pairs of bipolar transistors each having similar base depths and similar distances from the base to a heavily doped buried collector region. These similar profiles are achieved with complementary impurities having similar diffusion coefficients in the base and buried collector regions. For a silicon process the preferred dopants are phosphorus and boron. Since these species each have an atomic radius smaller than that of silicon, impurity atoms having a larger atomic radius may be added to reduce stress within the active lattice structure. Such an impurity may be arsenic, antimony, or germanium. The concentration of stress reducing impurity is sufficiently low as to not detrimentally affect the net dopant concentration of the buried collector regions.

A double level polysilicon process for making the bipolar transistors is preferred. A first conductor level of polysilicon is selectively doped with impurities which are later outdiffused to the underlying crystal to form extrinsic base regions of the bipolar transistors. The same polysilicon level also forms collector conductors and collector contact regions. The first conductor level is covered with an insulative layer and patterned to expose intrinsic base regions prior to the drive-in. After extrinsic base formation, an insulating layer is formed at least on the exposed base areas and intrinsic base impurities are then introduced.

Lateral spacers are formed on side walls of the first level of conductors and the top insulative layer adjacent the intrinsic base areas to diminish the size of the opening and define the subsequently formed emitter region. The insulative layer on the intrinsic base area separates the spacers from the intrinsic base areas. By forming the spacers after forming the intrinsic base, the extrinsic base to emitter spacing can be increased while maintaining adequate intrinsic base to extrinsic base overlap. The increased emitter to extrinsic base spacing increases current gain and emitter to base breakdown voltage and reduces emitter junction leakage. Preferably, the insulative layer is oxide and the spacers are nitride. This eliminates undercutting of the spacer and provides better control of the extrinsic base to emitter spacing.

The second level of polysilicon is next formed on the wafer. Portions of this second polysilicon layer contacting the intrinsic base areas of the first N and P islands are selectively doped with N and P impurities respectively to form emitter contacts. The impurities are outdiffused from the emitter contacts to form the emitter regions.

The resulting spacer design and impurity profiles provide bipolar transistor structures having high frequency response, high Early voltage, high breakdown voltage and high current gain. The transistors are formed in isolated islands with minimum geometry to maximize density. The impurity

concentration of the collector regions is kept low and the lateral dimensions of the emitter, base and collector are minimized.

Additional devices can be formed without requiring additional process steps. For example, a capacitor can be formed wherein the bottom plate is a region of the crystal layer and the top plate is the first polysilicon conductor. Resistors may be formed as thin films or in the substrate itself. JFETs and buried Zener diodes may also be formed without any additional processing steps.

Other objects, advantages and novel features of the present invention will become apparent from the following detailed description of the invention when considered in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1-9 are cross-sectional views of a wafer during various stages of fabrication according to the principles of the present invention;

Figure 10 is a cross-section of a diffused resistor incorporating the principles of the invention;

Figure 11 is a cross-section of an alternate embodiment diffused resistor incorporating the principles of the invention;

Figure 12 is a cross-sectional view of a JFET incorporating the principles of the invention;

Figures 13 and 14 are cross-sectional views of a wafer during fabrication of heavily doped buried collector regions;

Figure 15 is a schematic of a voltage feedback amplifier circuits of the invention;

Figure 16 is a block diagram of a current feedback amplifier incorporating the invention;

Figure 17 is a block diagram of sample and hold circuitry incorporating transistors according to the invention;

Figure 18A is a prior art cell of a digital to analog converter and Figures 18B and 18C are cells of a digital to analog converter incorporating the invention;

Figure 19 illustrates a switch stage incorporating the invention;

Figure 20 is a schematic of a current conveyor incorporating the invention;

Figure 21 is a schematic of a comparator incorporating the invention.

DETAILED DESCRIPTION OF THE INVENTION

A preferred embodiment of the invention is now described with application to dielectrically isolated devices formed in silicon. Other isolation techniques, e.g., junction isolation, may be used as well as semiconductor materials other than silicon. Figure 1 illustrates a stage in the fabrication process wherein heavily doped buried collector regions have been formed in more lightly doped silicon of several

dielectrically isolated islands. The islands are electrically isolated from an underlying substrate 10 by a dielectric layer 12. The islands 18A-18D are of N-type conductivity having N^+ buried regions 14A and 14C and P^+ buried regions 16B and 16D, respectively. Preferably, the N^+ regions are phosphorus doped, and the P^+ buried regions are boron doped. Since phosphorus and boron have very similar diffusion coefficients, the resulting complementary bipolar transistors have substantially matching collector widths. The ratio of the P and N impurity diffusion coefficients for the buried regions is in the range of 0.5 to 2.0. Lateral dielectric isolation is provided by trenches, the walls of which are lined with dielectric layers 20 and polysilicon 22.

The illustrated structure may be produced by wafer bonding, ZMR, SIMOX or other methods. One process flow would begin with an N layer formed over the dielectric layer 12. The buried layers 14A, 14C, 16B, and 16D may be formed with implants followed by epitaxial growth. The controlled epitaxial thickness is highly determinative in setting the desired distance between the transistor base and the buried collector layer of the invention. The preferred epi thickness ranges between 2.0 and 4.0 microns. The individual islands are formed by anisotropically etching trenches and forming an oxide layer 20 over the vertical trench sidewalls. As illustrated, the trenches may be filled with polysilicon 22. These and alternate process steps are well known and more fully

illustrated in U.S. Patents 4,900,689 to Bajor, et al; 4,929,566 to Beitman and 4,951,102 to Beitman, et al, all assigned to the assignee of the present invention and incorporated herein by reference.

The heavily doped regions 14 and 16 are formed with high concentrations of boron and phosphorus. Since these species have smaller atomic radii than silicon, substantial lattice defects can extend from this region of the crystal structure. If permitted, such defects would cause significant current leakage across junctions, thereby degrading analog performance characteristics in the transistors. Silicon has an atomic radius of 1.17 Å while boron and phosphorus have atomic radii of 0.88Å and 1.10Å, respectively. According to the invention, lattice strain, and resulting defects, are reduced by adding to the regions 14 and 16 impurities having larger atomic radii to offset the effects of boron and phosphorus on the lattice. Such impurities may be selected from the group consisting of arsenic, antimony, or germanium. For example, arsenic has an atomic radius of 1.18Å.

As illustrated in figure 13, an N^- layer 13 is formed on the dielectric layer 12 of substrate 10. A larger dose of N type impurities, for example, phosphorus, has been selectively implanted and driven in to form regions 14A and 14C. Next, the strain relieving impurities, for example, arsenic, are introduced, e.g., by a blanket implant, overall into the layer 13. Finally, P-type impurities, for example, boron, are

selectively implanted in regions 16B and 16D as shown in Figure 14. The wafer is then heated to drive-in the arsenic and the boron. The resulting concentration of stress compensating impurities should not significantly counter dope any of the regions formed. For example, the N type arsenic implant should be one tenth to two tenths the P type boron dose used to form the buried regions 16B and 16D.

With the heavily doped regions established, an NPN transistor will be formed in island 18A, a PNP transistor will be formed in island 18B, a buried Zener diode will be formed in island 18C and a capacitor will be formed on island 18D.

To form the collector region of the PNP transistor, P type impurities, for example boron, are introduced by ion implantation into island 18B. To form contacts to the buried regions 14A and 16B, N type impurities, for example phosphorus, are introduced into island 18A and P conductivity type impurities, for example, boron, are introduced into island 18B. Island 18C receives a N^+ implant to simultaneously form one element of a junction Zener diode and a buried contact to the buried N^+ region 14C. A P-type implant in island 18D forms a bottom capacitor plate. The wafer is then heated in the range of 1000°C to 1200°C for a period of 1/2 hour to 3 hours to drive-in all the P and N buried contacts as well as the front collector implants to link up with the respective buried N^+ and P^+ regions. As illustrated in figure 2, this results in N^+ collector contact 26A, P^+ collector contact 28B, N^+ Zener diode

region 26C, the buried contact regions 26C′, and P^+ capacitor bottom plate region 28D. The P^- collector region 24 is also formed in island 18B.

Preferably the N^- regions of the islands 18A, 18C and 18D have an impurity concentration in the range of 3 $X10^{15}cm^{-3}$ to $9x10^{15}cm^{-3}$ or a bulk resistivity in the range of 0.4 ohm-cm to 1.3 ohm-cm. The P^- collector region 24 is formed by implanting a dose ranging between $1x10^{12}cm^{-2}$ and $8x10^{12}cm^{-2}$ at an energy in the range of 200 Kev to 700 Kev. This results in a collector net impurity concentration ranging from $6x10^{15}cm^{-3}$ to $2x10^{16}cm^{-3}$. The dose of the N-type implant which forms regions 26 is in the range of $5x10^{14}cm^{-2}$ to $5x10^{15}cm^{-2}$ at an energy of 50 Kev to 200 Kev. The resulting N^+ contacts and diode region 26 have an impurity concentration in the range of $2x10^{18}cm^{-3}$ to $2x10^{19}cm^{-3}$. Similarly, the P^+ contact and plate region 28 are formed with an implant dose of $5x10^{14}cm^{-2}$ to $5x10^{15}cm^{-2}$ at an energy of 50 Kev to 200 Kev. The resulting P^+ contacts 28 to the buried regions 16 have an impurity concentration in the range of $2x10^{18}cm^{-3}$ to $2x10^{19}cm^{-3}$.

With standard LOCOS techniques, a thick recessed oxide region 30 is formed in the islands to define active device areas. The resulting structure is only schematically illustrated in figure 2 to show that the oxide regions 30 separate the collector contacts from the active base regions. The recessed oxide reduces the base to collector capacitance.

A high quality thin oxide layer 32 is thermally grown on the surface of the substrate to a thickness of 500Å to 2500Å. The thin oxide layer 32 is then patterned and etched to expose the base regions, the Zener region, the contact regions of figure 2 and a contact opening to the bottom capacitor plate region 28D. A remaining portion of layer 32 over plate region 28D serves as the capacitor dielectric.

A first conductor layer of undoped polysilicon is then deposited; selectively doped with a heavy implant; then patterned and etched to simultaneously form, as illustrated in figures 3 and 4, base contacts 40 and 42, collector contacts 41 and 43, Zener diode contact 44, anode contact 45, bottom capacitor plate contact 46 and top capacitor plate 47.

This is followed by the formation of a thick insulative layer 48, e.g., deposited oxide. The layer 48 and the first level of polysilicon are patterned to form contacts and intrinsic base openings. That is, as shown in figure 4, portions of the base contact regions 40 and 42 and overlying portions of the dielectric layer 48 are removed to form openings 49 and 50 which expose the intrinsic base portions of the islands 18A and 18B respectively. A plasma etch provides nearly vertical side walls to the openings 49 and 50 and minimizes overetch into the silicon where the intrinsic base regions will be formed.

Referring next to figure 5, impurities from the first layer of polysilicon are diffused into the single crystalline

islands to produce extrinsic base portions 52 and 56 and sustain ohmic contact portions 54, 56 and 57 in the collector contact regions. In addition, the diffusion step provides a buried Zener junction between previously formed cathode region 26C and an anode region 59 formed from the polysilicon layer 45. An ohmic contact portion similar to the contact portion 58 is also formed in the contact region 28D of the capacitor (not illustrated in figures 5-9). Outdiffusion into the ohmic contact portions compensates for any loss in dopant concentration along the surface which may result from the diffusion process.

During this diffusion, a thin oxide layer 60 is formed on the exposed intrinsic base areas. This oxide serves as a screen for future implants and consumes some of the crystal material which may have been damaged when etching the openings 49 and 50. Simultaneously, a thin sidewall oxide element 60A is formed along exposed portions of the first polysilicon layer as shown in figure 5. For simplicity of illustration, the sidewall element 60A along the first polysilicon layer is not illustrated in subsequent figures.

To form the P-type extrinsic base regions 52, a $5x10^{15}cm^{-2}$ dose of boron is implanted at an energy in the range of 50 Kev. To form the N-type extrinsic base regions 56, a $5x10^{15}cm^{-2}$ dose of phosphorus is implanted at an energy level in a range of 100 Kev. The implants are driven in at a temperature of 900°C to 1050°C for a period of 1/2 hour to 3 hours to produce diffused

P^+ and N^+ regions. The P^+ regions 52 have a net dopant concentration of $1 \times 10^{18} cm^{-3}$ to $1 \times 10^{20} cm^{-3}$ and a depth of 1000Å to 5000Å. The N^+ regions 56 have net dopant concentrations in the range of $1 \times 10^{18} cm^{-3}$ to $1 \times 10^{20} cm^{-3}$ and a depth in the range of 1000Å to 5000Å. Preferably the first polysilicon layer has a thickness in the range of 1000Å to 5000Å and the insulative layer 48 has a thickness in the range of 2000Å to 6000Å. The thin oxide layer 60 has a thickness in the range of 200Å to 1000Å.

A complete description of different formations of buried Zener diodes and their operation is discussed in U.S. patents 4,398,142 to Beasom and 4,652,895 to Roskos, also incorporated herein by reference. Combinations of steps of the present process may be used to form the structure as illustrated therein.

As illustrated in figure 5, P type impurities and N type impurities are selectively implanted through the openings 49 and 50 to form intrinsic base regions 62 and 64 in islands 18A and 18B, respectively. See figure 6.

To isolate the first level polysilicon conductors, and the diffused extrinsic base regions from emitter conductors (to be formed with a subsequent level of polysilicon), side wall spacers are formed along the edge of the first level polysilicon adjacent the emitter openings. Briefly, a nitride layer is deposited over the oxide layer 60 and then

anisotropically etched to form selfaligned insulative spacers 66 along the sides of all the openings in the polysilicon layer. The spacers extend from the first insulative layer 48 to the oxide layer 60. Nitride is the preferred spacer material for reasons discussed below. A feature of the process is that the spacer forms a narrower polysilicon opening to define the emitter region, effectively narrowing the emitter dimension. This reduces the emitter-base junction area, thereby increasing the speed of the resulting transistor.

According to the invention, implants for the intrinsic base regions 62 and 64 are performed after etching the first level of polysilicon and before the spacers 66 are formed. This is advantageous over a process sequence which introduces the intrinsic base implants after spacer formation. That is, with the intrinsic base implants performed prior to spacer definition there is assurance that the heat treatments used to drive in the intrinsic and extrinsic base implants provide sufficient overlap of the diffused regions, i.e., a linkage area sufficiently doped to prevent punch through of the base when the collector-base junction is reverse biased.

Since the spacer 66 is formed all along the sidewall of the first polysilicon level, it will separate the subsequently formed emitter region 74 (or 80) from the edge of the first polysilicon level. With the extrinsic base implants occurring prior to spacer formation, a feature of the present process is that the subsequent emitter implants are aligned with respect

to the spacers 66. Also, since the extrinsic base region 52 (or 56) is formed by outdiffusing dopant from this first polysilicon level, the net separation distance from the emitter to the extrinsic base region is predominantly determined by the width of the spacer less the length of the lateral diffusion of the extrinsic base. By implanting the intrinsic base prior to forming the spacers, the amount of lateral diffusion of the extrinsic base required to link up with the intrinsic base can be minimized. Thus, the resulting space between the extrinsic base and the emitter is a desirably large separation distance which maximizes the current gain and breakdown voltage of the emitter-base junction; and minimizes emitter-base leakage current. In summary the preferred process provides the most desirable bipolar transistor characteristics, e.g., high breakdown voltage and low leakage current, for high frequency analog applications.

Another feature of the preferred process is that the spacers 66 can be defined without damaging the implanted intrinsic base regions. The possibility of etching into the underlying silicon of the intrinsic base during spacer formation is to be avoided because this would remove the implanted dose in an uncontrolled manner. That is, important analog transistor parameters such as current gain, Early voltage, and breakdown voltage would be affected by changes in the integrated dopant concentration of the intrinsic base. The present process prevents degradation of these device parameters

by using the oxide layer 60 as an etch stop during spacer formation.

According to the preferred process, the thin oxide layer 60 is grown before implanting the intrinsic base and depositing the spacer 66. Known dry etch technology is sufficiently selective with respect to oxide that the nitride spacers 66 can be repeatably etched in a manufacturing environment without etching through the oxide layer 60. Thus, the silicon under the nitride/oxide sandwich is not damaged. Within the spacer opening, remaining oxide from the layer 60 is subsequently removed with a wet etchant. For example, a buffered HF solution is extremely selective with respect to both silicon and nitride. Thus, the integrity of the intrinsic base implant is sustained. As indicated in Figure 7, a residual filament of the oxide layer remains under the spacers 66 after the wet etch step. This filament assures electrical isolation between the polysilicon base contact regions and the emitter regions 74, 80.

Another advantage of having the thin oxide region 60 interposed between the nitride spacer and the intrinsic base region is that the quality of the silicon surface is maintained. Nitride films in direct contact with silicon will characteristically induce interface traps and recombination centers at the silicon surfaces. These interface traps and recombination centers will degrade current gain at low collector current levels. A shown in figure 7 the filament of

high quality, interposing thermal oxide region 60 remaining after wet etch will prevent this degradation from occurring.

A second conductor layer of polysilicon 68 is formed over the substrate, as illustrated in figure 7, contacting the exposed base regions of islands 18A and 18B. Patterned photoresist 70 provides an opening 72 to expose the portion of the second polysilicon layer 68 contacting the base region 62 of the NPN transistor. N-type impurities are introduced to the exposed polysilicon. The photoresist 70 is then removed and a second mask of photoresist 76, shown in figure 8, provides an opening 78 to expose the portion of the second polysilicon layer 68 contacting the base region 64 of the PNP transistor. P-type impurities are introduced to the exposed polysilicon. Referring now to figure 9, the second polysilicon layer 68 is patterned and etched to leave doped polysilicon contacts 68A and 68B. Next, the surface is covered with a patterned insulative layer 82, leaving the doped polysilicon contacts 68A and 68B exposed. The wafer is then heated to out- diffuse the implants from the second polysilicon layer into the underlying silicon. The resulting N^+ emitter region 74 and P^+ emitter region 80 are shown in Figure 9. Simultaneously, the ion implanted intrinsic base impurities are driven in to define P intrinsic base region 62 and N intrinsic base region 64.

Alternately, two heat processing steps can be performed. After the N impurities are ion implanted, a first heating step is performed. After the P impurities are ion implanted, the

second polysilicon layer 68 is patterned and the second insulative layer 82 is applied. Preferably the layer 82 is heavily doped, e.g., BPSG. This is followed by a second heating step.

The P type implant which forms the intrinsic base region 62 is, for example, boron with a dose in the range of $5x10^{12}cm^{-2}$ to $5x10^{13}cm^{-2}$ and implanted at an energy of 5 Kev to 40 Kev. The N type intrinsic base region 64 may be formed with a phosphorus implant having a dose in the range of $5x10^{12}cm^{-2}$ to $5x10^{13}cm^{-2}$, and implanted at an energy of 40 Kev to 90 Kev. The-N type implant which forms the emitter 74 is, for example, an arsenic dose in the range of $5x10^{15}cm^{-2}$ to $2x10^{16}cm^{-2}$ implanted at an energy of 50 Kev to 150 Kev. The P-type implant which forms the emitter 80 is, for example, a boron dose in the range of $5x10^{15}cm^{-2}$ to $2x10^{16}cm^{-2;}$ and implanted at an energy of 30 Kev to 80 Kev.

The first heating step is performed in the temperature range of 900°C to 1100°C for a period of one to 45 minutes and the second heating step is performed in the range of 850°C to 1000°C for one to 45 minutes. The resulting P intrinsic base region 62 has a peak net dopant concentration in the range of $4x10^{17}cm^{-3}$ to $1x10^{18}cm^{-3}$ and a depth of 2000Å to 4000Å. The N intrinsic base region 64 has a net peak dopant concentration in the range of $7x10^{17}cm^{-3}$ to $2x10^{18}cm^{-3}$ and a depth in the range of 2000Å to 4000Å. The N^+ emitter region 74 has a net dopant concentration in the range of $1x10^{19}cm^{-3}$ to $1x10^{20}cm^{-3}$ with a depth in the range of 200Å to 1000Å and the P^+ emitter region 80 has

a net dopant concentration in the range of $1x10^{19}cm^{-3}$ to $1x10^{20}cm^{-3}$ with a depth ranging from 200Å to 1000Å.

The resulting complementary bipolar transistor structure has substantially matched base widths in the range of 0.15 to 0.35 microns and substantially matched collector widths in the range of 0.70 to 1.5 microns for an epitaxial layer thickness of 2.0 to 4.0 microns.

The ratio of collector widths between the NPN transistor of island 18A and the PNP transistor of island 18B should be in the range of 0.75 to 1.3. This minimizes the collector series resistance while supporting a breakdown voltage greater than 12 volts. These ratios become possible when phosphorus is used for the N buried region and N base region (instead of arsenic or antimony), and boron is used for the P buried region and P base region. Since boron has a diffusion coefficient very similar to phosphorus, the resulting collector widths are similar.

Apertures 84 and 86 are etched in the insulative layer 82 and the insulative layer 48 before the second heat treatment. By forming the apertures before the second heat treatment a BPSG layer 82 provides smoother topology. After aperture formation, a thin film resistor 88 may be formed with a conventional photoresist lift off technique. This can be followed by forming two metal layers of interconnect.

Figure 10 illustrates a P-type island 18E wherein other resistor structures may be formed. A P^- region 24E is formed

at the time the collector region 24 of figure 2 is formed for the PNP transistor in island 18B. P^+ ohmic contacts 58E and 58E′ are formed in the P^- region by outdiffusion of impurities from the first level polysilicon conductors 43E and 43E′ formed simultaneously with the collector contact 43. Thus the island region 18E provides a resistor region.

A lower resistance, diffused resistor is illustrated in figure 11. An N island 18F having a buried region 14F has extrinsic resistor contact regions 52F and 52F′ formed by out diffusion from resistor contacts of the first level polysilicon layer 40F and 40F′. The intrinsic resistive portion 62F is formed simultaneously with the formation of the intrinsic base portion of the NPN transistor. Additionally, polysilicon resistors may also be formed on the integrated circuit by selectively doping either of the two polysilicon layers.

Junction field effect transistors, JFETS, may be formed alongside the bipolar devices without requiring any additional process steps. As illustrated in figure 12, a P^- island 18G, having a P^+ buried layer 16G and P^- region 24G, includes a P^+ bottom gate contact region 28G formed simultaneously with the buried collector contact region 28B of figure 2. The P^- region 24G forms the bottom gate. The N^+ source and drain regions 56G and 56G′ are formed by outdiffusion from source and drain conductors 42G and 42G′ formed from the first polysilicon layer. The P^+ contact region 58G is formed by outdiffusion from the first level polysilicon. The N channel region 64G is

formed simultaneously with the intrinsic base 64 of figure 9. The P^+ top gate 80G is formed by outdiffusion from a top gate contact 68G during formation of the emitter 80. The recessed dielectric isolated regions 30 are also provided in the bottom gate region 24G. A bottom gate contact 43G is also derived from the first polysilicon layer.

Achievable performance characteristics of an NPN and a PNP transistor formed according to the principles of the present invention are as follows:

Parameter	NPN	PNP
Ft	>7.0GHz	>3.0GHz
Current Gain	>100	>100
Early Voltage	>60V	>40V
BV_{CEO}	>12V	>12V
BV_{CBO}	>12V	>12V

The JFETs will have the following characteristics:

Parameter	NJFET
Ft	>4.0GHz
Vp	>0.5V
BVdss	>5.5V

As will be noted, an attempt has been made to optimize the frequency response along with the Early voltage and breakdown voltages. This is more critical in analog applications than just the frequency response Ft. In digital applications, the above device considerations are not nearly as critical. Some representative parameter ranges for analog and digital transistors are:

Parameter	Analog	Digital
Early voltage	>40V	>3V
Leakage	<100nA	<100μA
Noise	<100 nv/rt-Hz	<1000 nv/rt-Hz

The spacing between the base and buried layer of a transistor has a significant influence on the collector-base breakdown voltage BV_{CBO}, Early voltage, series collector resistance Rcs, and consequently, the frequency response Ft of the transistor. Unfortunately, breakdown voltage and Early voltage are tradeoffs against Rcs and Ft. In an analog application, proper control of each of these parameters is important, and, therefore, the space between the base and buried layer must be carefully designed. This becomes more difficult to accomplish in a complementary process because there are two such spacings to design and control. By using boron and phosphorus for the buried regions and the base regions, matched collector widths are possible. This provides lower collector series resistance while maintaining the collector-base breakdown voltage greater than 12 volts.

Some of the advantages of introducing the intrinsic base prior to spacer formation are as follows. Control over the depth and lateral diffusion of the extrinsic base becomes less critical because the intrinsic base is introduced in relatively close proximity to the extrinsic base prior to formation of the spacer 66; and the emitter implant is performed after spacer formation so that the extrinsic base can be kept relatively far away from the emitter. Among other benefits, this arrangement

sustains a higher current gain and a higher emitter to base breakdown voltage. Control over the width of the spacer becomes less critical because of the increased distance possible between the extrinsic base and the emitter.

The use of a nitride spacer separated from the islands by a thin oxide provides the following benefits to analog transistors. The control of current gain, Early voltage, and breakdown is not affected by the potential removal of silicon by the plasma etch. The leakage of the emitter-base junction is lower because the silicon surface is not damaged by the plasma. The noise of the transistor is less, again due to the silicon not being damaged.

The thin oxide 32, which forms the dielectric of the capacitor and also covers the surface of the islands, is created early in the process immediately prior to the deposition of the first polysilicon. This protects the surface of the islands as well as the purity of the dielectric of the capacitor and thereby improves its performance and reproducibility.

The present invention offers a unique combination of features not previously achievable in a single process and provides capability for designing and developing products that extend the state of the art in the circuit performance. Enhanced frequency response, Early voltage and breakdown voltage provide the products with higher levels of performance at higher frequencies while maintaining or improving the DC

characteristics and minimizing power dissipation. For a given current level, a 60 volt NPN Early voltage and a 40 volt PNP Early voltage, this complementary bipolar process offers about a ten-fold improvement in circuit frequency response over devices made with former processes. The capability is now provided for developing products with higher AC performance at a given level of power dissipation. Conversely, for a given frequency the power consumption can be reduced significantly.

The traditional operational amplifier is known as a voltage feedback amplifier and its application is in virtually all electronic systems. A specific family of operational amplifiers, referred to as high speed, are required in RF, signal processing, communications, medical/industrial imaging, and video systems. Voltage feedback amplifiers are better suited as active filters and integrators than current feedback amplifiers. A comparison of operating characteristics for prior art voltage feedback amplifiers with characteristics of amplifiers constructed with the present invention (figure 15) follow.

Parameter	Prior Art	Present Invention
Unity Gain Bandwidth	350 MHz	700 MHz
Slew Rate	1000V/μs	2500 V/μs
Settling Time (0.1%)	20 ns	6 ns
Supply current	40 mA	20 mA

A current feedback amplifier incorporating bipolar transistors of the present invention will have the following characteristics and is illustrated in block diagram form in figure 16.

Parameter	Prior Art	Present Invention
-3dB Bandwidth	150 MHz min.	500 MHz min
Output Voltage	+/-3Vpp into 100 ohm	+/-3Vpp into 100 ohm
Supply Current	18 mA max	24 mA max
Slew Rate	1600 V/μs	2000 V/μs min

From the above characteristics, it has been shown that a feedback amplifier incorporating the present integrated circuits has a bandwidth of at least 500 MHz and a slew rate of at least 2000 volts per microsecond. Also, the maximum current is below 24 milliamps, and the current feedback amplifier has a settling time of less than 20 ns.

The voltage feedback or current feedback amplifiers may be used to improve the performance of a sample and hold amplifier. A typical implementation is illustrated in figure 17 as including an input transconductance amplifier A1, a low leakage voltage switch SW, and an output integrating amplifier A2. This switch SW is controlled through a sample and hold gate. In previous designs A1 and A2 were voltage feedback amplifiers. With this process the circuit of figure 17 can be configured with either voltage or current feedback amplifiers having the following improved typical characteristics.

Parameter	Prior Art	Voltage Feedback	Current Feedback	
Acquisition Time		500 ns	50 ns	15 ns
Slew Rate	90 V/μs	150 V/μs	500 V/μs	
Bandwidth	4.5 MHz	45 MHz	200 MHz	
Resolution	12 bits	12 bits	12 bits	

Prior digital to analog converters (DACs) have achieved greater than 12 bit resolution by incorporating super Beta transistors and an operational amplifier in a servo loop (not illustrated). A typical prior art cell is illustrated in figure 18A. The speed of the DAC is limited by the bandwidth of the operational amplifier, the capacitance of the R-2R ladder, and the frequency response of the transistors. The superior frequency response provided according to the invention increases the bandwidth of the operational amplifier output by ten-fold for a given power level. Referring to figure 18B the super Beta device is replaced with an N channel JFET providing approximately a ten-fold speed advantage. If the transconductance of the JFET is insufficient to achieve 12 bit match in the DAC cell current source, the PNP/NPN combination shown in figure 18C can be used. The R-2R ladder can be eliminated thereby reducing capacitance by using a fully scaled design, e.g., ratioing device sizes between adjacent cells. This is made possible by smaller lithography. A comparison of the settling times to the one-half LSB is as follows.

Parameter Resolution	Prior Art		Present Invention		
Settling time to		12 bit	14 bit	8 bit	11-12 bit
1/2 LSB	250 ns	400-ns	<10 ns	25 ns	

The present invention provides a PNP transistor with satisfactory series-collector resistance and frequency response characteristics to enable integration of the voltage output

amplifier stage into a current mode DAC to provide current to voltage conversion. This eliminates the need for off-chip current to voltage conversion stages of the prior art DACs.

A switch stage of the pin driver circuit is illustrated in figure 19. It turns on or off the signal path between the input and output by turning on or off a controlled current source. When the switch stage is on, it becomes a low resistance path to DC and AC signals and thus yields small offset voltages and small AC attenuations. When the switch, output or control current sources is off, the output node becomes a high impedance point. Very often, a differential pair is used to turn on or turn off the current source. The output signal on the switch has a rise and a fall time of under one nanosecond.

The current conveyor of figure 20 consists of at least one low impedance input which acts as a virtual ground and at least one high impedance output. The input current injected into the current conveyor through the low impedance input via a resistor and a voltage source, or by at least one current source, is amplified or added to the current of another input before it reaches the output. A current conveyor incorporating a transistor according to the present invention has a high frequency response providing propagation delays of less than 1 nanosecond. The Beta-Early voltage product enables more linear current programming and higher output impedances. It may also be made with complementary bipolar transistors which maintains

the speed requirements while providing the capability of handling bidirectional signals.

An ultra high speed comparator is illustrated in figure 21 having applications in linear and mixed signal test systems, fiber optics communication and high speed data acquisition systems. It can be developed with ECL compatible logic outputs as well as with TTL outputs. The comparator of figure 21 incorporating transistors of the present invention exhibits propagation delays of 0.5 ns (ECL) and 1.0 ns (TTL).

The above examples illustrate improvements in standard circuits which incorporate transistors of the present invention. With these transistor characteristics new circuits heretofore unavailable can also be developed.

Although the present invention has been described and illustrated in detail, it is to be understood that the same is by way of example only, and is not to be taken by way of limitation. The spirit and scope of the present invention are to be limited only by the claims which follow.

WHAT IS CLAIMED:

1. A bipolar transistor formed in an electrically isolated semiconductor island, comprising:

a collector doped to a net first conductivity type and having a more heavily doped region;

a base formed in a region doped to a net second conductivity type concentration adjoining the collector; and

an emitter doped to the net first conductivity type adjoining the base, said transistor having an Early voltage of at least 40 volts, and a frequency response of at least 3 GHz.

2. A transistor according to claim 1 characterized by a current gain of at least 100 and a BV_{CBO} of at least 12 volts.

3. A transistor according to claim 1 in an integrated circuit formed along a planar semiconductor surface, wherein:

the transistor is vertically structured with respect to the surface;

the heavily doped region of the collector is buried below the surface;

the base is positioned above the heavily doped buried collector region; and

the emitter is positioned above the collector in a region surrounded by the doped region in which the base is formed.

4. The transistor of claim 3 wherein the collector is of N-type conductivity said transistor having a frequency response of at least 7 GHz.

5. An integrated circuit along a semiconductor surface comprising a first PNP transistor formed in a first electrically isolated semiconductor island and a second NPN transistor formed in a second electrically isolated semiconductor island wherein:

the first transistor includes a P-conductivity type collector having a heavily doped region adjoining a more lightly doped region of the same conductivity type; and

the second transistor includes a N-conductivity type collector having a more heavily doped region of the same conductivity type.

6. The integrated circuit of claim 5 wherein said first and second transistors each have an Early voltage of at least 40 volts, a BV_{CBO} of at least 12 volts and a frequency response of at least 3 GHz.

7. The integrated circuit of claim 6 wherein said NPN transistor has an Early voltage of at least 60 volts.

8. The circuit of claim 5 wherein the first and second transistors each have a current gain of at least 100.

9. The integrated circuit of claim 5 wherein the first and second transistors are each vertically structured with respect to the semiconductor surface with the heavily doped collector region below the surface and the more lightly doped collector region positioned between the surface and the heavily doped collector region, each transistor further including:

a base formed in a region adjoining the more lightly doped collector region; and

an emitter positioned above the heavily doped collector region and surrounded by the region in which the base is formed.

10. The circuit of claim 9 wherein at least one of the first and second transistors is characterized by the lightly doped collector region having a width in the range of 0.7 to 1.5 microns and a peak net dopant concentration in the base at least fifty times the peak net dopant concentration in the more lightly doped collector region.

11. The circuit of claim 9 wherein the first and second transistors are each characterized by:

a base width of 0.15 to 0.35 microns; and

a lightly doped collector width extending 0.7 to 1.5 microns from the base to the heavily doped collector region.

12. The circuit of claim 5 wherein the first and second transistors each have a base whose peak net dopant concentration is at least fifty times the peak net dopant concentration in the more lightly doped collector region.

13. The circuit of claim 5 wherein:

each island comprises a first epitaxially grown semiconductor layer of a first thickness formed over an adjoining second semiconductor layer of a second thickness;

the heavily doped collector region of each transistor is formed predominantly in the second layer of the transistor island;

a base region for each transistor is formed entirely in the first layer of the transistor island;

the more lightly doped collector region of each transistor is formed in the first layer of the transistor island between the base region and the heavily doped collector region;

the collector width for each transistor corresponds substantially to the portion of the first layer thickness between the base region and the heavily doped collector region; and

the width of the second transistor lightly doped collector region ranges from 0.75 to 1.3 times the width of the first transistor lightly doped collector region.

14. The circuit of claim 5 wherein the heavily doped region of the first transistor's collector is predominantly doped with boron and the heavily doped region of the second transistor's collector is predominantly doped with phosphorus.

15. The circuit of claim 9 wherein the bases of the first and second transistors have similar diffusion depths below the semiconductor surface providing each transistor with a substantially similar collector width.

16. The circuit of claim 9 wherein the base of the first transistor is doped with phosphorus and the base of the second transistor is doped with boron.

17. The circuit of claim 9 comprising a plurality of additional PNP and NPN transistors vertically structured like the first and second transistors with the emitter positioned above the collector and in a region surrounded by the region in which the base is formed.

18. The circuit of claim 17 further including an N-channel JFET having a frequency response of at least 4 GHz and formed in a third electrically isolated semiconductor island.

19. The circuit of claim 17 configured to perform digital to analog conversion with at least eleven bit resolution and a settling time to 1/2 LSB of less than 30 nanoseconds.

20. The circuit of claim 19 wherein some of the transistors are configured to provide an integrated current to voltage output stage for converted signals.

21. The circuit of claim 17 configured as a feedback amplifier characterized by a bandwidth of at least 500 MHz and a slew rate of at least 2,000 volts per microsecond.

22. The circuit of claim 21 capable of operating with a supply current less than 25 milliamps.

23. The feedback amplifier circuit of claim 21 characterized by a settling time less than 10 nanoseconds.

24. The circuit of claim 21 configured as a current feedback amplifier having an output voltage of ± 3 volts peak to peak into a 100 ohm load.

25. The circuit of claim 19 configured as a plurality of feedback amplifiers to provide a sample and hold circuit having an acquisition time less than 50 nanoseconds.

26. The sample and hold circuit of claim 25 characterized by a slew rate of at least 100 volts per microsecond and a bandwidth of at least 20 MHz.

27. The circuit of claim 19 configured as a comparator characterized by a propagation delay less than 1.5 nanoseconds.

28. The comparator circuit of claim 27 characterized by ECL compatible output levels and a propagation delay less than one nanosecond.

29. The circuit of claim 5 wherein:

the first and second transistor's collectors are each formed in monocrystalline semiconductor material predominantly comprising silicon;

the heavily doped region of the first transistor's collector is predominantly doped with boron to provide a net P type conductivity;

the heavily doped region of the second transistor's collector is predominantly doped with phosphorus to provide a net N type conductivity; and

at least one of the heavily doped transistor collector regions includes additional impurity, characterized by an atomic radius greater than the atomic radius of silicon, at a concentration less than the net dopant concentration to reduce lattice strain.

30. The circuit of claim 29 wherein said additional impurity is selected from the group consisting of arsenic, antimony and germanium.

31. The circuit of claim 9 wherein the distance from the base to the heavily doped collector region in the second transistor ranges from 0.75 to 1.3 times the distance from the base to the heavily doped collector region of the first transistor.

32. The circuit of claim 5 wherein the first and second semiconductor islands are formed on an insulative layer and electrically isolated from one another by a trench extending into the semiconductor surface to the insulative layer, said trench defined by a wall portion comprising dielectric material.

33. The circuit of claim 9 wherein the first and second transistors each include:

a collector contact region extending from the semiconductor surface to the heavily doped collector region; and

an insulative region recessed in the semiconductor surface to provide electrical isolation between the base and the collector contact region.

34. The circuit of claim 9 including a field effect transistor formed in a third semiconductor island comprising:

spaced apart source and drain regions formed along the semiconductor surface;

a channel region between the source and drain regions; and

a first gate region operatively positioned to control current flow between the source and drain regions within the channel region.

35. The circuit of claim 34 wherein the field effect transistor is a JFET with the first gate region formed along the semiconductor surface, said JFET further comprising a second gate region formed within the third island, said channel region positioned between the first and second gate regions.

36. The circuit of claim 34 wherein:

the bases of the first and second transistors each comprise an intrinsic base region surrounded by a more heavily doped extrinsic base region;

the channel region being formed during intrinsic base formation has similar structure to said intrinsic base; and

the source and drain regions being formed during extrinsic base formation has similar structure to said extrinsic base.

37. A method for fabricating a bipolar transistor having extrinsic and intrinsic base regions along a semiconductor surface with an emitter region formed within the intrinsic base region, comprising the steps of:

etching a first opening in a first conductor level overlying the surface for formation of the intrinsic base region;

outdiffusing dopant of a first conductivity type from the first conductor level adjacent the opening to form the extrinsic base region;

performing a dopant implant of the first conductivity type aligned with the etched opening to create the intrinsic base region;

forming a spacer element along the periphery of the etched opening to define a second opening within the first opening for emitter formation; and

forming the emitter region in the surface through the second opening with dopant of a second conductivity type.

38. The method of claim 37 wherein the step of forming the spacer element includes forming the spacer element of silicon nitride and anisotropically etching silicon nitride, said method further including the step of forming an oxide layer on the semiconductor surface prior to forming the spacer element.

39. A bipolar transistor formed on an integrated circuit structure comprising:

a layer of monocrystalline semiconductor material;

a first conductor layer overlying the semiconductor layer and having a first opening extending to the semiconductor layer;

an extrinsic base region in the semiconductor layer, extending along the first conductor layer and surrounding the first opening;

an intrinsic base region within the semiconductor layer, surrounded by the extrinsic base region and self-aligned with respect to the first opening;

a spacer element, within the first opening and adjoining the first conductor layer defining a second opening within the first opening; and

an emitter region within the intrinsic base region and self-aligned with respect to the second opening.

40. The transistor of claim 39 further comprising an oxide filament adjoining the first conductor layer and the intrinsic base region, said filament interposed between the semiconductor layer and the spacer element.

41. An integrated circuit in a silicon substrate comprising:

a NPN transistor with a heavily doped buried collector region having net conductivity established predominantly with phosphorus at a first concentration, said region further including second impurity atoms at a second concentration less than the first concentration, said second atoms having a larger atomic radius than silicon.

42. The circuit of claim 41 wherein the second impurity atoms are selected from the group consisting of arsenic, antimony and germanium at a second concentration in the range of 0.1 to 0.2 times the first concentration.

43. The circuit of claim 41 further comprising a PNP transistor with a heavily doped buried collector region having a net conductivity type established predominantly with boron at a third concentration, said region including fourth impurity atoms at a fourth concentration less than the third concentration, said fourth atoms having a larger atomic radius than silicon.

44. The circuit of claim 43 wherein:

the second and fourth impurity atoms are arsenic; and

the fourth concentration is in the range of 0.1 to 0.2 times the first concentration.

45. An integrated circuit structure comprising:

a monocrystalline layer of semiconductor material;

a layer of conductor contacting a surface of the semiconductor material, said conductor including an opening having a wall extending through said conductor from an upper surface thereof to the semiconductor surface;

an oxide filament against the semiconductor surface and against a portion of the wall adjoining the semiconductor surface;

a nitride spacer separated from the semiconductor surface by the filament and positioned against a portion of the wall extending from the filament toward the upper surface of said conductor.

46. The circuit structure of claim 45 including a transistor with an extrinsic base region formed in the semiconductor surface wherein said conductor physically contacts the base region.

47. The structure of claim 46 wherein the spacer defines an area on the semiconductor surface and the transistor includes an emitter region in the semiconductor layer, formed in the area and separated from the extrinsic base region.

48. A method for making a pair of complementary bipolar transistors comprising the steps of:

forming a heavily doped N-type buried region in an electrically isolated semiconductor layer with N-type impurities;

forming a heavily doped P-type buried region in a second electrically isolated semiconductor layer with P-type impurities having a diffusion coefficient similar to the diffusion coefficient of the N-type impurities; such that when thermally processed, the P-type and N-type impurities diffuse similar distances within respective semiconductor layers.

49. The method of claim 48 wherein the ratio of one diffusion coefficient to the other is in the range from 0.5 to 2.0.

50. The method of claim 48 wherein the P-type impurity is boron and the N-type impurity is phosphorus.

51. The method of claim 48 including the step of establishing a net dopant concentration in each transistor base region with an impurity of conductivity type different than that of the transistor's heavily doped buried region, wherein the ratio of diffusion coefficients between the base impurities is in the range of 0.5 to 2.0.

52. The method of claim 51 wherein the step of establishing the base region is performed to result in the

separation distance between the base and buried region in each transistor being in the range from 0.7 to 1.5 microns.

53. The method of claim 51 including the steps of forming a lightly doped collector region adjoining the buried region of each transistor; and

wherein for each transistor the base region includes a peak net dopant concentration at least fifty times the peak net dopant concentration in the lightly doped collector region.

54. The method of claim 48 wherein the semiconductor layers predominantly comprise monocrystalline silicon and the net dopant concentration in one of the buried layers is predominantly established with a first concentration of impurity atoms having a smaller radius than atomic silicon, the method including the additional step of:

introducing impurity atoms having a larger radius than atomic silicon into said one buried layer at a concentration less than the first concentration in order to reduce lattice defects.

55. A method of forming an integrated circuit structure comprising the steps of:

forming a layer of conductor material over a surface of a layer of semiconductor material;

forming an opening in the conductor layer which defines a wall extending through the conductor layer from an upper surface thereof to the semiconductor surface;

forming an oxide filament against the semiconductor surface and against the wall;

forming a nitride spacer against the wall with the oxide filament interposed between the spacer and the semiconductor surface.

56. The method of claim 55 wherein the spacer is isolated from the semiconductor surface by the filament.

57. The method of claim 55 wherein the steps of forming the filament and spacer include:

sequentially forming layers of oxide and nitride in the opening;

etching through the nitride layer to define a second opening extending through the nitride spacer to the oxide layer;

extending the second opening through the oxide layer to expose the semiconductor surface with an etchant more selective to oxide than nitride.

58. The method of claim 57 wherein the second opening is etched through the oxide layer with a buffered HF solution leaving the filament against the wall.

59. A process of fabricating an integrated circuit in a plurality of isolated islands on a wafer comprising:

forming first insulative regions having openings which expose at least the base area of a first island of a first conductivity type in which a bipolar transistor is to be formed;

forming a first layer of polycrystalline semiconductor on said wafer;

selectively doping portions of said first polycrystalline layer contacting said base area of said first island with impurities of a second conductivity type to form a base conductor;

forming a second insulative layer over said wafer;

removing a portion of said base conductor and superimposed second insulative layer to expose an intrinsic base area of said first island;

forming a third insulative layer over said exposed intrinsic base area;

diffusing said impurities from said base conductor into said first island to form an extrinsic base region;

selectively introducing second conductivity type impurities into said intrinsic base area of said first island to form an intrinsic base region;

forming lateral spacers on the lateral walls of said base conductor and on said third insulative layer adjacent said intrinsic base area, with exposed portions of said third

insulative layer therebetween, and separated from said intrinsic base region by said third insulative layer;

selectively removing said exposed portions of said third insulative layer; and

introducing impurities of said first conductivity type into said intrinsic base region to form an emitter region.

60. The process of claim 59, wherein the step of introducing impurities to form said emitter region includes:

forming a second layer of polycrystalline semiconductor on said wafer;

selectively doping portions of said second polycrystalline layer contacting said intrinsic base area of said first island with said first conductivity type impurities to form an emitter conductor; and

diffusing impurities from said emitter conductor into said first island to form said emitter region.

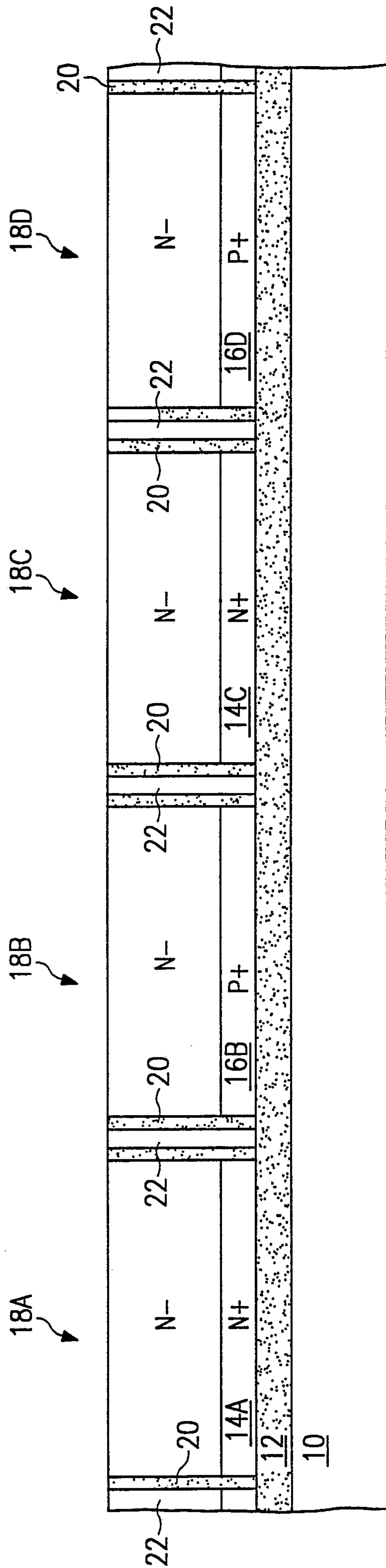

FIG. 1

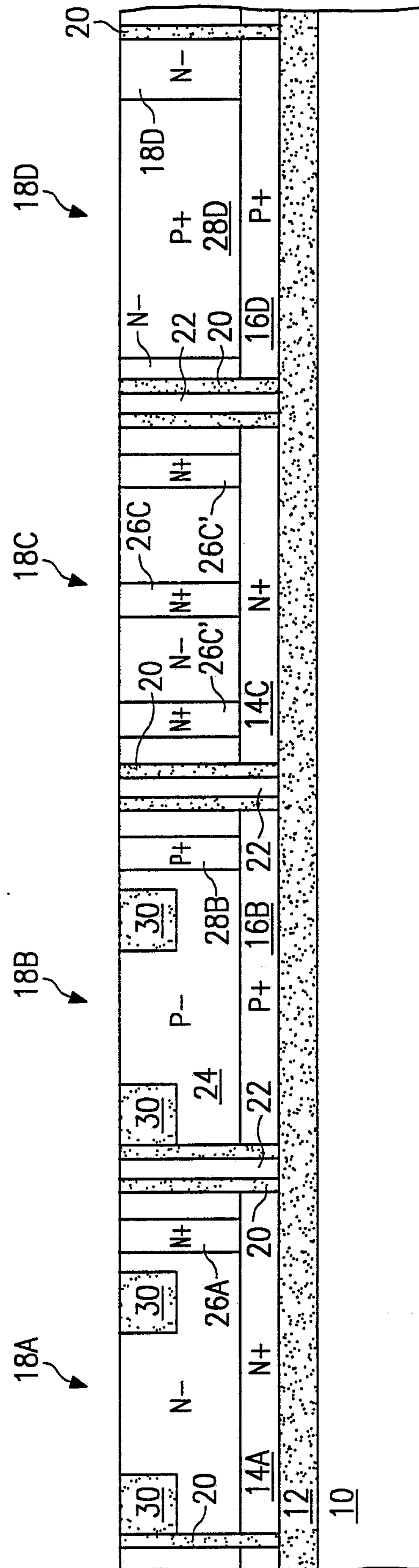

FIG. 2

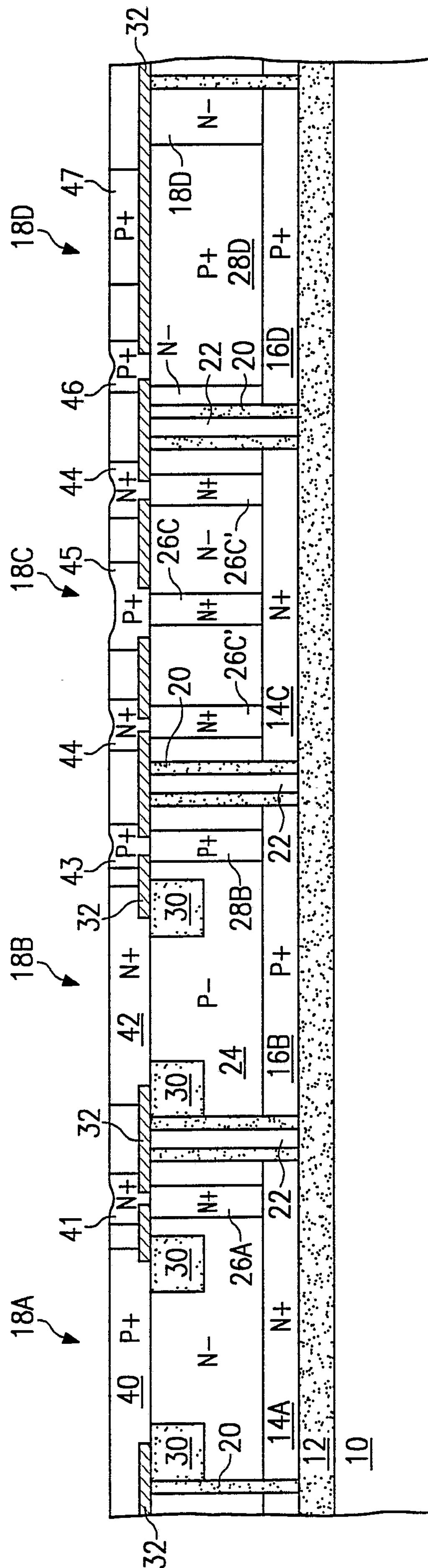

FIG. 3

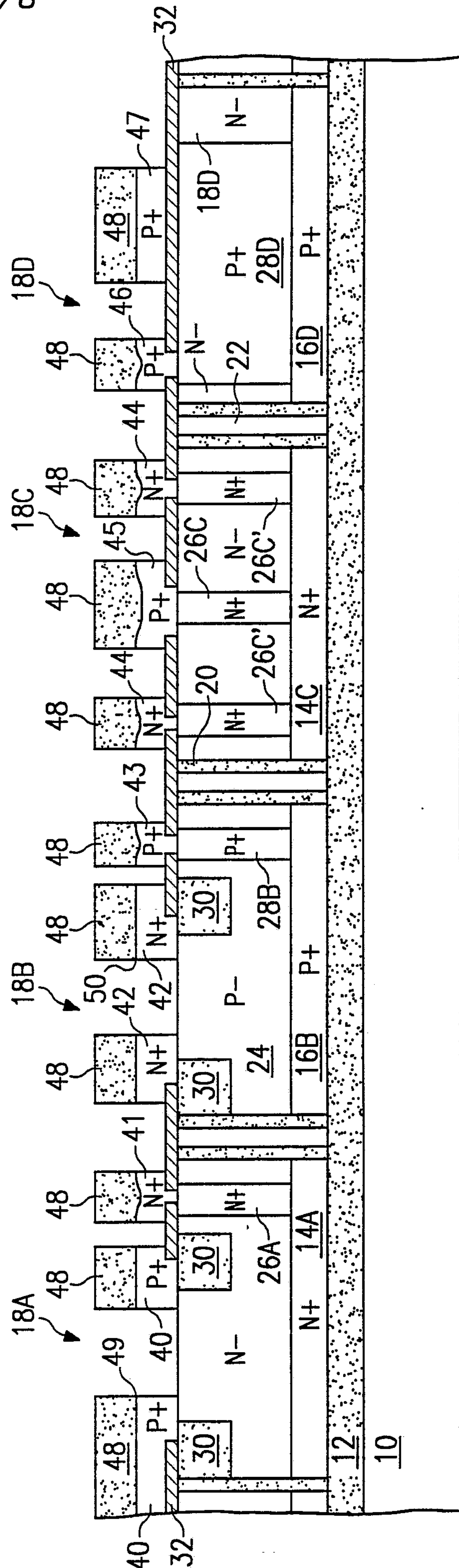

FIG. 4

FIG. 5

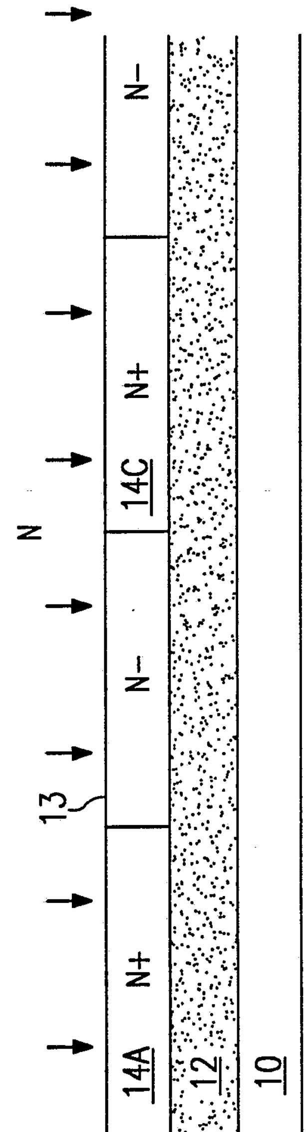

FIG. 13

FIG. 6

FIG. 14

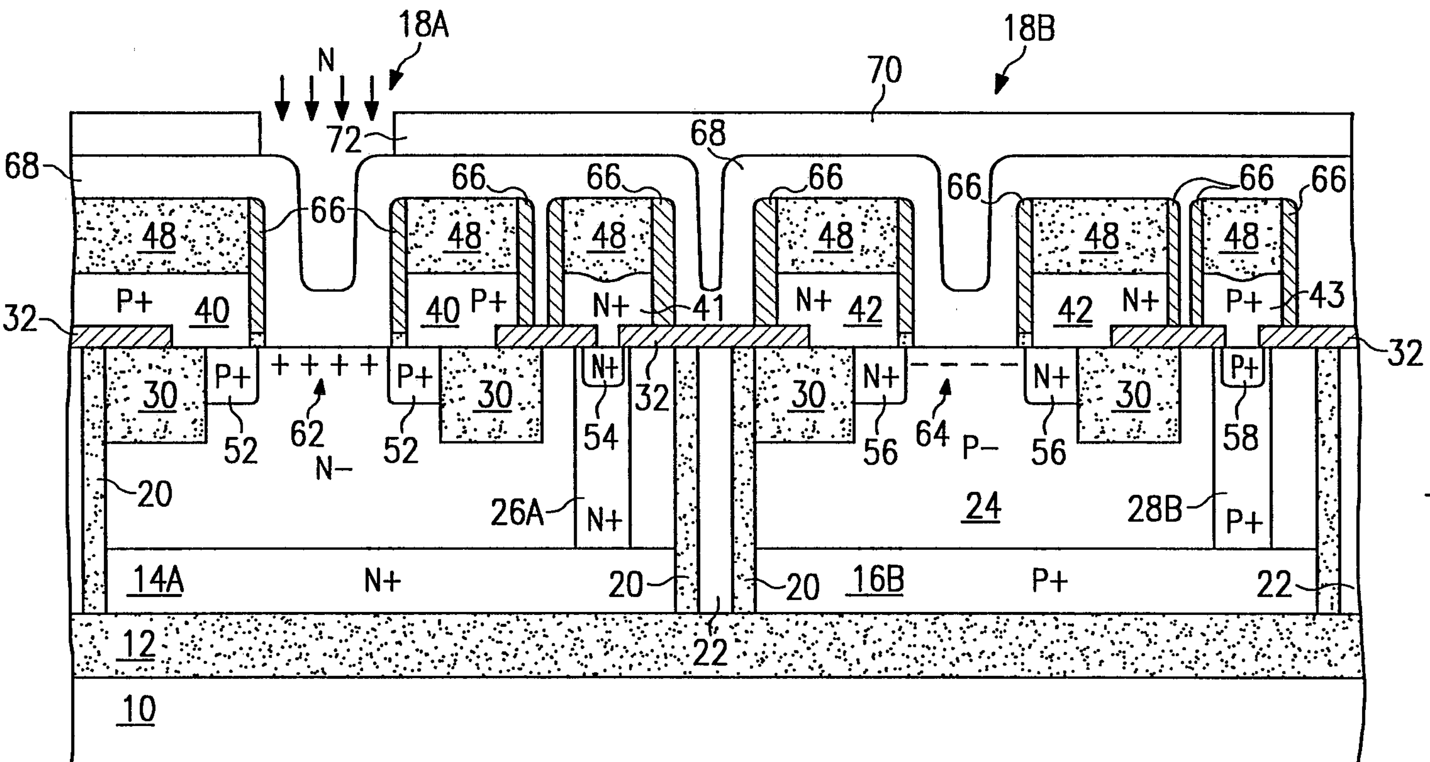

FIG. 7

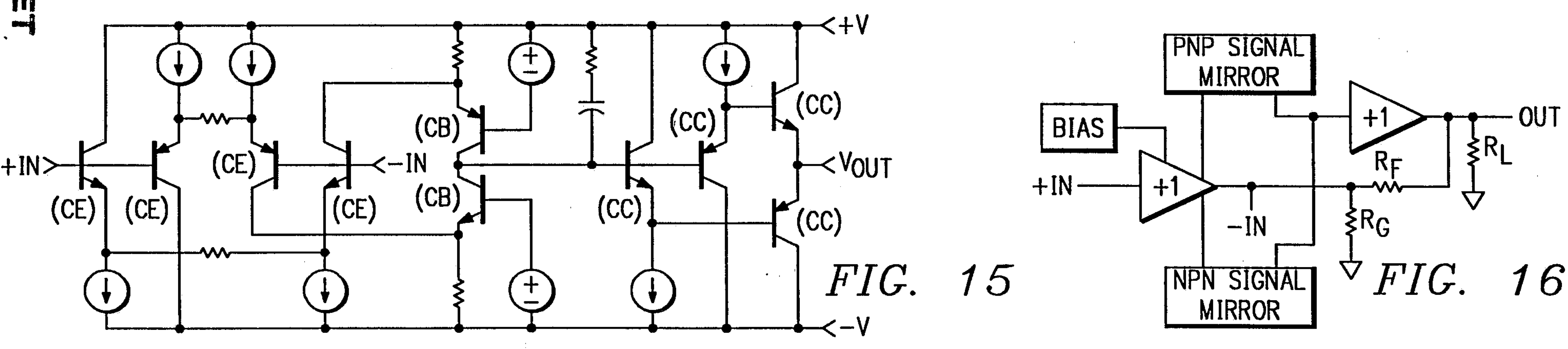

FIG. 15

FIG. 16

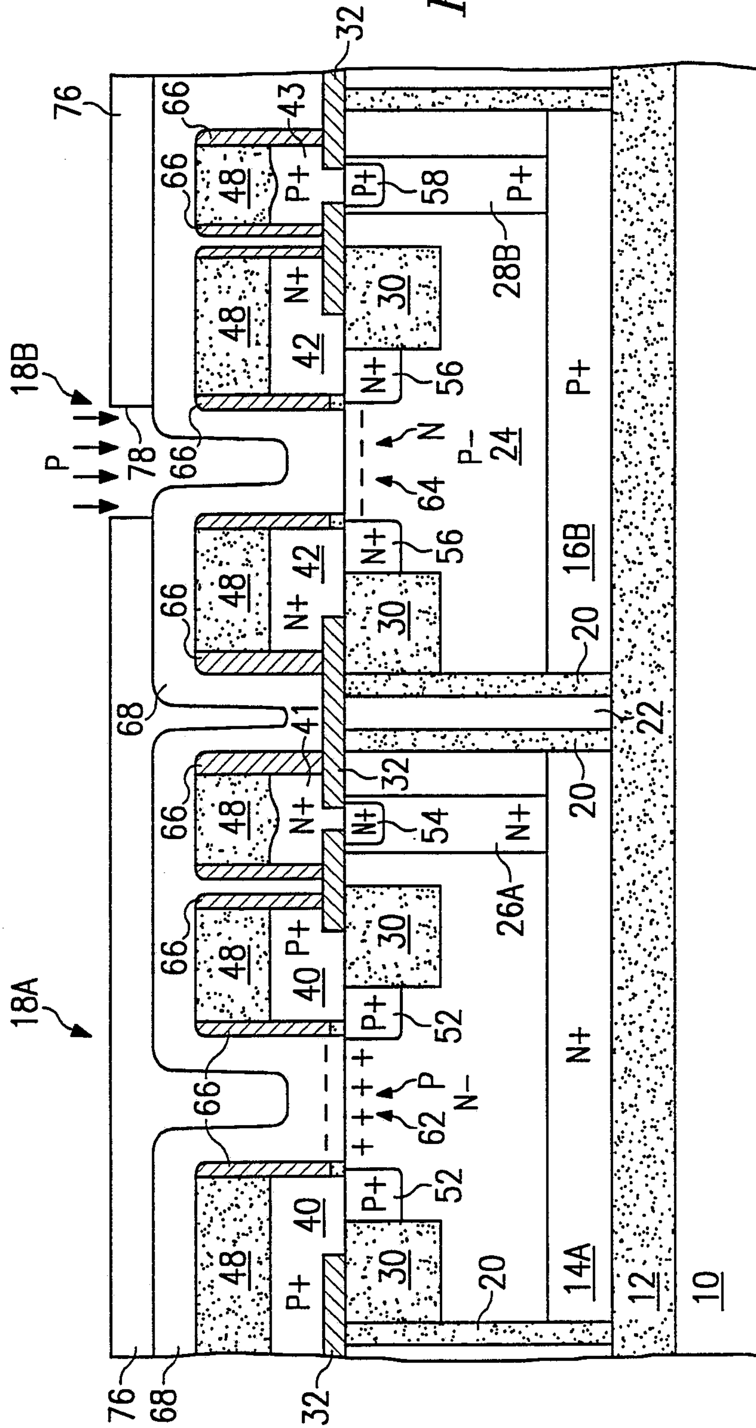

FIG. 8

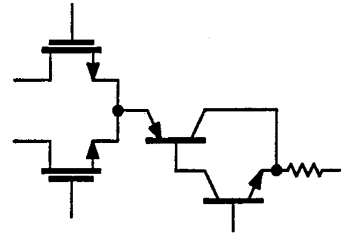

FIG. 18C

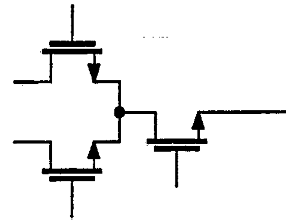

FIG. 18B

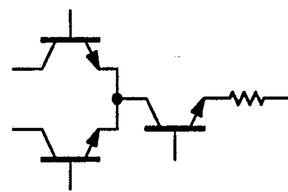

FIG. 18A (PRIOR ART)

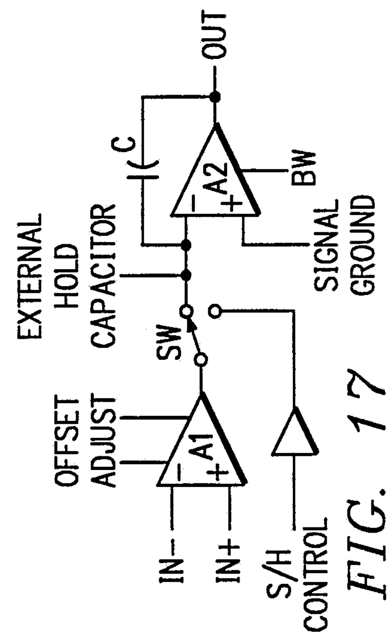

FIG. 17

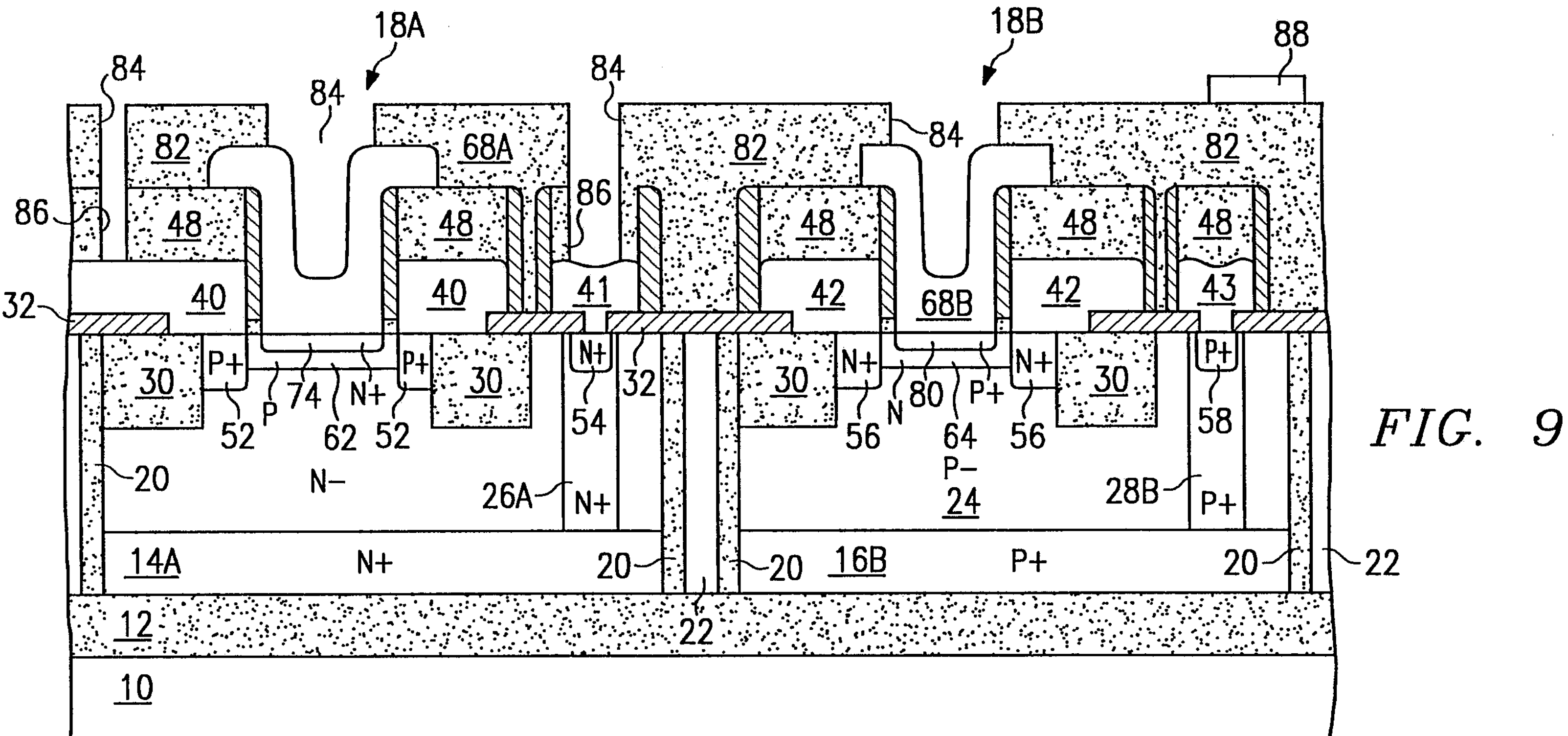

FIG. 9

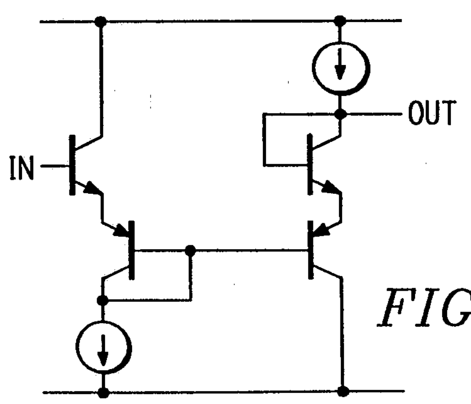

FIG. 19

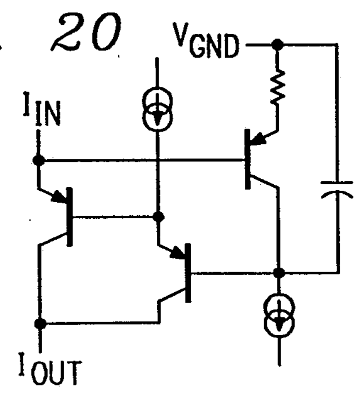

FIG. 20

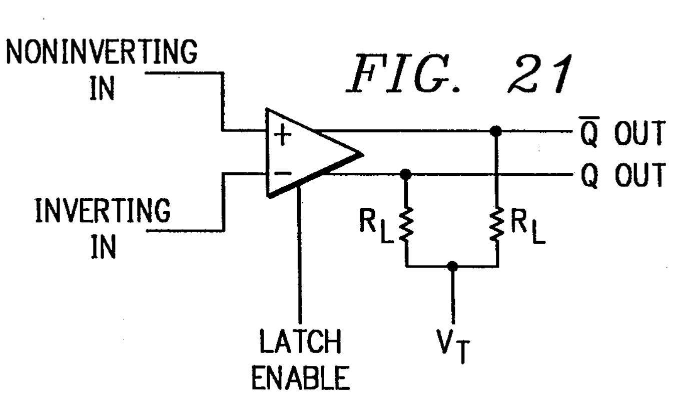

FIG. 21

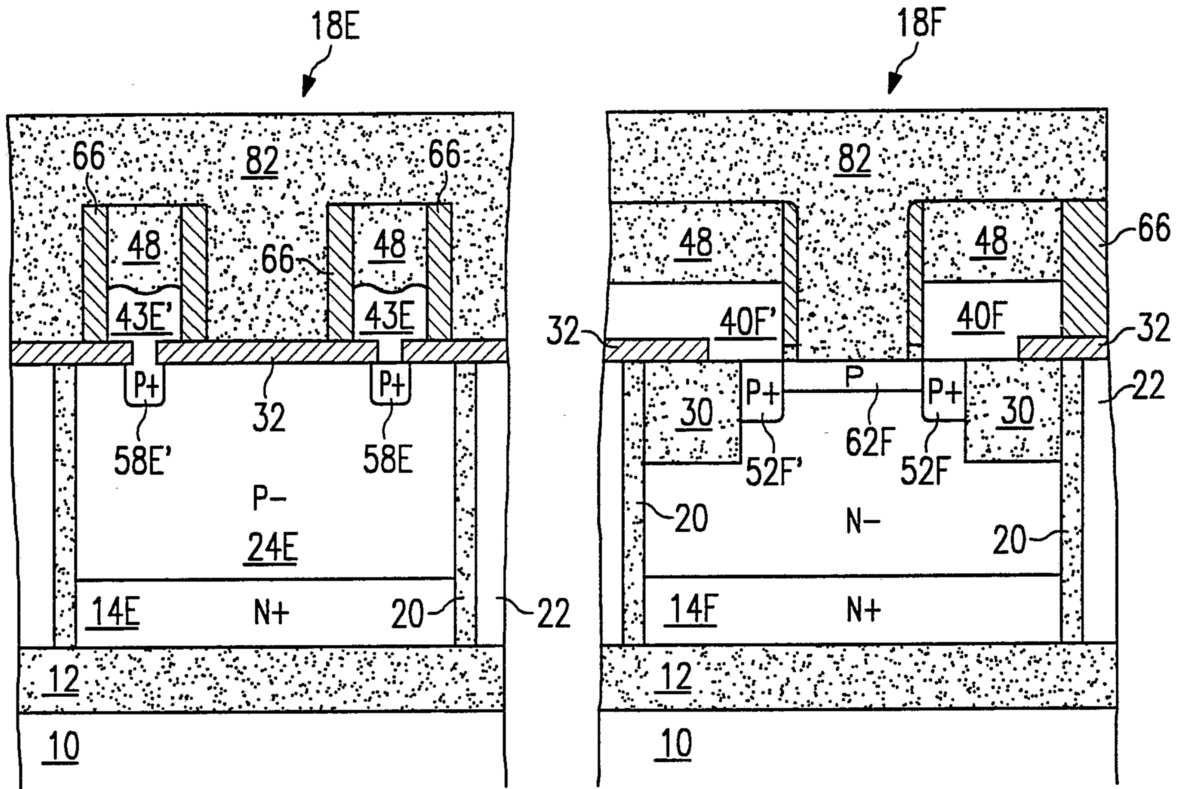

FIG. 10

FIG. 11

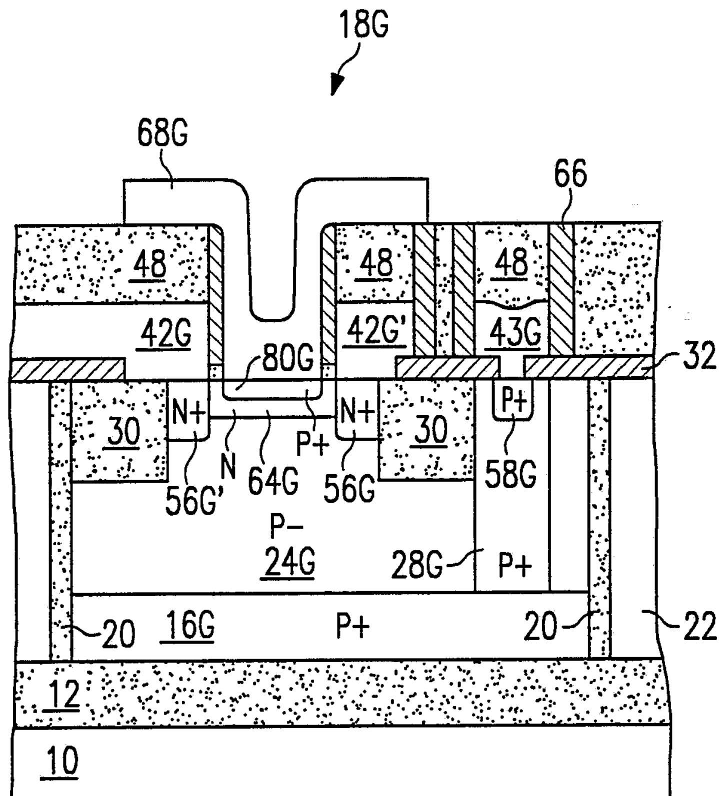

FIG. 12

INTERNATIONAL SEARCH REPORT

International Application No PCT/US 92/08211

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all)[6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC5: H 01 L 29/73, H 01 L 29/80, H 01 L 27/06

II. FIELDS SEARCHED

Minimum Documentation Searched[7]

Classification System	Classification Symbols
IPC5	H 01 L

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in Fields Searched[8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT[9]

Category *	Citation of Document,[11] with indication, where appropriate, of the relevant passages[12]	Relevant to Claim No.[13]
A	US, A, 4969823 (LAPHAM ET AL) 13 November 1990, see column 2, line 11 - line 44; abstract; figure 12; claim 1 --	1-60
P,A	US, A, 5065214 (LAPHAM ET AL) 12 November 1991, see the whole document --	1-60
A	EP, A1, 405045 (SGS-THOMSON MICROELECTRONICS S.R.L.) 2 January 1991, see column 2, line 52 - column 3, line 23; abstract; figure 3 --	1-60

* Special categories of cited documents: [10]

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IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
14th January 1993	02 FEB 1993
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	Stig Edhborg

Form PCT/ISA/210 (second sheet) (January 1985)

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category *	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No
A	US, A, 4583106 (ANANTHA ET AL) 15 April 1986, see column 2, line 32 - column 4, line 40; abstract; figures 1-5	37,38, 48-60
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A	US, A, 4786960 (JEUCH) 22 November 1988, see column 2, line 13 - column 3, line 19; abstract; figure 9	33,37-40,55-60
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ANNEX TO THE INTERNATIONAL SEARCH REPORT ON INTERNATIONAL PATENT APPLICATION NO. PCT/US 92/08211

SA 65257

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report.
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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US-A- 4969823	13/11/90	US-A- 5065214	12/11/91
US-A- 5065214	12/11/91	US-A- 4969823	13/11/90
EP-A1- 405045	02/01/91	NONE	
US-A- 4583106	15/04/86	DE-A- 3466832 EP-A-B- 0137906 JP-A- 60045065 US-A- 4546536	19/11/87 24/04/85 11/03/85 15/10/85
US-A- 4786960	22/11/88	EP-A-B- 0172772 FR-A-B- 2569055 JP-A- 61043469	26/02/86 14/02/86 03/03/86

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