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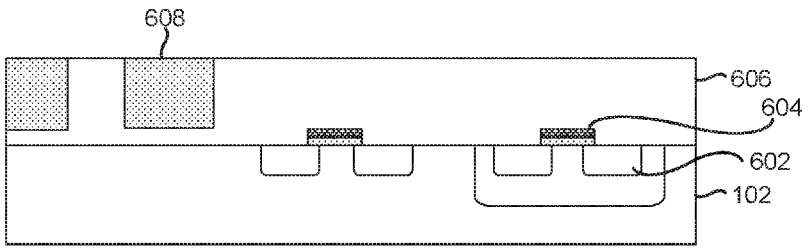

Figure 6B

(57) Abstract: A method for removing nuclei formed during a selective epitaxial growth process includes epitaxially growing a first group of one or more semiconductor structures over a substrate with one or more mask layers. A second group of a plurality of semiconductor structures is formed on the one or more mask layers. The method also includes forming one or more protective layers over the first group of one or more semiconductor structures. At least a subset of the second group of the plurality of semiconductor structures is exposed from the one or more protective layers. The method further includes, subsequent to forming the one or more protective layers over the first group of one or more semiconductor structures, etching at least the subset of the second group of the plurality of semiconductor structures.

Methods for Removing Nuclei Formed during Epitaxial Growth

TECHNICAL FIELD

[0001] This application relates generally to methods for manufacturing semiconductor devices. More particularly, the disclosed embodiments relate to methods for removing nuclei formed on semiconductor devices during epitaxial growth processes.

BACKGROUND

[0002] Epitaxial growth is a popular method of creating a crystalline region on a semiconductor substrate. However, formation of semiconductor structures in unwanted regions of the semiconductor substrate is undesirable. For example, any semiconductor structures grown in unwanted regions of the semiconductor substrate can adversely affect the electrical and/or mechanical properties of a device formed on the substrate.

[0003] Selective epitaxial growth (SEG) is used for creating a crystalline region on targeted areas of the semiconductor substrate. For a selective epitaxial growth, a semiconductor substrate is covered with a masking material, exposing certain areas of the underlying substrate. For such semiconductor substrate, the epitaxial growth occurs mainly on the exposed areas of the semiconductor substrate, and less so on the masking material. Although the selective epitaxial growth may reduce formation of structures (e.g., in the form of nuclei or layers) on the masking material during the epitaxial growth, depending on the process conditions, many semiconductor structures may still form on the masking material during the epitaxial growth.

[0004] Various attempts have been made to eliminate the formation of the epitaxially grown structures on the masking material. For example, certain growth conditions have been found to further suppress the formation of the epitaxially grown structures on the masking material. However, a small deviation from the prescribed growth conditions can easily lead to an increased formation of epitaxially grown structures on the masking material. Thus, the use of such growth conditions is limited.

SUMMARY

[0005] Thus, there is a need for improved methods of removing nuclei formed during epitaxial growth. In some embodiments, the methods would be less-sensitive to changes to the growth conditions. Thus, such improved methods would also enable faster epitaxial growth of semiconductor structures while reducing the formation of semiconductor structures on unwanted regions of the substrate during the epitaxial growth.

[0006] A number of embodiments that overcome the limitations and disadvantages described above are presented in more detail below. These embodiments provide devices and methods for making such devices.

[0007] As described in more detail below, some embodiments involve a method for removing nuclei formed during a selective epitaxial growth process that includes epitaxially growing a first group of one or more semiconductor structures on a substrate with one or more mask layers. A second group of a plurality of semiconductor structures is formed on the one or more mask layers. The method also includes forming one or more protective layers over the first group of one or more semiconductor structures. At least a subset of the second group of the plurality of semiconductor structures is exposed from the one or more protective layers. The method further includes, subsequent to forming the one or more protective layers over the first group of one or more semiconductor structures, etching at least the subset of the second group of the plurality of semiconductor structures.

[0008] In accordance with some embodiments, a semiconductor device includes a substrate; a first mask layer region that is located over the substrate; and a second mask layer region that is located over the substrate. The first mask layer region has a top surface and a lateral surface, and the second mask layer region has a top surface and a lateral surface. The semiconductor device also includes an epitaxially grown semiconductor structure of a first semiconductor material type. The epitaxially grown semiconductor structure is located between the lateral surface of the first mask layer region and the lateral surface of the second mask layer region, and the epitaxially grown semiconductor structure is in contact with the lateral surface of the first mask layer region and the lateral surface of the second mask layer region. The top surface of the first mask layer region and the top surface of the second mask layer region are not in contact with a semiconductor of the first semiconductor material type other than the epitaxially grown semiconductor structure located between the lateral surface of the first mask layer region and the lateral surface of the second mask layer region.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] For a better understanding of the aforementioned aspects as well as additional aspects and embodiments thereof, reference should be made to the Description of Embodiments below, in conjunction with the following drawings.

[0010] Figures 1A-1I are partial cross-sectional views of a semiconductor substrate in accordance with some embodiments.

[0011] Figures 2A-2C are partial cross-sectional views of a semiconductor substrate in accordance with some embodiments.

[0012] Figures 3A-3C are partial cross-sectional views of a semiconductor substrate in accordance with some embodiments.

[0013] Figures 4A-4C are partial cross-sectional views of a semiconductor substrate in accordance with some embodiments.

[0014] Figures 5A-5E are partial cross-sectional views of a semiconductor substrate in accordance with some embodiments.

[0015] Figures 6A-6B are partial cross-sectional views of a semiconductor substrate in accordance with some embodiments.

[0016] Figures 7A-7C are flow diagrams illustrating a method of removing nuclei formed during a selective epitaxial growth process in accordance with some embodiments.

[0017] Figures 8A-8B are scanning electron microscope (SEM) images of a semiconductor substrate prior to an etching process in accordance with some embodiments.

[0018] Figures 9A-9B are scanning electron microscope (SEM) images of a semiconductor substrate subsequent to an etching process in accordance with some embodiments.

[0019] Like reference numerals refer to corresponding parts throughout the figures.

[0020] Unless noted otherwise, the figures are not drawn to scale.

DESCRIPTION OF EMBODIMENTS

[0021] As explained above, formation of unwanted semiconductor structures in unwanted regions (e.g., over the masking material) can lead to poor electrical and/or

mechanical properties of a semiconductor device. Certain growth conditions have been found to reduce formation of the unwanted semiconductor structures in unwanted regions.

[0022] For example, the substrate is exposed to an etchant (e.g., an HCl gas) during the epitaxial growth (e.g., by mixing the HCl gas with a deposition gas), thereby allowing etching of the unwanted semiconductor structures during the epitaxial growth. By maintaining the etching rate by the etchant higher than the rate at which the unwanted semiconductor structures are formed and lower than the rate of epitaxial growth (of the target semiconductor structures), formation of the unwanted semiconductor structures is reduced or suppressed. However, the presence of an etchant affects the speed of epitaxially growing semiconductor structures. The rate of forming the target semiconductor structures is impeded by the etching reaction, and thus, is slower than the rate of forming the target semiconductor structures in the absence of the etchant. Thus, the reduced rate of forming the target semiconductor structure can be a bottleneck in the overall device fabrication process. In addition, the presence of an etchant affects the shape of the epitaxially grown semiconductor structures. In particular, a ratio of a growth rate in a dominant direction to a growth rate in a non-dominant direction is increased significantly. For example, in germanium epitaxial growth, (100) is the dominant growth direction. When the ratio of the growth rate in the dominant direction to the growth rate in the non-dominant direction is increased, the resulting epitaxially grown germanium structures have a pyramid shape with (311) slope. Thus, the presence of the etchant makes it more challenging to obtain semiconductor structures with shapes different from the pyramid shape. Furthermore, if germanium having the pyramid shape with (311) slope is formed to cover a certain area, the height of the germanium pyramid can be high, which makes it challenging to obtain a planarized surface (e.g., by using a chemical mechanical planarization (CMP) process).

[0023] In another example, lowering the temperature and pressure during the epitaxial growth is believed to reduce formation of the unwanted semiconductor structures during the epitaxial growth. However, lowering the deposition temperature decreases the crystallinity of the grown semiconductor structures, which lead to increased leakage current in the semiconductor device. Lowering the pressure can lead to a lower deposition rate and increase the roughness of the semiconductor structures, which will degrade the performance of the fabricated device.

[0024] In yet another example, increasing a pressure of germane gas (GeH_4) facilitates growth of flat germanium islands, but increases formation of the unwanted semiconductor structures during the epitaxial growth. Similarly, increasing a pressure of hydrogen gas (H_2) facilitates growth of flat germanium islands, but increases formation of the unwanted semiconductor structures during the epitaxial growth.

[0025] Methods that address the above problems are described herein. By epitaxially growing semiconductor structures with no (or less) etchant, the semiconductor structures can be grown faster. In addition, the shape of the semiconductor structures is less affected by the etchant, because no (or less) etchant is present during the epitaxial growth. Furthermore, the pressure and/or temperature need not be lowered during the epitaxial growth. Although the epitaxial growth with no (or less) etchant (and at the normal pressure and temperature) will lead to formation of semiconductor structures on unwanted regions, such as on the masking material, such semiconductor structures on the unwanted regions are subsequently removed by an etching process. Thus, semiconductor structures epitaxially grown in target areas of the substrate can be obtained with no or reduced semiconductor structures grown in the unwanted regions.

[0026] Reference will be made to certain embodiments, examples of which are illustrated in the accompanying drawings. While the underlying principles will be described in conjunction with the embodiments, it will be understood that it is not intended to limit the scope of claims to these particular embodiments alone. On the contrary, the claims are intended to cover alternatives, modifications and equivalents that are within the scope of the claims.

[0027] Moreover, in the following description, numerous specific details are set forth to provide a thorough understanding of the present invention. However, it will be apparent to one of ordinary skill in the art that the invention may be practiced without these particular details. In other instances, methods, procedures, components, and networks that are well-known to those of ordinary skill in the art are not described in detail to avoid obscuring aspects of the underlying principles.

[0028] It will also be understood that, although the terms first, second, *etc*. may be used herein to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from another. For example, a first group

could be termed a second group, and, similarly, a second group could be termed a first group, without departing from the scope of the claims. The first group and the second group are both groups (e.g., of semiconductor structures), but they are not the same group.

[0029] The terminology used in the description of the embodiments herein is for the purpose of describing particular embodiments only and is not intended to limiting of the scope of claims. As used in the description and the appended claims, the singular forms "a," "an," and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will also be understood that the term "and/or" as used herein refers to and encompasses any and all possible combinations of one or more of the associated listed items. It will be further understood that the terms "comprises" and/or "comprising," when used in this specification, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

[0030] Figures 1A-1I are partial cross-sectional views of a semiconductor substrate in accordance with some embodiments.

[0031] Figure 1A illustrates a substrate 102 and a mask layer 104 on the substrate 102. Although the substrate 102 is shown as a wafer in Figures 1A-1I, 2A-2C, 3A-3C, 4A-4C, and 5A-5E, the substrate 102 may include additional features not shown in Figures 1A-1I, 2A-2C, 3A-3C, 4A-4C, and 5A-5E. In some embodiments, the substrate 102 includes silicon devices (e.g., silicon complementary metal-oxide-semiconductor devices as well as any other structures typically formed during the front-end of the line (FEOL) processes). In some embodiments, the substrate 102 includes an oxide layer on the silicon devices (e.g., Figures 6A-6B).

[0032] In some embodiments, the mask layer 104 includes a dielectric material (e.g., silicon dioxide). In some embodiments, the mask layer 104 is made of a dielectric material (e.g., silicon dioxide). The mask layer 104 exposes one or more portions of the substrate 102. In some embodiments, the dielectric material is deposited on the substrate 102 and subsequently etched to expose the one or more portions of the substrate 102. In some embodiments, the substrate 102 is further etched. In some cases, this further etching provides a surface more suitable for epitaxial growth.

[0033] Figure 1B illustrates that a semiconductor structure 106 (e.g., a germanium island) is epitaxially grown. The conditions (e.g., pressure, temperature, and chemical

composition) for epitaxial growth of germanium are well known, and thus, are omitted herein for brevity. However, as explained above, the methods described herein do not require the use of an etchant (e.g., HCl gas) to suppress growth of semiconductor structures on the mask layer 104 during the epitaxial growth, although the use of an etchant is not precluded. The conditions for epitaxial growth can be adjusted to obtain the desired growth profile. Thus, it is possible to customize the shape of the epitaxially grown semiconductor structures.

[0034] Figure 1B also illustrates that semiconductor structures 108 (e.g., particles, which are also called herein nuclei) are also formed on the mask layer 104 during the epitaxial growth of the semiconductor structure 106. The semiconductor structures 108 typically have amorphous and/or poly-crystalline structures, whereas the semiconductor structure 106 has a crystalline structure.

[0035] Figure 1C illustrates that the semiconductor structure 106 continues to grow. Figure 1C also illustrates that additional semiconductor structures 108 are formed on the mask layer 104. Figures 8A and 8B are scanning electron microscope (SEM) images of a substrate after epitaxial growth of a germanium island, which are described in detail below.

[0036] Figure 1D illustrates that the semiconductor structures 108 are aggregated to form a film 110 in some embodiments.

[0037] Figure 1E illustrates that optionally, an adhesive layer 112 is applied (e.g., deposited) over the substrate 102. In Figure 1E, the adhesive layer 112 covers the semiconductor structure 106 and the film 110 on the mask layer 104. In some embodiments, the adhesive layer 112 is a low-thermal oxide. In some embodiments, the adhesive layer 112 is hexamethyldisilazane (HMDS). In some embodiments, the adhesive layer 112 promotes adhesion between the epitaxially grown semiconductor structure 106 and photoresist.

[0038] Figure 1F illustrates a protective layer 114 (e.g., a photo resist layer) is applied over the substrate 102. In Figure 1F, the protective layer 114 covers a portion of the adhesive layer 112 over the semiconductor structure 106. In Figure 1F, the protective layer 114 does not cover the film 110 (e.g., the film 110 is exposed from the protective layer 114, although the film 110 is covered with the adhesive layer 112).

[0039] Figure 1G illustrates that regions not covered by the protective layer 114 have been etched. As a result of etching, the film 110 (and any other unwanted semiconductor structures formed during the epitaxial growth of the semiconductor structure 106) is removed. In addition, a portion of the adhesive layer 112 located over the film 110 is also removed. In

some embodiments, a selective etching process, which removes the film 110 (and any other unwanted semiconductor structures formed during the epitaxial growth of the semiconductor structure 106) faster than protective layer 114, is used (such etching processes are called to have high selectivity) so that the semiconductor structure 106 is maintained while the film 110 and/or any other unwanted semiconductor structures formed during the epitaxial growth of the semiconductor structure 106 are removed. In some embodiments, the etching process is a dry etching process (e.g., plasma etching, deep reactive ion etching, etc.). In some embodiments, the etching process is a wet etching process (e.g., etching with liquid-phase etchants). For example, an advanced silicon etching instrument manufactured by Surface Technology Systems Plc. may be used for the selective etching.

[0040] Figure 1H illustrates that the protective layer 114 and the adhesive layer 112 are removed. Figures 9A and 9B are scanning electron microscope (SEM) images of a substrate after removing the protective layer 114, which are described in detail below.

[0041] Figure 1I illustrates that the semiconductor structure 106 is planarized (e.g., using a CMP process). Because the unwanted semiconductor structures (e.g., nuclei 108 or film 110) have been removed, a CMP process can be readily applied. In addition, because the shape of the semiconductor structure 106 can be adjusted to have a flat top, it is easier to perform a CMP process.

[0042] Figures 2A-2C are partial cross-sectional views of a semiconductor substrate in accordance with some embodiments.

[0043] The processes illustrated in Figures 2A-2C are similar to those illustrated in Figures 1F-1H except that the optional adhesive layer 112 (Figure 1E) is not used. Figure 2A illustrates that the protective layer 114 is applied directly on the semiconductor structure 106 shown in Figure 1D.

[0044] Figure 2B illustrates that regions not covered by the protective layer 114 have been etched, which is similar to the process described above with respect to Figure 1G. As a result of etching, the film 110 (and any other unwanted semiconductor structures formed during the epitaxial growth of the semiconductor structure 106) is removed.

[0045] Figure 2C illustrates that the protective layer 114 is removed, which is similar to the process described above with respect to Figure 1H. Subsequently, the semiconductor structure 106 can be planarized, as described above with respect to Figure 1I.

[0046] Figures 3A-3C are partial cross-sectional views of a semiconductor substrate in accordance with some embodiments.

[0047] The processes illustrated in Figures 3A-3C are similar to those illustrated in Figures 1E-1G except that the semiconductor structures 108 (e.g., particles) remain separate.

[0048] Figure 3A illustrates that the adhesive layer 112 is applied over the semiconductor structure 106 and the semiconductor structures 108 (e.g., particles) on the mask layer 104, which is analogous to the process described above with respect to Figure 1E.

[0049] Figure 3B illustrates that the protective layer 114 is applied over the substrate 102, which is analogous to the process described above with respect to Figure 1F.

[0050] Figure 3C illustrates that regions not covered by the protective layer 114 have been etched, which is similar to the process described above with respect to Figure 1G. As a result of etching, the semiconductor structures 108 are removed. In addition, a portion of the adhesive layer 112 located over the semiconductor structures 108 is also removed.

[0051] In some embodiments, the semiconductor substrate illustrated in Figure 3C is further processed as described above with respect to Figures 1H and 1I. For example, the protective layer 114 and the adhesive layer 112 are removed and the semiconductor structure 106 is planarized to obtain the semiconductor substrate illustrated in Figure 1I.

[0052] Figures 4A-4C are partial cross-sectional views of a semiconductor substrate in accordance with some embodiments.

[0053] The processes illustrated in Figures 4A-4C are similar to those illustrated in Figures 2A-2C except that the semiconductor structures 108 (e.g., particles) remain separate.

[0054] Figure 4A illustrates that the protective layer 114 is applied directly on the semiconductor structure 106 before the semiconductor structures 108 are aggregated.

[0055] Figure 4B illustrates that regions not covered by the protective layer 114 have been etched, which is similar to the process described above with respect to Figure 2B. As a result of etching, the semiconductor structures 108 are removed.

[0056] Figure 4C illustrates that the protective layer 114 is removed, which is similar to the process illustrated described above with respect to Figure 2C. Subsequently, the semiconductor structure 106 can be planarized, as described above with respect to Figure 1I.

[0057] Figures 5A-5E are partial cross-sectional views of a semiconductor substrate in accordance with some embodiments.

[0058] Figures 5A-5E clarify that the processes illustrated in Figures 1A-1I can be performed in forming multiple semiconductor structures (e.g., germanium islands) on a single semiconductor substrate.

[0059] Figure 5A illustrates that semiconductor structures 106 are epitaxially grown and that semiconductor structures 108 are formed on the mask layer 104.

[0060] Figure 5B illustrates that a protective layer 114 is applied on the semiconductor structures 106 while exposing the semiconductor structures 108.

[0061] Figure 5C illustrates that the semiconductor structures 108 are removed by etching.

[0062] Figure 5D illustrates that the protective layer 114 is removed.

[0063] Figure 5E illustrates that the semiconductor structures 106 are planarized (e.g., using a CMP process).

[0064] Certain features described with respect to Figures 1A-1I, 2A-2C, 3A-3C, and 4A-4C can be applied analogously to the processes illustrated in Figures 5A-5E. For example, the adhesive layer 112 may be applied over the semiconductor structures 106 before the protective layer 114 is applied (or formed) over the semiconductor structures 106. For brevity, such details are not repeated herein.

[0065] Figures 6A-6B are partial cross-sectional views of a semiconductor substrate in accordance with some embodiments.

[0066] Figure 6A illustrates that the substrate 102 includes complementary metal-oxide-semiconductor (CMOS) devices with source/drains 602 and gates 604. In Figure 6A, a mask layer 606 (e.g., silicon dioxide) is formed on the substrate 102. In some embodiments, the mask layer 606 includes silicon dioxide of at least 2 μm thickness, for growing a germanium layer thereon. The thickness of the silicon dioxide was found to improve the quality of the crystallinity of the epitaxially grown germanium.

[0067] Figure 6B illustrates that a semiconductor structure 608 (e.g., germanium) is formed using the processes described above with respect to Figures 1A-1I, 2A-2C, 3A-3C, 4A-4C, and 5A-5E.

[0068] Figures 7A-7C are flow diagrams illustrating a method 700 of removing nuclei formed during a selective epitaxial growth process in accordance with some embodiments.

[0069] The method 700 includes (702) epitaxially growing a first group of one or more semiconductor structures (e.g., the semiconductor structure 106 in Figure 1B) over a substrate (e.g., a silicon substrate) with one or more mask layers (e.g., the substrate 102 with the mask layer 104 in Figure 1B). A second group of a plurality of semiconductor structures (e.g., semiconductor structures 108 in Figure 1B) is formed on the one or more mask layers. In some embodiments, the second group of the plurality of semiconductor structures is formed concurrently with epitaxially growing the first group of the one or more semiconductor structures. In some embodiments, a first semiconductor structure of the first group of one or more semiconductor structures is larger than a second semiconductor structure of the second group of the plurality of semiconductor structures. In some embodiments, the one or more semiconductor structures are homo-epitaxially grown. In some embodiments, the one or more semiconductor structures are hetero-epitaxially grown.

[0070] In some embodiments, the first group of the one or more semiconductor structures is formed (704) in a single epitaxial growth process. For example, in Figures 1B-1C, the semiconductor structure 106 is formed in a single epitaxial growth process (e.g., instead of epitaxially growing a portion of the semiconductor structure 106, etching a portion of the semiconductor structure 106, and epitaxially growing an additional portion of the semiconductor structure 106).

[0071] In some embodiments, the method 700 includes (706) forming a plurality of semiconductor particles (e.g., the semiconductor structures 108 in Figure 1C) on the one or more mask layers (e.g., the mask layer 104 in Figure 1C) while epitaxially growing the first group of one or more semiconductor structures (e.g., the semiconductor structure 106 in Figure 1C) on the substrate with one or more mask layers. In some embodiments, the second group of the plurality of semiconductor structures includes the plurality of semiconductor particles.

[0072] In some embodiments, the second group of the plurality of semiconductor structures includes (708) a semiconductor film (e.g., the semiconductor film 110 in Figure 1D) on the one or more mask layers. In some embodiments, the second group of the plurality of semiconductor structures includes one or more semiconductor films on the one or more mask layers.

[0073] In some embodiments, the first group of one or more semiconductor structures includes (710) a column IV material (e.g., silicon, germanium, SiGe, etc.). In some embodiments, the first group of one or more semiconductor structures includes one or more III-V materials (e.g., GaAs, InGaAs, etc.).

[0074] In some embodiments, the first group of one or more semiconductor structures includes (712) germanium.

[0075] In some embodiments, the first group of one or more semiconductor structures is formed (714) on one or more regions of the substrate that are exposed from the one or more mask layers (e.g., not covered by the one or more mask layers). For example, in Figure 5A, the semiconductor structures 106 are formed on the regions of the substrate that are exposed from the mask layer 104.

[0076] In some embodiments, the first group of one or more semiconductor structures has (716) crystalline structures and the second group of the plurality of semiconductor structures has amorphous and/or poly-crystalline structures. For example, see Figure 8A, which shows that the first group of one or more semiconductor structures (e.g., the germanium island) has a crystalline structure and the second group of semiconductor structures has amorphous and/or poly-crystalline structures.

[0077] In some embodiments, the one or more mask layers include (718) a dielectric material.

[0078] In some embodiments, the one or more mask layers include (720) silicon dioxide.

[0079] The method 700 also includes (722, Figure 7B) forming one or more protective layers (e.g., the protective layer 114 in Figure 1F, such as one or more photoresist layers) over the first group of one or more semiconductor structures. At least a subset of the second group of the plurality of semiconductor structures is exposed from the one or more protective layers. For example, in Figure 1F, the film 110 is exposed from the protective layer 114. In some embodiments, the one or more protective layers are in direct contact with the first group of one or more semiconductor structures (e.g., Figure 2A). In some embodiments, one or more intermediate layers (e.g., one or more adhesive layers, such as hexamethyldisilazane (HMDS) or low-temperature thermal oxide) are located between the first group of one or more semiconductor structures and the one or more protective layers (e.g., Figure 1F).

[0080] In some embodiments, the method 700 includes (724) foregoing etching at least the subset of the second group of the plurality of semiconductor structures before the one or more protective layers are formed over the first group of one or more semiconductor structures. For example, in some embodiments, the second group of the plurality of semiconductor structures is not etched until after the one or more protective layers are formed over the one or more semiconductor structures to protect the one or more semiconductor structures from the etching process.

[0081] In some embodiments, the method 700 includes (726) foregoing etching at least the subset of the second group of the plurality of semiconductor structures subsequent to initiating the epitaxial growth of the first group of one or more semiconductor structures on the substrate until the one or more protective layers are formed over the first group of one or more semiconductor structures. For example, etching of at least the subset of the second group of the plurality of semiconductor structures is foregone during the epitaxial growth of the first group of one or more semiconductor structures. In some embodiments, etching at least the subset of the plurality of semiconductor structures is foregone after initiating the epitaxial growth of the first group of one or more semiconductor structures on the substrate and before forming the one or more protective layers over the one or more semiconductor structures.

[0082] In some embodiments, the one or more protective layers include (728) one or more photoresist layers. In some embodiments, the one or more protective layers are one or more photoresist layers.

[0083] In some embodiments, the method 700 includes (730) depositing one or more adhesive layers over at least the first group of one or more semiconductor structures prior to forming the one or more protective layers. For example, as illustrated in Figures 1E-1F, the adhesive layer 112 is applied over the semiconductor structure 106 before the protective layer 114 is applied. In some embodiments, the one or more adhesive layers are deposited on at least the first group of one or more semiconductor structures.

[0084] In some embodiments, the one or more adhesive layers include (732) hexamethyldisilazane and/or low-temperature thermal oxide.

[0085] In some embodiments, the method includes, subsequent to etching at least the subset of the second group of the plurality of semiconductor structures, removing the one or more adhesive layers. In some embodiments, the one or more protective layers and the one or

more adhesive layers are removed concurrently. In some embodiments, the one or more protective layers are removed subsequent to removing the one or more adhesive layers.

[0086] In some embodiments, the substrate includes silicon. In some embodiments, the substrate is a silicon substrate.

[0087] In some embodiments, the substrate includes (734) a plurality of semiconductor devices thereon (e.g., Figures 6A-6B). For example, the substrate may include a plurality of transistors prior to epitaxially growing the first group of one or more semiconductor structures.

[0088] In some embodiments, the substrate includes a plurality of transistors and a semiconductor structure of the first group of one or more semiconductor structures is electrically coupled to a source or a drain of a transistor of the plurality of transistors.

[0089] In some embodiments, the substrate includes (736) a plurality of complementary metal-oxide semiconductor (CMOS) devices thereon (e.g., Figures 6A-6B).

[0090] In some embodiments, the substrate includes thereon a plurality of complementary metal-oxide semiconductor devices, including a p-type metal-oxide-semiconductor transistor and an n-type metal-oxide-semiconductor transistor. In some embodiments, the method includes electrically coupling a first semiconductor structure of the first group of one or more semiconductor structures to a source or a drain of one of: the p-type metal-oxide-semiconductor transistor or the n-type metal-oxide-semiconductor transistor.

[0091] In some embodiments, the plurality of semiconductor devices is located (738) on the substrate below the one or more mask layers. For example, in Figures 6A-6B, the semiconductor devices (e.g., transistors) are located below the mask layer 606. In some embodiments, the plurality of semiconductor devices is located in the front-end of the line (FEOL) region of the substrate.

[0092] The method 700 further includes (740, Figure 7C), subsequent to forming the one or more protective layers over the first group of one or more semiconductor structures, etching at least the subset of the second group of the plurality of semiconductor structures. For example, in Figures 1F-1G, the film 110 is removed due to the etching process. In some embodiments, at least the subset of the plurality of semiconductor structures that is exposed from the one or more photoresist layers is completely etched (e.g., removed). In some embodiments, at least the subset of the plurality of semiconductor structures that is exposed

from the one or more photoresist layers is at least partially etched (e.g., removed). In some embodiments, one or more semiconductor structures of at least the subset of the plurality of semiconductor structures that is exposed from the one or more photoresist layers are etched (e.g., removed). In some embodiments, the entire second group of the plurality of semiconductor structures formed on the one or more mask layers is etched (e.g., removed).

[0093] In some embodiments, the method includes etching the entire subset of the second group of the plurality of semiconductor structures that is exposed from the one or more protective layers.

[0094] In some embodiments, the method 700 includes (742), subsequent to etching at least the subset of the second group of the plurality of semiconductor structures, removing the one or more protective layers (e.g., Figure 1H) and/or planarizing at least a subset of the first group of one or more semiconductor structures (e.g., using chemical-mechanical planarization). In some embodiments, the method 700 includes, subsequent to etching at least the subset of the second group of the plurality of semiconductor structures, removing the one or more protective layers. In some embodiments, the method 700 includes, subsequent to etching at least the subset of the second group of the plurality of semiconductor structures, planarizing at least a subset of the first group of one or more semiconductor structures. For example, in Figure 1I, the semiconductor structure 106 is planarized.

[0095] In some embodiments, etching at least the subset of the second group of the plurality of semiconductor structures includes (744) etching at least the subset of the second group of the plurality of semiconductor structures at a first rate and etching the one or more mask layers at a second rate that is lower than the first rate. For example, in Figures 1F-1G, the film 110 is etched faster than the mask layer 104 and the protective layer 114. In some embodiments, etching at least the subset of the second group of the plurality of semiconductor structures includes etching at least the subset of the second group of the plurality of semiconductor structures without etching the one or more mask layers. In some embodiments, the film 110 shown in Figure 1F is etched while the mask layer 104 and the protective layer 114 are not etched.

[0096] In some embodiments, etching at least the subset of the second group of the plurality of semiconductor structures includes foregoing etching of the one or more mask layers.

[0097] In some embodiments, etching at least the subset of the second group of the plurality of semiconductor structures includes (744) etching at least the subset of the second group of the plurality of semiconductor structures at a first rate and etching at least a subset of the first group of one or more semiconductor structures at a third rate that is lower than the first rate. For example, in Figures 1F-1G, the film 110 is etched faster than the semiconductor structure 106. In some embodiments, etching at least the subset of the second group of the plurality of semiconductor structures includes etching at least the subset of the second group of the plurality of semiconductor structures without etching the first group of one or more semiconductor structures. In some embodiments, the film 110 shown in Figure 1F is etched while the semiconductor structure 106 is not etched (e.g., because the semiconductor structure 106 is protected by the protective layer 114).

[0098] Certain features of the method 700 described with respect to Figures 7A-7C can be applied to processes illustrated in Figures 1A-1I, 2A-2C, 3A-3C, 4A-4C, 5A-5E, and 6A-6B. For brevity, these details are not repeated.

[0099] Figures 8A-8B are scanning electron microscope (SEM) images of a semiconductor substrate prior to an etching process in accordance with some embodiments.

[00100] Shown in Figures 8A and 8B are top-down views of the semiconductor substrate that corresponds to Figure 1C.

[00101] Figure 8A shows a germanium island that corresponds to the semiconductor structure 106 in Figure 1C (before the etching process). In addition, the second group of semiconductor structures is formed around the germanium island on the mask layer.

[00102] Figure 8B is a zoomed-out view of the semiconductor substrate. Multiple germanium islands and the second group of semiconductor structures formed on the mask layer are shown in Figure 8B.

[00103] Figures 9A-9B are scanning electron microscope (SEM) images of a semiconductor substrate subsequent to an etching process in accordance with some embodiments.

[00104] Figure 9A shows a germanium island that corresponds to the semiconductor structure 106 in Figure 1H (after the etching process). Figure 9A shows the absence of the second group of semiconductor structures around the germanium island on the mask layer.

[00105] Figure 9B is a zoomed-out view of the semiconductor substrate. Multiple germanium islands without the second group of semiconductor structures are shown in Figure 9B.

[00106] Thus, Figures 9A-9B show the effectiveness of the described methods in removing the second group of semiconductor structures formed on the one or more mask layers.

[00107] The foregoing description, for purpose of explanation, has been described with reference to specific embodiments. However, the illustrative discussions above are not intended to be exhaustive or to limit the invention to the precise forms disclosed. Many modifications and variations are possible in view of the above teachings. The embodiments were chosen and described in order to best explain the principles of the invention and its practical applications, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as are suited to the particular use contemplated.

What is claimed is:

1. A method for removing nuclei formed during a selective epitaxial growth process, comprising:

epitaxially growing a first group of one or more semiconductor structures over a substrate with one or more mask layers, wherein a second group of a plurality of semiconductor structures is formed on the one or more mask layers;

forming one or more protective layers over the first group of one or more semiconductor structures, wherein at least a subset of the second group of the plurality of semiconductor structures is exposed from the one or more protective layers; and,

subsequent to forming the one or more protective layers over the first group of one or more semiconductor structures, etching at least the subset of the second group of the plurality of semiconductor structures.

2. The method of claim 1, including:

foregoing etching at least the subset of the second group of the plurality of semiconductor structures before the one or more protective layers are formed over the first group of one or more semiconductor structures.

3. The method of claim 1 or 2, including:

foregoing etching at least the subset of the second group of the plurality of semiconductor structures subsequent to initiating the epitaxial growth of the first group of one or more semiconductor structures on the substrate until the one or more protective layers are formed over the first group of one or more semiconductor structures.

4. The method of any of claims 1-3, wherein the first group of the one or more semiconductor structures is formed in a single epitaxial growth process.

5. The method of any of claims 1-4, wherein:

the one or more protective layers include one or more photoresist layers.

6. The method of any of claims 1-5, including:

depositing one or more adhesive layers over at least the first group of one or more semiconductor structures prior to forming the one or more protective layers.

7. The method of claim 6, wherein the one or more adhesive layers include hexamethyldisilazane and/or low-temperature thermal oxide.

8. The method of claim 6 or 7, including:

subsequent to etching at least the subset of the second group of the plurality of semiconductor structures, removing the one or more adhesive layers.

9. The method of claim 8, wherein the one or more protective layers and the one or more adhesive layers are removed concurrently.

10. The method of claim 8, wherein the one or more protective layers are removed subsequent to removing at least a portion of the one or more adhesive layers.

11. The method of any of claims 1-10, further including:

subsequent to etching at least the subset of the second group of the plurality of semiconductor structures, removing the one or more protective layers.

12. The method of any of claims 1-11, further including:

subsequent to etching at least the subset of the second group of the plurality of semiconductor structures, planarizing at least a subset of the first group of one or more semiconductor structures.

13. The method of any of claims 1-12, including:

forming a plurality of semiconductor particles on the one or more mask layers while epitaxially growing the first group of one or more semiconductor structures on the substrate with one or more mask layers.

14. The method of any of claims 1-13, wherein the second group of the plurality of semiconductor structures includes one or more semiconductor films on the one or more mask layers.

15. The method of any of claims 1-14, wherein the first group of one or more semiconductor structures includes a column IV material.

16. The method of any of claims 1-15, wherein the first group of one or more semiconductor structures includes germanium.

17. The method of any of claims 1-16, wherein the first group of one or more semiconductor structures is formed on one or more regions of the substrate that are exposed from the one or more mask layers.

18. The method of any of claims 1-17, wherein the first group of one or more semiconductor structures has crystalline structures and the second group of the plurality of semiconductor structures has amorphous and/or poly-crystalline structures.

19. The method of any of claims 1-18, wherein the one or more mask layers include a dielectric material.

20. The method of any of claims 1-19, wherein the one or more mask layers include silicon dioxide.

21. The method of any of claims 1-20, wherein etching at least the subset of the second group of the plurality of semiconductor structures includes etching at least the subset of the second group of the plurality of semiconductor structures at a first rate and etching the one or more mask layers at a second rate that is lower than the first rate.

22. The method of any of claims 1-21, wherein etching at least the subset of the second group of the plurality of semiconductor structures includes foregoing etching of the one or more mask layers.

23. The method of any of claims 1-22, wherein the substrate includes a plurality of semiconductor devices thereon.

24. The method of claim 23, wherein the plurality of semiconductor devices is located on the substrate below the one or more mask layers.

25. The method of claim 23 or 24, wherein the substrate includes a plurality of transistors thereon and a semiconductor structure of the first group of one or more semiconductor structures is electrically coupled to a source or a drain of a transistor of the plurality of transistors.

26. The method of claim 25, wherein the substrate includes thereon a plurality of complementary metal-oxide semiconductor devices, including a p-type metal-oxide-semiconductor transistor and an n-type metal-oxide-semiconductor transistor.

27. The method of claim 26, including:

electrically coupling a first semiconductor structure of the first group of one or more semiconductor structures to a source or a drain of one of: the p-type metal-oxide-semiconductor transistor or the n-type metal-oxide-semiconductor transistor.

28. The method of any of claims 1-27, wherein the first group of one or more semiconductor structures and the second group of the plurality of semiconductor structures are formed concurrently.

29. The method of any of claims 1-28, wherein a first semiconductor structure of the first group of one or more semiconductor structures is larger than a second semiconductor structure of the second group of the plurality of semiconductor structures.

30. The method of any of claims 1-29, including:

etching the entire subset of the second group of the plurality of semiconductor structures that is exposed from the one or more protective layers.

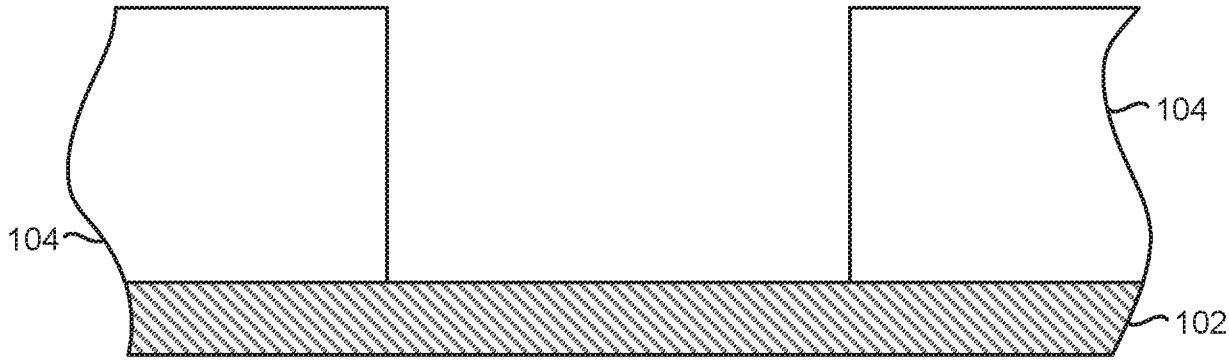

Figure 1A

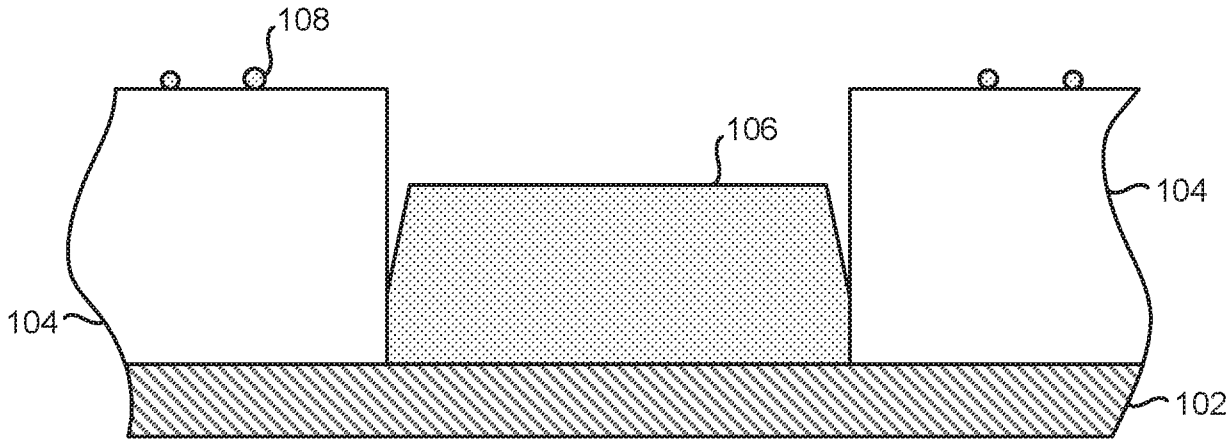

Figure 1B

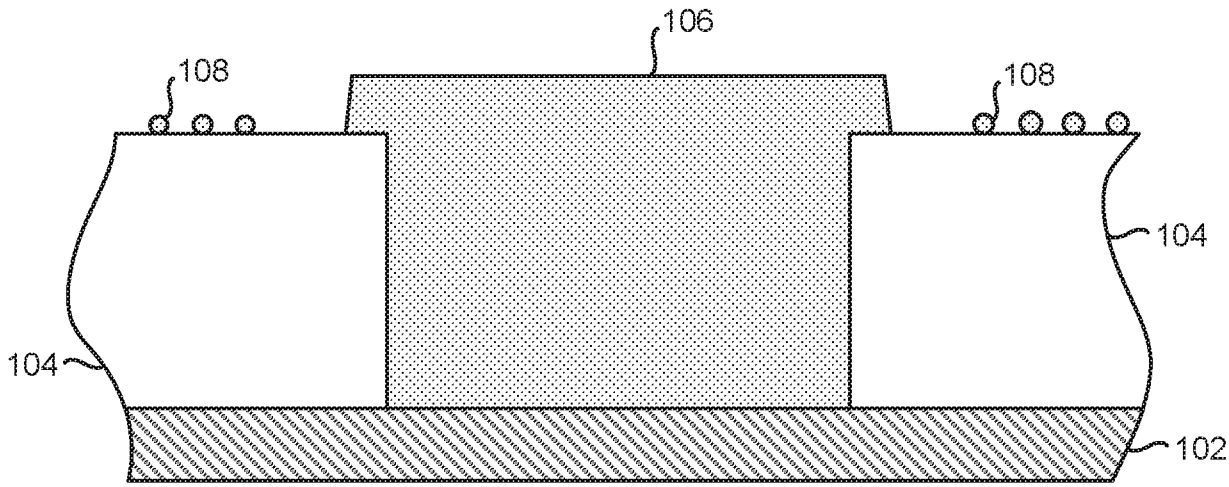

Figure 1C

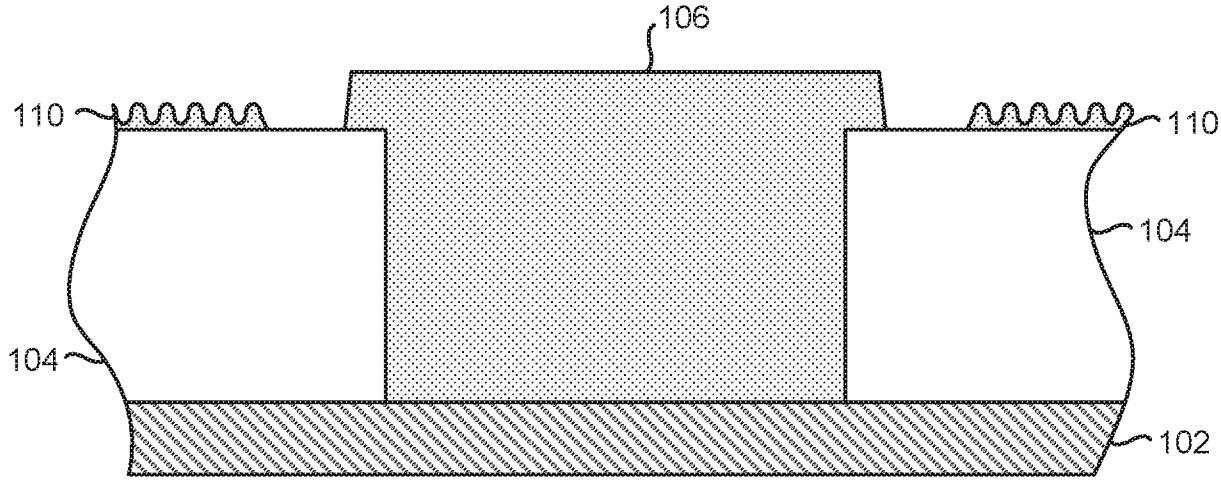

Figure 1D

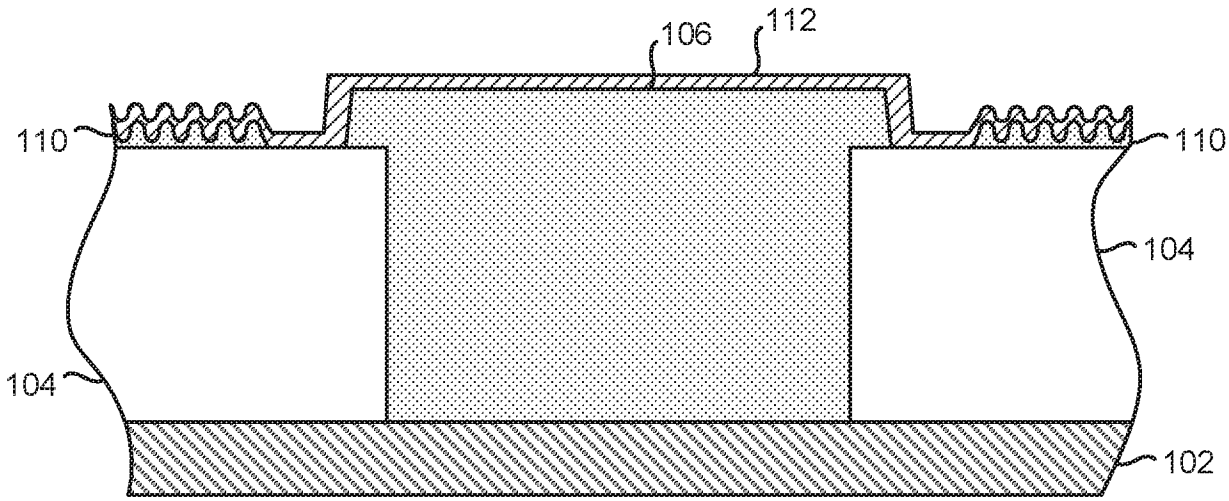

Figure 1E

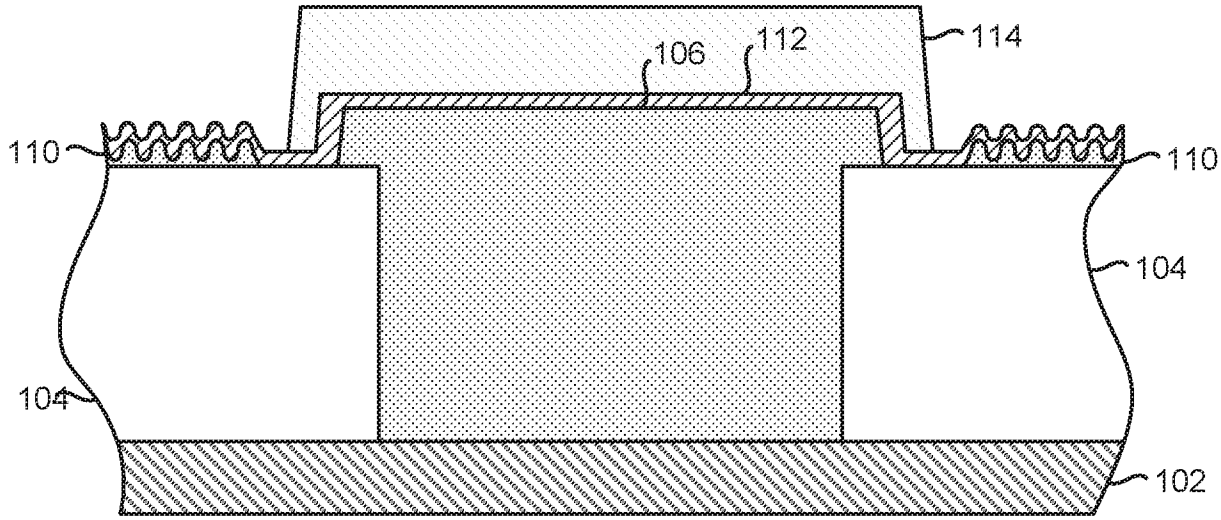

Figure 1F

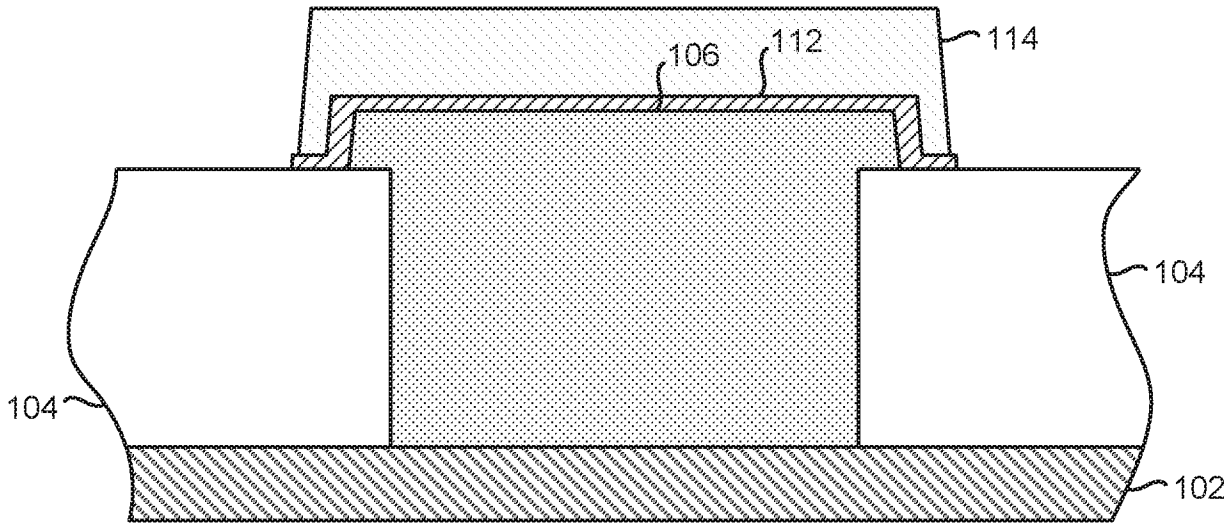

Figure 1G

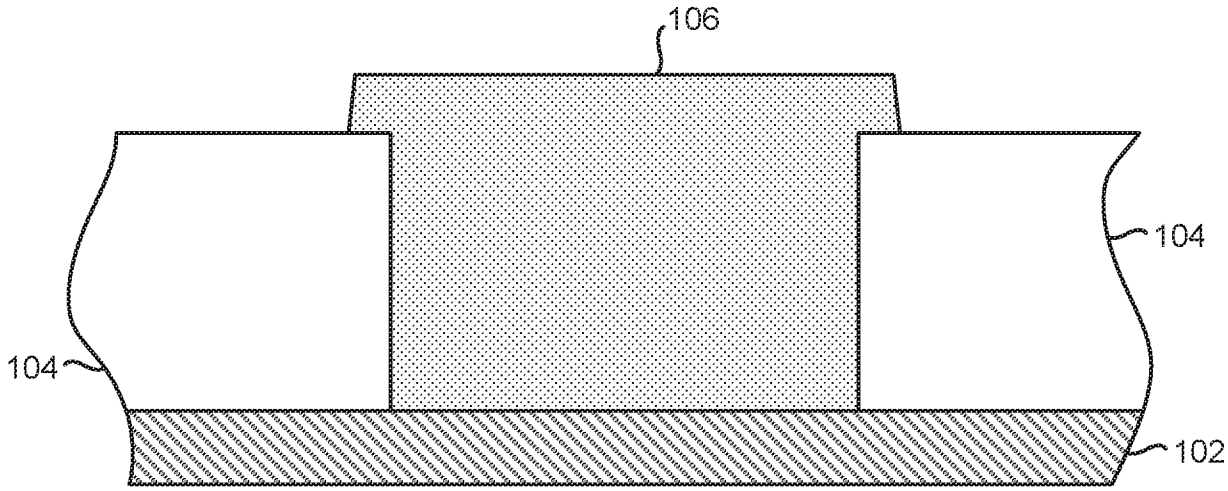

Figure 1H

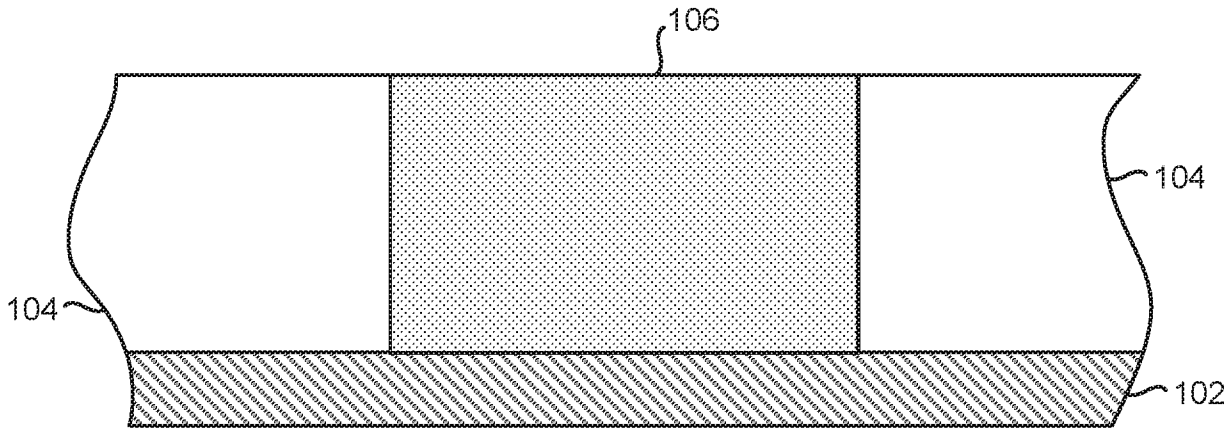

Figure 1I

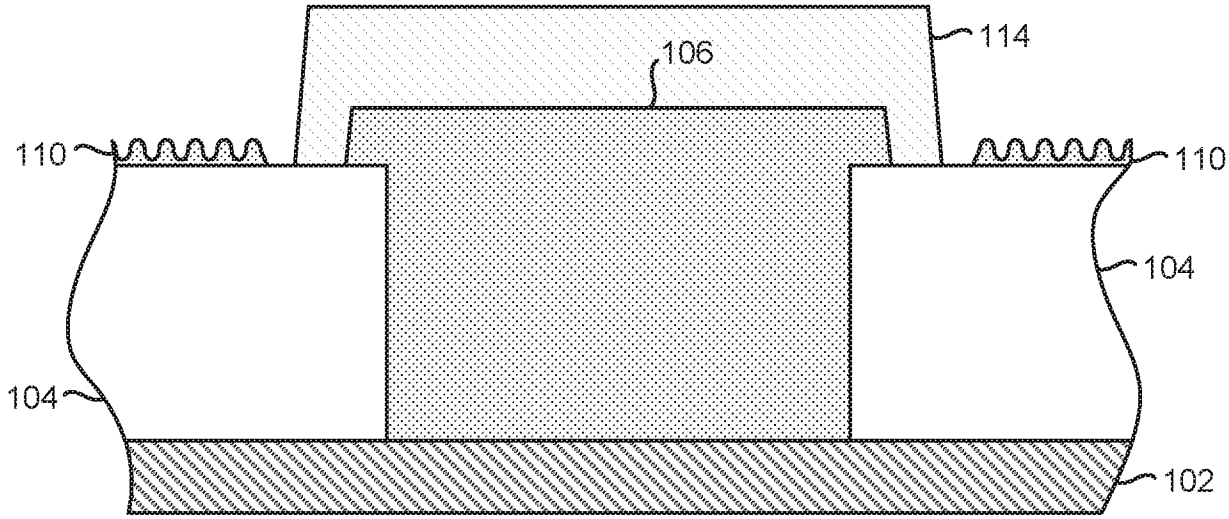

Figure 2A

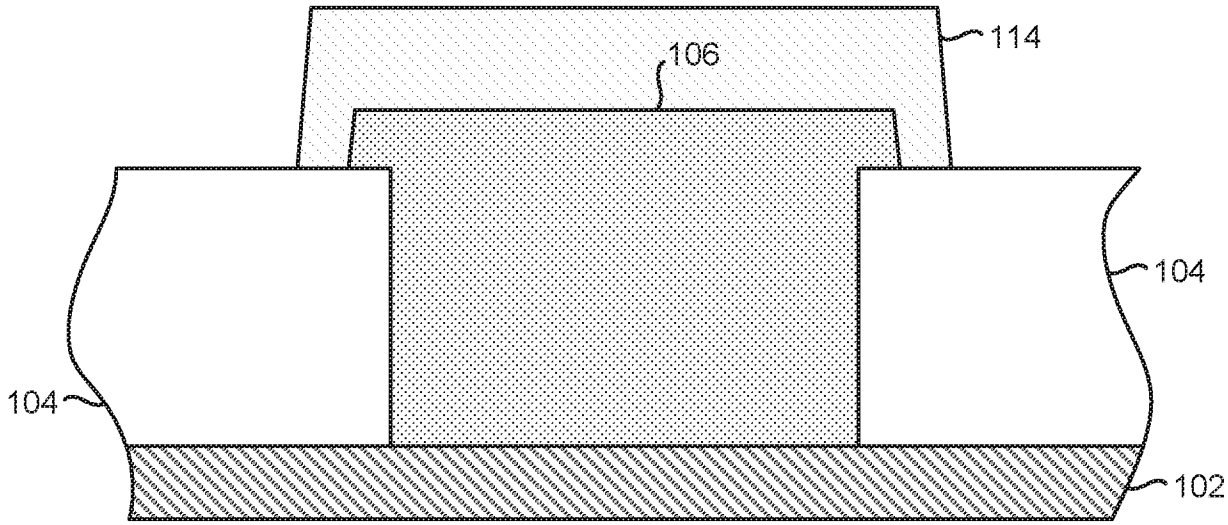

Figure 2B

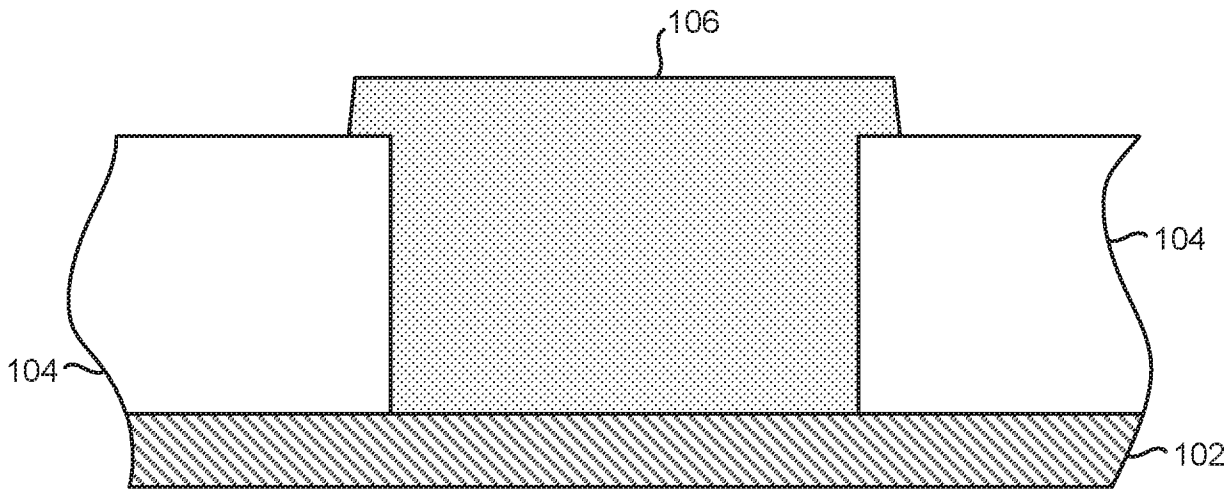

Figure 2C

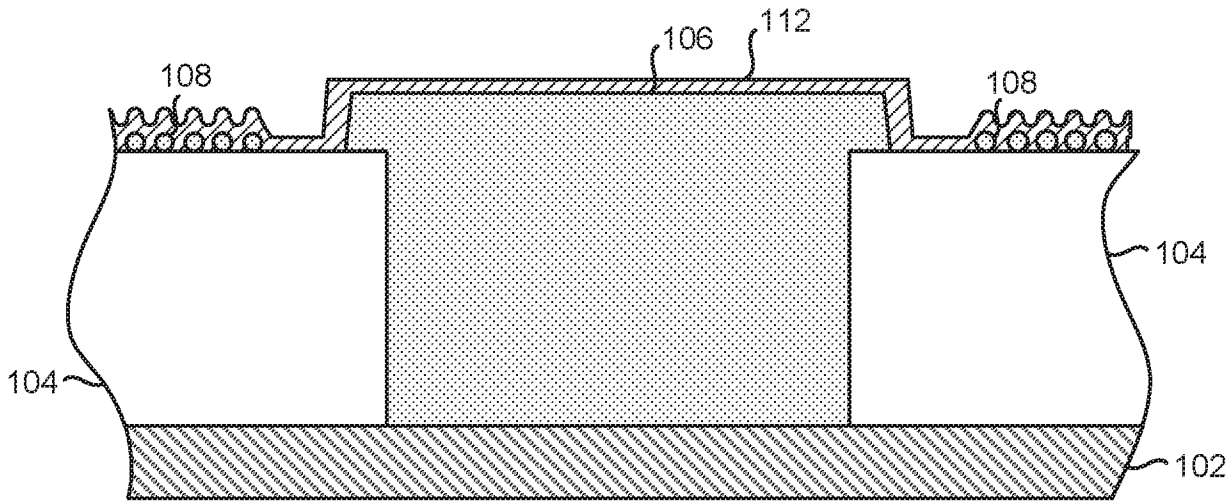

Figure 3A

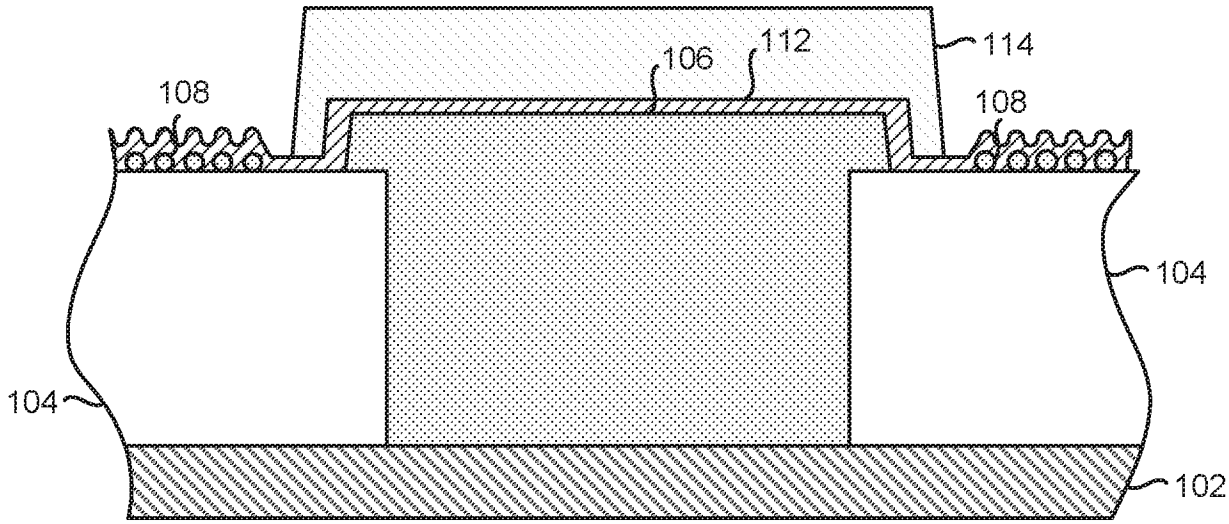

Figure 3B

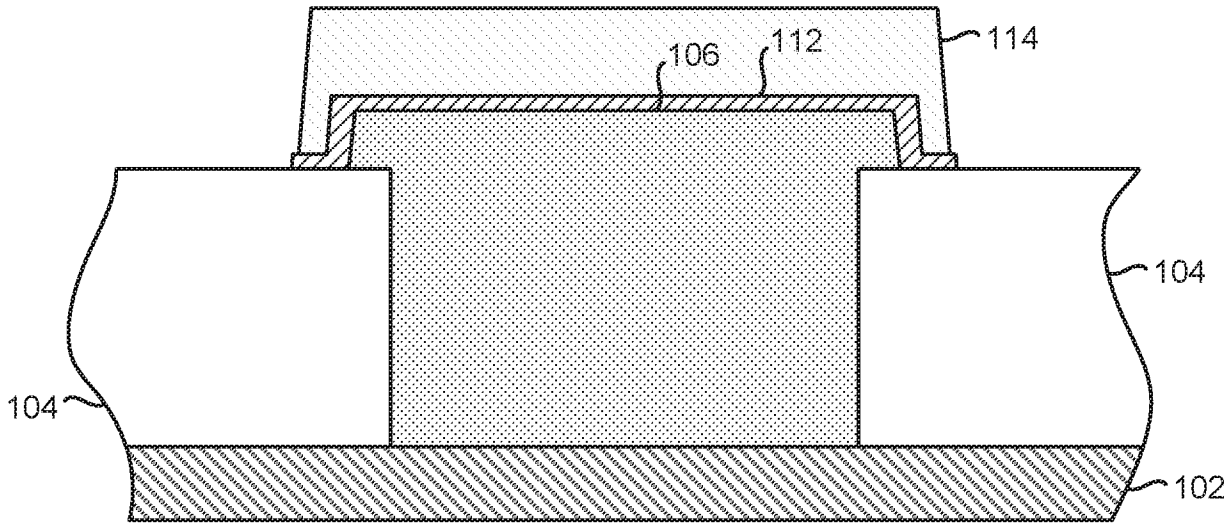

Figure 3C

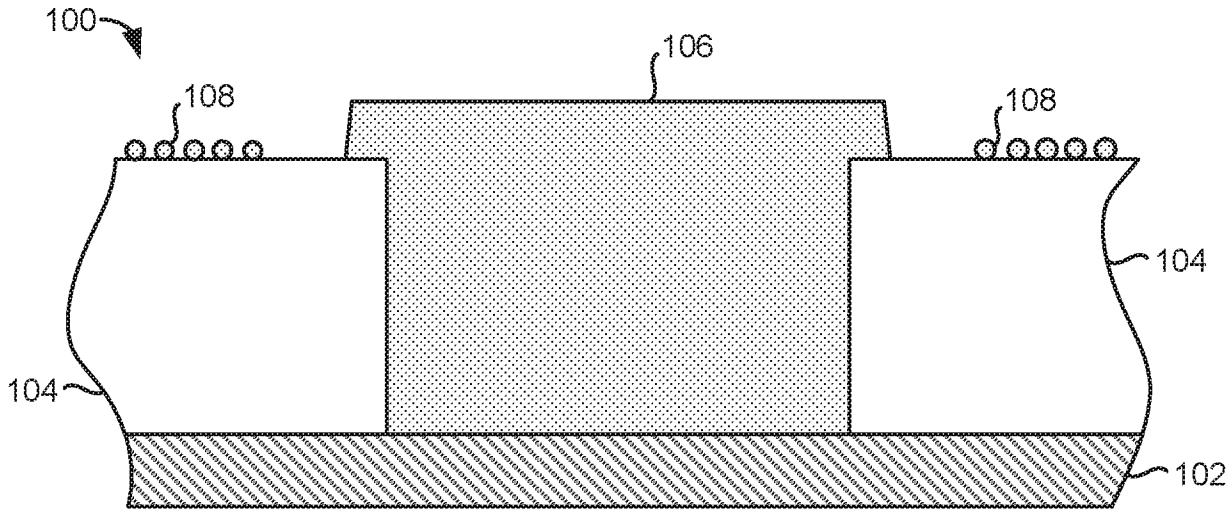

Figure 4A

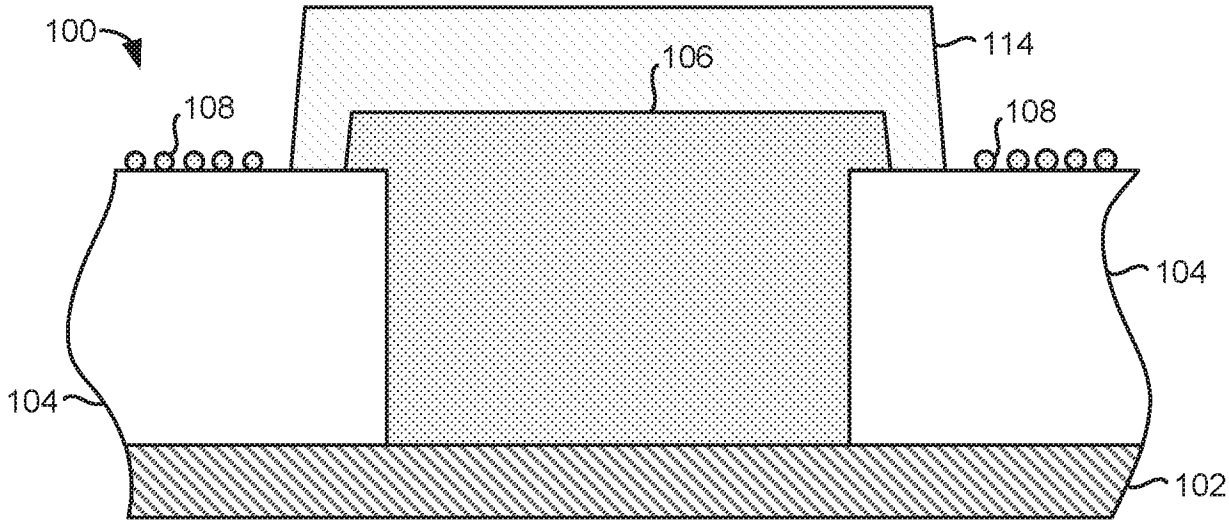

Figure 4B

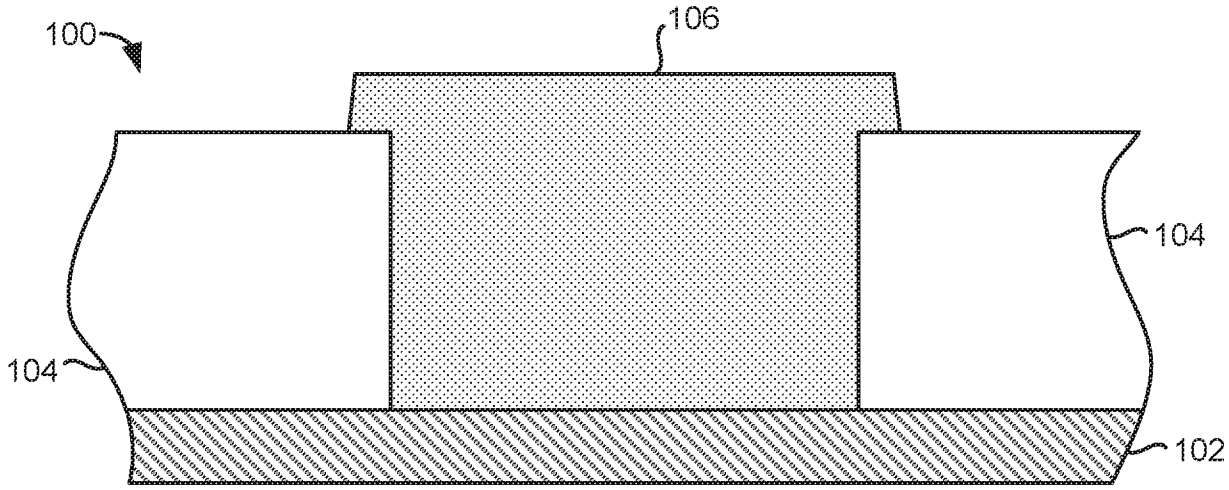

Figure 4C

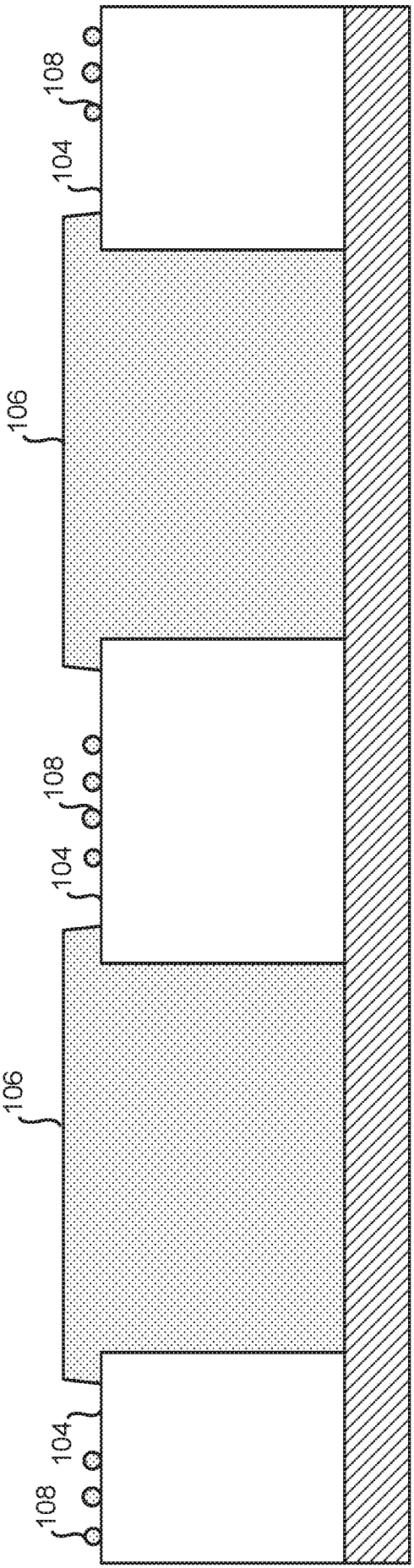

Figure 5A

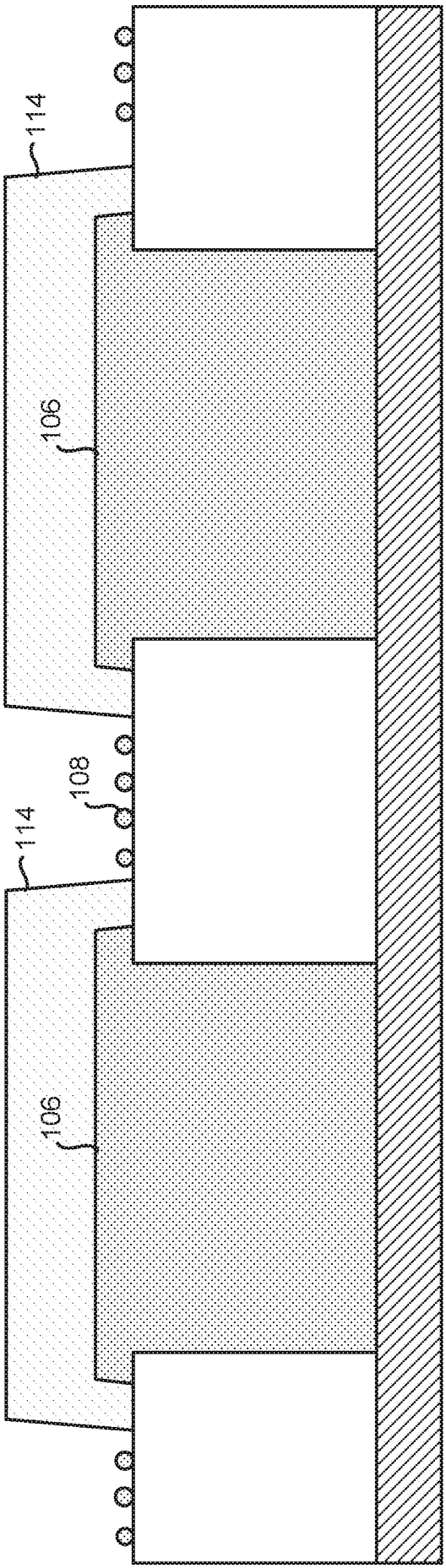

Figure 5B

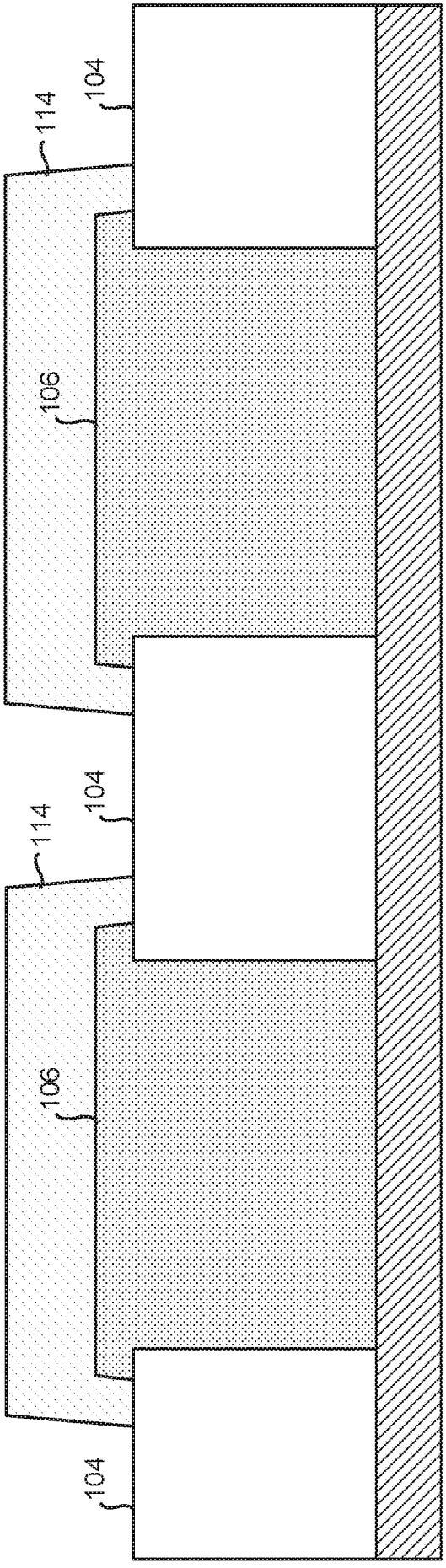

Figure 5C

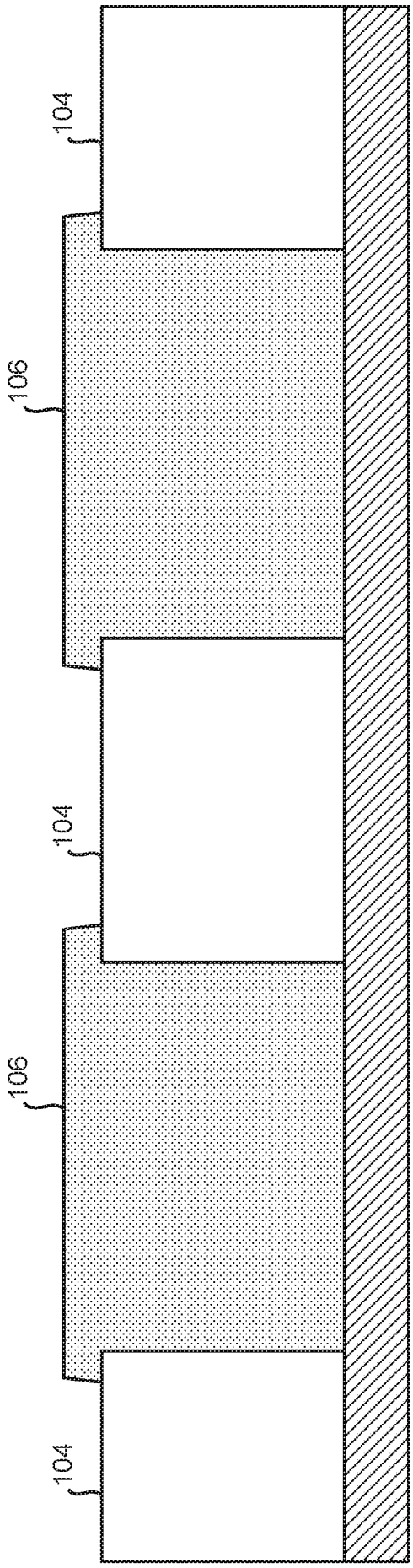

Figure 5D

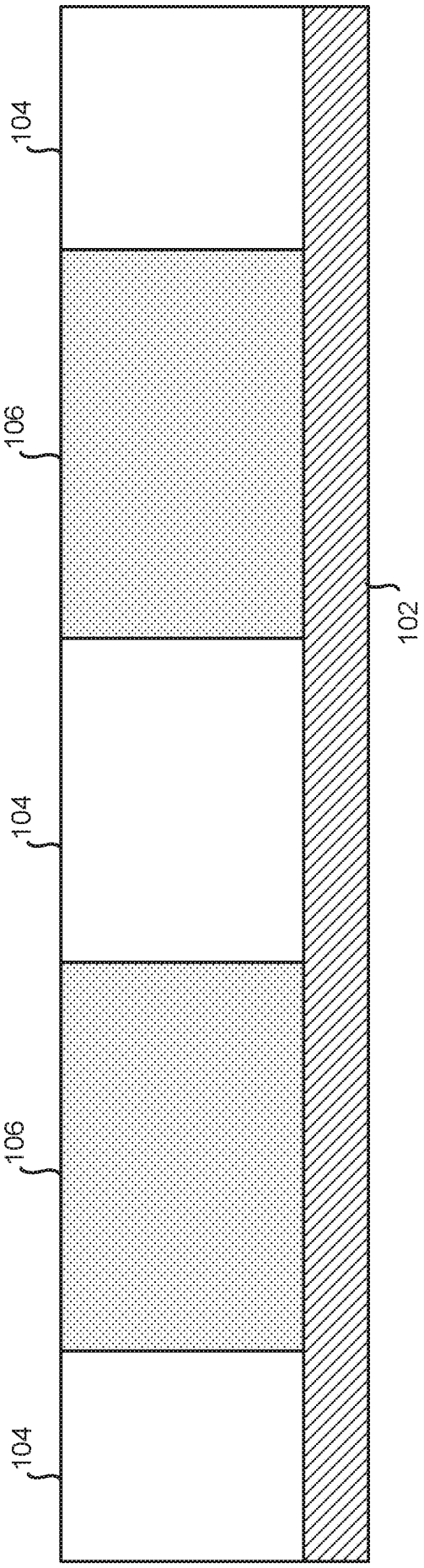

Figure 5E

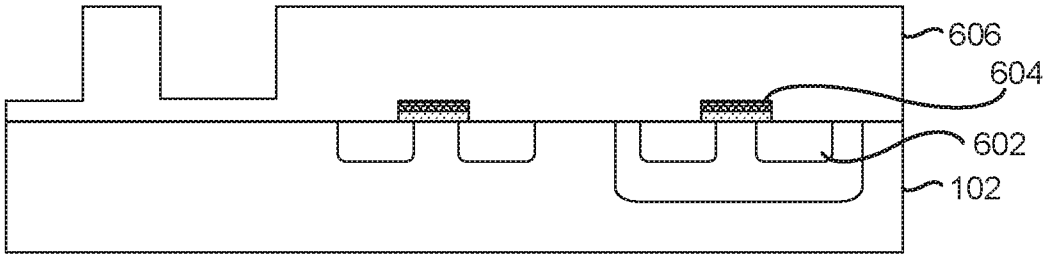

Figure 6A

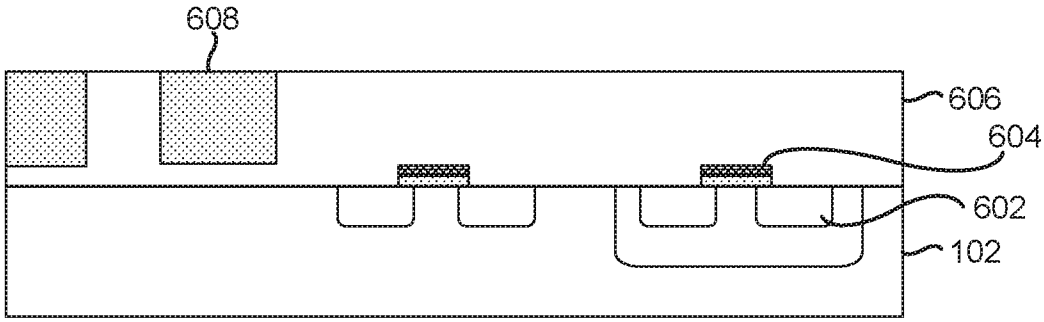

Figure 6B

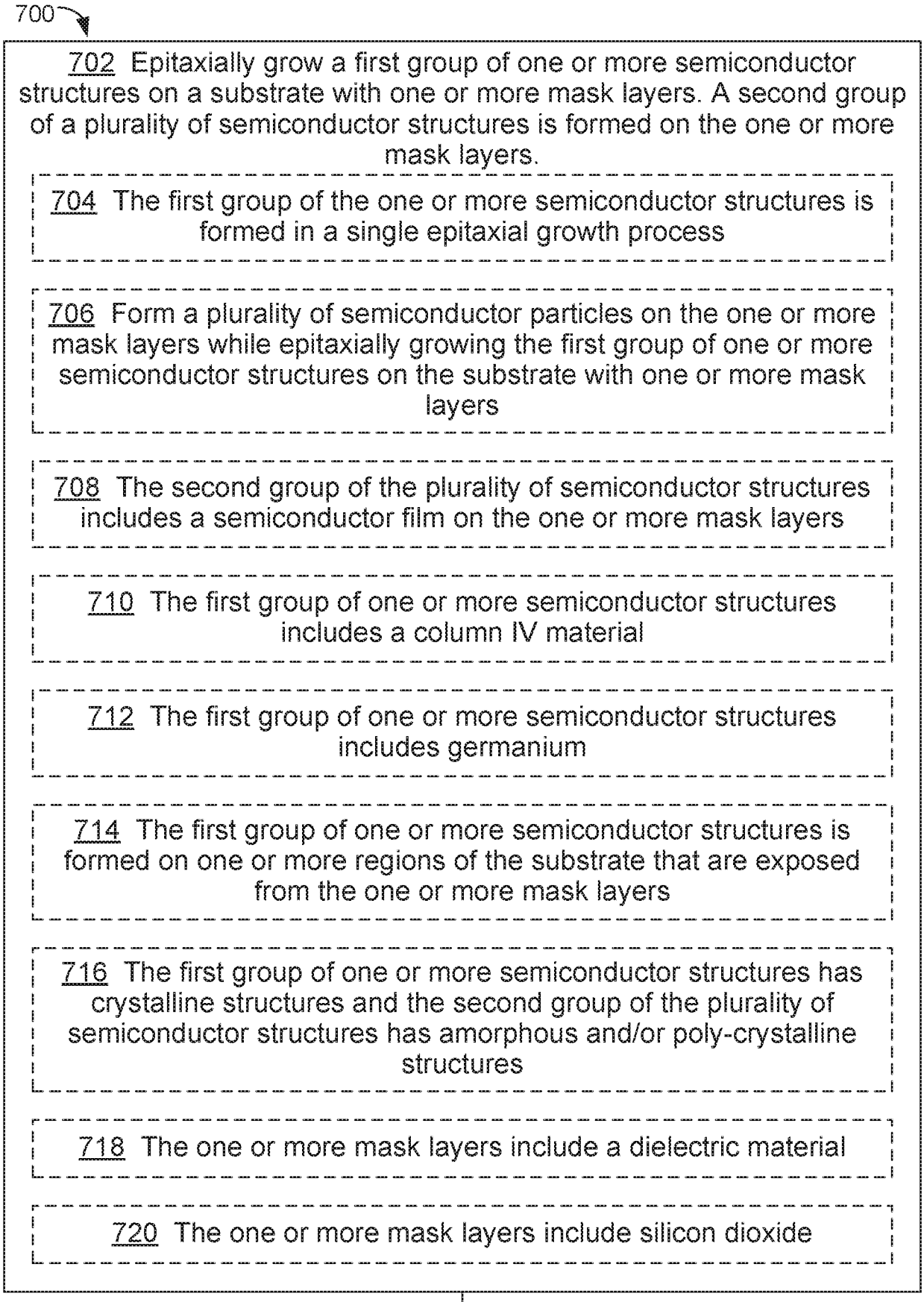
700
702 Epitaxially grow a first group of one or more semiconductor structures on a substrate with one or more mask layers. A second group of a plurality of semiconductor structures is formed on the one or more mask layers.
704 The first group of the one or more semiconductor structures is formed in a single epitaxial growth process
706 Form a plurality of semiconductor particles on the one or more mask layers while epitaxially growing the first group of one or more semiconductor structures on the substrate with one or more mask layers
708 The second group of the plurality of semiconductor structures includes a semiconductor film on the one or more mask layers
710 The first group of one or more semiconductor structures includes a column IV material
712 The first group of one or more semiconductor structures includes germanium
714 The first group of one or more semiconductor structures is formed on one or more regions of the substrate that are exposed from the one or more mask layers
716 The first group of one or more semiconductor structures has crystalline structures and the second group of the plurality of semiconductor structures has amorphous and/or poly-crystalline structures
718 The one or more mask layers include a dielectric material
720 The one or more mask layers include silicon dioxide
A

Figure 7A

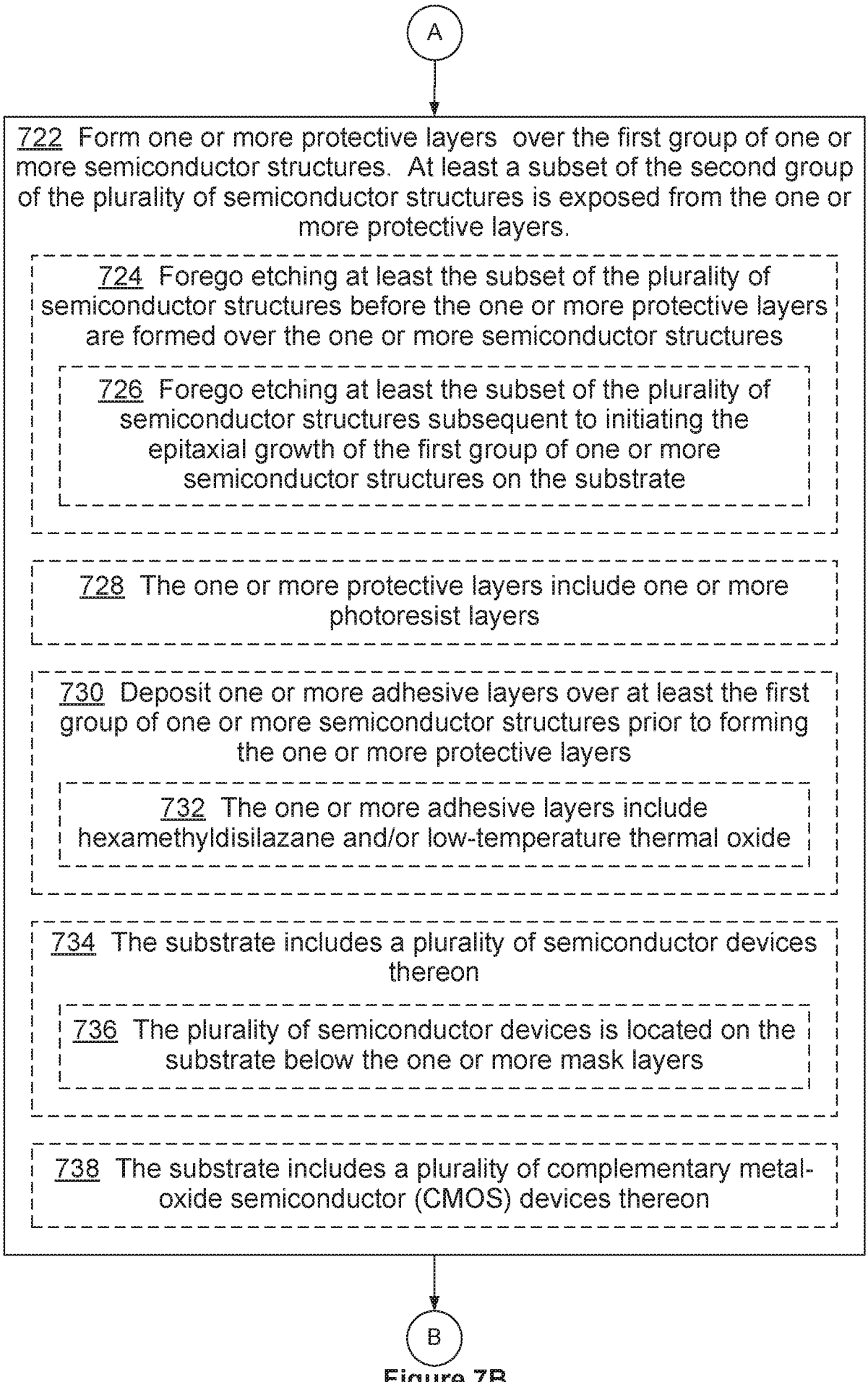
A
722 Form one or more protective layers over the first group of one or more semiconductor structures. At least a subset of the second group of the plurality of semiconductor structures is exposed from the one or more protective layers.
724 Forego etching at least the subset of the plurality of semiconductor structures before the one or more protective layers are formed over the one or more semiconductor structures
726 Forego etching at least the subset of the plurality of semiconductor structures subsequent to initiating the epitaxial growth of the first group of one or more semiconductor structures on the substrate
728 The one or more protective layers include one or more photoresist layers
730 Deposit one or more adhesive layers over at least the first group of one or more semiconductor structures prior to forming the one or more protective layers
732 The one or more adhesive layers include hexamethyldisilazane and/or low-temperature thermal oxide
734 The substrate includes a plurality of semiconductor devices thereon
736 The plurality of semiconductor devices is located on the substrate below the one or more mask layers
738 The substrate includes a plurality of complementary metal-oxide semiconductor (CMOS) devices thereon
B

Figure 7B

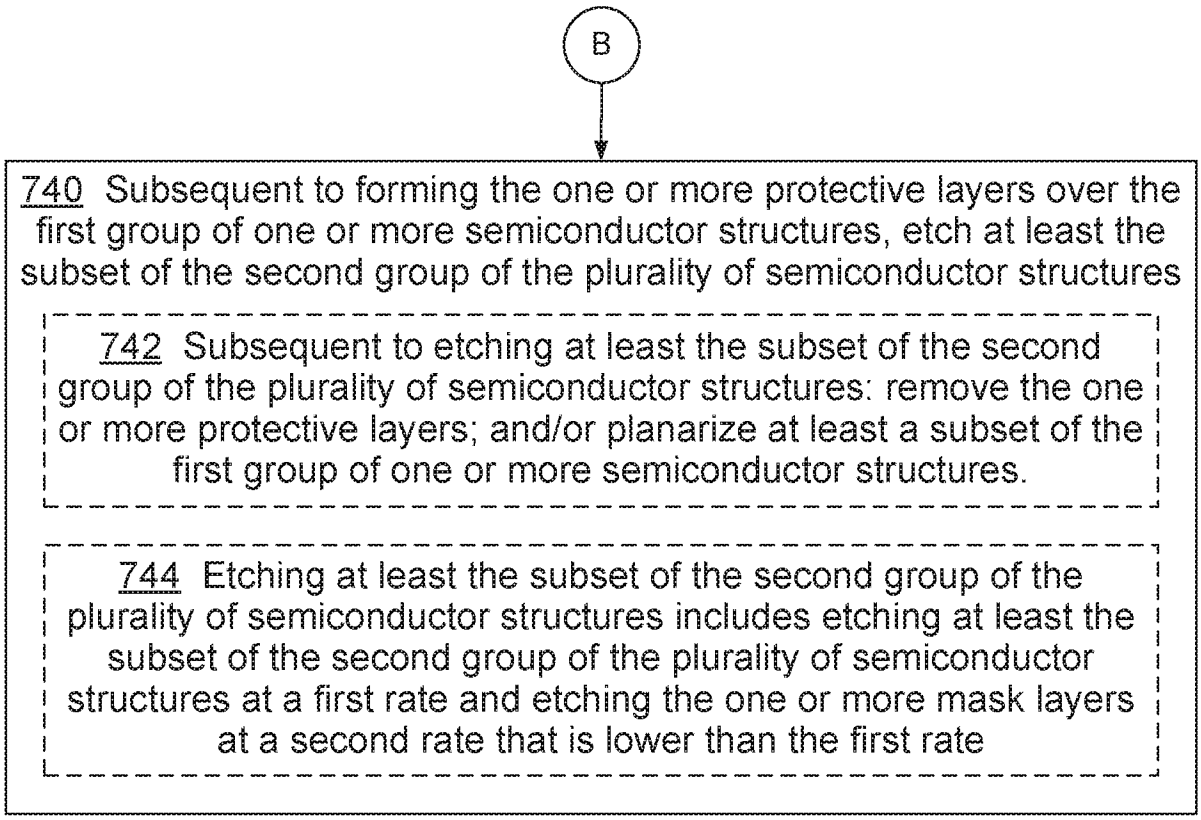
B
740 Subsequent to forming the one or more protective layers over the first group of one or more semiconductor structures, etch at least the subset of the second group of the plurality of semiconductor structures
742 Subsequent to etching at least the subset of the second group of the plurality of semiconductor structures: remove the one or more protective layers; and/or planarize at least a subset of the first group of one or more semiconductor structures.
744 Etching at least the subset of the second group of the plurality of semiconductor structures includes etching at least the subset of the second group of the plurality of semiconductor structures at a first rate and etching the one or more mask layers at a second rate that is lower than the first rate

Figure 7C

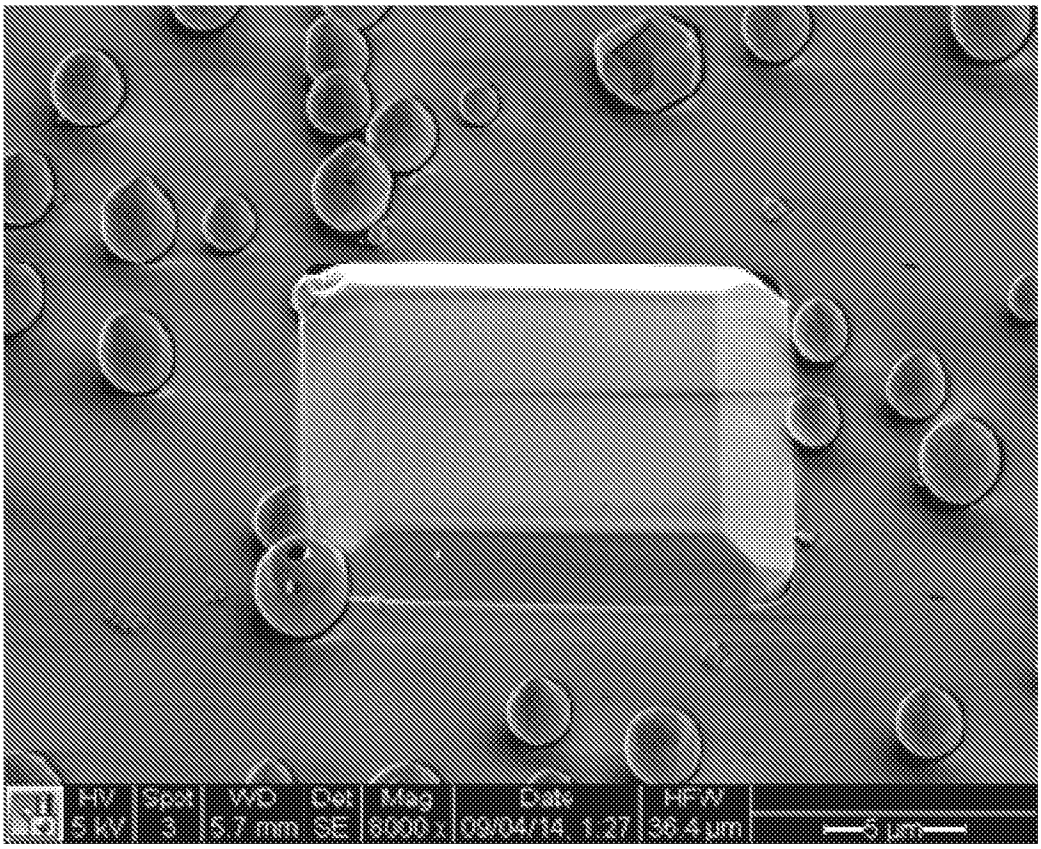

Figure 8A

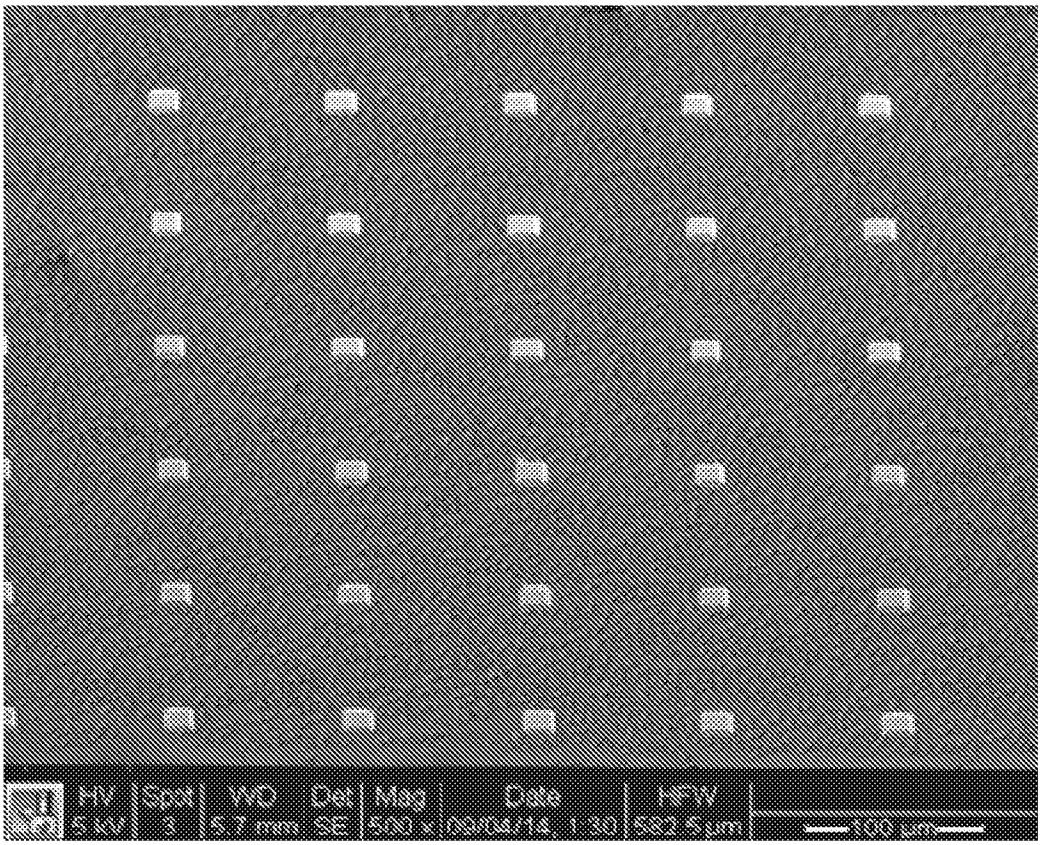

Figure 8B

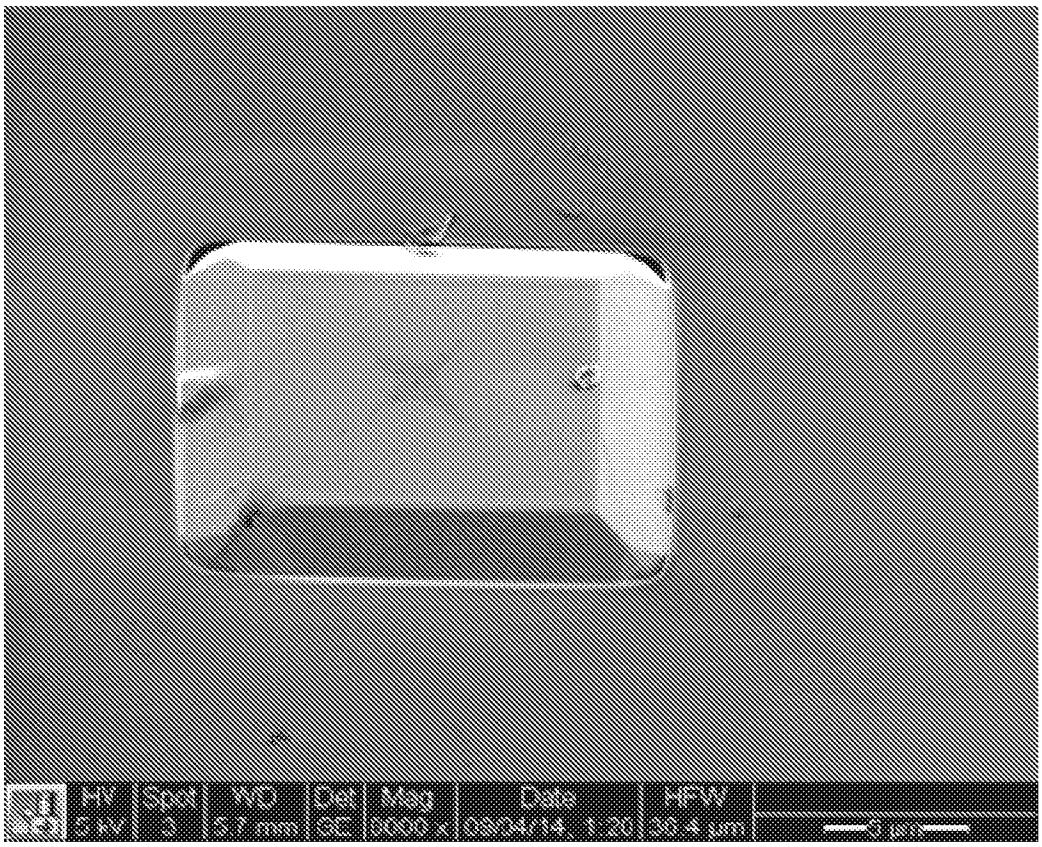

Figure 9A

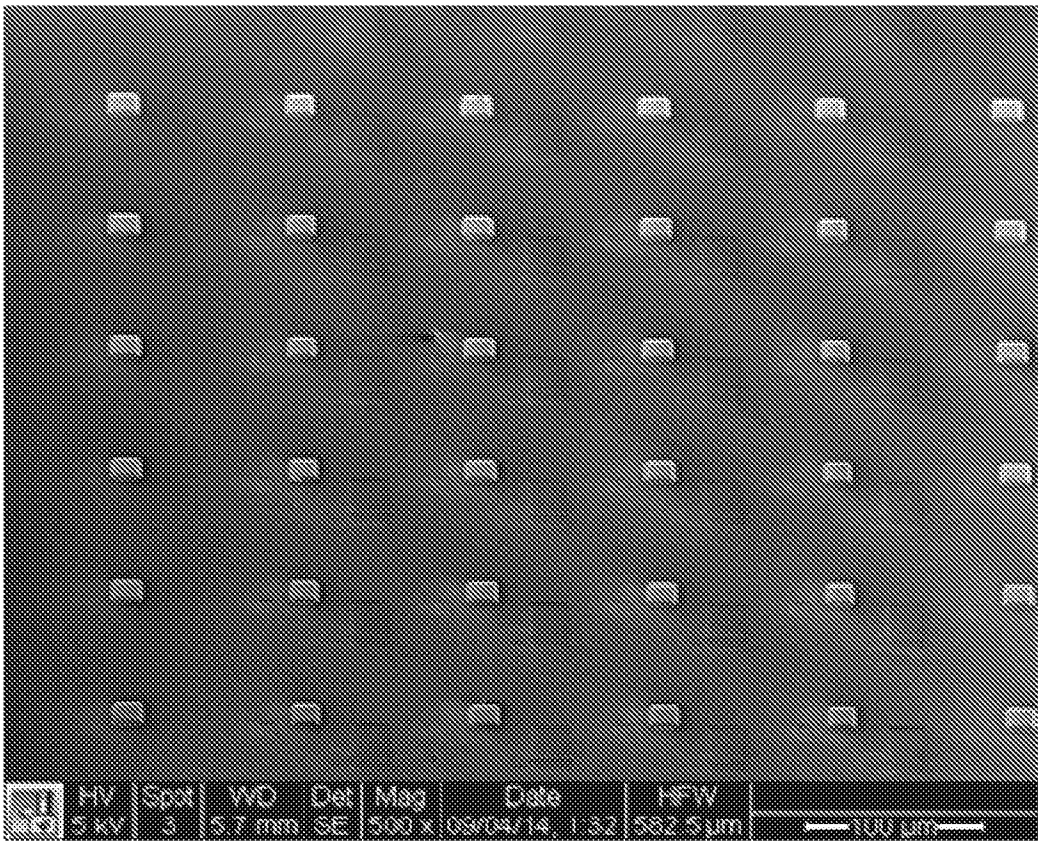

Figure 9B

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US16/33783

A. CLASSIFICATION OF SUBJECT MATTER
IPC: **H01L 21/02**(2006.01),**21/308**(2006.01)

USPC: 438/507
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 438/507

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Please See Continuation Sheet

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2013/0255567 A1 (WEI et al.) 03 October 2013 (03.10.2013), entire document.	1, 2, 3/1 and 3/2

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
11 August 2016 (11.08.2016)	18 AUG 2016
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450 Alexandria, Virginia 22313-1450 Facsimile No. (571) 273-3201	Authorized officer Seungsook Ham Telephone No. (571) 272-4300

Form PCT/ISA/210 (second sheet) (April 2007)

INTERNATIONAL SEARCH REPORT	International application No. PCT/US16/33783

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☒ Claims Nos.: 4-30
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
Claims 4-30 are improper multiple dependent claims and are not drafted in accordance with the second and third sentences PCT Rule 6.4(a).

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of any additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT	International application No. PCT/US16/33783

Continuation of B. FIELDS SEARCHED Item 3:
EAST: US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
Search Terms: epitaxial$3, semiconductor, protective, layer, particle, nuclei, protect$4