(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
15 May 2008 (15.05.2008)

PCT

(10) International Publication Number
WO 2008/057371 A3

(51) International Patent Classification:
G06F 13/00 (2006.01)

(21) International Application Number:
PCT/US2007/023050

(22) International Filing Date:
1 November 2007 (01.11.2007)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/856,053 1 November 2006 (01.11.2006) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI,

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(54) Title: TRAP-CHARGE NON-VOLATILE SWITCH CONNECTOR FOR PROGRAMMABLE LOGIC

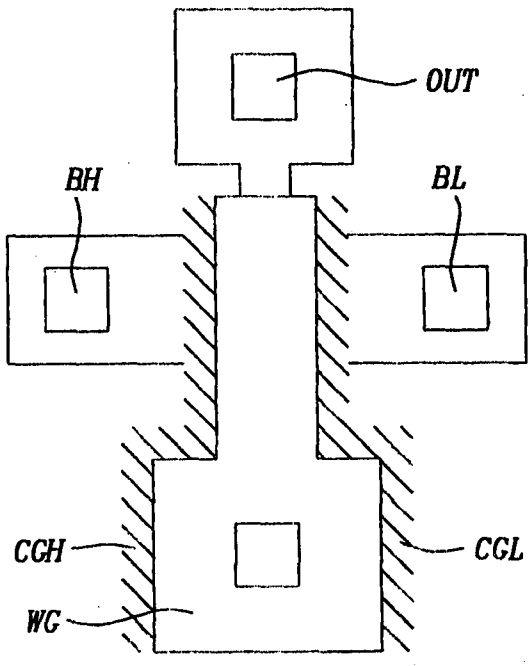

FIG. 6

(57) Abstract: A nonvolatile trap charge storage cell selects a logic interconnect transistor uses in programmable logic applications, such as FPGA. The nonvolatile trap charge element is an insulator located under a control gate and above an oxide on the surface of a semiconductor substrate. The preferred embodiment is an integrated device comprising a word gate portion sandwiched between two nonvolatile trap charge storage portions, wherein the integrated device is connected between a high bias, a low bias and an output. The output is formed by a diffusion connecting to the channel directly under the word gate portion. The program state of the two storage portions determines whether the high bias or the low bias is coupled to a logic interconnect transistor connected to the output diffusion.

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FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

— *of inventorship (Rule 4.17(iv))*

Published:

— *with international search report*

(88) Date of publication of the international search report:
23 October 2008

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 07/23050

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - G06F 13/00 (2008.01)
USPC - 711/101
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
USPC: 711/101

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC: 711/100, 101, 105, 154, 170; 710/8, 12, 22, 64, 73

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
USPTO WEST (PGPB, USPT, EPAB, JPAB); Google Scholar
Search terms: memory or storage or nonvolatile, trap charge, transistor connected in series, switch connector, word gate, logic element or array, p channel transistor, tunnel, programmable logic, switch on or off etc.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6,788,111 B2 (SUN et al.) 07 September 2004 (07.09.2004), abstract, Fig 2A, 2B, 3, col 2, ln 10-43, col 4, ln 21-64, col 6, ln 11 to col 7, ln 48	1-25
A	US 2005/0219900 A1 (KAMIGAKI et al.) 06 October 2005 (06.10.2005)	1-25
A	US 2005/0201189 A1 (FUJIWARA et al.) 15 September 2005 (15.09.2005)	1-25
A	US 2005/0012134 A1 (MASUOKA et al.) 20 June 2005 (20.06.2005)	1-25
A	US 2001/0019151 A1 (CAYWOOD) 06 September 2001 (06.09.2001)	1-25

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"A" document defining the general state of the art which is not considered to be of particular relevance
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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
18 February 2008 (18.02.2008)	31 MAR 2008
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (April 2007)