(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
22 December 2016 (22.12.2016)

WIPO | PCT

(10) International Publication Number
WO 2016/201526 A1

(51) International Patent Classification:
C23C 14/30 (2006.01) *H01L 21/70* (2006.01)
C23C 14/00 (2006.01) *H01L 21/77* (2006.01)
C23C 14/14 (2006.01) *H01L 41/00* (2013.01)
C23C 14/16 (2006.01) *H01L 41/02* (2006.01)
C23C 14/24 (2006.01) *H01L 41/04* (2006.01)
H01L 27/00 (2006.01) *H01L 41/08* (2006.01)
H01L 27/20 (2006.01) *H01L 41/18* (2006.01)
H01L 21/00 (2006.01) *H01L 41/35* (2013.01)
H01L 21/62 (2006.01)

(21) International Application Number:
PCT/AU2016/050520

(22) International Filing Date:
20 June 2016 (20.06.2016)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
2015902363 19 June 2015 (19.06.2015) AU

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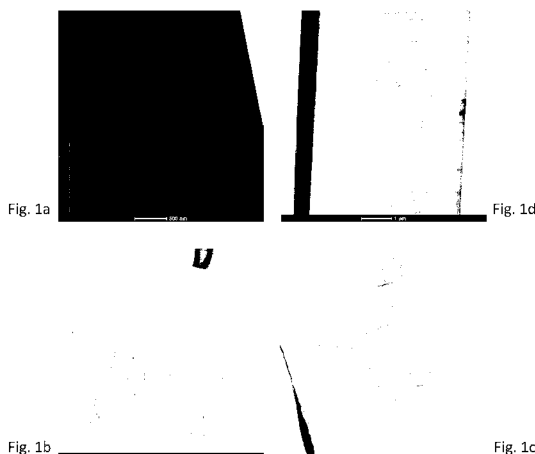
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report (Art. 21(3))*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

(54) Title: SILICON FILM AND PROCESS FOR FORMING SILICON FILM



(57) Abstract: A process for forming a thick silicon film comprises depositing a thick film of silicon by ultra-high vacuum electron beam deposition.

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SILICON FILM AND PROCESS FOR FORMING SILICON FILM

BACKGROUND

The disclosure relates to low stress, low thermal budget, high thickness silicon films, and a process for forming the films comprising depositing by ultra-high vacuum electron beam evaporation. The film and process are described particularly in relation to use in Micro-Electro-Mechanical Systems (MEMS). However, it will be clear to a person skilled in the art that the process and resultant film can be utilised for alternative uses.

SUMMARY

Disclosed in some forms is a process for forming a thick silicon film, the process comprising depositing silicon by ultra-high vacuum electron beam deposition.

The process allows formation of thick silicon films exhibiting excellent mechanical properties. Thick, low stress films are useful for high performance inertial sensors like accelerometers and gyroscopes as they allow the formation of high aspect ratio structures. Currently, such structures are formed either from SOI (Silicon-On-Insulator) or high temperature Chemical Vapor Deposited (CVD) epi-poly [2-4] or LPCVD based HARPSS (High Aspect Ratio Polysilicon Silicon Structures). However, these technologies may require chemical mechanical polishing or high temperature deposition and annealing, which is not appealing for low thermal budget applications.

In some forms the deposition occurs at a substrate deposition temperature of less than approximately 500°C, or less than approximately 460°C. In some forms the deposition occurs at a substrate deposition temperature of between 350°C and 400°C yet achieve full crystallisation.

Silicon films can be deposited at a low thermal budget using various techniques. They include LPCVD (Low Pressure Chemical Vapor Deposition), PECVD (Plasma Enhanced Chemical Vapor Deposition), sputtering, thermal evaporation. Among these techniques, LPCVD deposited polysilicon films have been extensively investigated and used for MEMS

applications. Films deposited at temperatures below 570oC are amorphous and highly compressive. Between the temperature 570oC and 610oC, they are semi-amorphous and highly tensile. Above 610oC, LPCVD films are fully crystallized and exhibit high compressive stress. High stress gradient at a low thermal budget is also the characteristics of LPCVD deposited silicon films. High temperature annealing in an inert atmosphere has been effective in reducing the stress in LPCVD polysilicon films. However, such a technique is not compatible with applications that do not tolerate high temperature processing. As a result, other methods compatible with low thermal budget have been reported. For example, LPCVD deposition of alternate thin tensile and compressive layers to form an almost overall stress free multilayered polysilicon film. But, these methods have very low deposition rates. More than 12 hours will be required to deposit just 4μm thick polysilicon film. Therefore, it is not suitable for thick silicon film formation. RF sputtered, PECVD deposited and thermal evaporated silicon films also suffer from the low deposition rates and difficulty in controlling residual stress, especially stress gradient.

In a second aspect, disclosed is a low stress thick polysilicon film formed by depositing silicon by ultra-high vacuum electron beam deposition.

In a third aspect, disclosed is a process for fabricating a MEMS or NEMS device comprising depositing a thick polysilicon film onto an integrated circuit or a CMOS die.

BRIEF DESCRIPTION OF THE FIGURES

The disclosure will now be described in view of the Figures, in which,

Fig. 1a shows an X-TEM image of a film of one embodiment of the present disclosure;

Fig. 1b shows an X-TEM image of a film of another embodiment of the present disclosure;

Fig. 1c shows an X-TEM image of a film of another embodiment of the present disclosure;

Fig. 1d shows an X-TEM image of a film of another embodiment of the present disclosure;

Fig 2 shows a graphical representation of the measured average distance of early crystallization from Si/SiO2 interface at various substrate temperatures;

Fig. 3(a) graphically represents the as-deposited film fraction of crystallization as a function of substrate deposition temperatures determined from Raman Spectra;

Fig. 3(b) graphically represents the as-deposited film fraction of crystallization with higher dopant concentrations at various deposition rates determined from Raman Spectra.

Fig. 4 graphically represents the as-deposited film ratio of (110)/(111) oriented grains in one embodiment of the disclosure;

Fig. 5 graphically represents the as-deposited film measured grain sizes at varied substrate temperatures;

Fig. 6 graphically represents the stress and surface roughness of 4μm thick as-deposited silicon films for various substrate temperatures at 100nm/min deposition rate;

Fig. 7 graphically represents the as-deposited film stress behaviour of 4μm thick evaporated silicon as a function of deposition rate at a substrate temperature of 500oC;

Fig. 8a shows an X-TEM image of a film of another embodiment of the present disclosure;

Fig. 8b shows an X-TEM image of a film of another embodiment of the present disclosure;

Fig. 8c shows an X-TEM image of a film of another embodiment of the present disclosure;

Fig. 8d shows an X-TEM image of a film of another embodiment of the present disclosure;

Fig. 8e shows an X-TEM image of a film of another embodiment of the present disclosure;

Fig. 8f shows an X-TEM image of a film of another embodiment of the present disclosure;

Fig. 9 graphically represents stress characteristics of silicon films evaporated at 100nm/min rate annealed at 600oC for 19 hours. The substrate temperature for each film is indicated on the plot.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE DISCLOSURE

Disclosed in some forms is a process for forming a thick silicon film, the process comprising depositing silicon by ultra-high vacuum electron beam deposition.

In some forms the deposition occurs at a substrate deposition temperature of less than approximately 460°C while achieving full crystallization.

In some forms the silicon is doped polysilicon. In some forms the silicon is doped with boron or phosphorous.

In some forms the silicon is boron doped and the deposition temperature is between approximately 350°C and approximately 460°C. In some forms the silicon is phosphorous doped and the deposition temperature is between approximately 320°C and approximately 400°C.

In some forms the silicon has a low doping level. A low doping level is a low concentration of dopant within the silicon. In some forms the silicon is doped at a concentration of less than or approximately 5x1018/cm3.

In some forms deposition occurs at between 10 – 400 nm/minute.

In some aspects, disclosed is a thick polysilicon film formed by depositing silicon by ultra-high vacuum electron beam deposition. A thick film includes a film of greater than 20µm, or in some cases a film of greater than 30µm.

In some forms the process occurs at a substrate deposition temperature of less than approximately 460 degrees Celsius.

In some forms the silicon is doped polysilicon.

In some forms the silicon is doped with boron or phosphorous.

In some forms the silicon is boron doped and the deposition temperature is between approximately 350°C and approximately 460°C.

In some forms the silicon is phosphorous doped and the deposition temperature is between approximately 320°C and approximately 400°C.

Complete crystallisation occurs at these low temperatures.

In another aspect, disclosed is a process for fabricating a Micro-Electro-Mechanical Systems device comprising depositing a thick silicon film directly onto an optimised integrated circuit or directly onto a CMOS die.

In yet another aspect, disclosed is a Micro-Electro-Mechanical Systems device fabricated by the methods described.

In another aspect, disclosed is a process for fabricating a piezoelectric actuator comprising depositing a thick silicon film by ultra-high vacuum electron beam deposition, and depositing a piezoelectric film on at least one surface of the silicon film. In some forms the piezoelectric film is deposited on the two opposing surfaces of the film.

A piezoelectric actuator fabricated by the method described.

The process avoids high temperature processing for silicon films with low stress. This allows for a thick, low thermal budget silicon film to be formed even in heat sensitive applications. It has potential benefits in building MEMS structures directly on top of optimised integrated circuits allowing for low thermal budget and fewer steps in production of MEMS.

The low temperature low stress application means that layers such as a piezoelectric layer are not destroyed by the deposition process. Processing can occur post CMOS/MEMS processing.

Figures 1 through 8 show the results in the as-deposited near intrinsic or low doping concentration silicon films.

Referring to Fig. 1, disclosed is a silicon film formed by ultra-high vacuum electron beam deposition. Fig. 1a shows a film evaporated at substrate temperatures of 200°C. Fig. 1b shows a film evaporated at substrate temperatures of 400°C. Fig. 1c shows a film evaporated at substrate temperatures of 500°C. Fig. 1d shows a film evaporated at substrate temperatures of 625°C. The film in Fig. 1a is amorphous. That in 1b is partially crystallised, that in 1c and 1d is fully crystallised.

Fig. 1 shows the X-TEM images for the silicon films evaporated at a rate of 100nm/min for various substrate temperatures. Fig 1a shows a film deposited at a substrate temperature of 200oC, Fig 1b shows a film deposited at a substrate temperature of 400oC, Fig 1c shows a film deposited at a substrate temperature of 500oC, and Fig 1d shows a film deposited at a substrate temperature of 625oC.Films evaporated at less than 300oC were amorphous. Those evaporated between 300oC and 400oC were semi-amorphous. Films deposited at 500oC were fully crystallised. Those deposited at 575oC or above were fully crystallised with a coarse grain

In some forms, the semi-amorphous E-beam evaporated silicon films have columnar microstructure on top of amorphous silicon layer as seen from Fig 1(b). On the other hand, semi- amorphous silicon films deposited by LPCVD have quite a different microstructure consisting of an amorphous silicon layer on top of devitrified elliptical grains.

The average distance at which early crystallization occurs above the Si/SiO2 interface is measured for various substrate deposition temperatures and plotted in Fig. 2 which utilises a near-intrinsic silicon film. The distance represents the average thickness of the amorphous layer above the Si/SiO2 interface. As can be seen from Fig. 2, the amorphous layer thickness reduces quite sharply initially for temperatures below 400°C with the onset of crystallization and then completely disappears at 500oC. The amorphous layer is reduced from 2500nm at 370oC to 600nm with only 30oC increase in substrate temperature. The reduction in the amorphous layer is only 100nm when the substrate temperature increases from 430oC to 460oC.

Fig. 3(a) shows the determined fraction of crystallization of the as-evaporated near-intrinsic silicon films with dopant concentration of approximately 5 x 1014 or 5 x 1015/cm3

at various substrate deposition temperatures. The films deposited at 300oC and below are completely amorphous with zero percentage of crystallization while those evaporated at 500oC and above are fully crystallized showing 100% of crystallization. Between 300oC and 500oC, the films are partially crystallized with percentage of crystallization exceeding 90% at 460oC. These characteristics of the evaporated silicon films are quite different from those silicon films formed using other deposition techniques such as LPCVD. LPCVD silicon films are known to be amorphous even at 570oC and only fully crystallized above 610oC. Hence, the E-beam evaporated silicon films uniquely display early crystallization, that is, crystal grain formation at comparatively lower substrate temperature. Such behaviour is particularly attractive for low thermal budget applications.

Fig. 3(b) shows the determined fraction of crystallization of the as-evaporated silicon films with higher dopant concentrations at various deposition rates as a function of substrate deposition temperatures demonstrating that full crystallisation is achieved at 400°C or lower with the appropriate dopant concentration and deposition rate. An example of this is phosphorus concentration of 5x1018/cm3 at a deposition rate of 50nm/min.

To observe the effect of the substrate temperature during deposition on the composition of grain orientations, the ratio of intensity peak for (110) oriented grains to that of (111) is plotted as a function of substrate temperature and presented in Fig. 4. The figure indicates that the ratio of (110) oriented grains to that of (111) increases exponentially with an increase in substrate temperature up to a substrate temperature of 575oC before it drops down quite sharply. A similar trend has also been observed for both (110)/(331) and (110)/(311) crystal orientations. This behaviour of E-beam evaporated silicon films is considerably different from those of LPCVD deposited silicon films even though similar crystal orientations exist in both cases. Semi-amorphous LPCVD silicon films formed typically at a substrate temperature ranging from 570°C to 610°C tend to have a higher proportion of (111) oriented grains while fully crystallized films above 610°C have predominantly (110) oriented grains.

Average grain size is obtained from TEM measurements for films deposited at various substrate temperatures and shown in Fig. 5. One can identify two regions from the figure. The first region covers the substrate temperatures ranging from 370oC to 575oC. It is

characterized by fine-grain formation and gradual increase in the average grain sizes. As the substrate temperature goes above 575oC, a second region that is characterized by a coarse-grain film formation is obtained. The average grain size in the second region is increased by 250% with only 50oC change in temperature.

Fig. 6 shows measured average residual stress of the E- beam evaporated near-intrinsic silicon films for various substrate temperatures. The amorphous films deposited at 300°C and below are tensile with the stress reducing as the substrate temperature increases. A rapid change in stress can be observed as the substrate temperature changes from 300oC to 370oC. This can be attributed to the onset of crystal grain formation in the film. The semi-amorphous films evaporated at 370oC and below 500oC exhibit low stress that vary from tensile at lower temperatures to compressive at higher temperatures. From observations of the TEM images, the semi-amorphous E-beam evaporated silicon films have a crystallized layer over an amorphous layer. The grain formation in the crystallized layer involves competitive crystal grain growth that results in the development of compressive stress in the layer. As the thickness of the crystallized layer increases with the substrate temperature above 370°C, the film becomes proportionally less and less tensile and eventually becomes compressive.

The stress-substrate temperature characteristic of the E-beam evaporated silicon films is very different from that of LPCVD silicon films in three ways: (i) The stress in as-deposited amorphous LPCVD silicon films is highly compressive while that of E-beam evaporated amorphous silicon films is highly tensile. (ii) The semi-amorphous LPCVD silicon films are highly tensile while those of evaporated semi-amorphous silicon films are low tensile or compressive. (iii) For as-deposited fully crystallized silicon films, LPCVD films are highly compressive while those of fully crystallized E-beam evaporated films exhibit relatively low compressive stress. It is important to note that the compressive stress in the fully crystallized E-beam evaporated silicon films change gradually with substrate temperature. Hence, it is more controllable. As the substrate temperature increases from 300oC to 370oC, a jump in surface roughness can be observed. This is related to the occurrence of film crystallization between these temperature ranges. As the deposition temperature increases further, the surface roughness increases only slightly up to 575oC and increases dramatically as the substrate temperature rises to 625oC.

The stress levels in the as-deposited silicon films can further be controlled by the deposition rate. Fig. 7 shows the film stress for various deposition rates at a substrate temperature of 500oC. Results indicate that the compressive stress in the film reduces as the deposition rate increases. The stress in the film is only -25MPa at the deposition rate of 400nm/min.

Smoother films can be formed by reducing deposition rate. The rms surface roughness is reduced by more than 50% when the deposition rate goes down from 100nm/min to 50nm/min. Although the surface roughness increases as the deposition rate rises, the increment in roughness is only small and even marginal at higher deposition rates. Similar trends have also been observed at other substrate temperatures.

The X-TEM images of E-beam evaporated silicon films formed at substrate temperatures of 200oC, 370oC and 430oC before and after annealing at 600oC are shown in Fig. 8. Annealing causes the amorphous and semi- amorphous films to fully crystallize. In the case of the amorphous film in Fig 8(a), the microstructure of the film after annealing as seen in Fig 8(b) is random and uniform across the cross-section. It is characterized by large grains, as large as 1μm. However, two different textures can be identified with the annealed semi-amorphous films in Fig. 8(d) and (f): fine columnar grains on the top and random large grains on the bottom. The fine columnar grains are from the crystallized layer of the film before the annealing and do not show any apparent change after the annealing. High tensile stress is not desirable in some applications as it may lead to film cracking and peeling. However, for fully and almost fully crystallized silicon films, annealing can help to relieve the compressive stress by introducing tensile stress.

Fig. 9 shows the post-deposition annealing behavior at 600°C for Si films deposited at 430oC, 460oC, 500oC, 575oC and 625oC substrate temperatures for various durations. The compressive stress reduces and even becomes tensile as the annealing time progresses. Most of the change in stress occurs during the first one hour of annealing and from there on further stress change is minimal. The reduction in the compressive stress is associated with the occurrence of recrystallization, which is known to cause film shrinkage in fine-grained polysilicon films and hence introduce tensile stress. It should be noted that this phenomena is different from the as-deposited film where the competitive crystal grain formation during

deposition produced compressive films. The introduced tensile stress is moderate and proportional to the difference between the deposition substrate temperature and the annealing temperature. The higher the difference is, the higher the introduced tensile stress is. Annealing the films evaporated at 460oC, 500oC and 575oC has introduced an additional 70MPa, 50MPa, and 20MPa tensile stresses, respectively. Annealing the film evaporated at 430oC substrate temperature resulted in comparatively higher tensile stress.

The surface morphology study on the annealed films has shown that the annealing does not affect the surface morphology of the evaporated films appreciably.

While the disclosure speaks of using the process of deposition of thick film polysilicon for MEMS fabrication, the process can be utilised for alternative polysilicon film applications.

It is to be understood that, if any prior art publication is referred to herein, such reference does not constitute an admission that the publication forms a part of the common general knowledge in the art, in Australia or any other country.

In the claims which follow and in the preceding description of the disclosure, except where the context requires otherwise due to express language or necessary implication, the word “comprise” or variations such as “comprises” or “comprising” is used in an inclusive sense, i.e. to specify the presence of the stated features but not to preclude the presence or addition of further features in various embodiments of the invention.

Claims:

1. A process for forming a thick silicon film, the process comprising:
depositing a thick film of silicon by ultra-high vacuum electron beam deposition.

2. A process as defined in claim 1, wherein the deposition occurs at a substrate deposition temperature of less than approximately 500oC.

3. A process as defined in claim 2, wherein the substrate deposition temperature is less than approximately 460oC.

4. A process as defined in any of the preceding claims, wherein the silicon is doped polysilicon.

5. A process as defined in claim 4, wherein the silicon is doped with boron or phosphorous.

6. A process as defined in claim 5, wherein the silicon is boron doped and the deposition temperature is between approximately 350oC and approximately 460oC.

7. A process as defined in claim 5, wherein the silicon is phosphorous doped and the deposition temperature is between approximately 320°C and approximately 400°C.

8. A process as defined in any one of claims 4 through 7, wherein the silicon has a low doping level.

9. A process as defined in claim 8, wherein the silicon is doped at a concentration of less than approximately 5x1018/cm3.

10. A process as defined in any of the preceding claims, wherein the deposition rate is between 10 – 400 nm/minute.

11. A thick polysilicon film formed by depositing silicon by ultra-high vacuum electron beam deposition to a thickness of greater than 20µm.

12. A film as defined in claim 11, wherein the process occurs at a substrate deposition temperature of less than approximately 460°C.

13. A film as defined in claim 11 or 12, wherein the silicon is doped polysilicon.

14. A film as defined in claim 13, wherein the silicon is boron doped and the substrate deposition temperature is between approximately 350°C and approximately 460°C.

15. A film as defined in claim 13, wherein the silicon is phosphorous doped and the deposition temperature is between approximately 320°C and approximately 400°C.

16. A process for fabricating a Micro-Electro-Mechanical Systems or a Nano-Electro Mechanical Systems device comprising depositing a thick silicon film directly onto an optimised integrated circuit.

17. A Micro-Electro-Mechanical Systems device or a Nano-Electro Mechanical Systems device fabricated by the method defined in claim 16.

18. A process for fabricating a piezoelectric actuator comprising depositing a thick silicon film by ultra-high vacuum electron beam deposition, and depositing a piezoelectric film on at least one surface of the silicon film.

19. A process as defined in claim 18, comprising depositing a piezoelectric film on two opposing surfaces of the silicon film.

20. A piezoelectric actuator fabricated by the method of claim 18 or 19.

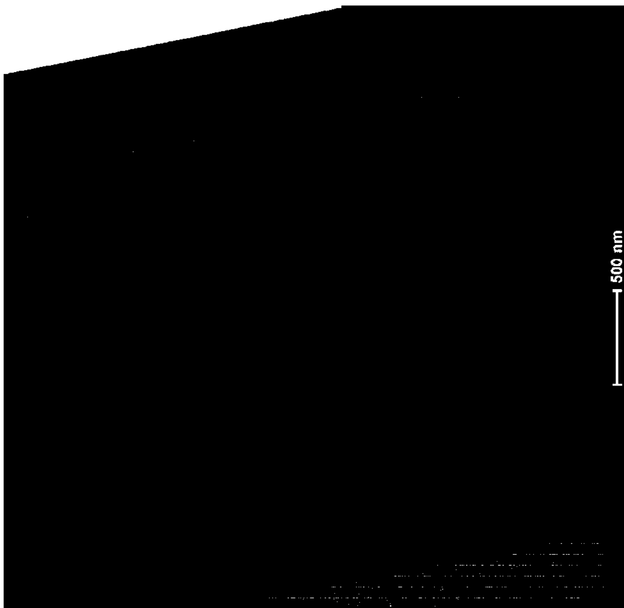

Fig. 1a

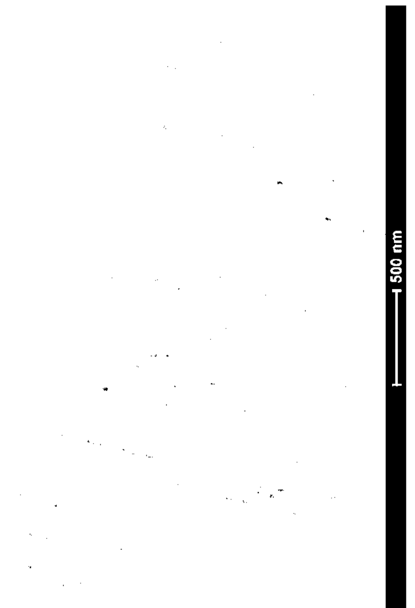

Fig. 1b

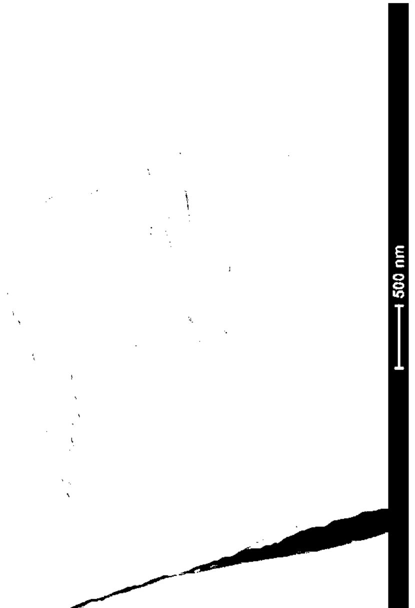

Fig. 1c

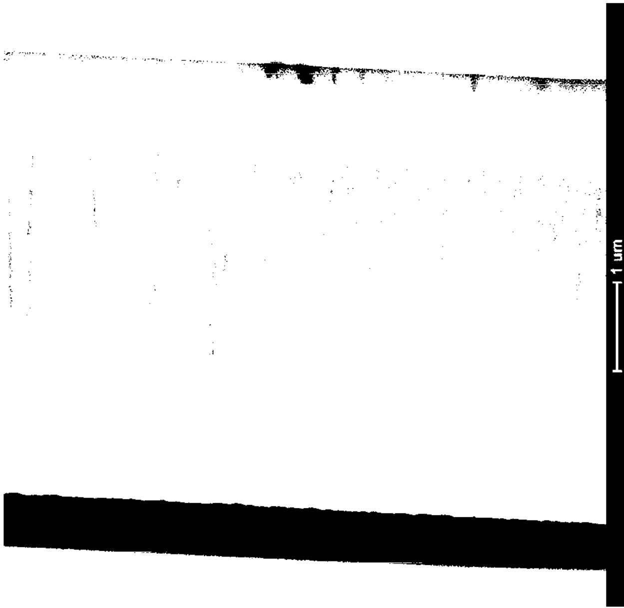

Fig. 1d

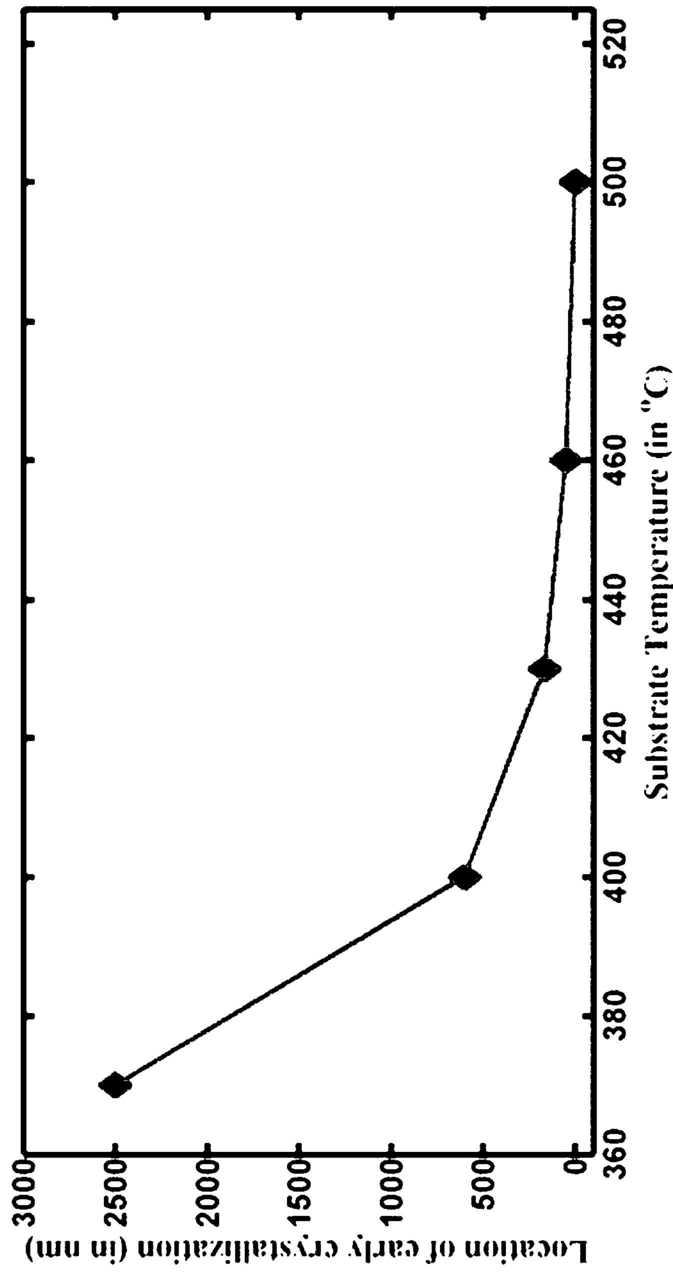

Fig. 2

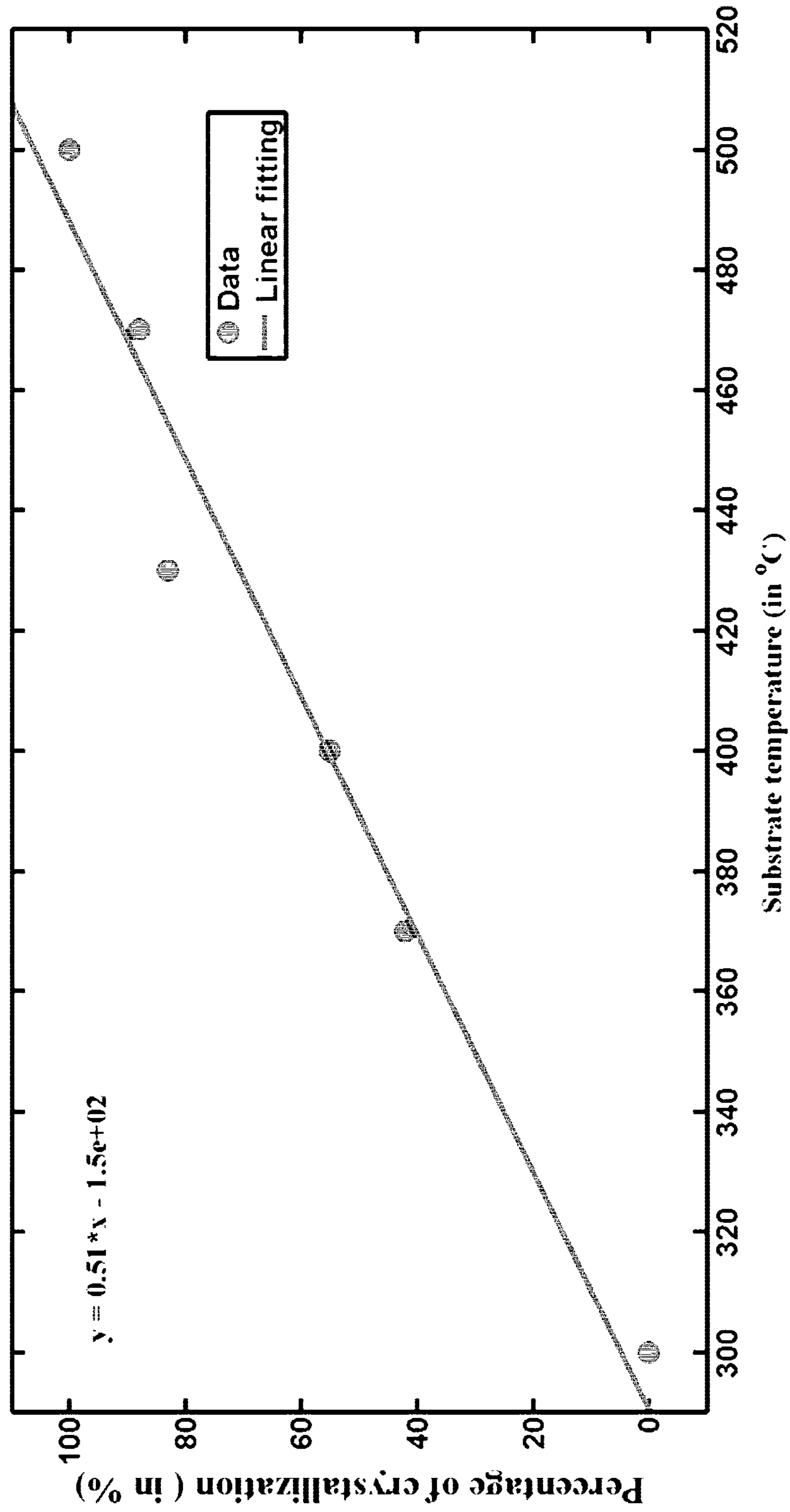

Fig. 3a

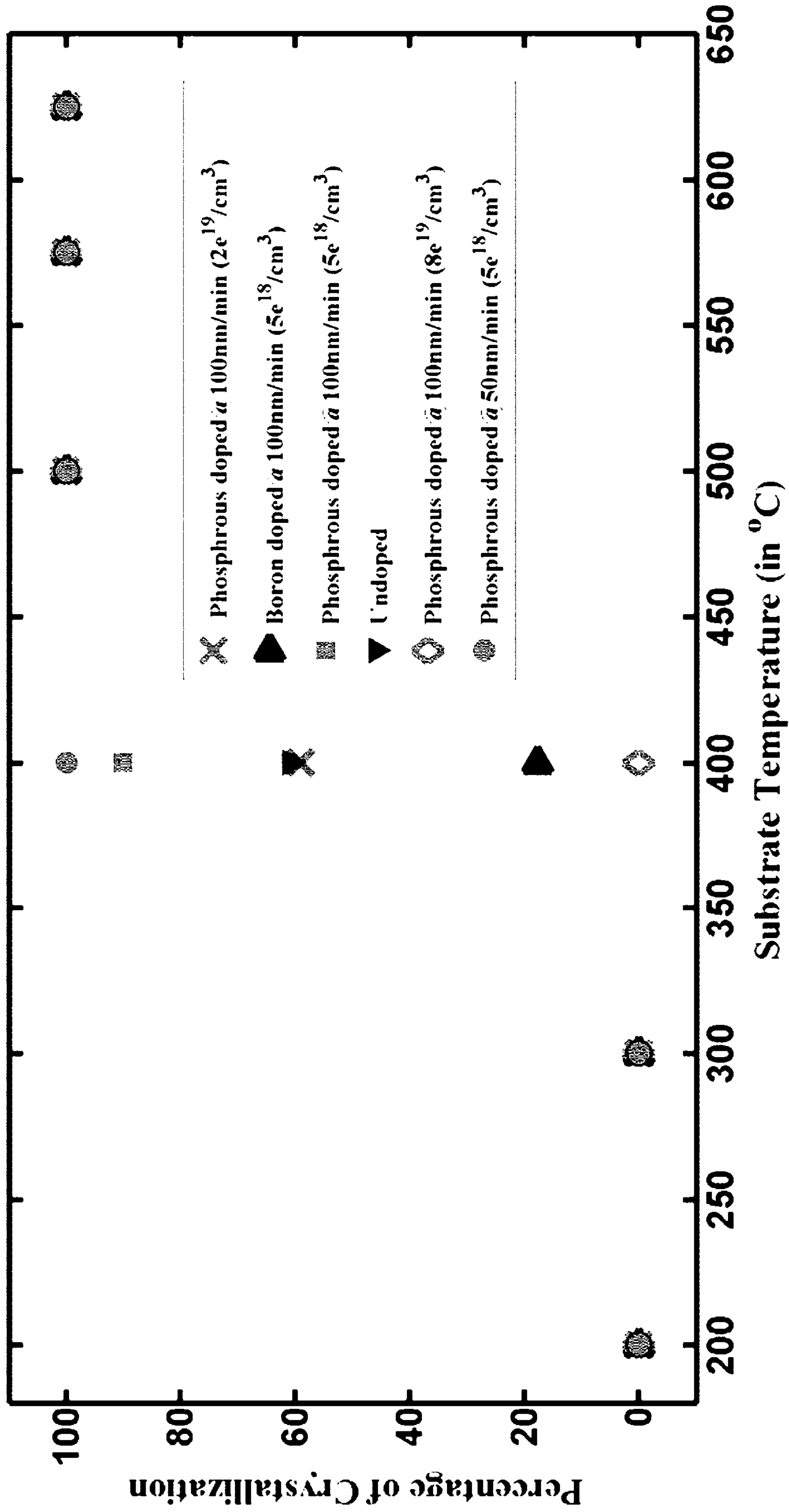

Fig. 3b

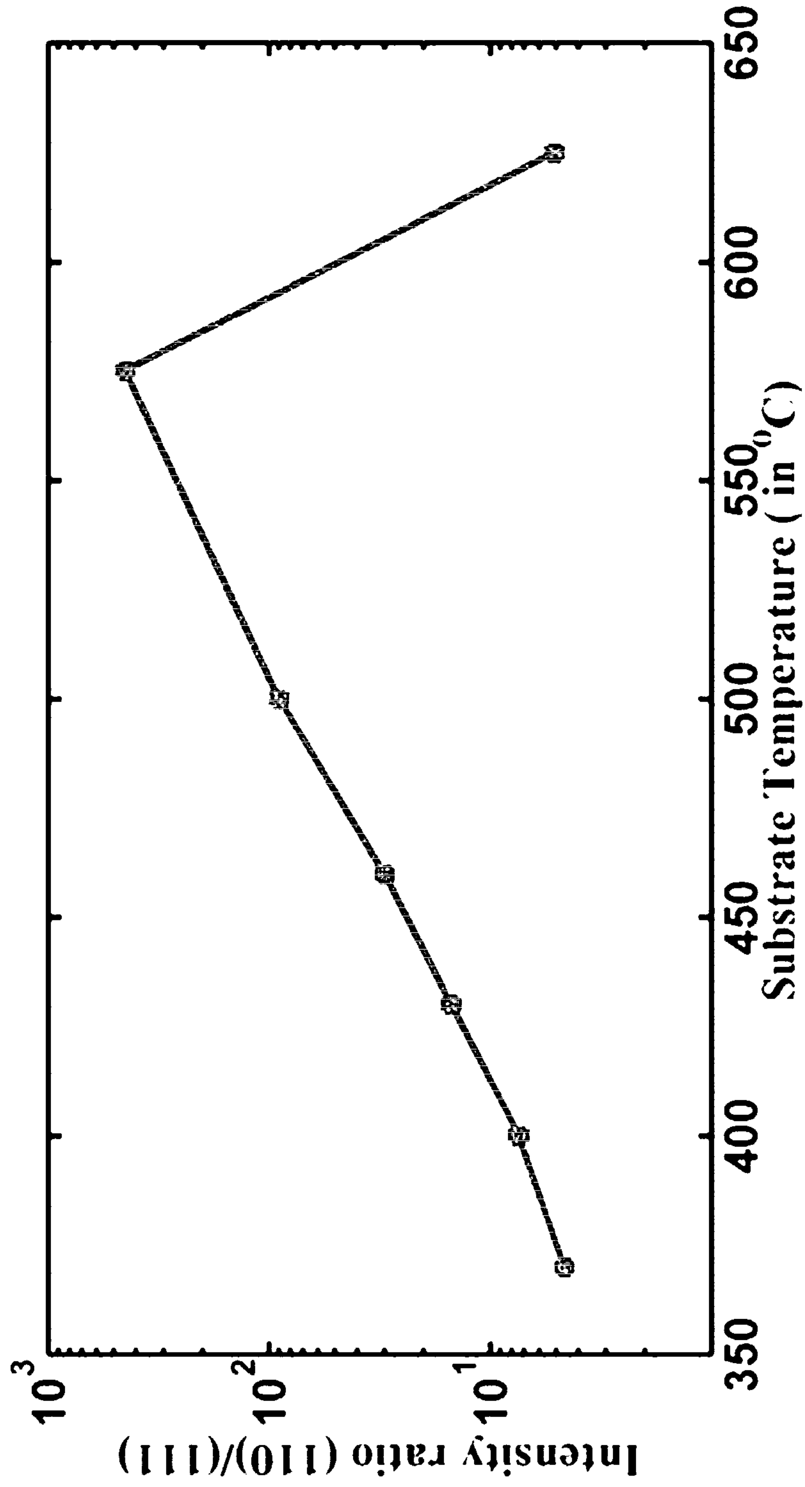

Fig. 4

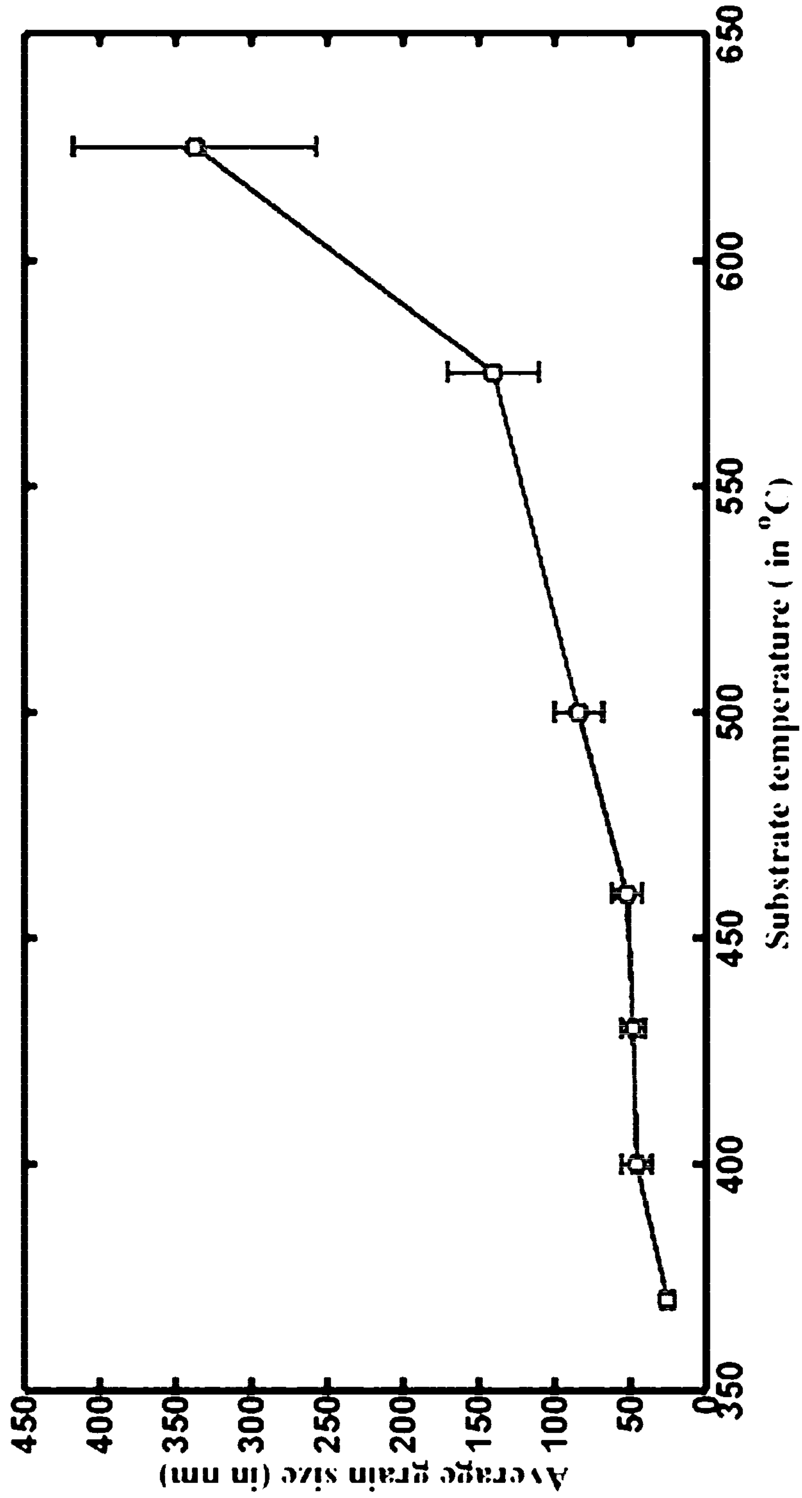

Fig. 5

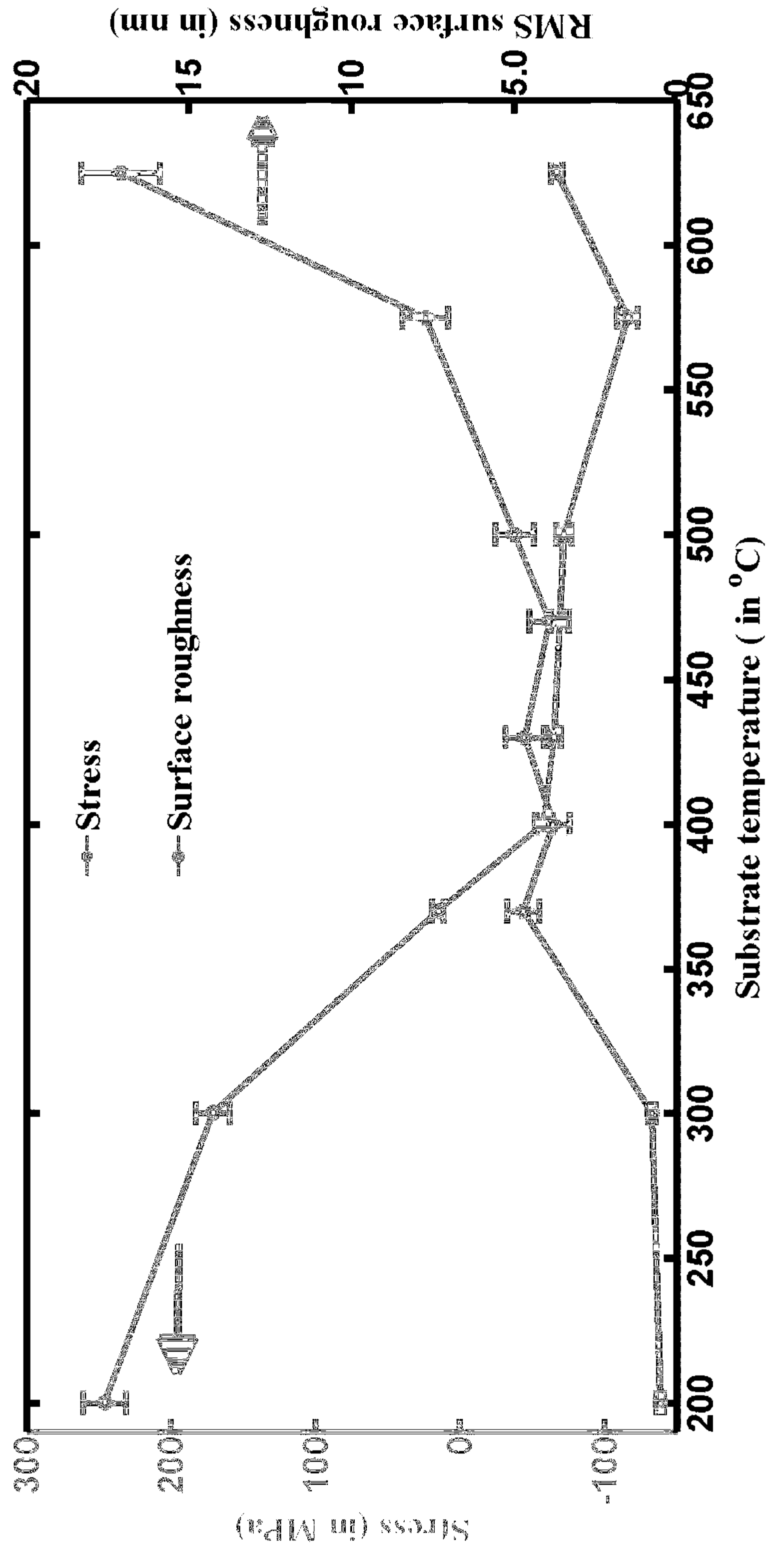

Fig. 6

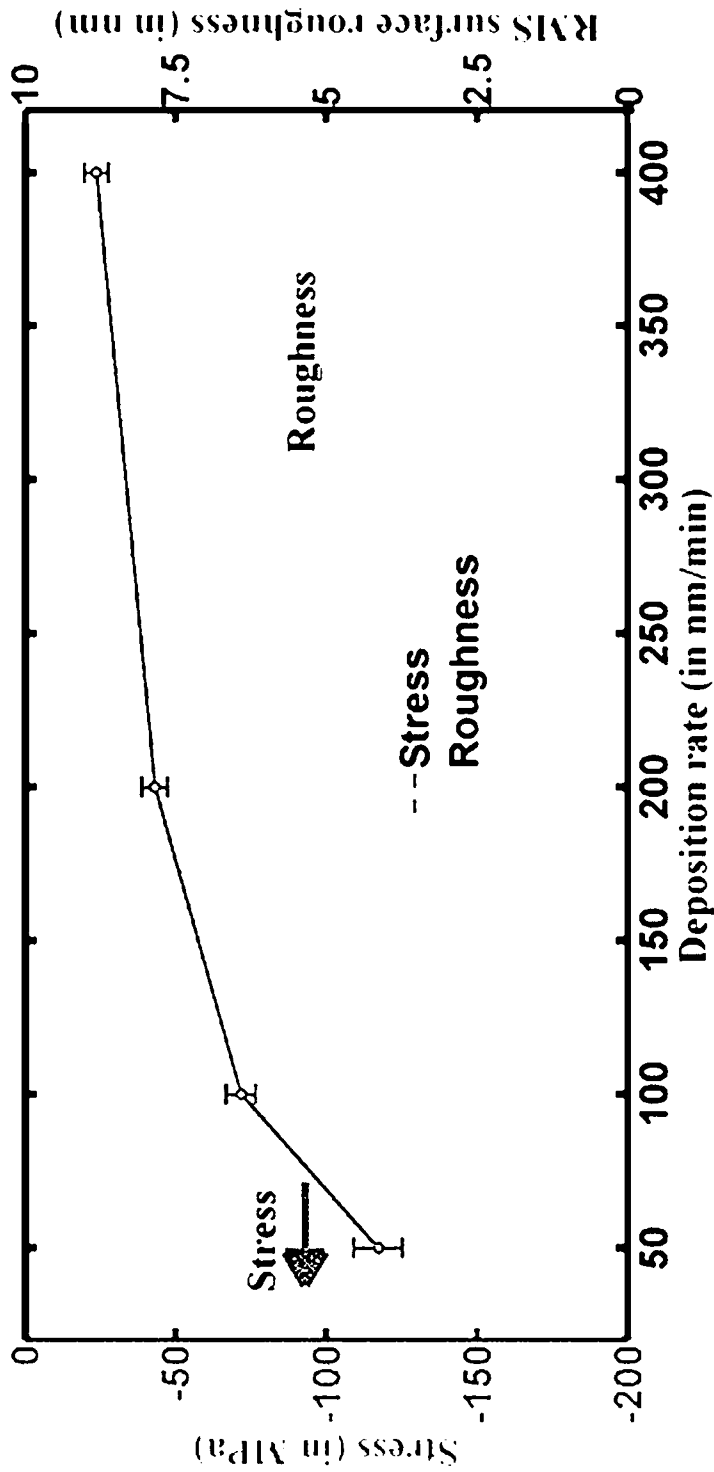

Fig. 7

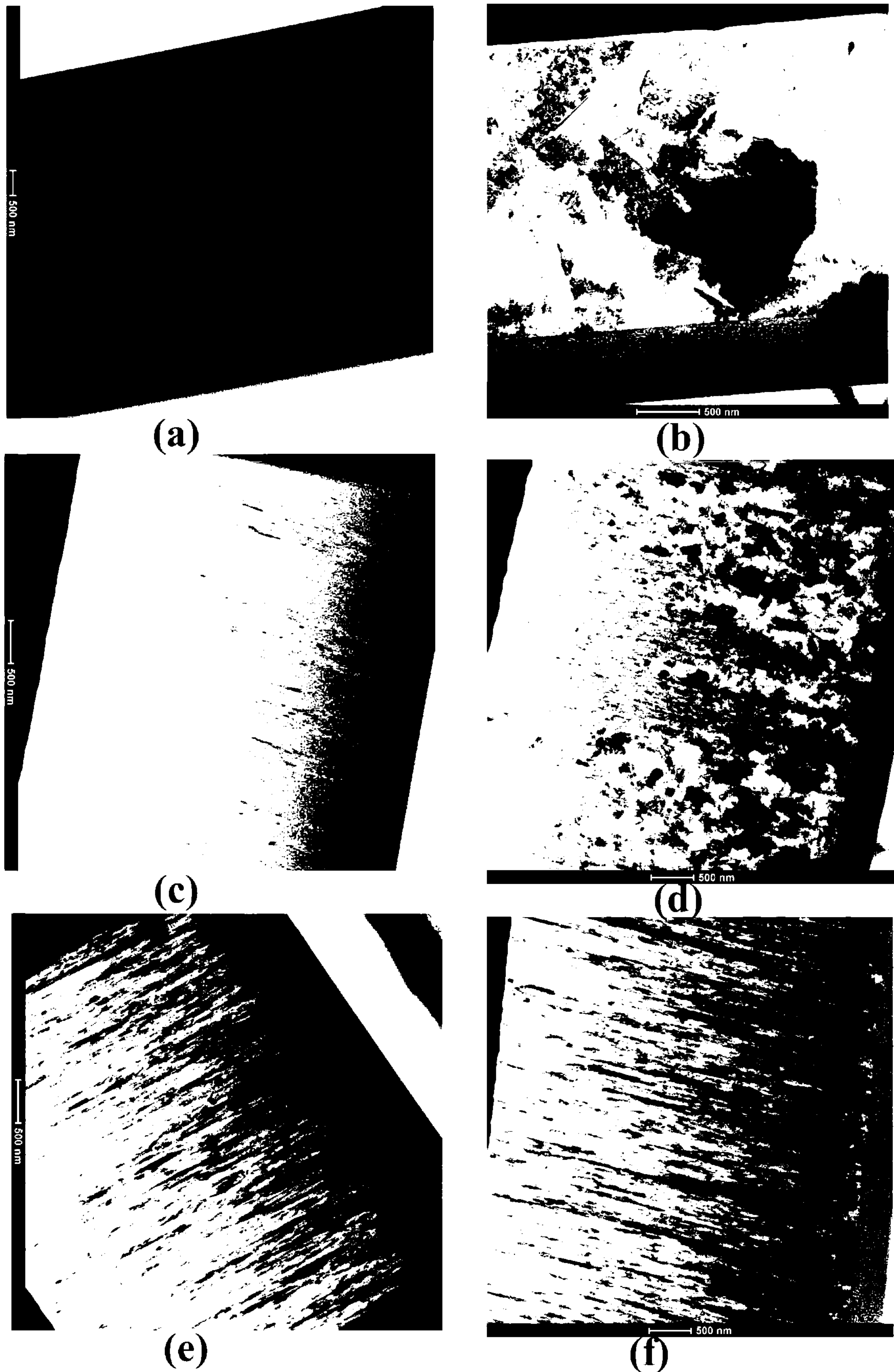

Fig. 8

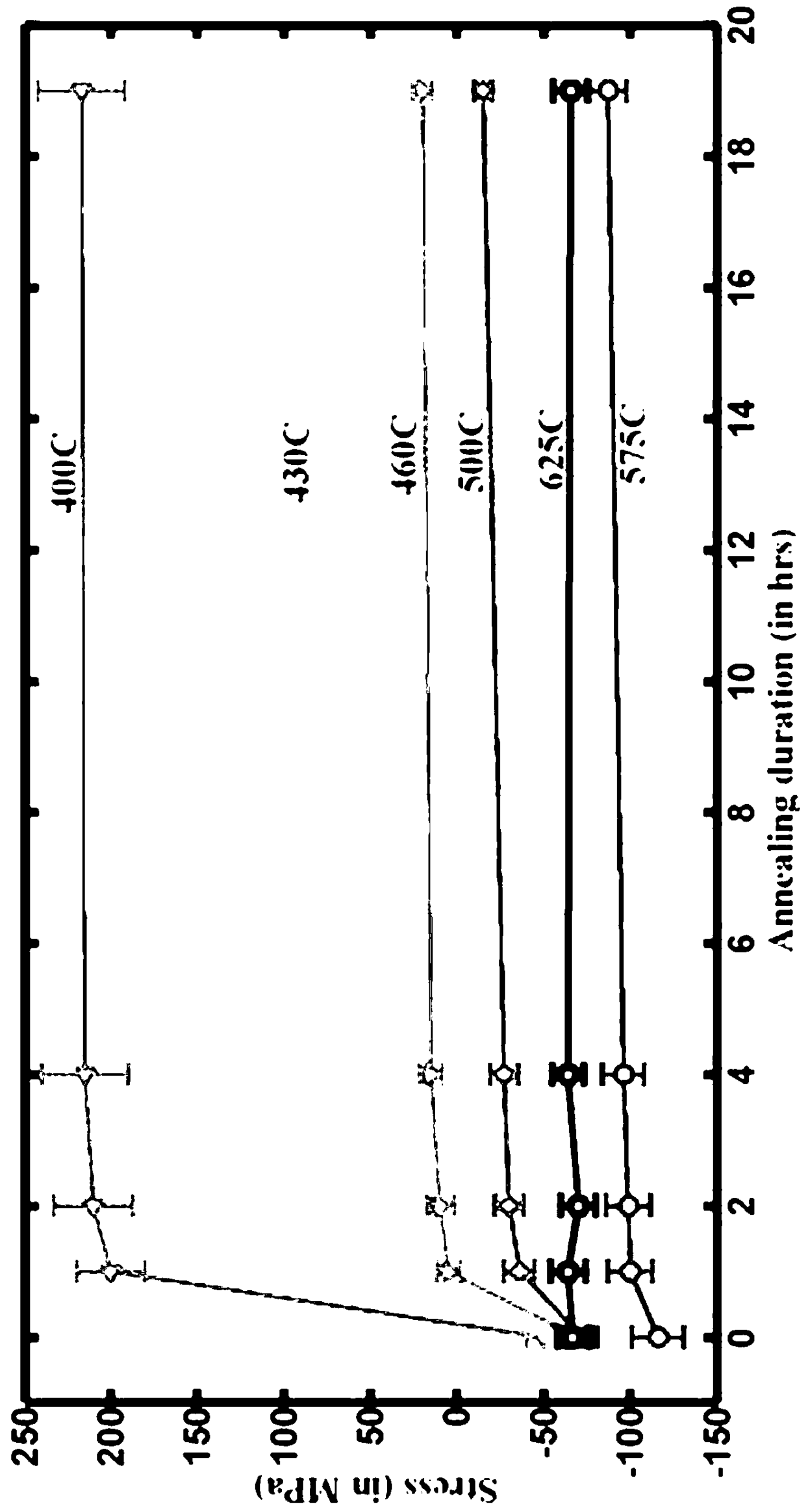

Fig. 9

INTERNATIONAL SEARCH REPORT	International application No. **PCT/AU2016/050520**

A. CLASSIFICATION OF SUBJECT MATTER

[See Supplemental Sheet]

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Databases consulted TXPEA, TXPEB, TXPEC, TXPEE, TXPEF, TXPEH, TXPEI, TXPEP, TXPEPEA, TXPES, TXPUSE0A, TXPUSE1A, TXPUSEA, TXPUSEB, TXPWOEA, EPODOC, WPIAP: search of H01L27/00, H01L27/20, H01L41/00, H01L41/02, H01L41/04, H01L41/08, H01L41/18, H01L41/35, H01L21/20/low, h01l21/02, C23C14/00, C23C14/14, C23C14/16, C23C14/24, C23C14/30 and keywords "Si", silicon+, poly_silicon+, MEMS, NEMS, Micro_electr+, nano_electr+, +electro_mecha+), Substrat+, (ultra-high or high) 1d vacuum+, OR +FILM+, +LAYER+, +COAT+, SURFAC+, Semi_conduct+, +piezo+, piezo_electric+, Actuator+, actuat+, (electron 3d beam+), EBPVD, PVD) and deposit+

Applicant(s)/Inventor(s) name searched in internal databases provided by IP Australia, and also in Espacenet and Google

ESPACENET AND GOOGLE Advanced Patent search with keywords: ultra high vacuum, silicon film, electron beam and like terms

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
	Documents are listed in the continuation of Box C	

[X] Further documents are listed in the continuation of Box C   [X] See patent family annex

* Special categories of cited documents:

- "A" document defining the general state of the art which is not considered to be of particular relevance
- "E" earlier application or patent but published on or after the international filing date
- "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- "O" document referring to an oral disclosure, use, exhibition or other means
- "P" document published prior to the international filing date but later than the priority date claimed
- "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
- "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
- "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
- "&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
18 November 2016	18 November 2016
Name and mailing address of the ISA/AU AUSTRALIAN PATENT OFFICE PO BOX 200, WODEN ACT 2606, AUSTRALIA Email address: pct@ipaustralia.gov.au	**Authorised officer** Gregory Diven AUSTRALIAN PATENT OFFICE (ISO 9001 Quality Certified Service) Telephone No. 0262832992

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:

   because they relate to subject matter not required to be searched by this Authority, namely:

   the subject matter listed in Rule 39 on which, under Article 17(2)(a)(i), an international search is not required to be carried out, including

2. ☐ Claims Nos.:

   because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos:

   because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a)

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

See Supplemental Box for Details

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☒ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT		International application No.
C (Continuation).	DOCUMENTS CONSIDERED TO BE RELEVANT	**PCT/AU2016/050520**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
	EP 0056737 A2 (HITACHI LTD) 28 July 1982	
X	abstract, page 5 line 27- page 6 line 3, page 9 lines 11-18, page 10 lines 18-21	1-6, 8-14
Y	abstract, page 5 line 27- page 6 line 3, page 9 lines 11-18, page 10 lines 18-21	18-20
	EP 1605499 A2 (INTERUNIVERSITAIR MICROELEKTRONICA CENTRUM) 14 December 2005	
X	abstract, paragraphs [0041], [0022], [0024], table 1	1
	US 2013/0284258 A1 (KARIN CHAUDHARI ET AL) 31 October 2013	
A	abstract	1
	US 2014/0242785 A1 (ASHOK CHAUDHARI) 28 August 2014	
A	abstract	1
	US 8227285 B1 (YANG) 24 July 2012	
X	abstract, column 3 lines 38-40, column 2 lines 5-7	16-17
Y	abstract, column 3 lines 38-40, column 2 lines 5-7	18-20
	US 2013/0207281 A1 (COMMISSARIAT A L'ENERGIE ATOMIQUE ET AUX ENE ALT) 15 August 2013	
A	abstract	16-17
	WO 2013/078141 A1 (QUALCOMM MEMS TECHNOLOGIES INC) 30 May 2013	
A	abstract	16-17
	JP S62-012697 A (NEC CORP) 21 January 1987	
X	whole document	1
	JP S61253855 A (HITACHI LTD) 11 November 1986	
X	whole document	1
	US 5907792 A (DROOPAD ET AL) 25 May 1999	
X	abstract, column 3 line 35- column 4 line 26	1

Supplemental Box

Continuation of: **Box III**

This International Application does not comply with the requirements of unity of invention because it does not relate to one invention or to a group of inventions so linked as to form a single general inventive concept.

This Authority has found that there are different inventions based on the following features that separate the claims into distinct groups:

- Claims 1-10, 11-15, 18-20 are directed to forming a thick silicon film by depositing a thick film of silicon using an electron beam and ultra-high vacuum. The feature of forming a thick silicon film by depositing a thick film of silicon using an electron beam and ultra-high vacuum is specific to this group of claims.

- Claims 16-17 are directed to a process for fabricating a MEMS or NEMS device comprising depositing a thick silicon film directly onto an optimised integrated circuit. The feature of to a process for fabricating a MEMS or NEMS device comprising depositing a thick silicon film directly onto an optimised integrated circuit is specific to this group of claims.

PCT Rule 13.2, first sentence, states that unity of invention is only fulfilled when there is a technical relationship among the claimed inventions involving one or more of the same or corresponding special technical features. PCT Rule 13.2, second sentence, defines a special technical feature as a feature which makes a contribution over the prior art.

When there is no special technical feature common to all the claimed inventions there is no unity of invention.

In the above groups of claims, the identified features may have the potential to make a contribution over the prior art but are not common to all the claimed inventions and therefore cannot provide the required technical relationship. The only feature common to all of the claimed inventions and which provides a technical relationship among them is depositing a thick silicon film onto a surface

However this feature does not make a contribution over the prior art because it is disclosed in:

EP 0056737 A2 (HITACHI LTD) 28 July 1982

Therefore in the light of this document this common feature cannot be a special technical feature. Therefore there is no special technical feature common to all the claimed inventions and the requirements for unity of invention are consequently not satisfied *a posteriori*.

Supplemental Box – IPC Marks

C23C 14/30 (2006.01)

C23C 14/00 (2006.01)

C23C 14/14 (2006.01)

C23C 14/16 (2006.01)

C23C 14/24 (2006.01)

H01L 27/00 (2006.01)

H01L 27/20 (2006.01)

H01L 21/00 (2006.01)

H01L 21/62 (2006.01)

H01L 21/70 (2006.01)

H01L 21/77 (2006.01)

H01L 41/00 (2013.01)

H01L 41/02 (2006.01)

H01L 41/04 (2006.01)

H01L 41/08 (2006.01)

H01L 41/18 (2006.01)

H01L 41/35 (2013.01)

INTERNATIONAL SEARCH REPORT Information on patent family members	International application No. **PCT/AU2016/050520**

This Annex lists known patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

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		US 2015263201 A1	17 Sep 2015
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Due to data integration issues this family listing may not include 10 digit Australian applications filed since May 2001.

INTERNATIONAL SEARCH REPORT Information on patent family members	International application No. **PCT/AU2016/050520**

This Annex lists known patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document/s Cited in Search Report		**Patent Family Member/s**	
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		US 2010187652 A1	29 Jul 2010
		US 8148781 B2	03 Apr 2012
		US 8227911 B1	24 Jul 2012
		US 8395252 B1	12 Mar 2013
		US 8421082 B1	16 Apr 2013
		US 2012248506 A1	04 Oct 2012
		US 8432005 B2	30 Apr 2013
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INTERNATIONAL SEARCH REPORT Information on patent family members	International application No. **PCT/AU2016/050520**

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Patent Document/s Cited in Search Report		Patent Family Member/s	
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JP S61253855 A	11 November 1986	JP S61253855 A	11 Nov 1986
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End of Annex

Due to data integration issues this family listing may not include 10 digit Australian applications filed since May 2001.