

[54] **COUNT DISPLAY SYSTEM**
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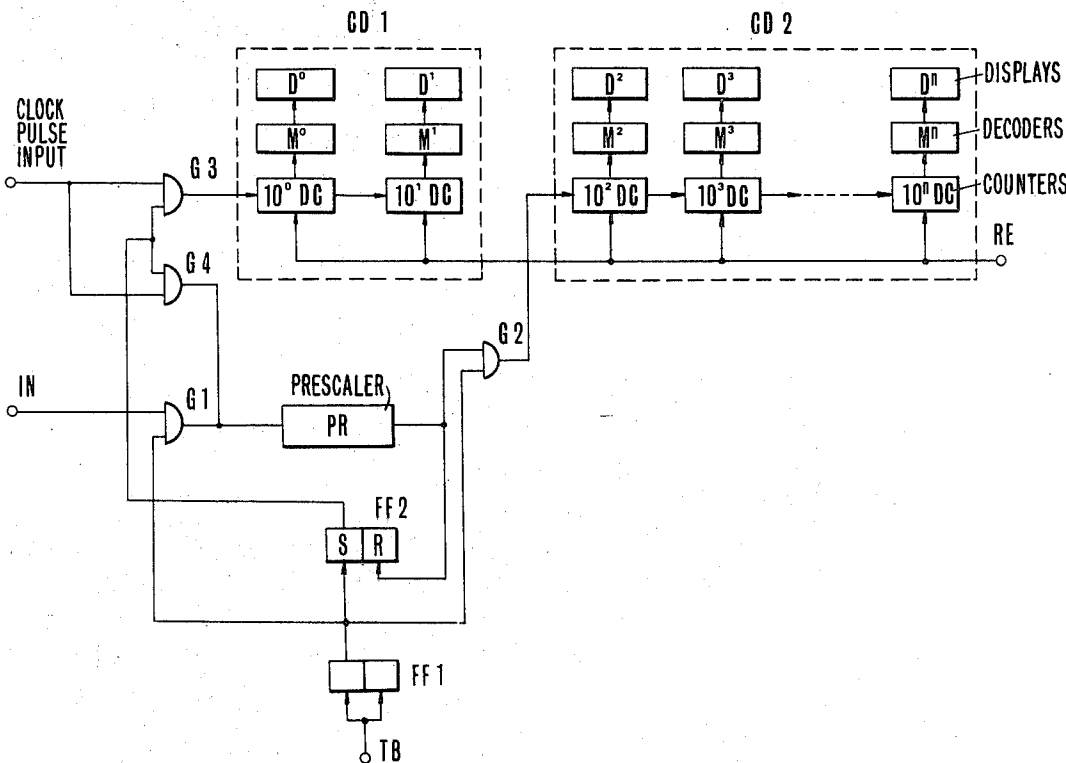
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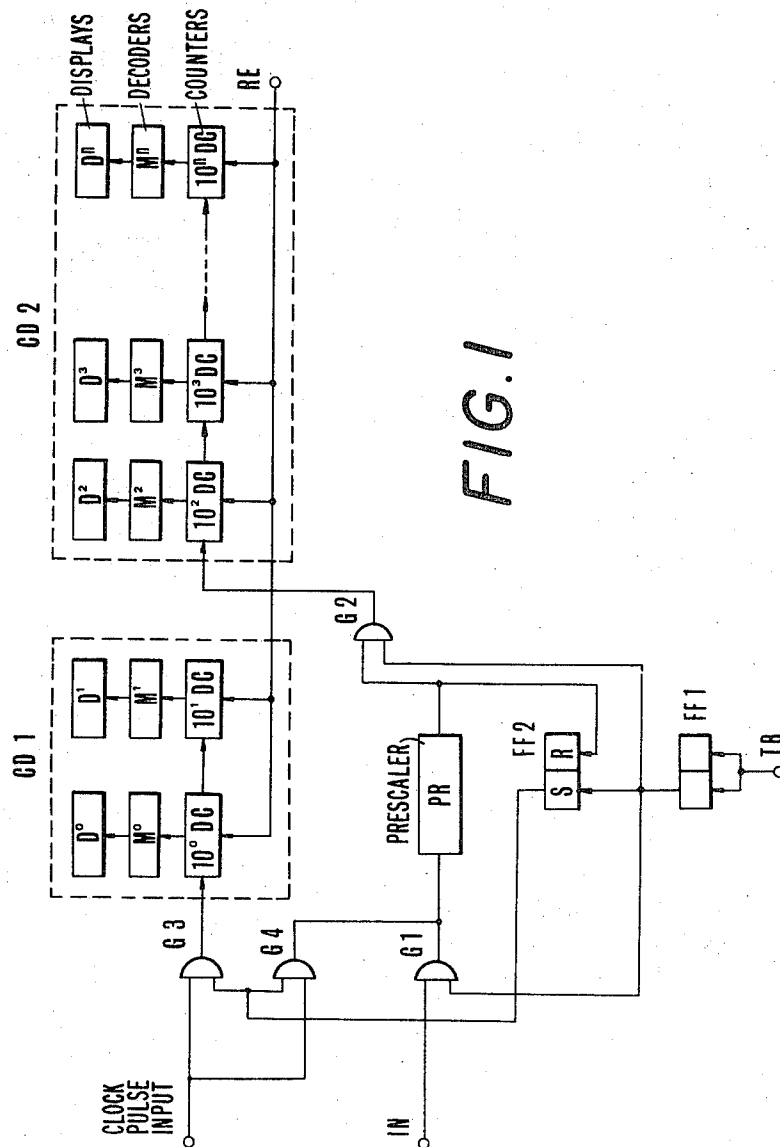
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[57] **ABSTRACT**
A count display system having count display devices for counting and displaying numerals of different orders of magnitude, a prescaler having a ratio of frequency division preset in accordance with the lower orders, a first gate circuit responsive to a gate control signal for supplying input signals to the prescaler for a predetermined time interval, a second gate circuit responsive to the gate control signal for supplying the output from the prescaler to the count display device of higher orders, additional circuits responsive to the gate control signal and the output from the prescaler for applying a supply of reference pulses, to the prescaler and for applying reference pulses of the same number as the reference pulses supplied to the prescaler to the count display device of the lower orders so as to calculate the difference between the limiting value of the frequency division of the prescaler and the value actually counted by utilizing the reference pulses.

5 Claims, 6 Drawing Figures

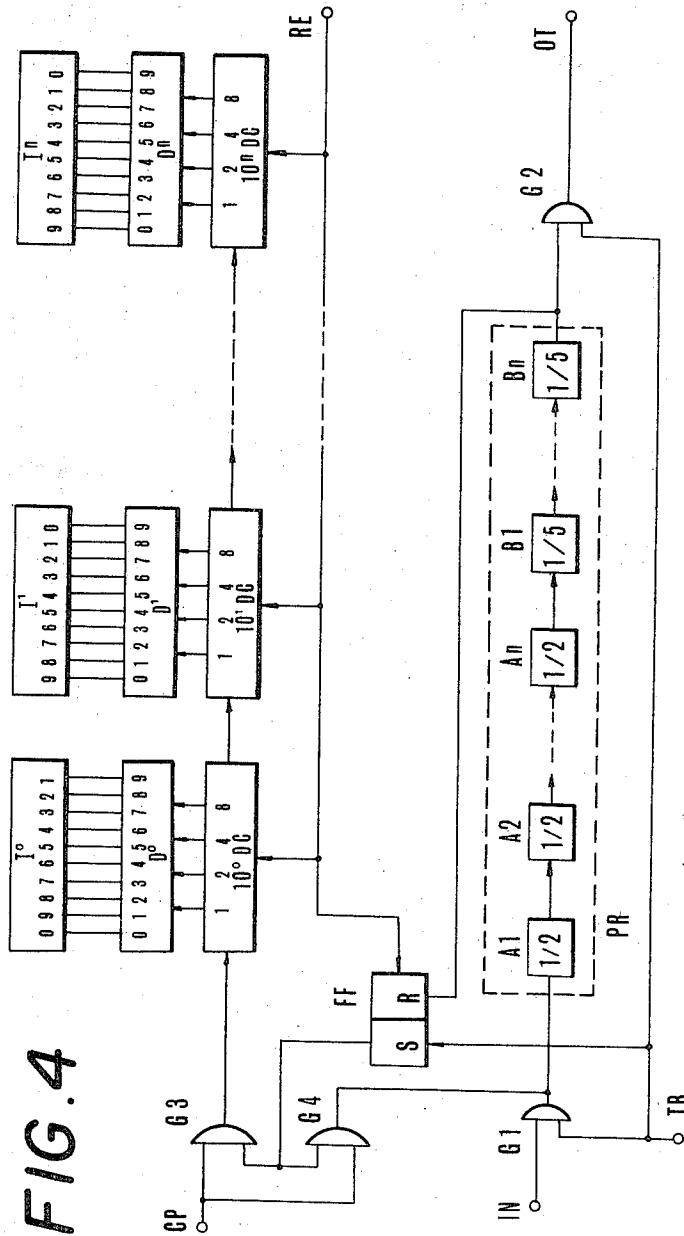




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FIG. 5

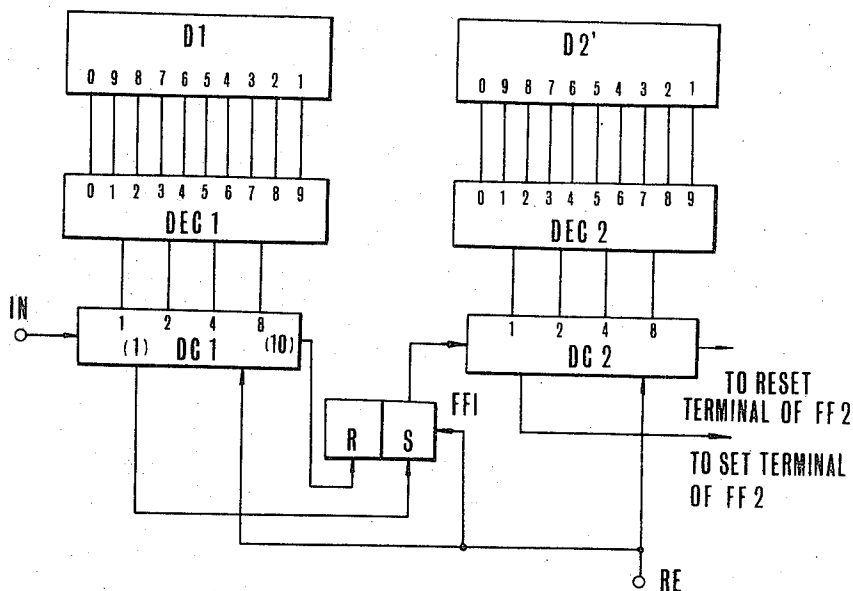
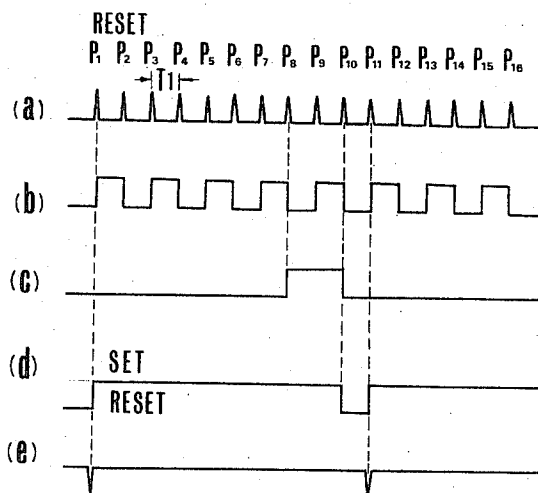


FIG. 6



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COUNT DISPLAY SYSTEM

BACKGROUND OF THE INVENTION

This invention relates to a count display system and more particularly to a count display system utilizing a prescaler system.

The prescaler system has been used to display counts of high frequency signals. According to this system, a prescaler of a predetermined ratio of frequency division is provided in front of a standard counter so as to divide the frequency of the high frequency signal at a prescribed ratio. The frequency divided high frequency signal is then supplied to a conventional counter thus indirectly counting or measuring the high frequency signal.

With this system, however, in order to improve the resolution of counting, it is necessary to increase the counting time in proportion to the ratio of frequency division, thus prolonging the measuring time. Although a method has been proposed wherein the resolution of counting is improved without increasing the counting time, the conditions generally required for the prescaler are strict and require a complicated combination of special counting circuits thus increasing the cost of the counting device. Another fatal defect of such a system lies in an extreme difficulty in reading out the content of the counter. For this reason it has been the common practice to reduce the ratio of frequency division or to use particular ratios such as one-tenth and one-hundredth, which sacrifices the resolution of counting.

SUMMARY OF THE INVENTION

Accordingly the principal object of this invention is to provide an improved count display system utilizing a prescaler.

Another object of this invention is to provide a novel count display system capable of manifesting a desired resolution without utilizing a too high ratio of frequency division.

Still another object of this invention is to provide a novel count display system which can decrease the measuring time with high resolution.

A further object of this invention is to provide an improved count display system in which the content of the prescaler can be readily read with a simple circuit.

Yet another object of this invention provide an improved count display system which does not require resetting the prescaler after counting.

A further object of this invention is to provide a count display system utilizing a novel prescaler consisting of a combination of a plurality of frequency dividers of the ratios of frequency division of one-half and one-fifth, thus simplifying the construction of the prescaler.

Another object of this invention is to provide a novel count display system utilizing an improved count display circuit.

According to one embodiment of this invention there is provided a count display system comprising a first count display device for counting and displaying numerals of lower orders of magnitude, a second count display device for counting and displaying numerals of higher orders of magnitude, a prescaler having a ratio of frequency division preset in accordance with the lower orders, first gate circuit means responsive to a

gate control signal for supplying input signals to the prescaler for a predetermined time interval, second gate circuit means responsive to the gate control signal for supplying the output from the prescaler to the second count display device, reference pulse control means responsive to the gate control signal and the output from the prescaler for controlling a supply the reference pulses, means controlled by the output from the reference pulse control means for supplying the reference pulses to the prescaler, and means for supplying pulses of the same number as the reference pulses supplied to the prescaler to the first count display device so as to calculate the difference between the limiting value of the frequency division of the prescaler and the value actually calculated by utilizing the reference pulse and to display the value actually counted.

According to a modified embodiment of this invention the prescaler is comprised by a plurality of serially connected frequency dividers of the ratio of frequency division of one-half each which are connected in the earlier stages of the prescaler and a plurality of serially connected frequency dividers of the ratio of frequency division of one-fifth each which are connected in series with the first mentioned frequency dividers in the later stages of the prescaler.

There is also provided a novel count display circuit comprising a plurality of serially connected decimal counting circuits for different orders of magnitude, a plurality of decoders for converting the outputs of respective decimal counting circuits into respective decimal numbers, a plurality of display units associated with respective decoders for displaying digits 0, 9, 8 . . . 2, 1 in response to the outputs 0, 1, 2 . . . 8, 9 of the decoders, and a plurality of bistable circuits, each one of the bistable circuits being connected between two adjacent decimal counting circuits such that it is set by a signal firstly applied to the preceding decimal counting circuit and reset by the tenth signal and that the bistable circuit sends a signal to the succeeding decimal counting circuit when it is in its set condition.

BRIEF DESCRIPTION OF THE DRAWING

The invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings in which:

FIG. 1 shows a block diagram of one embodiment of the novel count display system;

FIG. 2 shows waveforms for explaining the operation of various elements shown in FIG. 1;

FIG. 3 is a block diagram showing the relationship between the first count display device and a memory decoder shown in FIG. 1;

FIG. 4 shows a block diagram of a modified embodiment;

FIG. 5 shows a block diagram of an improved count display circuit and

FIG. 6 shows waveforms to explain the operation of the count display circuit shown in FIG. 5.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The preferred embodiment of the novel count display system shown in FIG. 1 comprises an input terminal IN supplied with an input signal of a frequency f_i ,

a gate control signal input terminal TB supplied with a gate control signal of a frequency f_0 and a clock pulse input signal CP supplied with a clock pulse (reference pulse) of a frequency f_c . The gate control signal applied to terminal TB is coupled to a flip-flop circuit FF1 for enabling various gate circuits to be described later for an interval T_1 . A gate circuit G_1 is enabled by the output from the flip-flop circuit FF1 for supplying the signal applied to input terminal IN to the succeeding stages for the interval T_1 . There is provided a prescaler PR connected to receive the output from gate circuit G_1 . In this example, it is assumed that the prescaler has a ratio of frequency division of 1/100. A gate circuit G_2 is connected to be enabled by the output from flip-flop circuit FF1 for supplying the signal from the prescaler PR to the second count display device CD2 in the succeeding stage for the interval T_1 . Another flip-flop circuit FF2 is provided which is connected to be set when the output from flip-flop circuit FF1 terminates and reset by the output from the prescaler PR. Gate circuits G_3 and G_4 are connected to be enabled by the output from flip-flop circuit FF2 for supplying the clock pulses applied to the clock pulse input terminal CP to succeeding stages for a predetermined time, the output of the gate circuit G_4 being connected to the output side of gate circuit G_1 , or the input side of prescaler PR.

There are provided a plurality of low speed counting circuits 10^0 DC to 10^n DC, memory decoders M^0 to M^n each connected to a corresponding one of low speed counting circuits 10^0 DC to 10^n DC and display units D^0 to D^n respectively connected to memory decoders M^0 to M^n . These elements are grouped as shown into a first count display device CD1 for counting numerals up to 100 (units order and tens order) and a second count display device CD2 for counting numerals more than 100 (hundreds and more significant orders). The low speed counting circuit 10^0 DC of the first count display device CD1 is supplied with the output from gate circuit G_3 whereas the low speed counting circuit 10^2 DC of the second count display device CD2 is supplied with the output from the gate circuit G_2 . Various elements of the second count display device CD2 have the same construction as those of a conventional count display circuit. A reset terminal RE is provided for supplying a reset signal to low speed counting circuits 10^0 DC to 10^n DC.

With reference now to FIG. 2, the operation of the novel count display system will be described hereunder.

Assume now that a gate control signal of a period T_1 as shown in FIG. 2a is impressed upon the gate control signal input terminal TB while an input signal (FIG. 2c) having a period f_s is continuously supplied to input terminal IN, then the flip-flop circuit FF1 will repeat its ON-OFF operations with the period T_1 as shown in FIG. 2b to enable gate circuits G_1 and G_2 for an interval T_1 . Consequently, the input signal supplied to input terminal IN is sent to the prescaler PR via gate circuit G_1 and counted by the prescaler. FIG. 2d shows the input signal to be counted. As above described, the prescaler is constructed to have a ratio of frequency division of 1/100, or to provide one output per 100 inputs thus producing one output each time it counts up 100 input signals which is applied to gate circuit G_2 . As this gate circuit is controlled by the output from flip-

flop circuit FF1, the gate circuit G_2 is maintained in the enabled condition when it receives the output from the prescaler so that the output from the prescaler is sent to the low speed counting circuit 10^2 DC of the second count display device CD2 and is then displayed by the display unit D^2 via memory decoder M^2 . At this time, since flip-flop circuit FF2 simultaneously, or substantially simultaneously receives a signal from flip-flop circuit FF1 and the reset signal from prescaler PR it does not enable gate circuits G_3 and G_4 .

Where the input signal supplied to input terminal IN has a longer period, for example, as shown in FIG. 2c', where only 76 input signals are supplied during the interval T_1 in which flip-flop circuit FF1 is operating, the prescaler PR will count 76 input signals during the interval T_1 , as shown in FIG. 2d' so that the prescaler PR does not produce any output within this interval T_1 . For this reason, flip-flop circuit FF2 is constructed to be set when flip-flop circuit FF1 does not send out any signal, as shown in FIG. 2g, thus enabling gate circuits G_3 and G_4 . Accordingly, the clock pulse supplied to the clock pulse input terminal CP is supplied to prescaler PR via gate circuit G_4 so that the prescaler adds the clockpulses to the count of 76 which has been counted up by this time and when it counts up a total of 100 signals it produces one output, as shown in FIG. 2e', which is supplied to gate circuit G_2 and to flip-flop circuit FF2, thus resetting the same. In this example, the number of clock pulses counted by prescaler PR equals 24 and the output from the prescaler is not sent to the second count display device CD2 because gate circuit G_2 is now disenabled. Gate circuits G_3 and G_4 are also disenabled so that no clockpulses are sent to succeeding stages.

Concurrently with the application of the clock pulse to the prescaler PR, the clock pulse is also sent to the low speed counting circuit 10^0 DC of the first count display device CD1 via gate circuit G_3 which is displayed by display unit D^0 through memory decoder M^0 . At this time, the number of clock pulses sent to the low speed counting circuit 10^0 DC is equal to the number of clock pulses that are counted by the prescaler PR, that is 24, in this case. As a consequence, two signals are supplied to low speed counting circuit 10^0 DC. After being decoded by memory decoders M^0 and M^1 these signals are supplied to display units D^0 and D^1 to display digits 7 and 6, respectively. At this time, since there is no input signal to the prescaler, it is not necessary to reset the same.

Where the input signal supplied to input terminal IN has a shorter period, for example when 176 input signals are supplied during the interval T_1 in which the flip-flop circuit FF1 is operating, the prescaler PR will produce one output when it counts up 100 input signals, which is sent to the low speed counting circuit 10^2 DC of the second count display device CD2 via gate circuit G_2 . When the next 76 pulses are supplied to the prescaler PR, the flip-flop circuit FF2 is set in the same manner as in the case discussed above where the period of the input signal is longer, thus enabling gate circuits G_3 and G_4 for supplying 24 clock pulses to the low speed counting circuit 10^0 DC of the first count display device CD1. Consequently, display unit D^2 of the second count display device CD2 displays a digit 1 whereas display units D^1 and D^0 of the first count display device CD1 display digits 7 and 6, respectively.

FIG. 3 shows the connection between displays units D^0 and D^1 , memory decoders M^0 and M^1 , and low speed counting circuits 10^0DC and 10^1DC of the first count display device $CD1$. The memory decoder is constructed to produce 10 outputs of 0,1...9 according to decimal system in response to signals 1,2,4,8 supplied by the low speed counting circuit 10^0DC . The display unit D^0 is connected to the outputs 0,1,...9 of the memory decoder M^0 in the order of 0,9,8,7...2,1. In the same manner, the memory decoder M^1 is constructed to provide 10 outputs in response to the signals supplied from the low speed counting circuit 10^1DC and the display unit D^1 is connected to the outputs 0,1,2,3...8,9 of the memory decoder M^1 in the order of 9,8,7,6...2,1,0.

Accordingly, in this example, memory decoders M^0 and M^1 provide output signals 4 and 2 whereby display units D^1 and D^0 display a numeral 76.

Considering the resolution of the system, when the interval of the clock pulses is $1\mu s$ and when the frequency f_s of the input signal equals 100 MHz , respective count display devices are required to have a resolution of at most 1 MHz . The counting time or measuring time is expressed by the sum of the time in which the gate control signal is supplied and the read out time. The former equals one second, for example, and the latter equals $100\mu s$ assuming the ratio of frequency division of the prescaler PR of $1/100$ and the interval of the clock pulses of $1\mu s$, so that the measuring time can be greatly reduced when compared with the prior art system.

As the prescaler is not required to have a precise ratio of frequency division it can be constructed with a conventional integrated circuit available on the market.

While in the above description it was assumed that the prescaler has a ratio of frequency division of $1/100$, it is to be understood that the ratio is not limited to this particular value. It desired a ratio of frequency division of $1/10$ can also be used.

Although in the illustrated example, low speed decimal counting circuits were shown, a combination of a purely binary counting circuit and a circuit which converts binary numbers into decimal can also be used. In such a case, all circuit elements can be fabricated as integrated circuit elements.

Thus, it will be noted that the invention provides a novel counting system which can count directly high frequency pulses, can provide the desired resolution without the necessity of increasing the ratio of frequency division, can greatly reduce the measuring time even when the resolution is increased, can readily read out indirectly the content of the prescaler and yet has a simple construction requiring low power. Moreover, according to this system it is not necessary to reset the prescaler to zero.

In the modified embodiment shown in FIG. 4 reference characters CP, IN and TB show identical input terminals as those shown in FIG. 1. In this case, however, a single flip-flop circuit FF is used for enabling gate circuits G_3 and G_4 for the interval T_1 in response to the control signal supplied to the gate control signal input terminal TB. Gate circuit G_1 is connected to be enabled by the gate control signal supplied to gate control signal input terminal TB for supplying the signal supplied to input terminal IN to succeeding

stages for interval T_1 . In this embodiment, the prescaler PR comprises n cascade connected frequency dividers $A_1, A_2 \dots A_n$, each having a ratio of frequency division of $1/2$, and n cascade connected frequency dividers $B_1, B_2 \dots B_n$, connected in series with the first group and each having a ratio of frequency division of $1/5$. Thus, the overall ratio of the frequency division of the prescaler equals $1/10^n$. The reason of disposing the group of the frequency divider circuits of the ratio $1/2$ in front of the group of the frequency divider circuits of the ratio of $1/5$ is based on the consideration of the characteristics of the component parts presently available on the market. More particularly, since signals of considerably high frequencies are supplied to the earlier stages of the prescaler, frequency divider circuits of the ratio of $1/2$ which can be readily formed to have relatively high frequency characteristics, about 500 MHz for example, are included in the earlier stages.

Gate circuit G_2 is connected to be enabled by the gate control signal supplied to terminal TB for supplying the output signal from the prescaler to the succeeding count display devices for interval T_1 .

Flip-flop circuit FF functions to supply the output to the succeeding stages in response to the gate control signal and to stop supply of the output in response to the output from the prescaler and is reset by the reset signal supplied to the reset terminal in a manner to be described later. As above described, gate circuits G_3 and G_4 are enabled by the output from flip-flop circuit FF for supplying the clock pulses supplied to the clock pulse input terminal CP to the succeeding stages for a predetermined interval, the output of the circuit G_4 being connected to the output of gate circuit G_1 or the input to the prescaler PR. n decimal counting circuits 10^0DC to 10^nDC are connected in series and decoders D_0 to D^n are respectively connected to the outputs of the decimal counting circuit. Each decoder functions to convert the outputs 1, 2, 4, 8 from each counting circuit into decimal digits of 0, 1, 2...8, 9 as in the first embodiment. Again, display units D^0 to D^n are connected to the outputs of respective decoders.

The reset signal is supplied to a reset terminal RE for resetting decimal counting circuits 10^0DC to 10^nDC and flip-flop circuit FF and the output from the prescaler is sent to a conventional count display device, not shown, via gate circuit G_2 and an output terminal OT.

The embodiment shown in FIG. 4 operates substantially in the same manner as that shown in FIG. 1, especially when the ratio of frequency division of the prescaler equals $1/100$.

As above described according to this embodiment the prescaler is comprised by a number of serially connected frequency dividers of the ratios of frequency division of $1/2$ and $1/5$, respectively. Consequently, to provide a ratio of frequency division of $1/100$ it is only necessary to use two frequency dividers of the ratio of $1/2$, each, and two frequency dividers of the ratio of $1/5$, each, thus obviating the necessity of using two frequency dividers of the ratio of $1/10$ which have more complicated circuit construction. As a consequence, a resolution of only 25 MHz is sufficient for each frequency divider of the ratio of $1/5$. To provide an overall ratio of frequency division of $1/1000$, it is necessary to use only three frequency dividers of the ratio of $1/2$ in

the earlier stages and three frequency dividers of the ratio of 1/5 in the later stages.

In the operation of the count display device shown in FIG. 4 when six input signals are supplied these signals are first counted by decimal counting circuit 10⁰DC and are thence sent to decoder D⁰ which functions to convert the input signal to a decimal number which is supplied to output terminal 6. At this time since no input signal is supplied to decoder D¹ from decimal counting circuit 10¹DC an output appears on its 0 output terminal. The display unit I⁰ receives the output of decoder D⁰ appearing at output terminal 6 at the corresponding input terminal 4 whereas the display unit I¹ receives the output at the output terminal 0 of decoder D¹ at the corresponding input terminal 9, thus displaying a numeral 94 which is a complement of 6 with respect to 100.

With such a construction, however, when these decimal counting circuits 10⁰DC and 10¹DC are reset by a reset signal supplied to reset terminal RE, the outputs of both decoders D⁰ and D¹ appear at their 0 output terminals thus displaying a numeral 90 upon resetting.

The invention further contemplates the provision of a novel count display device or circuit free from such defect.

FIG. 5 shows a block diagram of the novel count display circuit comprising a flip-flop circuit FF1 having a set terminal S and a reset terminal R. To the set terminal S is applied a set signal when a decimal counting circuit DC1 produces a 1 output. More particularly, flip-flop circuit FF1 is set by the first pulse supplied to flip-flop circuit FF1 and maintains its set state until a reset signal is supplied to reset terminal RE. Further, the flip-flop circuit is connected to receive at its reset terminal R a reset signal from decimal counting circuit DC1 when it counts up 10 input signals. The output of flip-flop circuit FF1 is connected to the input of a decimal counting circuit DC2 of the next order of magnitude to supply a set output.

Display unit D2' for displaying digit of tens order corresponds to the display unit I' shown in FIG. 4 but differs therefrom in that its input terminal 0 is positioned to the left of input terminal 9. In other words, ten output terminals 0, 1, 2 . . . 8, 9 of decoder DEC2 correspond respectively to input terminals 0, 9, 8, 7 . . . 2, 1 of display unit D2'. For example, input terminal 0 of display unit D2' corresponds to output terminal 0 of decoder DEC2 whereas input terminal 9 of display unit D2' to output terminal 1 of decoder DEC2. In other words, display unit D1 and decoder DEC1 for units order of magnitude and display unit D2' and decoder DEC2 for tens orders of magnitude are constructed identically.

The operation of the count display circuit shown in FIG. 5 will be described with reference to FIG. 6.

When pulses having a period T1 as shown in FIG. 6a are impressed upon input terminal IN, decimal counting circuit DC1 counts successively these pulses to provide outputs at terminals 1, 2, 4 and 8 corresponding to respective counts. FIG. 6b shows the output 1 whereas FIG. 6c output 8. Consequently, the decimal counting circuit DC1 supplies a set signal to the set terminal of flip-flop circuit FF1 in response to the first signal P1 to set the flip-flop circuit FF1 as shown in FIG. 6d.

Whereupon the output of the flip-flop circuit FF1 is supplied to the second decimal counting circuit DC2 to cause it to provide an 1 output. Decoder DEC2 converts this output into a decimal number which is supplied to display unit D2' through terminals 1 and 9, thus displaying a digit 9. At this time, since a signal is supplied to the input terminal 9 of display unit D1 from the output terminal 1 of decoder DEC1 this display unit D1 also displays 9. Thus these display units cooperate to display a numeral 99 when the first signal P1 is supplied.

The set condition of flip-flop circuit 1 is maintained until decimal counting circuit DC1 counts up 10 signals and when the tenth signal P₁₀ is supplied the counting circuit DC1 supplies a reset signal to the reset terminal R of the flip-flop circuit FF1 to reset the same. At this time, although no output is supplied to decimal counting circuit DC2 from flip-flop circuit FF1, since the output is continuously supplied to input terminal 9 of display unit D2' from output terminal 1 of decoder DEC2, display unit D2' still displays a digit 9. Consequently, both display units D1 and D2' cooperate to display a numeral 90.

Upon receiving the eleventh signal P₁₁ at the input terminal IN, decimal counting circuit DC1 functions to supply a set signal to the set terminal S of the flip-flop circuit in the same manner as when it receives the first signal P1. Accordingly, the flip-flop circuit FF1 is set and provides an output to the decimal counting circuit DC2, so that an output is supplied to decoder DEC2 from the output terminal 2 of counting circuit DC2. Decoder DEC2 converts this output into a decimal number which is supplied to display unit D2' through output terminal 2, whereby display unit D2' displays a digit 8. Since at this time display unit D1 is displaying a digit 9 the overall display is 98. The same operations are repeated for succeeding input signals.

Although the above description refers to the display of numerals of two orders of magnitude it will be clear the number of the orders of magnitude can be increased to any desired value. For example, to display numerals of three orders of magnitude, a flip-flop circuit FF2 is added between decimal counting circuit DC2 and the decimal counting circuit (not shown) for the hundreds order such that when decimal counting circuit DC2 receives the first signal the flip-flop circuit FF2 is set and when the decimal counting circuit DC2 receives the tenth signal the flip-flop circuit is reset.

Thus, according to this improved count display circuit, complements of the signals supplied to the input terminal can be displayed exactly. Accordingly, this display circuit is suitable to display a remaining period.

What is claimed is:

1. A count display system comprising a first count display device for counting and displaying numerals of lower orders of magnitude, a second count display device for counting and displaying numerals of higher orders of magnitude, a prescaler having a ratio of frequency division preset in accordance with said lower orders, first gate circuit means responsive to a gate control signal for supplying input signals to said prescaler for a predetermined time interval, second gate circuit means responsive to said gate control signal for supplying the output from said prescaler to said second count display device, reference pulse control means respon-

sive to said gate control signal and the output from said prescaler for controlling a supply of reference pulses, means controlled by the output from said reference pulse control means for supplying said reference pulses to said prescaler, and means for supplying pulses of the number as the reference pulses supplied to said prescaler to said first count display device so as to calculate the difference between the limiting value of the frequency division of said prescaler and the value actually counted by utilizing said reference pulses whereby to display the value actually counted.

2. A count display system comprising a plurality of successive count display devices, a prescaler having a ratio of frequency division preset in accordance with the number of orders of magnitude to be displayed, first gate means responsive to a gate control signal for supplying input signals to said prescaler for a predetermined time interval, second gate circuit means responsive to said gate control signal for supplying the output from said prescaler to succeeding count display devices, reference pulse control means responsive to said gate control signal and the output from said prescaler for controlling a supply of reference pulses, means controlled by the output from said reference pulse control means for supplying said reference pulses to said prescaler, and means for supplying pulses of the same number as the reference pulses supplied to said prescaler to said count display devices, said prescaler including a plurality of serially connected frequency dividers of the ratio of frequency division of $1/2$ each which are connected in the earlier stages of said prescaler and a plurality of serially connected frequency dividers of the ratio of frequency division of $1/5$ each which are connected in series with said first mentioned frequency dividers in the later stages of said

prescaler, so that the difference between the limiting value of the frequency division of said prescaler and the value actually calculated is determined by utilizing said reference pulses, whereby to display the value actually counted.

3. The count display circuit according to claim 2 wherein said count display devices comprise a plurality of serially connected decimal counting circuits for different orders of magnitude, a plurality of decoders for converting the outputs of respective decimal counting circuits into respective decimal numbers, a plurality of display units associated with respective decoders for displaying digits 0, 9, 8, . . . 2, 1 in response to the outputs 0, 1, 2 . . . 8, 9 of said decoders and a plurality of bistable circuits, each one of said bistable circuits being connected between two adjacent decimal counting circuits such that it is set by a signal firstly applied to the preceding decimal counting circuit and reset by the tenth signal applied to the preceding decimal counting circuit, said bistable circuit being adapted to send a signal to the succeeding decimal counting circuit with it in its set condition.

4. The count display system according to claim 1 wherein each of said count display devices comprises a decimal counting circuit, a decoder connected to said decimal counting circuit for converting the outputs thereof into decimal numbers and a display unit for displaying said decimal numbers.

5. The count display system according to claim 2 wherein each of said count display devices comprises a decimal counting circuit, a decoder connected to said decimal counting circuit for converting the outputs thereof into decimal numbers and a display unit for displaying said decimal numbers.

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