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IN-CIRCUIT TESTING OF LSI-BASED PCBs, ELECTRONIC PROD'N, SEP .82. "FUNCTIONAL & IN-CIRCUIT TESTING TEAM UP TO TACKLE VLSI IN THE '80's", ELECTRONICS, APR. 21,1981

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Description

This invention is concerned with improvements in or relating to circuit testers and methods of testing circuits.

The increasing use of digital logic in circuit assemblies and the increasing complexity of these digital logic circuits has generated a search for test techniques other than the traditional "functional test" methods that apply digital patterns to the circuit assembly inputs and compare the response from the circuit assembly outputs to expected values. These functional test input signals may be complex and difficult to specify properly since they must cause digital circuit activity to propagate from the circuit assembly inputs through various digital devices to the site of a potential fault and further cause transmission of signals from the fault site to the assembly output. One alternative technique is known as "in-circuit" testing. In this technique, one applies a digital pattern directly to the device under test, and detects the output from that device in order to verify proper operation.

The popularity of in-circuit testing is due to digital devices being testable, using this technique, as though they were separated from surrounding circuitry. This electrical isolation is obtained by forcing node states required by the test onto the input nodes of the device under test and looking for an expected response at its outputs. When an input node is not in agreement with the forced state, the output of the 'upstream', or driving, device must be overdriven. The amount of current required to overdrive this device is usually in excess of normal currents specified by manufacturers.

For most devices, forcing a high output state to a low state is equivalent to short-circuiting the output to ground; current flows out of the device and into the tester. When forcing a low output state to a high state, sufficient current must be supplied by the tester and backdriven into the device. The highest potential for failure as a result of overdrive current or the resulting temperature rise exists at the output stage of the overdriven device and not necessarily at the device under test. These failures will most commonly appear as bondwire failures or junction failures.

Visibility into the circuit being tested is gained through the use of a bed-of-nails fixture. This fixturing technique is a very convenient and effective way of gaining electrical access to each node in the circuit being tested. However, this fixturing interface can also lead to signal degradation. Signal degradation can compromise the quality of the in-circuit test, and potentially damage parts susceptible to voltage overshoot and undershoot. If the voltage at an input or output of a CMOS device is greater than the positive power supply voltage or less than the negative power supply voltage, the device can potentially be destroyed by CMOS latchup.

Although an in-circuit test can contribute to damage in a device due to current flow, temperature rise, and voltage over/undershoot, it is in popular use today currently for three overriding reasons.

Firstly, in-circuit testing is very effective at finding the types of faults that occur most commonly during the assembly of a printed circuit board. It is the lowest cost solution for finding solder shorts, wrongly inserted components, components damaged during the assembly process, and missing or incorrect components. In addition, in-circuit testing can also be effective at finding bad or marginal components, operational faults, and detecting process problems and trends.

The second major reason in-circuit testing is popular is the ease with which in-circuit test programs can be generated. A test program for a digital component is simply selected from a library of tests. The programmer does not have to understand the operation of the board or be able to generate stimulus that is meaningful while testing the board. In-circuit testing is highly compatible with automatic methods for test generation, and vendors of in-circuit test equipment are taking full advantage of that compatibility.

Finally, in-circuit testing is popular because it inherently produces component level diagnostic messages. If a device is isolated from surrounding circuitry through the node forcing technique, and that device fails a test of its operation, then that device is bad. Sophisticated back-tracing routines are not needed for high confidence failure messages.

Early implementation of such a technique using a probe is described in the September 1972 issue of the Hewlett-Packard Journal in an article entitled "Logic Pulser and Probe: a New Digital Troubleshooting Team", by Robin Adler and Jan R. Holland. The implementation of such a technique is disclosed in U.S. Patent Specifications Numbers 3,543,154; 3,641,509; 3,670,235; 3,781,689; and 3,965,468.

Further developments have occurred in the class of test equipment using this test technique. These developments include the ability to pulse more than one node or device at one time, the ability to pulse larger numbers of patterns in order to test more complex devices, the ability to handle third state data and others. Such equipment is manufactured by GenRad, Inc., of Concord, Massachusetts, USA. The implementations of such techniques are described in U.S. Patent Specifications Numbers 3,870,953; 4,236,246.

Other developments are described by Hansen, P. in "Functional and in-circuit testing team up to tackle VLSI in the '80s" (Electronics, 21st April 1981, pp. 189-195) and by Finnell, T.E. in "In-circuit testing of LSI-based PCBs" (Electronic Production, September 1982, pp 47-53).

The implementation of the "in-circuit" test technique requires application of a pattern directly to the device under test and measurement of the response from the device. Since digital logic circuits, except those at the input or output of the circuit assembly, are generally connected to other digital logic circuits, the application of the pattern requires overdriving the pattern which is applied by the "upstream" logic devices during normal device operation. Upstream logic devices are those devices whose outputs drive the inputs of the device under test.

Figure 1 represents a prior art design. Prior art techniques of pattern application involve taking a file of generic patterns for a specific device, combining it with a topological description of the board, and applying these patterns device by device to the board under test. The design is capable of providing a sequence of patterns to the device under test for suitable periods long enough to test the individual device. Between each test, there is a delay caused by automatic tester overhead and used for the protection of devices. These fixed periods of time permit devices upstream to cool. However, several problems are apparent. Firstly, the fixed time period between tests, unrelated to the actual time necessary for the devices upstream to cool, reduces throughput. Secondly, In order to test certain complex logic devices, it is necessary first to place these devices into a known state before beginning the test. This process, known as "homing", consists of applying a pattern or a short series of patterns of input signals, until the device responds with a certain predetermined pattern of output signals. When this pattern has been received, the device is in a known state or homed. However, if the device fails to home because of a defect, the homing pattern would be applied continuously until a fail safe timer in the circuit tester shuts down the hardware. The fail safe timer is designed to prevent the tester from applying a set of patterns indefinitely and is usually set for the maximum possible test time for the entire test sequence to be applied. This could be long after upstream devices have been damaged. Thirdly, the drivers used in the prior art have no provision for the control of overshoot which increases the risk of CMOS "latch up".

One of the primary concerns of the in-circuit test technique is the possibility of damage to the devices which are "up-stream". Since the patterns are applied directly to the device under test, this necessitates that the outputs of the up-stream device be overdriven (Figure 2). This may lead to damaging the device through various mechanisms including three specific damage mechanisms, namely CMOS "latchup", bond wire fusing, and device damage through die heating.

Table I is a list of the failure mechanisms most likely to cause device failure or significant degradation of device lifetime during in-circuit testing. Each of these failure mechanisms is accelerated by one or more of the three failure accelerators discussed above; current, temperature and voltage.

TABLE I

Failure Mechanisms	Accelerated By
Bulk Failures	
Second Breakdown	Temperature
Metallization Failures	
Electromigration	Temperature, current
Corrosion	Temperature
Interaction with other materials	Temperature
Surface Reconstruction	Temperature
Si and Si/SiO_2 Interface Failures	
Dielectric Breakdown	Temperature, voltage
Surface Charge Accumulation	Temperature
Charge Injection	Temperature, voltage
Bonding Failures	
Intermetallic Growth	Temperature
Thermal Fatigue	Temperature
Chip Mount Failures	
Thermal Fatigue	Temperature
Unique Failures	
CMOS Latchup	Voltage
Source-Drain Punchthrough	Voltage
SiO_2 Breakdown	Voltage
Bondwire Failure	Temperature, Current

Device damage can be broken into two categories. Lifetime degradation may occur during a test such that the device passes during testing and works properly in the final product, but fails prematurely in the customer's hands. The second type of damage is catastrophic, such that the device is damaged during testing and it will not operate properly in the product.

Each of the failure mechanisms in Table I was analyzed for its potential for both lifetime degradation and catastrophic failure during testing. The objectives of the research were to derive the worst case overdrive conditions under which the test might be executed, and under those conditions (subject to some imposed test constraints), minimize the potential for damage to devices during in-circuit testing. It was desirable to do this using device parameters readily available in manufacturer's data sheets, and to make the damage analysis automatic and flexible, anticipating its use for custom or proprietary parts.

Overdrive Currents

An empirical method was used to derive the worst case overdrive currents required by various logic families. Schematics of the internal circuitry of devices were analysed for worst case overdrive requirements. The results of the analysis are shown in Table II.

TABLE II

Theoretically Derived Worst Case Overdrive Currents
Values are in mA, per pin overdriven

Family	Iod	Normal Output Current	Iod/Normal
TTL	272	16	17
LTTL	23	4	6
HTTL	529	20	26
STTL	273	20	14
LSTTL	270	8	34
ASTTL	720	48	15
ALSTTL	270	8	34
CMOS	4	1	4
ECL	215	40	5

Note: For buffers, line drivers or other high current devices, the overdrive current can be larger than the values shown in this table.

MOS data is not given since it varies considerably from device to device and with the value of Vdd. If Vdd is restricted to 5 Volts then no ratios of greater than 34 were observed, so LSTTL and ALSTTL show the greatest current ratios. The worst case observed value for MOS is 175 mA.

It is important to realize that when several outputs are being overdriven in a similar manner simultaneously, the sum of the individual overdrive currents will flow through a power supply bondwire in the device. For example, if 16 address lines on a MOS microprocessor are simultaneously overdriven from a low to a high state, up to 2.8 amps of current could be required to flow through the Vcc bondwire of the processor.

Test Constraints

Some constraints are imposed on the in-circuit test before the analysis of failure mechanisms is done. The junction temperature of an IC should never be allowed to exceed the manufacturer's specified maximum. Prior to a test, the junction will always be at some temperature above ambient. A typical maximum ambient rating is 75 degrees C. If the corresponding maximum junction temperature rating is 125 degrees C, and both specifications are to be met, then the junction must be less than 50 degrees C above ambient. For a test environment ambient of 25 degrees C, the junction would be less than 75 degrees C, and a 50 degrees C rise is allowed before exceeding the manufacturer's specification of 125 degrees C. Therefore, the temperature rise of the junction should be restricted to 50 degrees C or less during an in-circuit test.

CMOS "latchup" is a self destructive property of CMOS logic. The damage is caused by the formation of a parasitic SCR. Once the parasitic SCR has turned on, it conducts large amounts of current from Vdd to Vss which causes large power dissipation which in turn destroys the device. Vdd and Vss are voltages on the supply rails (i.e., the connections to the power supplies). Once the parasitic SCR has turned on, it will remain on until power is removed from the device or the device fails. Referring to Figure 3, it can be seen that the SCR is formed by the positive feedback of an NPN-PNP series transistor pair Q1-Q2. Figure 4

shows that Q1 is the vertical NPN transistor formed by the N+ Source (emitter), the P-Tub (base) and the N-Sub (collector). Q2 is the lateral PNP transistor formed by the P+ Source (emitter), the N-Sub (base) and the P-Tub (collector). R-Sub is the spreading resistance encountered by a current in the N-Sub material from a carrier source to a N+ contact. R-Tub is the spreading resistance encountered by a current in the P-Tub from a carrier source to a P+ contact. With either the transistor Q1 or Q2 turned on, the circuit will have positive feedback as long as the beta of the vertical transistor times the beta of the horizontal transistor is greater than unity. Note that a small current through R-Sub or R-Tub can start the positive feedback process.

CMOS "latchup" may be caused during in-circuit tests by allowing a voltage, which exceeds either supply rail of the device by one diode junction potential, to be applied to the output of the upstream device or to the input of the device under test. Such voltages are caused by the driver of the test apparatus under certain conditions. Figure 5 shows a driver which is connected to the device under test through wire of various lengths. This wire has inductance. Capacitance is present between the wires connecting the driver to the device under test. Figure 6 illustrates that when the driver applies a low or a high signal, this inductance and capacitance can cause overshoot. If this overshoot exceeds the diode junction potential, then current will be injected into the substrate or tub causing current which will lead to CMOS "latchup".

A constraint imposed on in-circuit testing is the restriction of bondwire temperature rise. The constraint on bondwire rise is to restrict the absolute temperature to less than 40% of the lowest melting point of the various bondwire materials. Bondwires are made from one of two materials; aluminium or gold. Because of material inter-actions between aluminium wire and plastic encapsulants, gold wire is always used in plastic packages. Aluminium or gold wire may appear in ceramic packages, but aluminium yields the worst case thermal analysis especially in ceramic packages. The melting point for gold is 1060 degrees C, and the melting point of aluminium is 660 degrees C. So, the bondwire temperature should be restricted to a maximum of 264 degrees C, or about a 230 to 240 degrees C rise. By restricting the temperature rise to 200 degrees C, or less, the amount of wire flexure during testing is kept to a minimum, and the wire is never in danger of melting.

Bond wire fusing is caused by excessive heating of the bond wires. It can occur on a device upstream from the device under test. Figure 7 is a schematic of the output stage of a standard TTL device as shown in Figure 8. This device represents an output stage of a device upstream from a device under test. If the device is attempting to apply a "false" or logic level 0 to the device under test, and the driver is attempting to apply a "true" or logic level 1 to the device under test, there will be a large current drawn through the lower transistor of the output driver. This is a highly likely occurrence during portions of an in-circuit test sequence. There may be a multiplicity of devices upstream from the device under test. If several of these devices are located in the same package, then the high currents through this package may cause damage. While the currents through the output bond wire will usually be in a safe region because only one overdrive current flows through such wire, currents through the Vcc and Vdd supply lines are additive and if more than one output of the same package is overdriven in the same direction, then the current through these supply lines will add. The large amount of current flowing through the supply bond wire will cause resistive heating, and if this occurs for long enough, the bond wire will melt similarly to a fuse. Once this occurs the device is ruined.

Devices may also be damaged through die heating. Die heating is caused in the upstream device by a process which is similar to bond wire fusing. Referring again to Figure 7, the lower transistor in the totem pole is turned on attempting to sink current from the output until the output approximately equals the supply voltage. The transistor is normally driven into saturation and the voltage drop across the transistor is small. After the current has been switched, the current through the device is low, so that the power dissipated in the transistor is low. However, when the device is being overdriven, the transistor is brought out of saturation and into the active region where the voltage across the transistor instead of being small is approximately equal to the difference between the output and supply rail. As stated above the current through the transistor is also high, thereby resulting in a large power dissipation. The ability to handle this power dissipation depends on several factors. Firstly, how many outputs in the package that are connected to the device under test are being overdriven. Secondly, what type of package (for example, ceramic or plastics) is the device held in, and thirdly, how the chip is attached to the package. The type of package and the method of attachment are often combined into a factor known as the thermal resistance. These factors are known as safeguard parameters. If the device is permitted to heat up to too high a temperature, then the output transistor will be damaged. This damage may appear immediately as a bad device at the time of test or it may appear later as a significantly reduced operational lifetime of that device.

Lifetime Degradation

If the constraints on bondwire and junction temperature rise are met during an in-circuit test, estimates of consumed lifetime can be empirically derived. Increasing the stress on a part as a result of current, temperature or voltage, usually results in exponentially increased degradation. This relationship is expressed for temperature accelerated failure mechanisms by the Arrhenius model, and similar models are available for current and voltage accelerated failures mechanisms.

The lifetime degradation of a part during in-circuit testing is expressed in equivalent normal lifetime consumed by operating the device at stressed levels. For example, a 1 msec in-circuit test (under the above constraints) will contribute to no more than 185 msec of device lifetime consumption as a result of electromigration failure acceleration. Table III shows the result for the other failure mechanisms under consideration.

TABLE III

Failure Mechanism	Comments
Second Breakdown	Triggering temperature is well above maximum temperature experienced during properly designed in-circuit test.
Electromigration	A 1ms test will contribute to no more than 185ms of normal operation.
Corrosion	A 1ms test will contribute to no more than 25.8 ms of normal operation
Interaction With Other Materials	Reaction rate is insignificant under in-circuit test conditions.
Intermetallic Growth	A 1ms test will contribute to no more than 296ms of normal operation.
Surface Reconstruction	An in-circuit test will not cause sufficient thermal cycling for the onset of this failure mechanism.

TABLE III (contd.)

Dielectric Breakdown	A 1ms test, under appropriate voltage level constraints, will contribute to no more than 9 ms of device lifetime.
Surface Charge Accumulation	A 1ms in-circuit test will contribute to no more than 1500ms of device lifetime in MOS devices and 226 ms of lifetime in bipolar devices.
Charge Injection	Not significant during in-circuit test, under normal conditions.
Thermal Fatigue	Not a problem if temperature rise is restricted. Potential for failure varies with bondwire and package material.
CMOS Latchup	An appropriately designed in-circuit test will not cause CMOS latchup.
Source - Drain Punchthrough	In-circuit test voltages are not of sufficient magnitude to cause this failure.
SiO_2	In-circuit test voltages are not of sufficient magnitude to cause this failure.

When the effects of all the failure mechanisms are considered together, a 1 msec test will contribute to no more than 750 msec of normal device lifetime for bipolar devices, and no more than 2000 msec of lifetime for MOS devices.

Catastrophic Damage

Bondwire failure or junction failure due to temperature rise, and CMOS device latchup due to degraded test signals are the catastrophic failures most likely to occur during in-circuit testing. The potential for damage from temperature related failures is minimized by adhering to the temperature rise constraints discussed earlier. If these constraints are exceeded by a test then the risk of device damage increases dramatically.

It is unnecessary to discuss in detail the variety of ways in which signal quality can be maintained on an in-circuit test system. However, there are three items which must be considered -- overdrive levels, signal rise times, and fixturing techniques. Overdrive levels should be high enough to maintain adequate noise margins, yet also maintain a margin between the peak signal voltage and the power supply voltage. By slowing signal rise times somewhat, less overshoot will occur at the device being tested. However, fast rise

times must be available when testing logic like Schottky. Finally there is a variety of fixturing techniques which can minimize signal degradation. These include: impedance matching, sufficient ground returns, drive and ground placement, and fixturing materials.

In order to detect when a test might potentially damage overdriven parts as a result of temperature rise, it is necessary to perform a thermal analysis on the device being overdriven. The thermal analysis predicts the temperature rise during the test. If this rise is greater than the constraining safe rise, derived above, then the potential for damage exists and the programmer should be notified.

According to the present invention there is provided a method of testing circuits of the type in which test signals are applied to a circuit under test, the circuit including individual semiconductor components, and output signals from the circuit under test are monitored, the method being characterized by the step of inserting during the test cool down intervals having minimal durations sufficient to avoid damage to the circuit due to overheating of the semiconductor components of the circuit, the durations being calculated using the junction and bondwire thermal characteristics of the components.

The present invention further provides a circuit tester for testing a circuit including individual semiconductor components, the tester comprising: means for applying test signals to nodes of the circuit under test; means for monitoring signals on the nodes of the circuit under test; characterized by means for inserting cool down intervals into circuit tests; data files containing information of circuit topology and information of junction and bondwire thermal characteristics of circuit semiconductor components; a damage analyzer responsive to the circuit topology information and junction and bondwire thermal information in the data files for calculating minimal length cool down intervals sufficient to prevent overheating damage to the semiconductor components; and a controller responsive to signals from the damage analyzer to control the length of each cool down interval.

The invention represents an improved method of pattern application which permits increased throughput while decreasing the risk of damage to the device under test and to the devices upstream from the device under test.

A method according to the invention can reduce the overshoot or undershoot on inputs or outputs of a CMOS device without reducing drive voltage. It also facilitates the identifying of which test will potentially damage devices and can prevent those tests from being executed.

A method according to the invention can also provide for selecting an inter-test delay necessary to protect the device from damage while increasing throughput, and can prevent damage caused by homing a device which fails to home.

There now follows a detailed description which is to be read with reference to Figures 9 to 17 of the accompanying drawings of a circuit tester and a method of testing according to the invention; it is to be clearly understood that this circuit tester and method of testing has been selected for description to illustrate the invention by way of example and not by way of limitation.

In the accompanying drawings:-

Figure 9 is a block diagram of a preferred test system apparatus operating in accordance with the method of the invention;

Figure 10A is a block diagram of a driver module which reduces the overshoot and undershoot;

Figure 10B is a table indicating the operative relationship between the current sources of the drive module shown in Figure 10A;

Figure 11 is a simplified model of a lumped RC transmission line providing a thermal model of an integrated circuit;

Figure 12 is a graph of the thermal response of a typical integrated circuit;

Figure 13 is a further simplified model of an IC; and

Figures 14 - 17 illustrate further models.

An automatic method for determining the potential for damage due to in-circuit testing can be developed using simple thermal models for the IC junction and bondwire. Device data, such as thermal resistance, overdrive current, overdrive voltage and package type are required for the analysis and can be supplied by the test programmer. Test data, such as actual test duration and number of outputs potentially overdriven simultaneously are derived from a library of tests for digital devices.

The actual test duration is calculated knowing the maximum number of test steps which could be executed during the test, and the application rate of those test steps. Then, a constraint is calculated based on the lower time given by constraining the junction to a safe temperature rise (Equation 3), and constraining the bondwire to a safe temperature rise (Equation 8). If the actual test time is greater than this temperature rise constraint, then the potential for damage exists and the test system programmer should be notified.

The actual temperature rise of the junction and bondwire can be calculated by knowing the actual

duration of the test using Equations 1 and 10. A cool down requirement can then be calculated as the longer of the cool down constraints based on junction cooling (Equation 5) and bondwire cooling (Equation 11). Because of the nature of these equations, they allow pre-cooling of the over-driven parts prior to the test. As a result, no calculations are performed at execution time, and the safe execution of the tests remains order independent.

In addition to evaluating each test automatically for potential damage, an in-circuit tester can also minimize the potential for damage by intelligently selecting fixture interface points, optimal overdrive voltages and optimum edge speeds.

If the safe constraints for voltage overshoot and undershoot, junction temperature rise and bondwire temperature rise are met, then a 1 msec in-circuit test will contribute to no more than 2 seconds of normal device lifetime. However, if any of these constraints are violated, the potential for damage and the amount of lifetime degradation increases dramatically.

It is convenient to model thermal problems as electrical problems using the following analogies:

Thermal resistance	=	Electrical resistance
Thermal capacity	=	Electrical capacitance
Temperature rise	=	Voltage
Heat flow	=	Current

The most accurate thermal model of an integrated circuit would be a lumped RC transmission line. A simplification of this complex model can be represented by Figure 11. This model of Figure 11 adequately predicts the 'three-humped' curve, (Figure 12), often shown in research on thermal response of ICs. However, most of the values required for the model of Figure 11 are not generally specified by manufacturers.

The model of Figure 11 can be simplified further. With respect to other values in the thermal model, the junction thermal capacity (Cj) can be neglected. This thermal capacity is device specific, but for a junction .0762mm square by .0041mm thick is about 5×10^{-8} J/°C, and the thermal time constant is typically about 10×10^{-6} seconds (see - D.W. Raymond and J.S. Smith, "IC Response to Transient Current Overloads", from a paper presented at the Advanced Techniques and Failure Analysis Symposium (ATFA), Sept., 1977 and Louis J. Sobotka, "The Effects of Backdriving Digital Integrated Circuits During In-circuit Testing", Proceedings of IEEE International Test Conference, 1982, p.270.).

The package thermal capacity (Cc) can be modelled as a short circuit for pulses of short duration. Experimental evidence indicates that the thermal time constant for the package is 10 seconds or more. If the pulse duration is significantly less than 10 seconds then Cc is essentially a short circuit.

If package heating is ignored for a single pulse, and the junction thermal capacity is neglected then the thermal model becomes that shown by Figure 13. Since the values of Rjd and Rdc cannot be determined explicitly, it is desirable to derive a proportional relationship of the two which gives the worst case thermal transfer model. A worst case model would describe the fastest way the junction could heat, and the slowest way it could cool.

Consider the case when the switch in Figure 13 is closed and the voltage at node 1 (temperature at the junction) begins to rise. The fastest rise occurs when Rjd is small and Rdc is large. When the switch is opened, the slowest discharge also occurs when Rjd is small and Rdc is large. A worst case model exists if all of Rjc (Rjd + Rdc) is lumped into Rdc and Rjd is assumed to be zero. This yields the model shown in Figure 14.

The model of Figure 14 can be used to describe the behavior of a single output being overdriven assuming the package acts as a heat sink at a constant temperature during the overdrive period.

Figure 15 shows a model of multiple output junctions being overdriven simultaneously. If there is no package heating, the model can, again, be simplified to that shown in Figure 13 where the source is equal to the sum of the power being generated in each junction, and the junction-to-die * thermal resistance is Rjd/n, where n is the number of outputs being overdriven simultaneously. If this model is simplified to that shown in Figure 14 it yields a conservative model for heat flow with multiple outputs overdriven. Since Rjd/n + Rdc (which is lumped into Rjc in the model) will always be less than the actual value of Rjc, the model is conservative. Future die shrinkages or technologies which put junctions closer together will be adequately covered by this model.

* silicon substrate.

Junction Temperature

Classical electrical equations can be used to describe both the heating and cooling of the junction based on the model of Figure 14. Equation 1 can be used to calculate the junction temperature rise after time t.

$$Trise = P*Np*Rjc*(1-e^{(-t/(Rjc*Cd))}) \quad \text{(Eq. 1)}$$

Where:

- Trise = temperature rise at time t.
- P = overdrive power per output overdriven.
- Np = number of outputs overdriven.
- Rjc = thermal resistance junction to-die.
- Cd = thermal capacity of the die.

Note:

- P*Np*Rjc = steady state temperature (maximum temperature rise).
- Rjc*Cd = thermal time constant.

The thermal capacity of the die is not a readily available parameter, but a reasonable value can be calculated from Equation 2 assuming a worst case die size, and knowing the heat capacity and density of silicon.

$$Cd = Volume * Heat\ Capacity * Density \quad \text{(Eq. 2)}$$

Equation 1 can be solved for time, and can then be used to predict the amount of time a test can last before rising the junction temperature by some given amount, Trise. This relationship is shown in Equation 3.

$$t = Rjc*Cd*\ln(1-Trise/(P*Np*Rjc)) \quad \text{(Eq. 3)}$$

Equation 3 can be used to predict the maximum test duration allowed to prevent heating a junction more than a predefined temperature rise, for a single test. But if the tester is looping on a test or for some other reason repetitively overdriving a device, heat can build up cumulatively. Even if a single test does not cause a temperature rise sufficient to violate the junction rise constraint, if the junc tion is not allowed to cool between tests, its temperature will eventually exceed the maximum specified by manufacturers.

The equation for the decay of the simple RC circuit shown in Figure 14 is:

$$Tcool = To * e^{(-t/(Rjc*Cd))} \quad \text{(Eq. 4)}$$

Where =

- Tcool = the temperature after time t.
- To = the initial temperature.

The value of To could be obtained by adding the result of Equation 1 (using the actual test time for t) to the pre-test temperature of the junction. Equation 4 could then be solved for time and the required time to cool to some acceptable temperature could be calculated. But this temperature must then be stored and used as the pre-test initial temperature in future heat and cool calculations. This requires that a considerable amount of data about the initial conditions of each part being overdriven are calculated and stored in real time.

A better way to calculate cool down constraints is to assume the device is at its maximum allowed temperature rise before the test. The cool down time is then enforced prior to the test such that the junction is brought down to a temperature where the rise from the test will not allow the junction to exceed the maximum allowed temperature.

This makes the execution of the tests order independent and no initial temperatures need be calculated or stored. Required cool-down times can be precalculated before testing ever begins.

Equation 4 can be solved for time and the maximum allowed temperature substituted for To. Tcool becomes the actual temperature rise from the test calculated from Equation 1 using the actual test time for t. The actual test time (t) is calculated knowing the maximum number of test steps in the test and the test

step application rate.

$t = -Rjc*Cd*\ln((Tmax - Tactual)/Tmax)$ (Eq. 5)

The above equations ignore the effects of package heating. If a device is repetitively overdriven, package heating can become significant. Experiments have shown that for up to 100 repetitive tests, the package will heat about 15 degrees C. If the maximum allowed temperature rise is decreased by 15 degrees C, then the above equations for junction heating and cooling will adequately predict maximum test duration and required cooling times for up to 100 repetitive tests. If more than 100 repetitions of a test are performed then an extended cool down should be inserted to keep the package from rising by more than 15 degrees C.

Bondwire Temperature

The two major types of wire-bonding material in use today are aluminium (usually alloyed with about 1% silicon) and gold. There are also two major package types in use --plastic and ceramic. Due to material interactions between aluminium and plastic encapsulants, gold bondwires are always used in plastic packages. Either gold or aluminium are used in ceramic packages but aluminium provides the worst case thermal analysis. Because the two packaging techniques have dramatically different thermal behavior, each type of package must be analyzed separately.

The gold bondwire in a plastic encapsulated package has two modes of heat transfer -- radial conduction to the plastic encapsulant and axial conduction along the wire to the die and lead frame. If the die, lead frame and package are modelled as heat sinks at constant temperature, a simple heat transfer model can be constructed. Again, an electrical analogy can be used where heat flow is modelled by current, thermal resistance by a resistor, thermal capacity by a capacitor, and temperature rise by voltage. The heat transfer model is shown in Figure 16. Radial conduction is modelled with Rr and axial conduction is modelled with Ra. Cw represents the thermal capacity of the wire. The current source represents the internal heat generation in the wire due to Joule heating.

The equation for temperature rise for a gold bondwire in a plastic package is given by:

$T = Req*Q*(1-e^{(-t/(Req*Cw))})$ (Eq. 6)

Where :

- T = temperature rise of wire.
- Cw = thermal capacity of wire.
- Req = equivalent resistance of Rr in parallel with Ra.
- Q = internal heat generation given by:

$Q = I^2 * Rw$ (Eq. 7)

Where :

- I = the current through the wire.
- Rw = the resistance of the wire.

Rw will vary with temperature, so Equation 6 must be solved iteratively. Values for Ra and Rr can be derived, (see pages 31-33, 63-67 of J.P. Holman, Heat Transfer, 4th Edition, 1976, McGraw-Hill, Inc., New York).

Solving Equation 6 for time yields Equation 8. This equation predicts the maximum test duration allowed to restrict the temperature rise in the bondwire to T degrees Celsius. The equation is invalid for overdrive current which cause the value of [1-t/(Teq*Q)] to be less than zero. Such currents are below the steady state current carrying capability of the wire.

$t = -Req*Cw*\ln(1-T/(Req*Q))$ (Eq. 8)

The aluminium bondwire in a ceramic package has three modes of heat transfer. Heat can be transferred by radial free convection to the air in the package, axial conduction along the wire to the die and lead frame, and radial radiation into the package. If the package, lead frame and die are modelled as infinite

heat sinks and air is assumed to remain at constant temperature, the heat transfer can be modelled as shown in Figure 17. Rrh represents the radial convection thermal resistance, Ra is axial conduction thermal resistance, and Rrad is radial radiation thermal resistance.

Equation 8 can also be used to determine the maximum test duration allowed to restrict the temperature rise to T, for aluminium bondwires in a ceramic package. Req is Rrh, Ra and Rrad in parallel, Cw is the thermal capacity of the bondwire. Values for Rrh, Ra and Rrad can be determined, (see pages 31-33. 237-240 and 342 of J.P. Holman, Heat Transfer referenced above).

Equations for bondwire cooling are derived in the same way as Equations 4 and 5. Steady state temperature (Tss) is given by:

$$Tss = Rw*Req*(I*Np)^2 \quad \text{(Eq. 9)}$$

The actual temperature rise in the wire as a result of the test is:

$$Tactual = Tss*(1-e^{(-ta/(Req*Cw))}) \quad \text{(Eq.10)}$$

And the cool down time required prior to the test is given by Equation 11:

$$t = -Req*Cw*\ln((Tmax - Tactual)/Tmax) \quad \text{(Eq. 11)}$$

Figure 9 shows part of the improved circuit tester according to the present invention. The process of applying the patterns begins with three input files 91-93. File 91 contains a topological description of the board under test, file 92 contains a set of safeguard parameters for each of the devices on the board under test, and file 93 contains a set of pre-generated generic patterns for each of the devices under test. These files are then analyzed by a topological analyzer 94. This analyzer, among other things, sorts through the generic patterns and selects patterns which are suitable for testing the device and selects the driver module to be used with this device. These patterns, along with the topological and safeguard data are passed on to a damage analyzer 95.

The damage analyzer 95 is responsible for, among other things, the calculation of the time interval that the test will require, a determination of whether the test may possibly damage upstream components, and calculation of the required variable inter-test delay times. This data, along with the safeguard parameters, is passed to a test controller 96.

The controller 96 applies the patterns to a device 98 under test through a driver module 97, receives the response of the device 98 through a sensor module 99 and compares this response to an expected response. The controller inserts the variable inter-test delays in order to protect devices upstream from damage.

The driver module 97 must be capable of overdriving the output of the upstream device. However, the driver 97 must be capable of controlling overshoot in order to prevent CMOS "latchup".

In order to overdrive devices without causing damage through bond wire fusing or die overheating, the application of patterns must be analyzed in two steps. Firstly, the test must not be so long as to cause overheating or damage. Secondly, the tests of two devices, one after the other, must not be so close in time as to cause the damage. In order to prevent the first type of damage, a maximum allowable test duration is determined. If the length of the test exceeds the maximum allowable test duration, then the test is flagged not to be executed. To determine the maximum allowable test duration, the damage analyzer 95 examines the maximum test time for both bond wire fusing and die overheating. In order to prevent the second damage phenomenon, the minimum allowable cooling delay is calculated by the damage analyzer 95 and used by the test controller 96 between tests to assure that no number of tests when combined will exceed the maximum allowable temperatures for the devices. Again the analysis is done for both bond wire fusing and die overheating types of damage.

The maximum overdrive duration due to bond wire overheating constraints is a function primarily of package material and the amount of overdrive current through the supply lines. This duration limit is calculated by the damage analyzer 95 for each supply pin of the upstream devices. Then the minimum of these duration times is used by the damage analyzer to determine the maximum test duration. The following formula is used to calculate the delay for each supply pin:

For ceramic packages:

max time = -0.00716 * ln(1- .3865/((Np*I)/Nw)**2)

For plastics packages:

max time = -0.00129 * ln(1- 2.825/((Np*I)/Nw)**2)

Where:

Np = The number of device outputs being overdriven and causing current to flow through this supply pin,

I = The amount of current caused by each overdriven output, and

Nw = The number of bond wires absorbing the overdrive current.

The preferred algorithm uses worst case analysis for Np and it estimates the Np for the upstream device to be the lesser of the number of outputs attached to the device under test inputs or the maximum number of outputs which could be functioning at a state requiring overdriving by the tester. The maximum number of outputs which could be functioning at a state requiring overdriving and the overdrive current per output for each bond wire are device dependent parameters which are provided by file 92.

The maximum overdrive duration is also constrained by die overheating considerations. This duration is a function of the thermal resistance of the package, the power being dissipated in the output transistor, and the number of overdriven outputs in the device. The maximum duration of such a test is calculated as follows:

max time = (-Rjc/2000)*ln(1-25/(Rjc*Pw*Np))

Where:

Rjc = The junction to case thermal resistance,

Pw = The power dissipated by each overdriven output, and

Np = The number of overdriven outputs on the device.

Again the preferred embodiment uses a worst case analysis. Np will be estimated for each upstream device as the number of its outputs attached to the device-under-test inputs. Rjc and Pw are both device dependent parameters supplied by the file 92. The maximum duration for a test is the minimum duration due to wire bond heating or due to die heating.

The device thermal analysis by the damage analyzer 95 keeps track of the effects of a sequence of device tests on each overdriven device's temperature. For each device test, each of the devices it overdrives will be analyzed in turn to calculate the longest cool down delay such that each of those overdriven devices can recover from the effects of the test.

The delay may be placed either before or after the test for which the delay was calculated. However, cooling before the test offers an advantage because only the heating caused by the next test to be performed is important. If cooling is done after performing the test, then either the cooling calculation must provide for cooling for the duration required for the worst case heating or else the heating caused by the next test must be known. Use of pre-cooling means that the device is allowed to cool for only as long as necessary for the next test to be performed and reduces the amount of calculations necessary to keep the temperature from exceeding a certain value selected to protect the circuit. The maximum temperature permitted by the preferred embodiment for any device is 40 degrees Celsius above ambient and this assumption is reflected in the calculations below.

Two different types of cool down delays are used. The first type of cool down delay is calculated on the assumption that a test on a component has not been continuously repeated in a test program loop more than a hundred times. Furthermore, these delays are calculated assuming that die cooling, under either the first or second delay calculation, will exceed the time necessary for bond wire cooling. It is calculated using the following formula:

Temp rise = Pw * Rjc * Np * (I-e**(-2000*Ton/Rjc))

normal delay = -(Rjc/2000)*ln(I-Temp rise/40)

Where:

Pw = The instantaneous power absorbed by one device output pin being overdriven,

Np = The number of pins on the device being overdriven, and

Rjc = The case/junction thermal resistance for the package class.

Ton = The time duration of pattern application.

Pw and Rjc are package dependant. The parameter Ton will be calculated for each test as a function of the pattern cycle time.

The second type of cool down delay is used when a test is being continuously looped. This calculation ensures that the duty cycle will not cause the average power fed into the overdriven device to exceed its steady state capacity to dissipate power. In either case minimum delay is the tester overhead and the maximum delay is five times the package time constant. The steady state delay is calculated as follows:

steady state delay = Ton * (Pw*Np*(Rjc + 100)/15 -1).

Ceramic packages provide less heat dissipation for bond wires, because the bond wires are not encapsulated. For this reason the cooling time constant for ceramic packages is slow enough that bond wire cooling delay will override both the normal and steady state delays, based on die heating, discussed above. The bond wire cooling delay is never allowed to exceed 5 times the cooling time constant for ceramic packages. Again, the analysis assumes that the bond wire temperature is the maximum allowed. If the current test will cause a rise in excess of 200 degrees Celcius, the maximum time constant will be used. Otherwise the following formula will be used:

Bond Temp = 517.5 * (I*Np)**2 * (1-e**(-Ton/ .00716))

Bond Cool = -.00716 * ln(1-Bond Temp/200)

The delay calculated is in seconds.

In order to prevent damage during homing of a device having a fault which prevents it from going into a known state, the homing capability in the controller 96 includes a maximum loop count. If the device never meets the exit conditions specified in the homing loop, the homing loop will execute once more after the loop count is exhausted. From the exact number of homing loops it is possible to compute the exact time of the homing sequence. Note that this is different from fail safe timing which shuts down the hardware after a long time has gone by. The fail safe time must be set for the maximum total test time otherwise it might shut a good test off prematurely. The preferred method of homing is superior since the homing time is separate from the fail safe time and need only be as long as necessary to home the device.

In order to use the variable delays which were calculated above, the test controller must be capable of measuring the time since the last pattern is applied. These timers are activated at the end of the last test and the cool down period must pass before the next device test is started.

Figure 10A shows a driver circuit 110 utilized in the driver module 97. The driver module 97 consists of a multiplicity of identical driver circuits 110 which are assigned by the topological analyzer 94 to inputs of a device 98 under test. These circuits are responsible for converting the internal true, false and third state signals of a test sequence in the test controller 96 to the physical voltage signals which are understood by the device under test. The driver circuit 110 also is capable of controlling the slope of the voltage signal through the use of a pair of variable current drive sources 120 and 124 under the control of the controller 96 and a slope controller 119.

The driver circuit 110 utilizes a transistor 111 connected in series with a transistor 112. The emitter 113 of the transistor 111 is connected at a node 114 to the emitter 115 of the transistor 112. The collector 116 of the transistor 111 is connected to a source 127 of voltage V_{pulse} high and the collector 117 of the transistor 112 is connected to a voltage source 128 of voltage $V_{pulse\ low}$. The driver output 118 is connected to the node 114 to provide the driver output signals.

To prevent CMOS latchup, the slope of the driver output signals is limited as stated above by use of the slope controller 119 and a variable current source 120 which are connected to the base 122 of the transistor 111. The slope control is also effected by use of the slope controller 119 with the variable current source 124 which are connected to the gate 126 of the transistor 112. When the controller 96 changes the current supplied by the source 120, the rate of change of the voltage applied to the base 122 is limited by the slope controller 119. In the preferred embodiment, the slope controller 119 is a capacitor of sufficient size to limit the slope of the driver output signal sufficiently to avoid CMOS latch-up. Similarly, the combination of the slope controller 119 and the variable current source 124 produces a signal of limited slope to base 126. The output state of each driver is determined by the current from the sources 120 and 124. Figure 10B shows the correspondence between driver output signal states DRIVE HIGH, DRIVE LOW and THIRD STATE and the current sources 120 and 124.

When a third state driver output is desired, both current sources are off. When the controller desires to produce a high driver output it activates the current source 120 to its selected level. This causes current from the variable current source 120 to flow to the transistor 111 and the slope controller 119. As the slope control component begins to charge up, the transistor 111 turns on and the driver output 118 follows the voltage on the slope control 119. The driver output voltage is approximately equal to the reference voltage PULSE HIGH. The slope steepness is controlled by the amount of current, and the choice of the slope controller. When the controller 96 desires a low driver output, it activates the current source 124 to the selected level after turning the current source 120 off. This turns off the top transistor 111 and turns on the bottom transistor 112 which connects the DRIVER OUTPUT at the low driver potential thereby applying a low or false state. In the preferred embodiment the variable current sources are controlled to provide either no current or one of two non-zero currents. The larger of these two non-zero currents results in a steeper

slope of driver output that can be used in testing TTL and other high current circuits. The smaller of these two non-zero currents results in a slower rate of change in the driver output signal appropriate in avoiding CMOS latch-up when a CMOS circuit is under test.

Claims

1. A method of testing circuits of the type in which test signals (96,97) are applied to a circuit under test (98), the circuit including individual semiconductor components, and output signals (99,96) from the circuit under test are monitored, the method being characterized by the step (92) of inserting during the test cool down intervals having minimal durations sufficient to avoid damage to the circuit due to overheating of the semiconductor components of the circuit, the durations being calculated using the junction and bondwire thermal characteristics of the components.

2. A method according to Claim 1 wherein each cool down interval is inserted into the test before that portion of the test for which its length was determined.

3. A circuit tester for testing a circuit including individual semiconductor components, the tester comprising: means (96,97) for applying test signals to nodes of the circuit under test (98); means (99,96) for monitoring signals on the nodes of the circuit under test; characterized by means (92) for inserting cool down intervals into circuit tests; data files (91) containing information of circuit topology and information of junction and bondwire thermal characteristics of circuit semiconductor components; a damage analyzer (95) responsive to the circuit topology information and junction and bondwire thermal information in the data files for calculating minimal length cool down intervals sufficient to prevent overheating damage to the semiconductor components; and a controller (96) responsive to signals from the damage analyzer to control the length of each cool down interval.

4. A circuit tester according to Claim 3 wherein the inserting means is operable to insert each cool down interval into the test before that portion of the test for which its length is determined.

5. A circuit tester according to Claims 3 or 4 wherein the slope of the test signals can be varied.

Revendications

1. Procédé pour tester des circuits, du type dans lequel des signaux de test (96, 97) sont appliqués à un circuit testé (98), le circuit contenant des composants semi-conducteurs individuels, et dans lequel des signaux de sortie (99, 96) du circuit testé sont surveillés, le procédé étant caractérisé par l'étape (92) consistant à intercaler, au cours du test, des intervalles de refroidissement ayant des durées minimales suffisantes pour éviter l'endommagement du circuit par échauffement excessif des composants semi-conducteurs du circuit, les durées étant calculées en utilisant les caractéristiques thermiques des jonctions et des fils de connexion des composants.

2. Procédé selon la revendication 1, dans lequel chaque intervalle de refroidissement est intercalé dans le test avant la partie du test pour laquelle la longueur de cet intervalle a été déterminée.

3. Testeur de circuits pour tester un circuit contenant des composants semi-conducteurs individuels, le testeur comprenant: un moyen (96, 97) pour appliquer des signaux de test à des noeuds du circuit testé (98), ainsi qu'un moyen (99, 96) Pour surveiller des signaux sur les noeuds du circuit testé, caractérisé par un moyen (92) pour intercaler des intervalles de refroidissement dans des tests de circuit; des fichiers de données (91) contenant de l'information relative à la topologie du circuit et de l'information relative aux caractéristiques thermiques de jonctions et de fils de connexion de composants semi-conducteurs du circuit; un analyseur de dommages (95) sensible à l'information relative à la topologie du circuit et à l'information thermique sur les jonctions et les fils de connexion dans les fichiers de données pour calculer des intervalles de refroidissement de longueur minimale suffisants pour empêcher l'endommagement des composants semi-conducteurs par suite d'un échauffement excessif; ainsi qu'un dispositif de commande (96) sensible à des signaux provenant de l'analyseur de dommages et servant à ajuster la longueur de chaque intervalle de refroidissement.

4. Testeur de circuits selon la revendication 3, dans lequel le moyen pour intercaler les intervalles de

refroidissement est conçu pour pouvoir intercaler chaque intervalle de refroidissement dans le test avant la partie du test pour laquelle est déterminée sa longueur.

5. Testeur de circuits selon la revendication 3 ou 4, dans lequel la pente des signaux de test peut être variée.

Patentansprüche

1. Verfahren zum Testen von Schaltkreisen, bei dem Testsignale (96,97) an einen im Test befindlichen Schaltkreis (98) angelegt werden, der Schaltkreis einzelne Halbleiter-Komponenten aufweist und Ausgangssignale (99,96) von dem im Test befindlichen Schaltkreis überwacht werden, **gekennzeichnet** durch den Verfahrensschritt (92), während des Tests Abkühlintervalle minimaler Dauer einzufügen, die ausreicht, Beschädigungen des Schaltkreises durch Überhitzen der Halbleiterbestandteile des Schaltkreises zu verhindern, wobei die Dauer unter Verwendung der thermischen Eigenschaften der Verbindungen und Bonddrähte der Komponenten berechnet wird.

2. Verfahren nach Anspruch 1, bei dem jedes Abkühlintervall in den Test vor demjenigen Teil des Testes eingefügt wird, für welchen die Länge des Abkühlintervalls bestimmt worden ist.

3. Schaltkreistestgerät zum Testen von Schaltkreisen mit einzelnen Halbleiterkomponenten mit: Vorrichtungen (96,97) zum Anlegen eines Testsignales an Knotenpunkte des im Test befindlichen Schaltkreises (98), Vorrichtungen (99,96) zum Überwachen der Signale an den Knotenpunkten des im Test befindlichen Schaltkreises, **gekennzeichnet** durch eine Vorrichtung (92) zum Einfügen von Abkühlintervallen in die Schaltkreistests, Dateien (91) mit Informationen über Schaltkreis-Topologie und über thermische Verbindungs- und Bonddraht-Eigenschaften der Halbleiter-Komponenten des Schaltkreises, einen Schadenanalysator (95), der abhängig von den Informationen über Schaltkreis-Topologie und thermisches Verhalten der Übergänge und Bonddrähte in den Dateien die kürzeste Dauer von Abkühlintervallen berechnet, die ausreicht, um Überhitzungsschäden an den Halbleiterkomponenten zu verhindern, und eine Steuereinrichtung (96), die abhängig von den Signalen des Schadenanalysators die Länge jedes Abkühlintervalles steuert.

4. Schaltkreistestgerät nach Anspruch 3, bei dem die Einfügevorrichtung jedes Abkühlintervall in den Test vor dem Teil des Testes, für welchen seine Länge bestimmt worden ist, einfügt.

5. Schaltkreistestgerät nach Anspruch 3 oder 4, bei dem der Verlauf der Testsignale veränderlich ist.

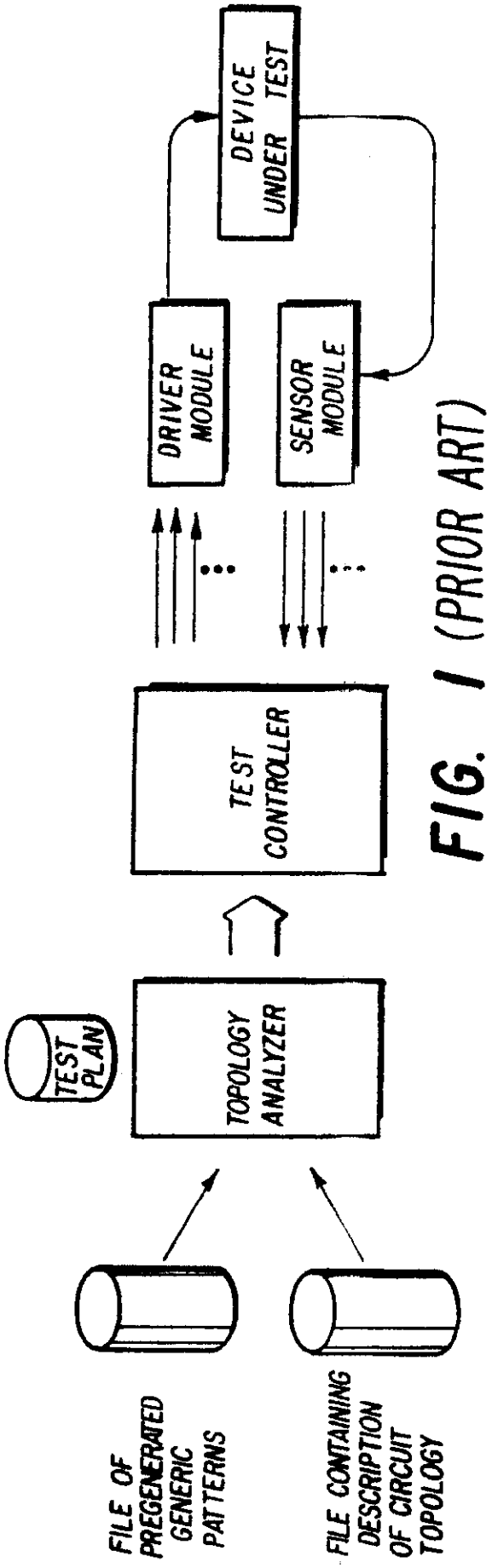


FIG. 1 (PRIOR ART)

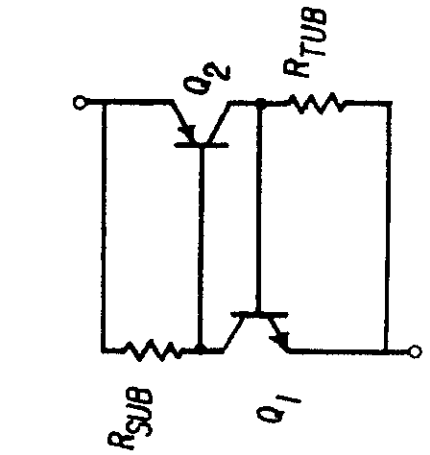


FIG. 3

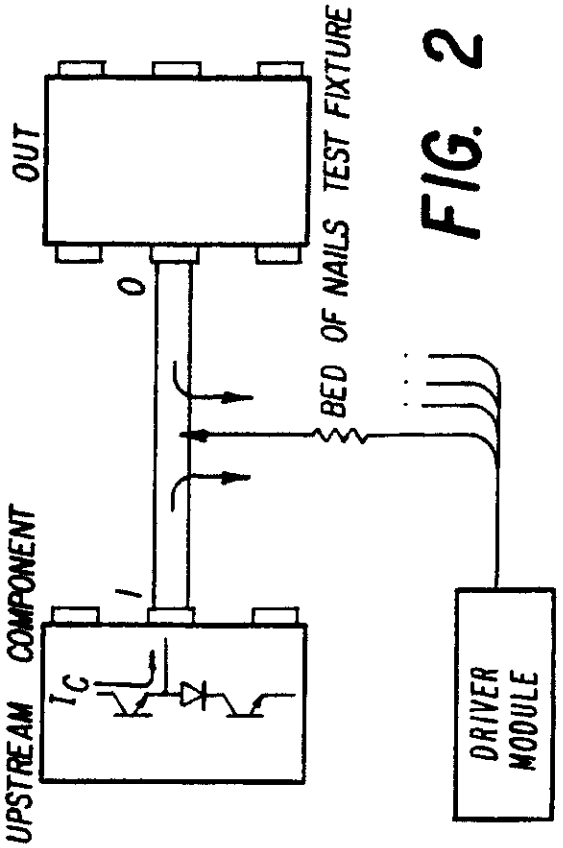


FIG. 2

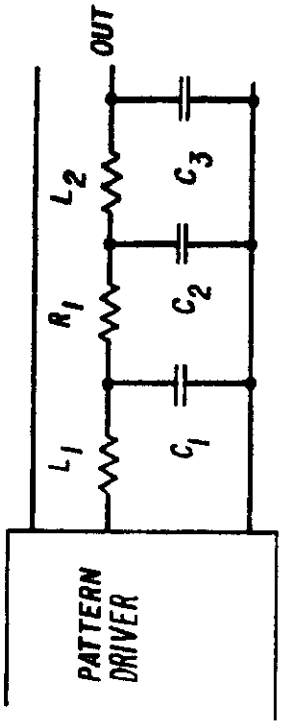


FIG. 5

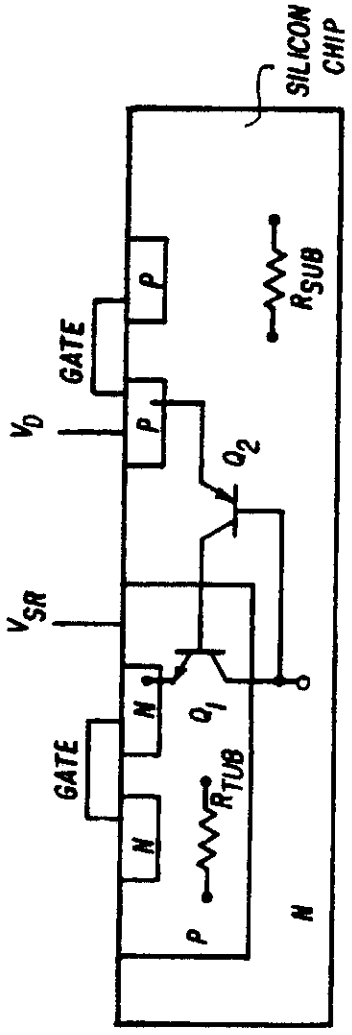


FIG. 4

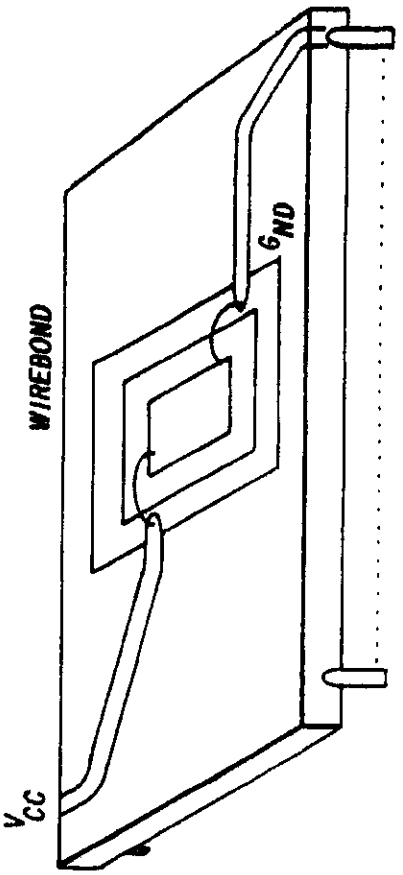


FIG. 8

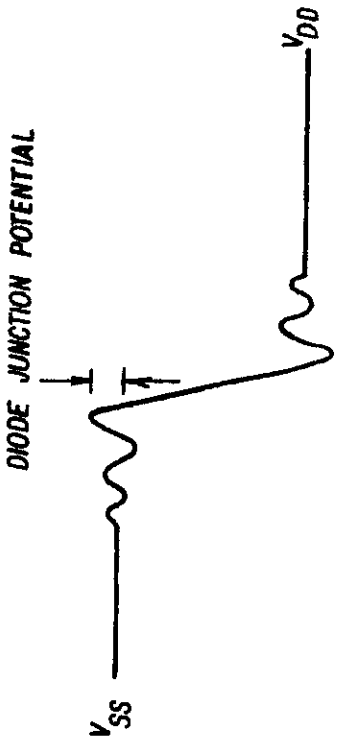


FIG. 6

FIG. 10A

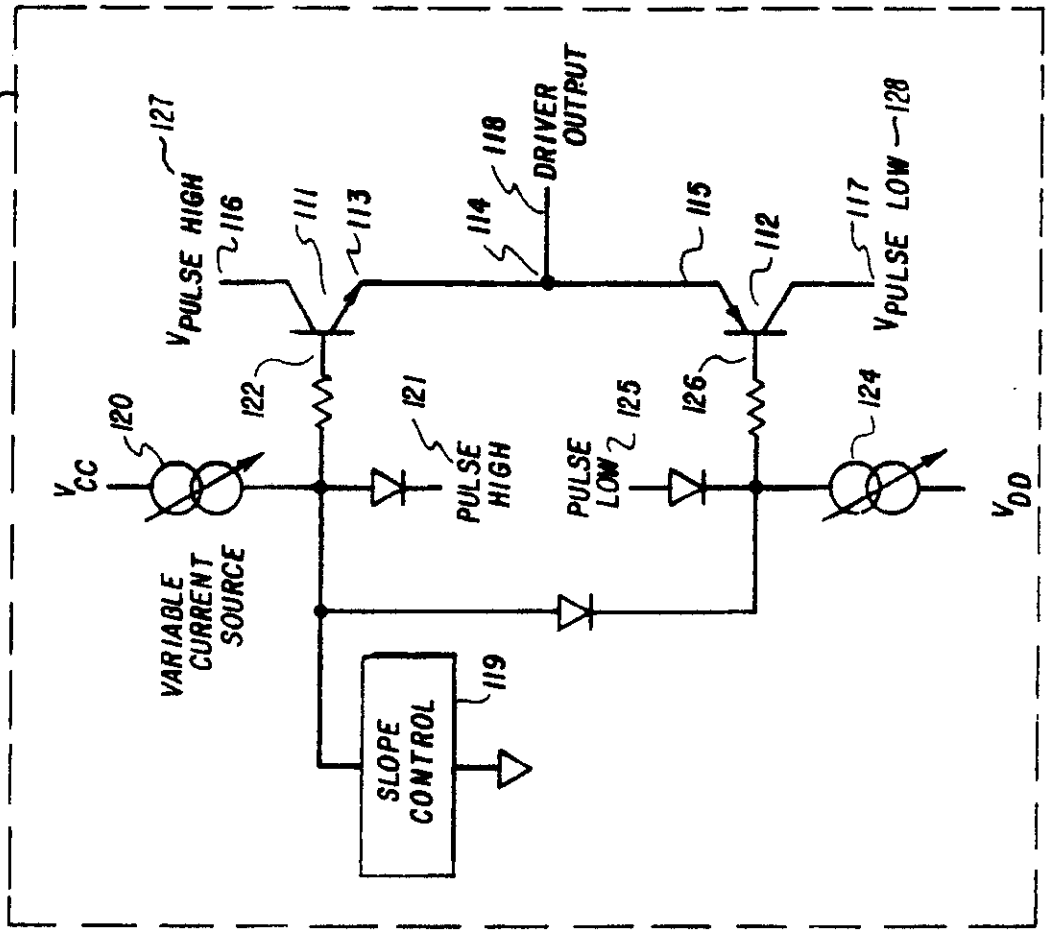
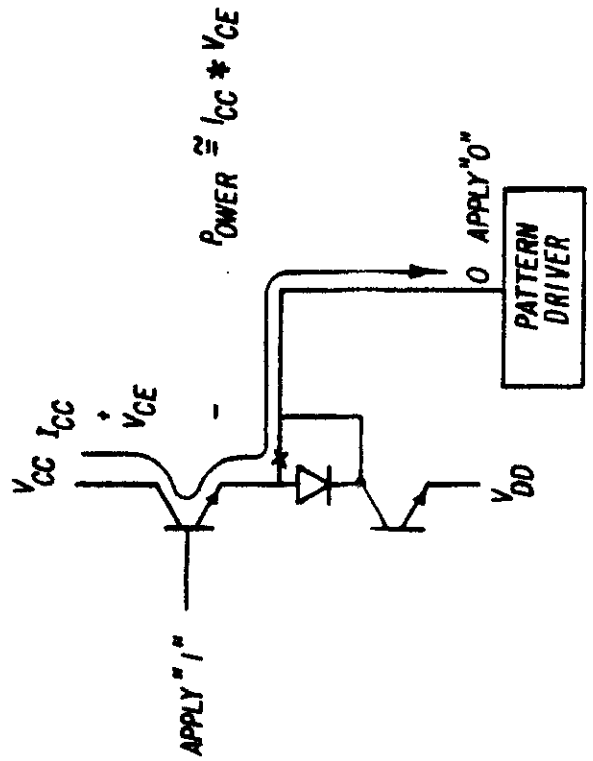

110
127
$V_{PULSE\ HIGH}$
116
111
113
114
118
DRIVER OUTPUT
115
112
117
$V_{PULSE\ LOW}$
128
120
V_{CC}
122
121
PULSE HIGH
PULSE LOW
125
126
124
V_{DD}
VARIABLE CURRENT SOURCE
SLOPE CONTROL
119

FIG. 7


$P_{OWER} \cong I_{CC} * V_{CE}$
V_{CC} I_{CC}
V_{CE}
APPLY "1"
APPLY "0"
PATTERN DRIVER
V_{DD}

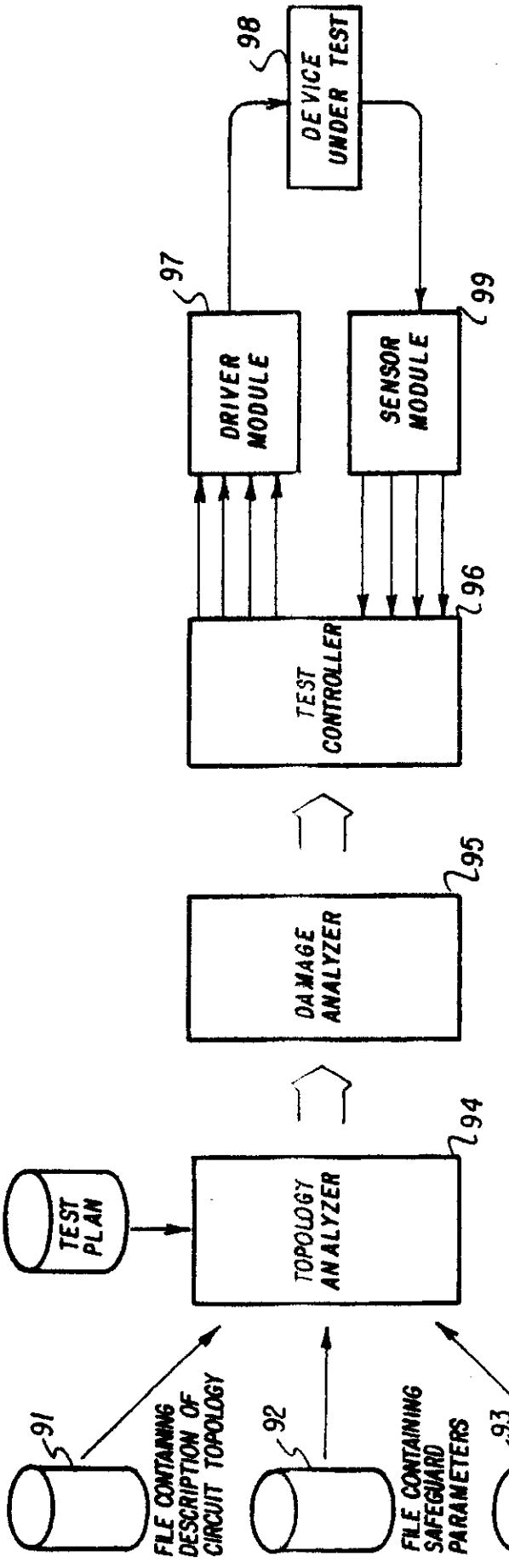
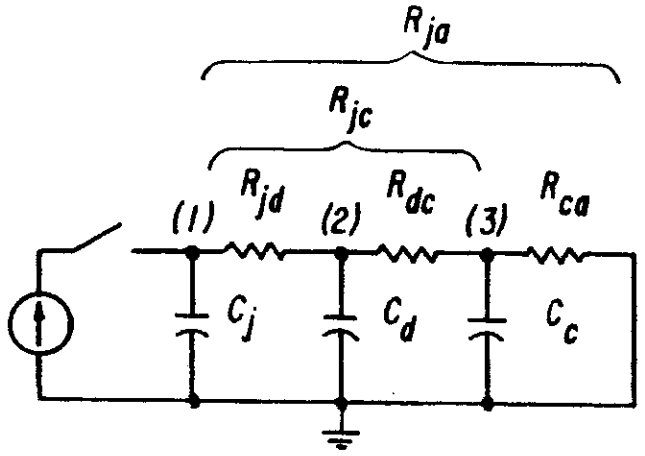


FIG. 9

		VARIABLE CURRENT SOURCE 120	VARIABLE CURRENT SOURCE 124
DRIVE	LOW	NO CURRENT	SELECTED CURRENT
DRIVE	HIGH	SELECTED CURRENT	NO CURRENT
THIRD	STATE	NO CURRENT	NO CURRENT

FIG. 10B



R_{jd} = THERMAL RESISTANCE, JUNCTION TO DIE
R_{dc} = THERMAL RESISTANCE, DIE TO CASE (PACKAGE)
R_{ca} = THERMAL RESISTANCE, CASE TO AMBIENT

C_j = THERMAL CAPACITY, JUNCTION
C_d = THERMAL CAPACITY, DIE
C_c = THERMAL CAPACITY, CASE (PACKAGE)

FIG. 11

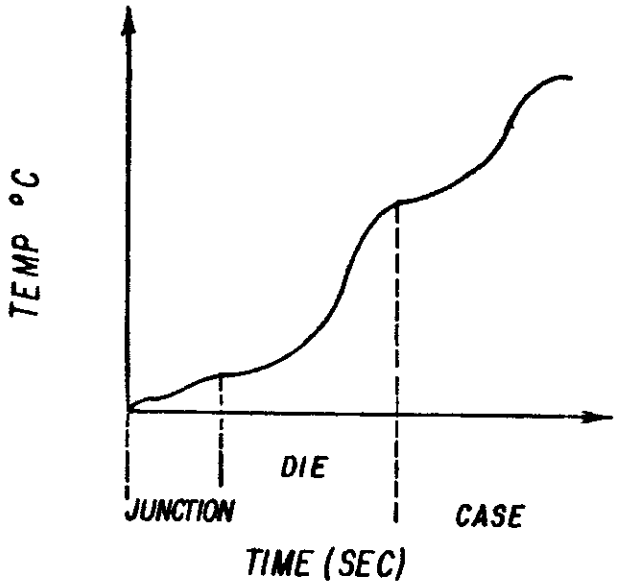


FIG. 12

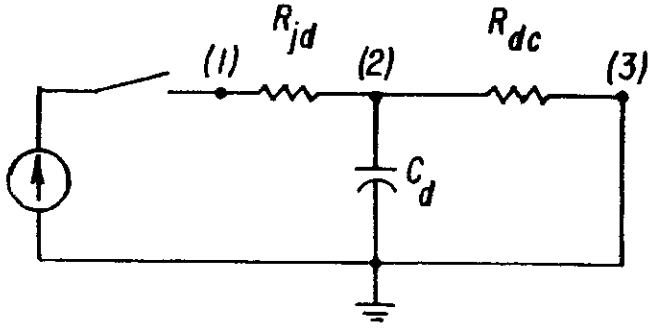


FIG. 13

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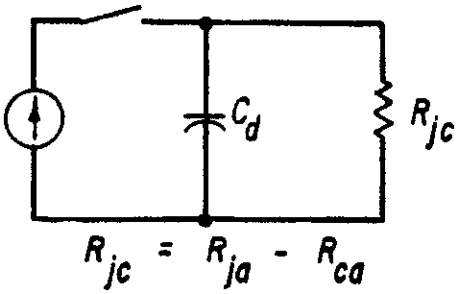

FIG. 14

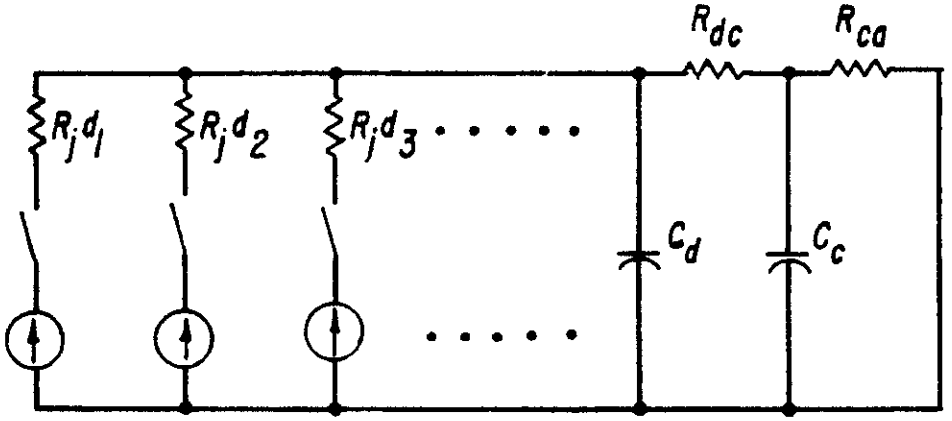

FIG. 15

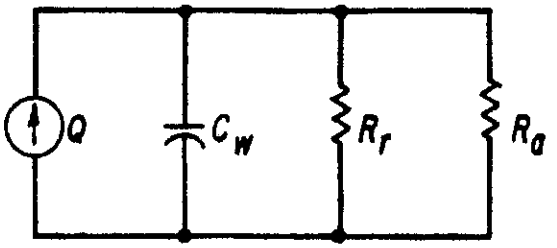

FIG. 16

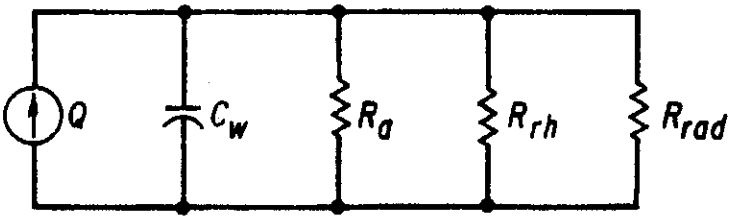

FIG. 17

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Title HIGH THROUGHPUT CIRCUIT TESTER AND TEST TECHNIQUE AVOIDING OVERDRIVING DAMAGE

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