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(54) **Title**: ELECTRONIC DEVICE AND APPARATUS AND METHOD FOR POWER MANAGEMENT OF AN ELECTRONIC DEVICE

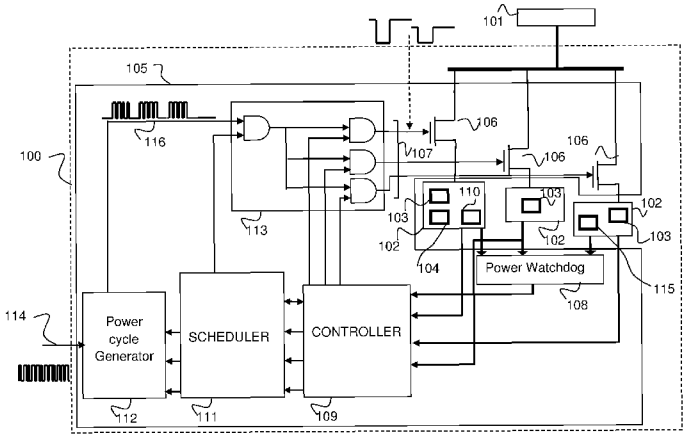

FIG. 1

(57) **Abstract**: An electronic device, typically a microcontroller 100, which is divided into a multiplicity of power domains 102 comprising one or more intelligent peripherals 103, is provided with an on-board power management module (105) for switching power to one or more domains for pre-determined time periods and in a predetermined sequence. The values of the predetermined time periods and sequence may be pre-programmed by the design engineer or user of the device 100. In one example, power is switched to domains in a round robin fashion. An optional interrupt capability permits selective application of power to a dormant intelligent peripheral requesting it at the expense of others and based on a priority scheme. Consumption of current supplied to power domains may be monitored by a power watchdog 108 or alternatively via a dedicated power monitor associated with each intelligent peripheral. The invention helps to reduce device power consumption without any associated reduction in processing performance.

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Title : Electronic device and apparatus and method for power management of an electronic device

Description

Field of the invention

This invention relates to an electronic device and to an apparatus and method for power management of an electronic device and has particular application, though not exclusive, to power scheduling for an electronic device such as a microprocessor or microcontroller and is particularly suitable for application to electronic devices which may be divided into power domains or islands.

Background of the invention

Power consumption in devices such as microcontrollers becomes an ever increasing problem with the reduction in size of semiconductor devices as smaller geometries tend to have larger leakage currents. Various techniques have been proposed for reducing the power consumption of microcontrollers and microprocessors. One specific power reduction technique involves stopping (or “gating”) the clock signals that drive inactive circuit portions. A similar technique involves the capability of reducing the frequency of clock signals that drive circuit portions during operating modes which are not time critical. US 6,826,704 describes a system which employs a performance throttling mechanism so that a reduced number of execution units are active at any one time. Another method, mentioned in US 7,941,682 puts currently inactive parts of a circuit into a sleep mode. Another technique which can reduce current leakage involves the removal (or “gating”) of power from inactive circuit portions.

Summary of the invention

The present invention provides an electronic device and an apparatus and a method for power management of an electronic device as described in the accompanying claims.

Specific embodiments of the invention are set forth in the dependent claims.

These and other aspects of the invention will be apparent from and elucidated with reference to the embodiments described hereinafter.

Brief description of the drawings

Further details, aspects and embodiments of the invention will be described, by way of example only, with reference to the drawings. In the drawings, like reference numbers are used to identify like or functionally similar elements. Elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale.

FIG. 1 is a simplified block diagram of an example of an electronic device comprising a power management capability; and

FIG. 2 is a simplified flowchart of an example of a method for power management of an electronic device.

Detailed description of the preferred embodiments

Because the illustrated embodiments of the present invention may for the most part, be implemented using electronic components and circuits known to those skilled in the art, details will not be explained in any greater extent than that considered necessary as illustrated above, for the understanding and appreciation of the underlying concepts of the present invention and in order not to obfuscate or distract from the teachings of the present invention.

An electronic device 100 may receive power from an external power supply 101. The electronic device 100 may be a processor for example. The processor 100 may for example be a microprocessor, such as a general purpose microprocessor, a microcontroller, a coprocessor, a digital signal processor or an embedded processor. The processor may have one or more processor cores. The processor may, in addition to the processor core, further comprise inputs/outputs and/or other components, such as communication interface, e.g. external bus interfaces, DMA (Direct Memory Access) controllers, and/or coprocessors and/or analog-to-digital converters and/or clocks and reset generation units, voltage regulators, memory (such as for instance flash, EEPROM, RAM), error correction code logic and/or timers, and/or hardware accelerators or other suitable components. The processor may for example be implemented as an integrated circuit, that is, on one or more dies provided in a single integrated circuit package.

The processor 100 may comprise a plurality of regions 102 or “power domains” or "power islands" which may be arranged so that they can be independently and selectively powered. Each region 102 may comprise one or more functional modules 103 sometimes referred to as “intelligent peripherals. Functional modules may comprise for example a controller area network (CAN), local interconnect network (LIN), Ethernet, a timer. Each of the functional 103 modules comprising a region may be connected together in a "power" sense such that when power is applied to a region, all functional modules comprising that region receive power and are “active” and when power is removed from a region, all other functional modules comprising that region may go into a “sleep” mode and are considered to be “inactive.” One region may be deemed to have a higher priority than other regions. More than one region may be powered on simultaneously.

In the example of FIG.1 three regions 102 are illustrated. A first region may comprise three functional modules which may be a timer, a direct memory access (DMA) module and an analog to digital converter. A second region may comprise a serial peripheral interface (SPI) and a LIN. A third region may comprise a Media Local Bus (MLB) and an Ethernet module. One or more of the functional modules 103 may be provided with an associated power monitor 104 for monitoring the current consumed by a functional module 103 with which it may be associated.

The processor 100 may include a power management module 105 for selectively controlling the application of power (supplied by the external power supply 101, for example) to each region 102 for predetermined time periods and in a predetermined sequence. In another example, the power management module 105 may be a separate device which may be connected in a suitable

manner to an electronic device such as a microprocessor or microcontroller for example which comprises a plurality of power domains.

The power management module 105 may comprise one or more switching elements 106. In one example embodiment a switching element may comprise a CMOS power transistor. Each switching element may be operably coupled between the external power supply 101 and one of the regions 102 and arranged to switch power to the region to which it is operably coupled in response to a control signal on one of an associated control line 107.

The power management module 105 may comprise a power watchdog 108 operably coupled to each region 102 and may be arranged to monitor the power consumed by each region. The power watchdog 108 may also be operably coupled to a power monitor 104 associated with a functional module 103 for receiving a measurement of current consumed by the module, for example. The power management module 105 may also comprise a controller 109. The power watchdog 108 and each region 102 may be operably coupled to the controller 109. The controller 109 may, in one example embodiment, comprise a finite state machine and may have an interrupt control capability.

In one example embodiment, one or more functional modules 103 may be provided with a power request module 110 for generating a request for power to be applied to the region comprising that functional module.

The power management module 105 may also comprise a scheduler 111, a power cycle generator 112, and a logic block 113. The controller 109 may be operably coupled with the scheduler 111 and to inputs of the logic block 113. The power cycle generator 112 may be operably coupled to the scheduler 111 and to the logic block 113. The power cycle generator 112 may receive a signal from an external clock source (not shown) on line 114. The external clock source may be a low-power clock source. The power cycle generator 112 may produce a power clock signal on its output which may be operably coupled to an input of the logic block 113. The logic block 113 may comprise, in one example, a plurality of AND gates. The outputs of the logic block 113 may comprise the aforementioned control signal lines 107 for controlling the switching elements 106. The scheduler 111 may be provided with a timer facility.

In one embodiment, a region 102 may include a power baton controller 115 which may be arranged to inhibit removal of power from the region holding the baton until a particular task is completed by one or more of the functional modules 103 which are included in the region. In an alternative embodiment, a functional module 103 may include a power baton controller 115 which may be arranged to inhibit removal of power from the functional module holding the baton until a particular task is completed by that functional module.

The power management module 105 may be arranged to operate such that at specific timed intervals it will power-on certain regions 102 whilst keeping others off. So for example during a first time interval T1, functional modules comprising a first region 102 of FIG.1 are powered on and therefore active while the functional modules comprising second and third regions are powered off and inactive. At the end of the first time interval T1, the power management module 105 may be

arranged to simultaneously remove power from the first region and to switch power to the second and third regions. This situation may persist for a second time interval T2 whereby at the end of this second time interval, different region or regions are powered on and off in accordance with a pre-determined power switching schedule which may be stored in or programmed into the scheduler 111. Application of power to the region may be facilitated by the switching elements 106 under the control of the logic block 113. A user of the processor 100 may set the time intervals and predetermined power switching schedule via a user interface (not shown) to the power management module 105. Alternatively the processor design engineer may set the time intervals and power switching schedule.

Exemplary embodiments may thus enable immediate (that is a low latency) and automatic response to a power demand by direct adjustment of the powering of regions (power domains) of an electronic device and without requiring any software modification. In one embodiment, a maximum power budget for each of the regions comprising the electronic device may be set and the power management module 105 may be arranged to switch power to the various regions such that this maximum power budget is not exceeded at any one time.

In one example embodiment the power management module 105 may be arranged to operate as a fixed time bound switching matrix (as is known in the art) whereby power is switched to the appropriate regions in the round robin fashion. Those regions which are to be active during a pre-determined time interval may be assigned an active timeslot for consuming power with the remaining regions being forced to be inactive.

Advantageously, the powering of individual regions of an electronic device such as a microcontroller independently of each other allows a power budget to be smoothed across an application lifetime, thereby minimising maximum power. A minimisation of maximum power allows a maximum thermal budget to be reduced. This results in a reduced system cost since the amount of thermal exchange is also reduced. Further, minimising maximum power allows external regulator support infrastructure to be downsized, saving power cost and size.

In one example embodiment, the power management module may be arranged to assert a power interrupt on receipt, for example, of a request for power from a functional module currently in a sleep mode, thereby ensuring that all regions 102 still retain the capability to power-up in a synchronous manner.

A further advantage of the example embodiments is that they do not require an increase in software overhead.

The functionality of the components comprising the power management module 105 will now be described in greater detail with reference to FIG.1. A clock signal from a low power clock source (not shown) may be provided at an input of the power cycle generator 112. The power cycle generator 112 may be arranged to generate a power clock signal on its output on line 116, the signal having a specific mark/space ratio which may be specified by the scheduler 111 which in turn, may be under the control of the controller 109. For example, the scheduler 111, driven by the controller 109 may create a clock window requirement for the power cycle generator 112. Depending on the requirement, the power clock signal may then be adjusted accordingly.

The logic block 113 may receive the power clock signal and also may receive inputs from the scheduler 111 and the controller 109. The controller 109 may provide an enable signal to the logic block in respect of a region 102 in order to set those regions 102 which are to be powered "on" during a next power clock cycle. So for example, one of the outputs from the logic block 113 may be set high, for example, so driving one of the switching elements "on" resulting in power being applied to that region 102 associated with that switching element 106 (for as long as the switching element is held on). Conversely one of the outputs from the logic block 113 may be set low, so holding one of the switching elements 106 off and thereby resulting in power being removed or withheld from the region 102 associated with that switching element 106.

The power watchdog 108 may signal to the controller 109 that power in a particular region 102 is within acceptable limits. The power watchdog108 may also monitor how many regions are powered at any time. Additionally, it may monitor the total power consumed by the processor 100 in order to ensure that device-wide limits are being respected. In the event that limits are about to be crossed, it may be arranged to raise an exception to the controller 109.

Each functional module 103 may raise a request for power in the form of an interrupt, for example. In one example, this may be done by a power request module 110 associated with a functional module whereby, in response to the request, a flag may be raised (in the controller, for example) signifying that the region comprising that functional module should be powered. The controller 109 may be arranged to pass on an interrupt to the scheduler 111 or, alternatively, to ignore it until a more suitable power window occurs.

Some examples of a method for power management of an electronic device will now be described with reference to FIG. 1 and to the simplified flowchart of FIG.2. At 201, a powering sequence for the various regions 102 may be set. Time periods for which the individual regions may be powered may also be set. Optionally, a maximum power value may be set. At 202, drive signals may be applied on one or more control lines 107 to appropriate switching elements 106 in order to switch power from the external power supply 101 to a region 102 for the purpose of powering the functional modules 103 included within that region. Functional modules included in regions which are not powered during any particular time period are "dormant" and may be put into a sleep mode.

At 203 the power or current consumed within the regions 102 may be monitored. In one example, if a maximum power value has been set, the power management module may be arranged to ensure that this maximum power value becomes a constant average power consumed by the processor. This has the advantage that power dips and surges may be filtered out. This may be achieved by pre-loading the scheduler 111 with a preset value of current for each functional module 103 in each region 102 for each preset time period. In one example, current consumed by a functional module 103 may be measured by a current monitor 104 associated with the functional module103. Alternatively, current consumed may be monitored by the power watchdog 108. The schedule 111 may be preloaded with a maximum current value that an application wishes to

consume. The power management module 105 may then ensure that this maximum current value is not exceeded. This may be done by limiting the number of regions receiving power at any one time.

An interrupt control facility, within the controller 109 of FIG. 1 for example, may be arranged whereby the power management module 105 has the capability to detect any activity within a dormant functional module 103. In one example, each functional module may be provided with a power request module 110 for requesting power to be supplied to it. This power request module may assert this request as an interrupt signal to the controller 109 on occurrence of certain predefined events. Hence at 205, the power management module 105 may detect a request for power from a dormant functional module 103 by receiving an interrupt signal. The controller 109 may then service this interrupt signal by indicating to the scheduler 111 that an exception has occurred and that power must be applied to the region 102 which includes the dormant functional module which has raised the request.

In one exemplary embodiment, the interrupt signals may be priority based. In such a case, a request for power from a dormant functional module 103 may be ignored or queued until a suitable power window occurs. For example, an interrupt control capability in the controller 109 may be arranged to allow the received interrupt signals to be masked by a set of “inhibit” or “mask” flags, for example. In this way, the power management module 105 may disallow certain conditions and ignore the requests for power to be applied to a dormant functional module 103. Alternatively, the request for power may be placed in a standard queue system and the power management module may be arranged to determine when enough power is available to service the request and to apply the power accordingly (at 206).

In an alternative arrangement, a “power baton” concept may be employed whereby each functional module 103 may effectively take control of the power to the region 102 in which it is located or solely to itself until a particular task is completed and then relinquish power ownership by passing the baton on to a second functional module. This second functional module may be included in the same region or may be in a different region. Such a power baton or power token may be a control flag whereby a functional module would maintain power to itself at the exclusion of other dormant functional modules. Once the controlling functional module controlling the power baton has completed its task it may release the power baton (or token) and pass it along to another functional module by means of a simple notification scheme via a register control for example. Once the power baton is released, the releasing functional module may power itself down whereupon a newly enabled functional module may take over and power itself up.

It will be appreciated from the foregoing that an electronic device (such as a microcontroller) which includes examples of the power management module 105 may exhibit certain advantages. For example, such a microcontroller may be arranged to include a power scheme designed to prevent simultaneous operation of all regions of the microcontroller. Further, the microcontroller

may operate a power scheme which is designed to operate independent power domains in a controlled manner. The microcontroller may also have the capability to assert a power interrupt even when certain sections of the microcontroller are powered down. The microcontroller may be configured to respond to power interrupts, determine priorities and take appropriate power allocation decisions. The microcontroller may be arranged to allow time division of power with a variable duty cycle between power domains. The microcontroller may be arranged in order to ensure that at least one power domain is not affected by power excursions. The microcontroller may also be arranged to determine the optimum power delivery to each domain. The microcontroller may be configured such that power ownership may be passed from a section comprising one or more functional modules of the microcontroller to another. The microcontroller may be configured whereby power is switched from one region to another with an applied power smoothing scheme thereby preventing spurious power spikes or dips.

The invention may also be implemented in a computer program for running on a computer system, at least including code portions for performing steps of a method according to the invention when run on a programmable apparatus, such as a computer system or enabling a programmable apparatus to perform functions of a device or system according to the invention.

As an example, a tangible computer program product may be provided having executable code stored therein to perform a method for power management in an electronic device. A computer program is a list of instructions such as a particular application program and/or an operating system. The computer program may for instance include one or more of: a subroutine, a function, a procedure, an object method, an object implementation, an executable application, an applet, a servlet, a source code, an object code, a shared library/dynamic load library and/or other sequence of instructions designed for execution on a computer system.

The computer program may be stored internally on computer readable storage medium or transmitted to the computer system via a computer readable transmission medium. All or some of the computer program may be provided on computer readable media permanently, removably or remotely coupled to an information processing system. The computer readable media may include, for example and without limitation, any number of the following: magnetic storage media including disk and tape storage media; optical storage media such as compact disk media (e.g., CD-ROM, CD-R, etc.) and digital video disk storage media; nonvolatile memory storage media including semiconductor-based memory units such as FLASH memory, EEPROM, EPROM, ROM; ferromagnetic digital memories; MRAM; volatile storage media including registers, buffers or caches, main memory, RAM, etc.; and data transmission media including computer networks, point-to-point telecommunication equipment, and carrier wave transmission media, just to name a few.

A computer process typically includes an executing (running) program or portion of a program, current program values and state information, and the resources used by the operating system to manage the execution of the process. An operating system (OS) is the software that

manages the sharing of the resources of a computer and provides programmers with an interface used to access those resources. An operating system processes system data and user input, and responds by allocating and managing tasks and internal system resources as a service to users and programs of the system.

The computer system may for instance include at least one processing unit, associated memory and a number of input/output (I/O) devices. When executing the computer program, the computer system processes information according to the computer program and produces resultant output information via I/O devices.

In the foregoing specification, the invention has been described with reference to specific examples of embodiments of the invention. It will, however, be evident that various modifications and changes may be made therein without departing from the broader spirit and scope of the invention as set forth in the appended claims. For example, the connections as discussed herein may be any type of connection suitable to transfer signals from or to the respective nodes, units or devices, for example via intermediate devices. Accordingly, unless implied or stated otherwise, the connections may for example be direct connections or indirect connections. The connections may be illustrated or described in reference to being a single connection, a plurality of connections, unidirectional connections, or bidirectional connections. However, different embodiments may vary the implementation of the connections. For example, separate unidirectional connections may be used rather than bidirectional connections and vice versa. Also, plurality of connections may be replaced with a single connection that transfers multiple signals serially or in a time multiplexed manner. Likewise, single connections carrying multiple signals may be separated out into various different connections carrying subsets of these signals. Therefore, many options exist for transferring signals.

Each logical signal described herein may be designed as positive or negative logic. In the case of a negative logic signal, the signal is active low where the logically true state corresponds to a logic level zero. In the case of a positive logic signal, the signal is active high where the logically true state corresponds to a logic level one. Note that any of the logical signals described herein can be designed as either negative or positive logic signals. Therefore, in alternate embodiments, those signals described as positive logic signals may be implemented as negative logic signals, and those signals described as negative logic signals may be implemented as positive logic signals.

Those skilled in the art will recognize that the boundaries between logic and functional blocks are merely illustrative and that alternative embodiments may merge logic and functional blocks or circuit elements or impose an alternate decomposition of functionality upon various logic blocks or circuit elements. Thus, it is to be understood that the architectures depicted herein are merely exemplary, and that in fact many other architectures can be implemented which achieve the same functionality. For example, the functionality of the controller 109, scheduler 111, logic block 113 and power cycle generator 112 of FIG. 1 may be combined and implemented in one or more

modules. Further, any arrangement of components to achieve the same functionality is effectively "associated" such that the desired functionality is achieved. Hence, any two components herein combined to achieve a particular functionality can be seen as "associated with" each other such that the desired functionality is achieved, irrespective of architectures or intermedial components. Likewise, any two components so associated can also be viewed as being "operably connected," or "operably coupled," to each other to achieve the desired functionality.

Furthermore, those skilled in the art will recognize that boundaries between the above described operations merely illustrative. The multiple operations may be combined into a single operation, a single operation may be distributed in additional operations and operations may be executed at least partially overlapping in time. Moreover, alternative embodiments may include multiple instances of a particular operation, and the order of operations may be altered in various other embodiments.

The electronic device of FIG.1 comprising a power management capability may be implemented in an integrated circuit. Such an integrated circuit may be a package containing one or more dies. Alternatively, the power management module 105 may be implemented in a separate integrated circuit device which may be connected with an electronic device, such as a microcontroller or microprocessor, in a suitable manner for managing power thereof. An integrated circuit device may comprise one or more dies in a single package with electronic components provided on the dies that form the modules and which are connectable to other components outside the package through suitable connections such as pins of the package and bondwires between the pins and the dies.

Also for example, the examples, or portions thereof, may implemented as soft or code representations of physical circuitry or of logical representations convertible into physical circuitry, such as in a hardware description language of any appropriate type.

Also, the invention is not limited to physical devices or units implemented in non-programmable hardware but can also be applied in programmable devices or units able to perform the desired device functions by operating in accordance with suitable program code, such as mainframes, minicomputers, servers, workstations, personal computers, notepads, personal digital assistants, electronic games, automotive and other embedded systems, cell phones and various other wireless devices, commonly denoted in this application as ‘computer systems’.

However, other modifications, variations and alternatives are also possible. The specifications and drawings are, accordingly, to be regarded in an illustrative rather than in a restrictive sense.

In the claims, any reference signs placed between parentheses shall not be construed as limiting the claim. The word ‘comprising’ does not exclude the presence of other elements or steps then those listed in a claim. Furthermore, the terms “a” or “an,” as used herein, are defined as one or more than one. Also, the use of introductory phrases such as “at least one” and “one or more” in

the claims should not be construed to imply that the introduction of another claim element by the indefinite articles "a" or "an" limits any particular claim containing such introduced claim element to inventions containing only one such element, even when the same claim includes the introductory phrases "one or more" or "at least one" and indefinite articles such as "a" or "an." The same holds true for the use of definite articles. Unless stated otherwise, terms such as “first” and “second” are used to arbitrarily distinguish between the elements such terms describe. Thus, these terms are not necessarily intended to indicate temporal or other prioritization of such elements The mere fact that certain measures are recited in mutually different claims does not indicate that a combination of these measures cannot be used to advantage.

Claims

1. Apparatus (105) for the management of power in an electronic device (100) comprising a plurality of independently-powerable regions (102) wherein each region comprises at least one functional module (103), and wherein the apparatus (105) is arranged to selectively switch power to one or more of said regions for pre-determined time periods and in a pre-determined sequence.

2. The apparatus (105) of claim 1 comprising a plurality of switching elements (106) for coupling to a respective one of said regions (102), wherein each of said switching elements is arranged to switch power to a region in accordance with a control signal (107).

3. The apparatus (105) of either preceding claim arranged to switch power to each of said regions (102) in a round robin fashion.

4. The apparatus (105) of any preceding claim comprising a current monitor (108) arranged to monitor current consumed by one or more functional modules (103) and arranged to limit a consumed current to a pre--set maximum value .

5. The apparatus (105) of any preceding claim comprising an interrupt controller (109) arranged to detect a request for power at from at least one functional module (103).

6. The apparatus (105) of claim 5 wherein the interrupt controller (109) is arranged to generate a control signal for allowing power to be switched to the region comprising the functional module (103) requesting power.

7. An electronic device (100) comprising a plurality of independently-powerable regions (102) wherein each region comprises at least one functional module (103), and including the apparatus (105) of any preceding claim and implemented in an integrated circuit.

8. The electronic device (100) of claim 7 arranged to inhibit removal of power by said apparatus (105) from a powered region (102) until a particular task has been completed by one or more functional modules (103) comprising the region (102).

9. A method (200) for power management of an electronic device (100) comprising a plurality of independently-powerable regions (102), the method comprising selectively switching power (202) to one or more of said regions for pre-determined time periods and in a predetermined sequence.

10. A tangible computer program product (105) having executable code stored therein to perform a method for power management in an electronic device (100) in accordance with claim 9.

11. The tangible computer program product of Claim 10 wherein the tangible computer program product comprises at least one from a group consisting of: a hard disk, a CD-ROM, an optical storage device, a magnetic storage device, a Read Only Memory, a Programmable Read Only Memory, an Erasable Programmable Read Only Memory, EPROM, an Electrically Erasable Programmable Read Only Memory and a Flash memory.

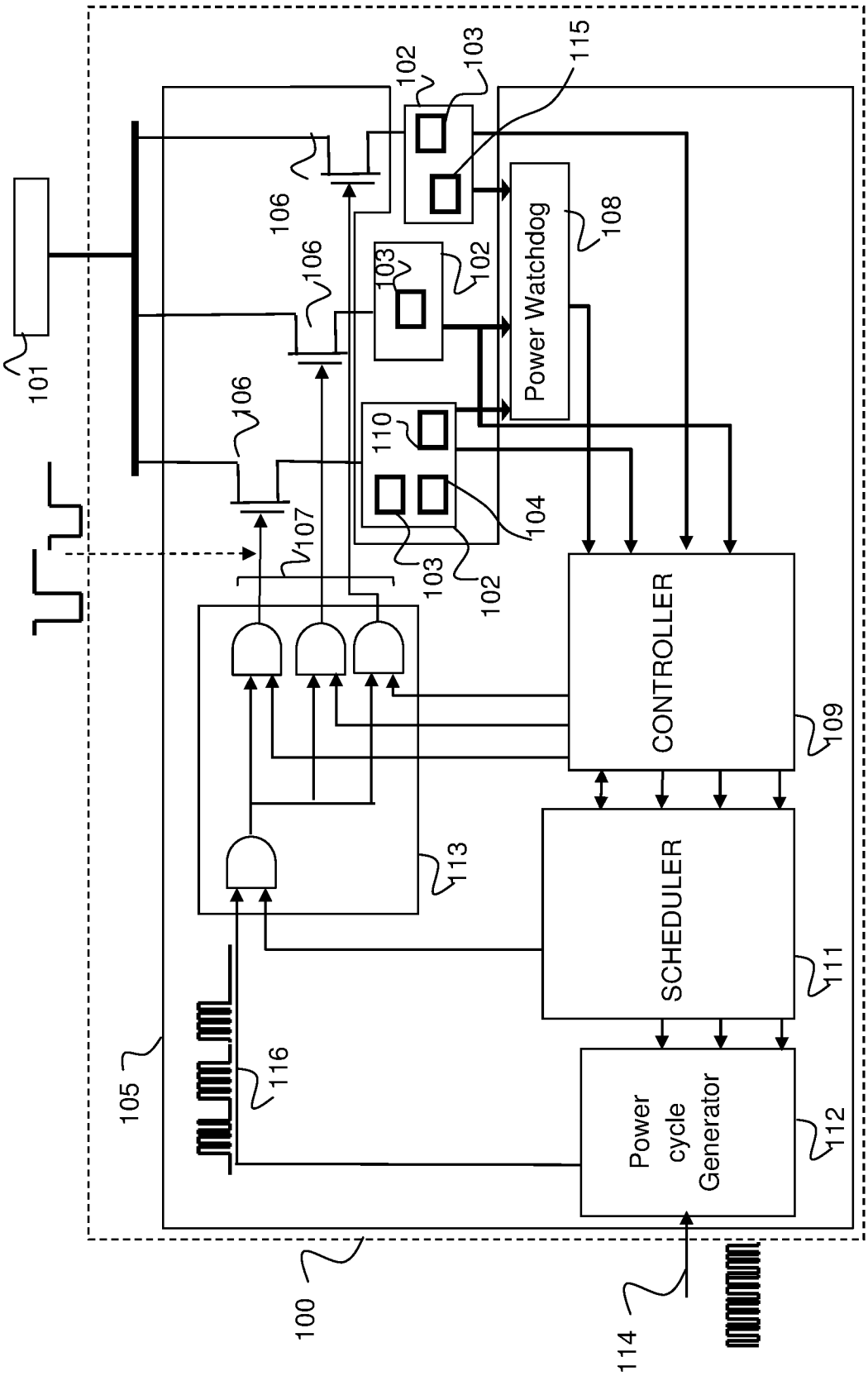
100
101
102
103
104
105
106
107
108
109
110
111
112
113
114
115
116
Power Watchdog
CONTROLLER
SCHEDULER
Power cycle Generator

FIG. 1

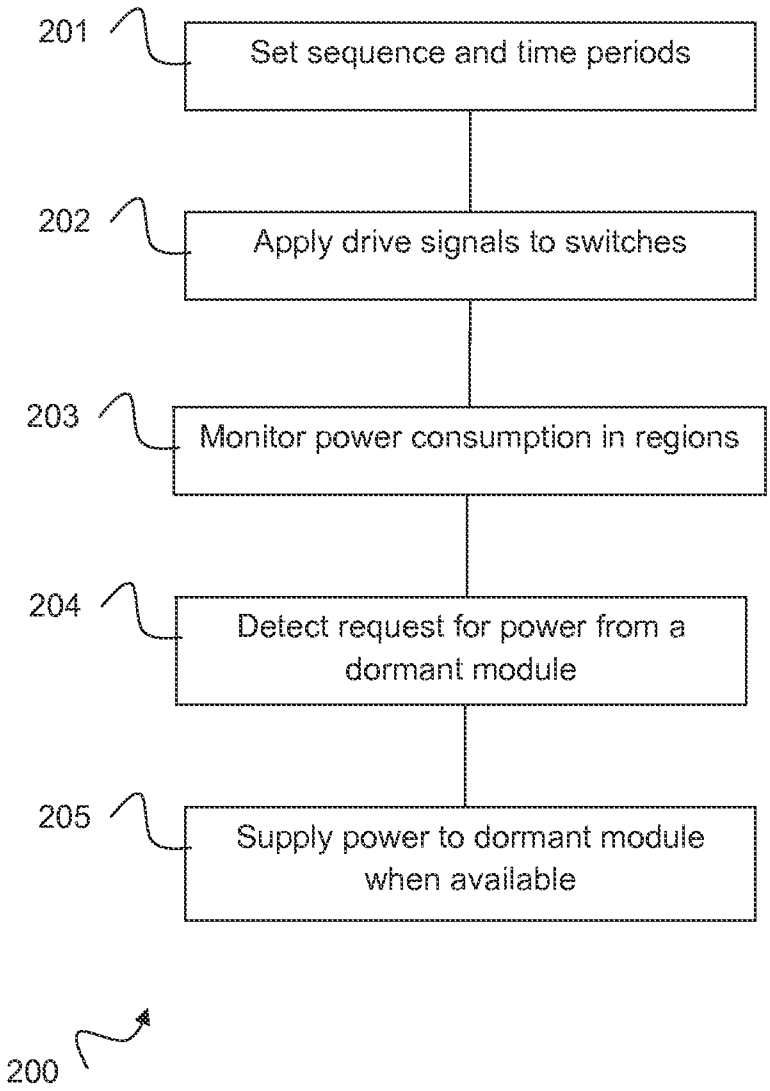
201
Set sequence and time periods
202
Apply drive signals to switches
203
Monitor power consumption in regions
204
Detect request for power from a dormant module
205
Supply power to dormant module when available
200

FIG. 2

INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB2013/058935

A. CLASSIFICATION OF SUBJECT MATTER

G06F 1/26(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G06F 1/26; G06F 1/28; G05B 13/02; G05B 11/01; H04W 52/02; G06F 1/12

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & keywords: independent, power, switch, period, sequence

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2011-0283130 A1 (HONG-REN PAI et al.) 17 November 2011 See paragraphs [0017]-[0019]; and figures 1-2.	1-3,9-11
A	US 8543226 B2 (ASHOK DEEPAK SHAH et al.) 24 September 2013 See column 10, line 25 - column 11, line 26; and figures 1, 4.	1-3,9-11
A	US 2012-0120306 A1 (FREDERICK R. SCHINDLER et al.) 17 May 2012 See paragraphs [0032]-[0042]; and figures 1, 3.	1-3,9-11
A	US 2013-0111254 A1 (TOSHINARI TAKAYANAGI et al.) 2 May 2013 See paragraphs [0069]-[0072]; and figures 3-6.	1-3,9-11
A	US 2013-0166089 A1 (JASON CRAIG et al.) 27 June 2013 See paragraphs [0055]-[0069]; and figures 1-2.	1-3,9-11

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
24 June 2014 (24.06.2014)	**25 June 2014 (25.06.2014)**

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB2013/058935

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☒ Claims Nos.: 6,8
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
The claims 6 and 8 do not comply with PCT Article 6 because they are respectively referring to unsearchable claims 5 and 7.

3. ☒ Claims Nos.: 4,5,7
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required addtional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of any additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/IB2013/058935

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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