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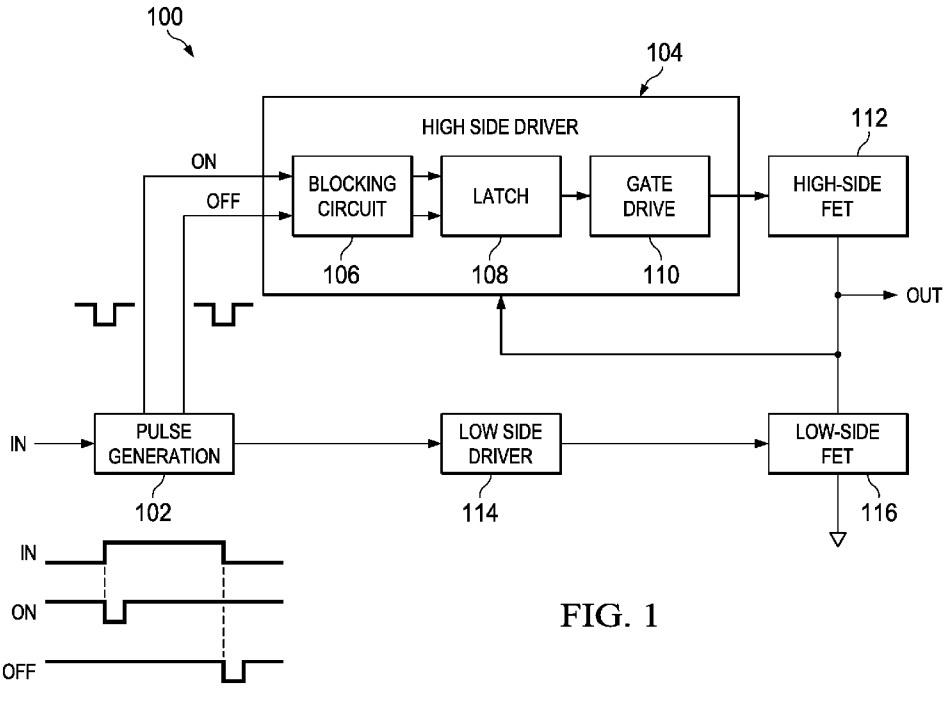


FIG. 1

(57) Abstract: A lever shifter (100) includes an output driver (112) and a high-side gate driver (104). The high-side gate driver (104) is configured to drive the high-side output transistor (112), and is coupled to an on pulse signal line that conducts an on pulse, and is coupled to an off pulse signal line that conducts an off pulse. The high-side gate driver (104) includes a blocking circuit (106) configured to enable generation of a drive signal to the high-side output transistor (112) based on a voltage of a first of the on or off pulse signal line being greater than a first predetermined amount and a voltage of a second of the on or off signal line being less than a second predetermined amount.

[Continued on next page]

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HIGH VOLTAGE LEVEL SHIFTER WITH SHORT PROPAGATION DELAY

BACKGROUND

[0001] Level shifters are utilized in electronic circuits for changing the voltage of a signal from one voltage level to another voltage level. For example, some electronic circuits employ different power domains, wherein different reference voltages are used to power the circuitry in each power domain. The reference voltage in a power domain defines the voltage levels that represent an asserted logic state (e.g. a logic value of "1") and a negated logic state (e.g. a logic value of "0") for signals in the power domain. In order to ensure proper communication of information between power domains, a level shifter can be employed to shift the voltage of a signal communicated across the power domains so that the logic state represented by the signal is consistent over the power domains.

[0002] Level shifters are sometimes used in applications where input logic voltage level signals are translated to output signals at higher voltage levels. For example, automotive, electronic data processing, and industrial control applications may require high voltage level shifters to drive various peripheral devices. Such circuits are often implemented in application specific integrated circuits (ASICs) or as independently packaged circuits. High voltage level shifters may translate a logic level (e.g., 0 to 5 volts) input signal to signals at higher voltage levels.

SUMMARY

[0003] High voltage level shifters having short propagation delay are disclosed herein. In one embodiment, a high voltage lever shifter includes an output driver, a pulse generator, and a high-side gate driver. The output driver is configured to switch a voltage of at least 200 volts. The output driver includes a high-side output transistor. The pulse generator is configured to generate an on pulse at a first edge of an input signal received at an input terminal of the level shifter and to generate an off pulse at a

second edge of the input signal. The high-side gate driver is configured to drive the high-side output transistor. The high-side gate driver is coupled to an on pulse signal line that conducts the on pulse and is coupled to an off pulse signal line that conducts the off pulse. The high-side gate driver includes a blocking circuit configured to detect a voltage of the on pulse signal line, to detect a voltage of the off pulse signal line, and to inhibit generation of a drive signal to the high-side output transistor based on a difference of the voltage of the on pulse signal line and the voltage of the off pulse signal line being less than a predetermined amount.

[0004] In another embodiment, a transistor driver includes a pulse generator, a blocking circuit coupled to the pulse generator, and a latch coupled to the blocking circuit. The pulse generator is configured to generate an on pulse at a leading edge of an input signal received at an input terminal of the high-side transistor driver and to generate an off pulse at a trailing edge of the input signal. The pulse signal generator is configured to drive an on pulse signal line that conducts the on pulse and to drive an off pulse signal line that conducts the off pulse. The blocking circuit is configured to enable state change of a drive signal to drive a high-side drive transistor based on voltage of the on pulse signal line exceeding a first threshold and voltage of the off pulse signal line not exceeding a second threshold, or voltage of the off pulse signal line exceeding the first threshold and voltage of the on pulse signal line not exceeding the second threshold.

[0005] In a further embodiment, a level shifter includes an output driver, a pulse generator, and a high-side gate driver. The output driver is configured to switch a voltage of at least 200 volts. The output driver includes a high-side output transistor. The pulse generator is configured to generate an on pulse at a leading edge of an input signal received at an input terminal of the level shifter and to generate an off pulse at a trailing edge of the input signal. The high-side gate driver is configured to drive the high-side output transistor. The high-side gate driver is coupled to an on pulse signal line that conducts the on pulse and coupled to an off pulse signal line that conducts the off pulse. The high-side gate driver includes a blocking circuit comprising a plurality of transistors configured to inhibit a change in state of the drive signal to the high-side output transistor based on simultaneous assertion of signals on both the on pulse signal

line and the off pulse signal line, and based on simultaneous negation of signals on both the on pulse signal line and the off pulse signal line.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] For a detailed description of various examples, reference will now be made to the accompanying drawings in which:

[0007] Figure 1 shows a block diagram for a high-voltage level shifter that includes blocking circuitry to reduce the effects of transient disturbances in accordance with various embodiments;

[0008] Figure 2 shows a schematic diagram for a high-voltage level shifter that includes blocking circuitry to reduce the effects of transient disturbances in accordance with various embodiments;

[0009] Figure 3 shows a schematic diagram for a high-voltage level shifter that includes blocking circuitry to reduce the effects of transient disturbances in accordance with various embodiments; and

[0010] Figure 4 shows examples of signals in high voltage level shifters with and without blocking circuitry as disclosed herein.

DETAILED DESCRIPTION

[0011] Certain terms are used throughout the following description and claims to refer to particular system components. As one skilled in the art will appreciate, different companies may refer to a component by different names. This document does not intend to distinguish between components that differ in name but not function. In the following discussion and in the claims, the terms “including” and “comprising” are used in an open-ended fashion, and thus should be interpreted to mean “including, but not limited to… .” Also, the term “couple” or “couples” is intended to mean either an indirect or direct wired or wireless connection. Thus, if a first device couples to a second device, that connection may be through a direct connection or through an indirect connection via other devices and connections. The recitation “based on” is intended to mean “based at least in part on.” Therefore, if *X* is based on *Y*, *X* may be based on *Y* and any number of other factors.

[0012] In the drawings and description that follow, certain features of the invention may be shown exaggerated in scale or in somewhat schematic form, and some details of conventional elements may not be shown in the interest of clarity and conciseness. The present disclosure is susceptible to embodiments of different forms. Specific embodiments are described in detail and are shown in the drawings, with the understanding that the present disclosure is to be considered an exemplification of the principles of the disclosure, and is not intended to limit the disclosure to that illustrated and described herein. It is to be fully recognized that the different teachings and components of the embodiments discussed below may be employed separately or in any suitable combination to produce desired results.

[0013] To provide a high power density, power converters may implement a high switching frequency. Such power converters require transistor (e.g., field effect transistor) drivers with a low propagation delay. Conventional transistor drivers for switching less than 200 volts can provide propagation delay in a range of 15 nanoseconds (ns) to 30ns. However, in the 600V range, conventional drivers may provide no less than 90 ns of propagation delay. Isolated gate driver technology can achieve 20 ns propagation delay, but is not cost competitive with other conventional driver technologies.

[0014] Conventional high voltage transistor drivers include a de-glitch filter to prevent disturbing signals (such as common mode signals) from affecting driver output. Unfortunately, the de-glitch filter increases driver propagation delay. Embodiments of the present disclosure provide immunity from erroneous driver transitions caused by common mode and other disturbing signals without implementation of a de-glitch filter. Instead of de-glitch filters that filter out a disturbing signal, the driver circuits disclosed herein include blocking circuitry that monitors the signals setting driver output state and blocks propagation of the signals if the signals are determined to be a result of a disturbing signal, such as a common mode transient. Because the drivers disclosed herein do not include a de-glitch filter, propagation delay may be substantially reduced relative to conventional drivers that employ a de-glitch filter. For example, embodiments of the high voltage driver and level shifter disclosed herein may provide a propagation delay of about 30 ns (e.g., 30 ns ± 5 ns) or less when switching 200 or more volts (e.g., 600 volts in some embodiments).

[0015] Figure 1 shows a block diagram for a high-voltage level shifter 100 that includes blocking circuitry to reduce the effects of transient disturbances in accordance with various embodiments. The level shifter 100 includes pulse generation circuitry 102, a high side driver 104, a high side transistor 112, a low side driver 114, and a low side transistor 116. The pulse generation circuitry 102 receives an input signal (IN) and generates a pulse at each edge or transition of the IN signal from one logic level to another. For example, the pulse generation circuitry 102 may generate a pulse on the signal line labeled ON responsive to the IN signal transitioning from a "0" logic state to a "1" logic state, and generate a pulse on the signal line labeled OFF responsive to the IN signal transitioning from a "1" logic state to a "0" logic state.

[0016] The pulse generation circuitry 102 is coupled to the high side driver 104 via the ON signal line and the OFF signal line. The high side driver 104 includes a blocking circuit 106, a latch 108, and a gate driver 110. The blocking circuit 106 receives signals on the ON signal line and the OFF signal line. Outputs of the blocking circuit 108, which may correspond to the signals on the ON and OFF signal lines, set and reset the latch 108. An output of the latch 108 drives the high-side transistor 112 via the transistor gate driver 110. The high side driver 104 may be referenced to the output of the level shifter 100. That is, the output of the level shifter 100 may set a ground voltage for the high side driver 104. A power rail for the high side driver 104 may float, for example, from a supply voltage used to power the pulse generator 102, or other circuitry of the level shifter 100, to a voltage exceeding a high voltage connected to the high-side transistor 112 (e.g., >200 volts). Thus, the high side driver 104 reference voltage may be ground while the high-side transistor 112 is turned off and a much higher voltage (e.g., 600 volts) while the high-side transistor 112 is turned on in order to allow the high-side driver 104 to maintain control of the high-side transistor 112 while the high-side transistor 112 is on.

[0017] One or more outputs of the pulse generator 102 drive the low-side driver 114, which in turn drives the low-side transistor 116. Because the low-side transistor 116 is referenced to ground, control of the low-side transistor 116 is substantially less complex than control of the high-side transistor 112, and is not described herein.

[0018] The blocking circuit 106 monitors the voltage on the ON signal line and the voltage on the OFF signal line to determine whether signals present on the ON and OFF

signal lines are pulses generated by the pulse generation circuitry 102. If the blocking circuit 106 determines that the signals on the ON and OFF signal lines are pulses generated by the pulse generation circuitry 102, then the blocking circuit 106 propagates the signals to the latch 108. If the blocking circuit 106 determines that the signals on the ON and OFF signal lines are not generated by the pulse generation circuitry 102, then blocking circuit 106 does not propagate the signals to the latch 108. The blocking circuit 106 may determine whether the signals present on the ON and OFF signal lines are to be propagated to the latch 108 based on the voltage levels present on the ON and OFF signal lines.

[0019] As shown in Figure 1, at any time (e.g., at an edge of the signal IN), the pulse generation circuitry 102 drives a pulse onto only one of the ON or OFF signal lines. Accordingly, during normal pulse generation, the voltages on the ON and OFF signal lines will be substantially different. In contrast, noise (such as a common mode transient) may induce a simultaneous pulse on both the ON and OFF signal lines. Thus, voltages induced on the ON and OFF signal lines by a disturbance, such as a common mode transient, may produce a similar voltage level (e.g., a simultaneous pulse) on the ON and OFF signal lines. In embodiments of the driver 104, if the voltage on one of the ON or OFF signal lines is greater than a first predetermined voltage, and the voltage on the other of the ON or OFF signal lines is less than a second predetermined voltage, then the blocking circuitry 106 may propagate the signals to the latch 108, and the output of the latch 108 may change responsive to the signals. If the voltages on the ON and OFF signal lines are such that these conditions are not met (i.e., one is not higher than the first predetermined voltage or the other is not lower than the second predetermined voltage), then the blocking circuitry 106 may not pass the signals to the latch 108, and the output of the latch 108 will remain unchanged. Thus, the blocking circuit 106 prevents spurious transitions in the drive signal provided to the high-side transistor 112, while reducing propagation delay relative to conventional high-voltage drivers.

[0020] Figure 2 shows a schematic diagram for a high-voltage level shifter 200 that includes blocking circuitry 226 to reduce the effects of transient disturbances in accordance with various embodiments. The high-voltage level shifter 200 is an embodiment of the high-voltage level shifter 100. The high-voltage level shifter 200

includes pulse generation circuitry 102, high side driver 104, high side transistor 112, low side driver 114, and low side transistor 116. The pulse generation circuitry 102 includes pulse logic 214, clamp and slew detection circuitry 216, transistors 218 and 220, and current sources 222 and 224. Transistors 218 and 220 may be laterally diffused metal oxide semiconductor (LDMOS) transistors. The clamp and slew detection circuitry 216 generates a clamp voltage that drives the control terminal (e.g., gate) of the transistors 218 and 220 to ensure proper operation. The clamp and slew detection circuitry 216 may also detect slewing in the high side driver 104 via the parasitic capacitance of the transistor 218 and/or the transistor 220. The pulse logic 214 generates pulse TurnON or TurnOff at each transition of the IN signal. The pulses TurnON and TurnOff control the current sources 222 and 224 respectively, which in turn produce corresponding pulses on the ON and OFF signal lines. The signals on the ON and OFF signal lines may be active low signals.

[0021] The high side driver 104 includes a blocking circuit 226, a latch 108, and a gate driver 110. The blocking circuit 226 may be an embodiment of the blocking circuit 106. The blocking circuitry 226 includes comparators 202, 204, 206, and 208, and "AND" gates 210 and 212. The comparators 202, 204, 206, and 208 compare the voltages present on the ON and OFF signal lines to reference voltages to determine whether the signals present on the ON and OFF signal lines should be propagated to the latch 108. In Figure 2, the reference voltages are designated V1 and V2. The voltages V1 and V2 may be set as needed to specify a desired differential between and level of the voltage of the ON and OFF signal lines required to propagate signals to the latch 108. For example, in the level shifter 200, V1 may be set to HB-2 volts, and V2 may be set to HB-1 volt. Other embodiments may apply different values of V1 and V2.

[0022] Comparators 202 and 208 are coupled to the "AND" gate 210 to control resetting of the latch 108, and the comparators 204 and 206 are coupled to the "AND" gate 212 to control setting of the latch 108. If the signal voltage on the OFF signal line exceeds reference voltage V2 and the signal voltage on the ON signal line is lower than the reference voltage V1, then the blocking circuitry 226 will drive a SET input of the latch 108. Similarly, if the signal voltage on the ON signal line exceeds reference voltage V2 and the signal voltage on the OFF signal line is lower than the reference voltage V1, then

the blocking circuitry 226 will drive a RESET input of the latch 108. If the signals on the ON and OFF signal lines provide neither of these two specific conditions, then the state of the latch 108 is unchanged. As noted above, common mode transients and other disturbing signals tend to induce a similar voltage on both the ON and OFF signal lines. Accordingly, if the signal on the ON signal line exceeds the reference voltage V1, the blocking circuitry 226 prevents change in the driver output regardless of whether signal on the OFF signal line exceeds the reference voltage V2. Similarly, if the signal on the OFF signal line exceeds the reference voltage V1, the blocking circuitry 226 prevents change in the driver output regardless of whether signal on the ON signal line exceeds the reference voltage V2. Accordingly, the blocking circuitry 226 prevents common mode transients from causing unintended changes in the state of the output of the high side driver 104 with little or no increase in propagation delay through the high side driver 104.

[0023] Figure 3 shows a schematic diagram for a high-voltage level shifter 300 that includes blocking circuitry 326 to reduce the effects of transient disturbances in accordance with various embodiments. The high-voltage level shifter 300 is an embodiment of the high-voltage level shifter 100, and the blocking circuitry 326 is an embodiment of the blocking circuitry 106. The high-voltage level shifter 300 includes the various components of the high-side level shifter 100, but the pulse generation circuitry 102, low side driver 114, and the low side transistor 116 are not shown in Figure 3. In the level shifter 300, the blocking circuitry 326 includes a number of transistors 302-312 arranged to control propagation of signals on the ON and OFF signal lines to the latch 108. The signals on the ON and OFF signal lines may be active low signals. In the blocking circuitry 326, the difference in voltage of the ON signal line and the OFF signal line needed to trigger propagation of signal to the latch 108 may be defined by the voltage thresholds at which the transistors 302-312 turn on or off.

[0024] Transistors 302, 304, and 306 form a latch set circuit that controls propagation of signals to the set input of the latch 108. Generally, the set input of the latch 108 will be asserted when the voltage on the OFF signal line is “high” and the voltage on the ON signal line is “low.” The high signal voltage on the OFF signal line turns off transistor 302, thereby pulling down the control terminal (e.g., the gate) of, and turning on, transistor 306. The low signal voltage on the ON signal line turns on transistor 304, thereby enabling

current flow through transistors 304 and 306, and asserting the set input of the latch 108. The transistors 302, 304, and 306 hold the set input of the latch 108 negated under all conditions of the ON and OFF signal lines other than when high signal voltage is present on the OFF signal line and low signal voltage is present on the ON signal line.

[0025] Transistors 308, 310, and 312 form a latch reset circuit that controls routing of signals to the reset input of the latch 108. Generally, the reset input of the latch 108 will be asserted when the voltage on the ON signal line is "high" and the voltage on the OFF signal line is "low." The high signal voltage on the ON signal line turns off transistor 308, thereby pulling down the control terminal (e.g., the gate) of, and turning on, transistor 312. The low signal voltage on the OFF signal line turns on transistor 310, thereby enabling current flow through transistors 310 and 312, and asserting the reset input of the latch 108. The transistors 308, 310, and 312 hold the reset input of the latch 108 negated under all conditions of the ON and OFF signal lines other than when high signal voltage is present on the ON signal line and low signal voltage is present on the OFF signal line. Accordingly, the blocking circuitry 326 prevents common mode transients from causing unintended changes in the state of the output of the high side driver 104 with little or no increase in propagation delay through the high side driver 104.

[0026] Figure 4 shows examples of signals in high voltage level shifters with and without blocking circuitry as disclosed herein. In Figure 4, a pulse 402 is received by the pulse generation circuitry 102, and in turn, the pulse generation circuitry 102 produces pulse 404 responsive to the leading edge of the pulse 402 and produces pulse 406 responsive to the trailing edge of the pulse 402. The signal DIFF reflects the difference between the voltages on the ON and OFF signal lines.

[0027] The signal 408 represents the output of a conventional level shifter that includes a de-glitch filter. As shown in Figure 4, the output of the level shifter is substantially delayed from the leading edge of the pulse 404 by the de-glitch filter. Similarly, the output of the level shifter is substantially delayed from the leading edge of the pulse 406 by the de-glitch filter.

[0028] The signal 410 represents the output of the level shifter 100 that includes blocking circuitry 106 rather than a de-glitch filter. As shown in Figure 4, the delay of the signal 410 is greatly reduced relative to the signal 408 produced using a de-glitch filter.

[0029] The signal 412 represents the output of level shifter that lacks both a de-glitch filter and the blocking circuitry 106. As shown in Figure 4, the delay of the signal 412 is similar to that provided by the level shifter 100. However, the level shifter that generated output 412 is prone to erroneous output transitions caused by transient signals. Signal 414 represents a high voltage common mode signal in the level shifters. Mismatches between components (i.e., transistors, resistors, etc.) of the level shifter can result in signal voltage differentials that trigger a state change in the level shifter that lacks a de-glitch filter or the blocking circuitry 106. In Figure 4, the common mode pulse 416 produces pulses 418 and 420 on the ON signal line and the OFF signal line with sufficient differential to erroneously set the output 412. The blocking circuitry 106 of the level shifter 100 prevents the state of the latch 108 from changing responsive to the pulses 418 and 420.

[0030] The above discussion is meant to be illustrative of the principles and various embodiments of the present invention. Numerous variations and modifications will become apparent to those skilled in the art once the above disclosure is fully appreciated. It is intended that the following claims be interpreted to embrace all such variations and modifications.

CLAIMS

What is claimed is:

1. A lever shifter, comprising:

an output driver configured to switch a voltage, the driver comprising:

a high-side output transistor;

a pulse generator configured to generate an on pulse at a first edge of an input signal received at an input terminal of the level shifter and to generate an off pulse at a second edge of the input signal; and

a high-side gate driver configured to drive the high-side output transistor, the high-side gate driver coupled to an on pulse signal line that conducts the on pulse and coupled to an off pulse signal line that conducts the off pulse, the high-side gate driver comprising:

a blocking circuit configured to:

detect a voltage of the on pulse signal line;

detect a voltage of the off pulse signal line; and

inhibit state change of a drive signal to the high-side output transistor based on a difference of the voltage of the on pulse signal line and the voltage of the off pulse signal line being less than a predetermined amount.

2. The level shifter of claim 1, wherein the blocking circuit is configured to enable state change of the drive signal to the high-side output transistor based on the difference of the voltage of the on pulse signal line and the voltage of the off pulse signal line being greater than the predetermined amount.

3. The level shifter of claim 1, wherein the blocking circuit comprises circuitry configured to inhibit a state change of the drive signal to the high-side output transistor based on assertion of signals on both the on pulse signal line and the off pulse signal line; and based on negation of signals on both the on pulse signal line and the off pulse signal line.

4. The level shifter of claim 3, wherein the blocking circuit comprises a first plurality of comparators configured to compare the voltage of the on pulse signal line to a first reference voltage and compare the voltage of the off pulse signal line to a second reference voltage.

5. The level shifter of claim 4, wherein the blocking circuit comprises circuitry configured to assert drive to the high-side output transistor based on the voltage of the on pulse signal line being less than the first reference voltage and the voltage of the off pulse signal line being greater than the second reference voltage.

6. The level shifter of claim 4, wherein the blocking circuit comprises a second plurality of comparators configured to compare the voltage of the on pulse signal line to the second reference voltage and compare the voltage of the off pulse signal line to the first reference voltage.

7. The level shifter of claim 6, wherein the blocking circuit comprises circuitry configured to negate drive to the high-side output transistor based on the voltage of the on pulse signal line being greater than the first reference voltage and the voltage of the off pulse signal line being less than the second reference voltage.

8. The level shifter of claim 1, wherein the high-side gate driver comprises a latch coupled to the blocking circuit, the latch configured to generate a signal to drive the high-side transistor based on an output of the blocking circuit indicating that the voltage of the on pulse signal line and the voltage of the off pulse signal line comprise a pulse produced by the pulse generator.

9. The level shifter of claim 1, wherein the blocking circuit comprises:

a latch set circuit comprising a first plurality of transistors configured to set the drive signal to a first state based on the voltage of the on pulse signal line being below a first threshold and the voltage of the off pulse signal line being above a second threshold; and

a latch reset circuit comprising a second plurality of transistors configured to set the drive signal to a second state based on the voltage of the off pulse signal line being below the first threshold and the voltage of the on pulse signal line being above the second threshold.

10. A transistor driver, comprising:

a pulse generator;

a blocking circuit coupled to the pulse generator; and

a latch coupled to the blocking circuit;

wherein the pulse generator is configured to generate an on pulse at a leading edge of an input signal received at an input terminal of the high-side transistor driver and to generate an off pulse at a trailing edge of the input signal, the pulse signal generator configured to drive an on pulse signal line that conducts the on pulse and an off pulse signal line that conducts the off pulse; and

wherein the blocking circuit is configured to:

enable state change of a drive signal to drive a high-side drive transistor based on voltage of the on pulse signal line exceeding a first threshold and voltage of the off pulse signal line not exceeding a second threshold, or voltage of the off pulse signal line exceeding the first threshold and voltage of the on pulse signal line not exceeding the second threshold.

11. The transistor driver of claim 10, wherein the blocking circuit is configured to inhibit generation of the drive signal to the high-side drive transistor based on a difference of the voltage of the on pulse signal line and the voltage of the off pulse signal line being less than a predetermined amount.

12. The transistor driver of claim 11, wherein the blocking circuit is configured to enable generation of the drive signal to the high-side drive transistor based on the

difference of the voltage of the on pulse signal line and the voltage of the off pulse signal line being greater than the predetermined amount.

13. The transistor driver of claim 11, wherein the blocking circuit comprises circuitry configured to inhibit a change in state of the drive signal to the high-side output transistor based on assertion of signals on both the on pulse signal line and the off pulse signal line, or based on negation of signals on both the on pulse signal line and the off pulse signal line.

14. The transistor driver of claim 13, wherein the blocking circuit comprises a first plurality of comparators configured to compare the voltage of the on pulse signal line to the first threshold and compare the voltage of the off pulse signal line to the second threshold.

15. The transistor driver of claim 14, wherein the blocking circuit comprises circuitry configured to assert the drive signal based on the voltage of the on pulse signal line being less than the first threshold and the voltage of the off pulse signal line being greater than the second threshold voltage.

16. The transistor driver of claim 14, wherein the blocking circuit comprises a second plurality of comparators configured to compare the voltage of the on pulse signal line to the second threshold and compare the voltage of the off pulse signal line to the first threshold.

17. The transistor driver of claim 16, wherein the blocking circuit comprises circuitry configured to negate drive to the high-side drive transistor based on the voltage of the on pulse signal line being greater than the first threshold and the voltage of the off pulse signal line being less than the second threshold.

18. The transistor driver of claim 11, wherein the blocking circuit comprises:

a latch set circuit comprising a first plurality of transistors configured to set the drive signal to a first state based on the voltage of the on pulse signal line being below the first threshold and the voltage of the off pulse signal line being above the second threshold; and

a latch reset circuit comprising a second plurality of transistors configured to set the drive signal to a second state based on the voltage of the off pulse signal line being below the first threshold and the voltage of the on pulse signal line being above the second threshold..

19. A level shifter comprising:

an output driver configured to switch a voltage of at least 200 volts, the driver comprising a high-side output transistor;

a pulse generator configured to generate an on pulse at a leading edge of an input signal received at an input terminal of the level shifter and to generate an off pulse at a trailing edge of the input signal; and

a high-side gate driver configured to drive the high-side output transistor, the high-side gate driver coupled to an on pulse signal line that conducts the on pulse and coupled to an off pulse signal line that conducts the off pulse, the high-side gate driver comprising:

a blocking circuit comprising a plurality of transistors configured to inhibit a change in state of a drive signal to the high-side output transistor based on simultaneous assertion of signals on both the on pulse signal line and the off pulse signal line, and based on simultaneous negation of signals on both the on pulse signal line and the off pulse signal line.

20. The level shifter of claim 19, wherein delay in the level shifter from assertion of the input signal to activation of the high side drive transistor is about 30 nanoseconds.

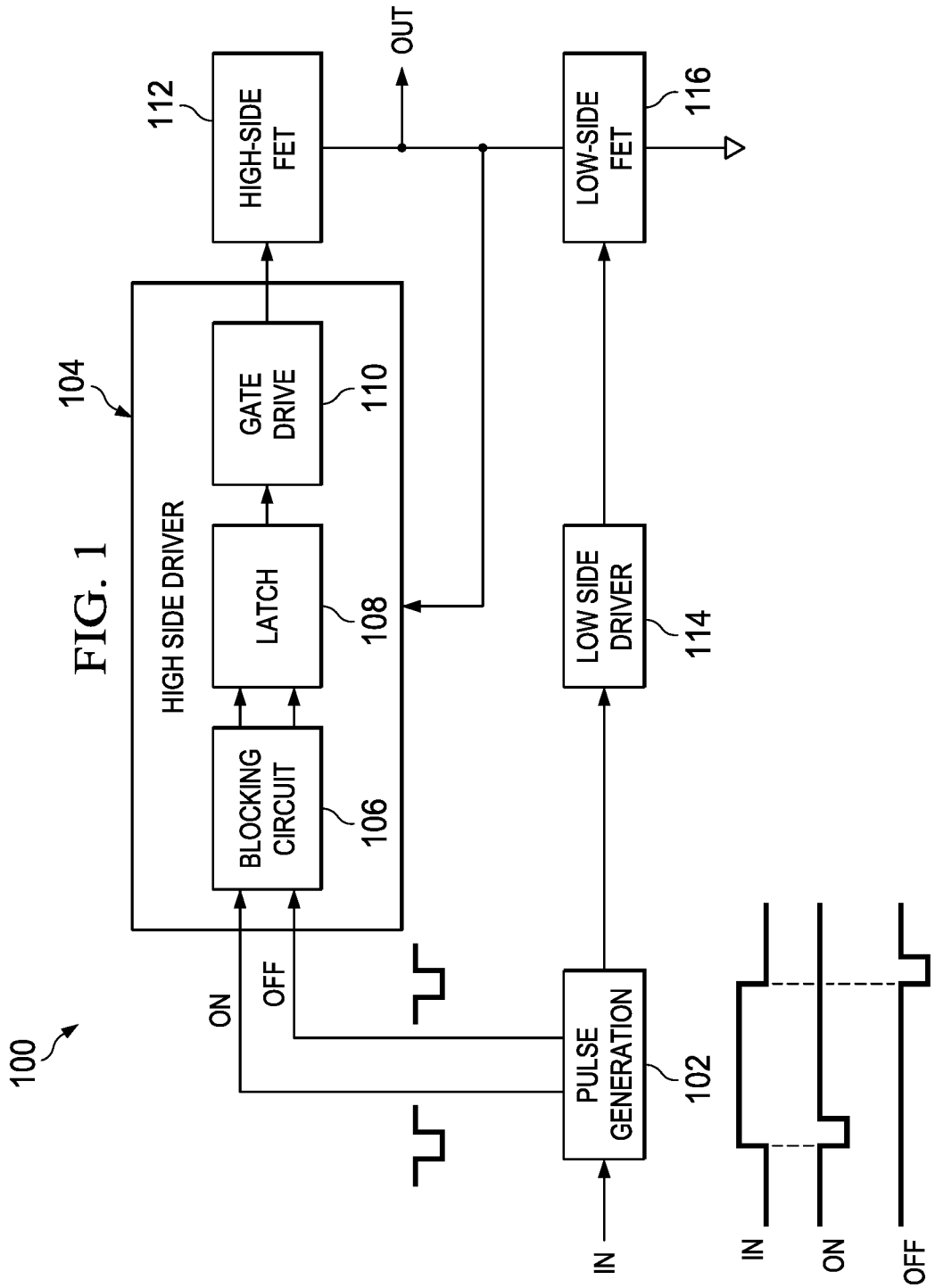

100
ON
OFF
IN
PULSE GENERATION
102
HIGH SIDE DRIVER
104
BLOCKING CIRCUIT
106
LATCH
108
GATE DRIVE
110
HIGH-SIDE FET
112
OUT
LOW SIDE DRIVER
114
LOW-SIDE FET
116
IN
ON
OFF

FIG. 1

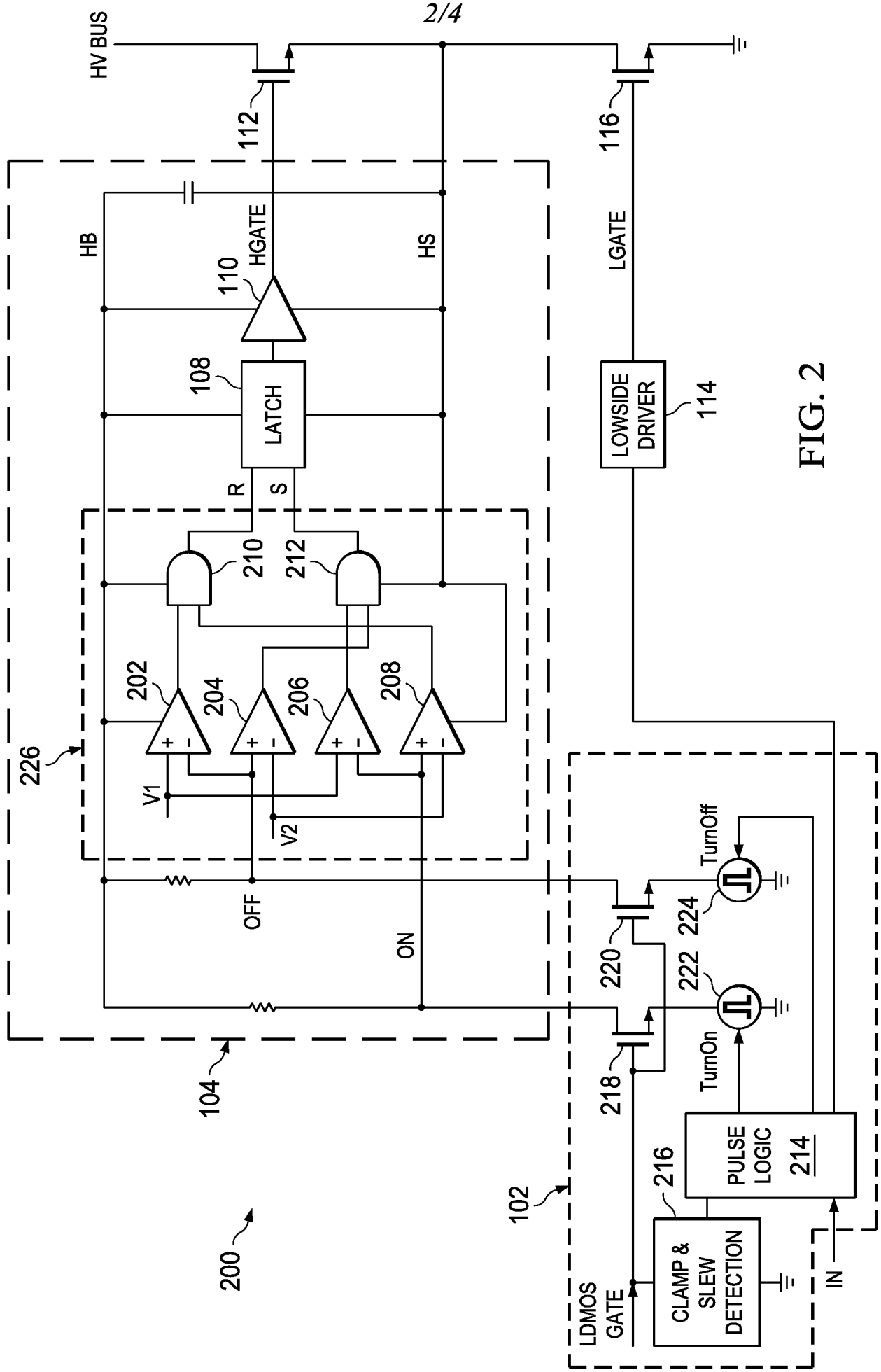

HV BUS
112
116
HB
HGATE
HS
LGATE
110
108
LATCH
LOWSIDE DRIVER
114
R
S
210
212
202
204
206
208
226
V1
V2
OFF
ON
TurnOff
224
220
222
218
TurnOn
104
102
200
216
PULSE LOGIC 214
CLAMP & SLEW DETECTION
LDMOS GATE
IN

FIG. 2

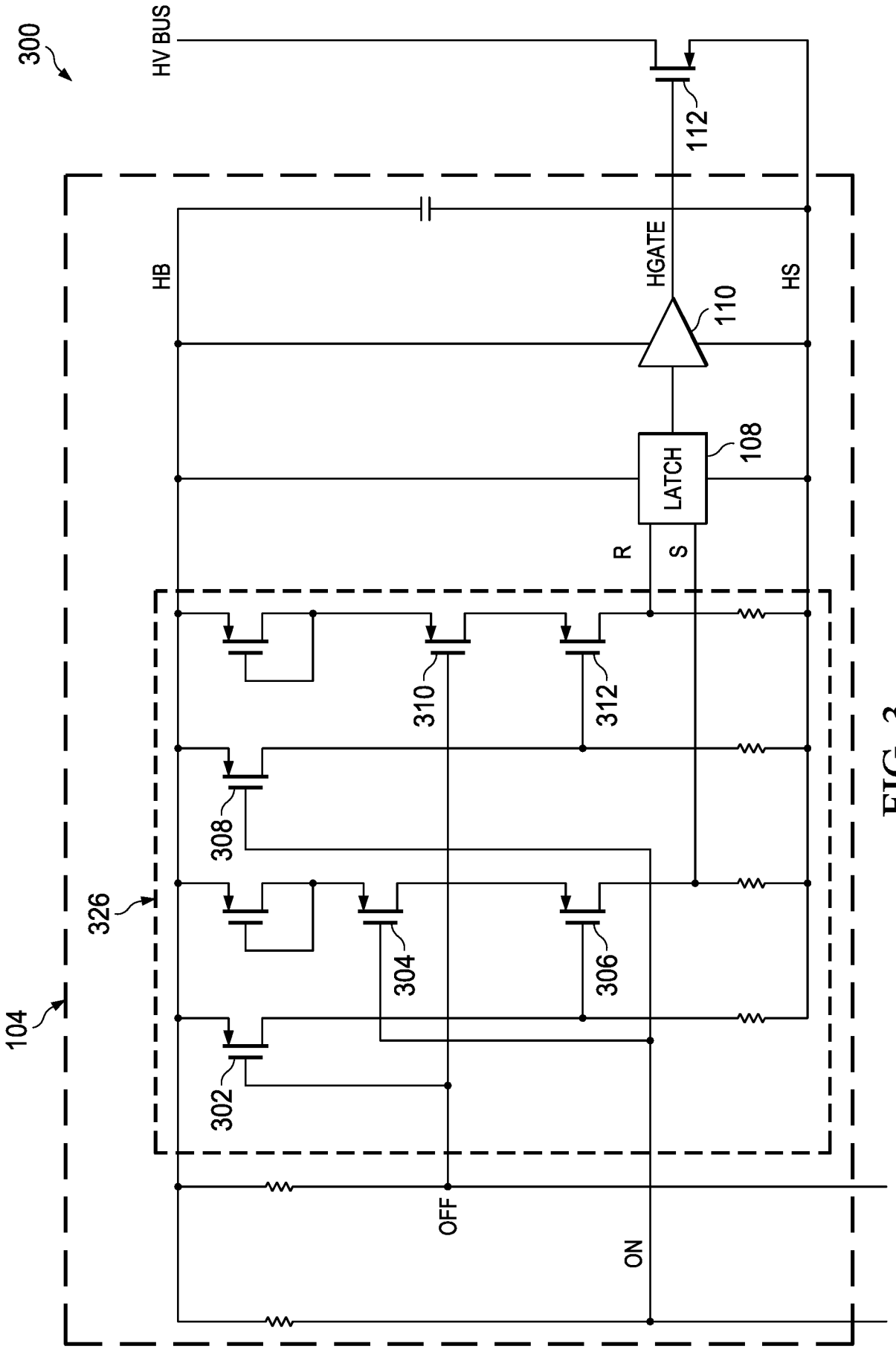

300
HV BUS
112
HB
HGATE
HS
110
LATCH
108
R
S
310
312
308
326
304
306
104
302
OFF
ON

FIG. 3

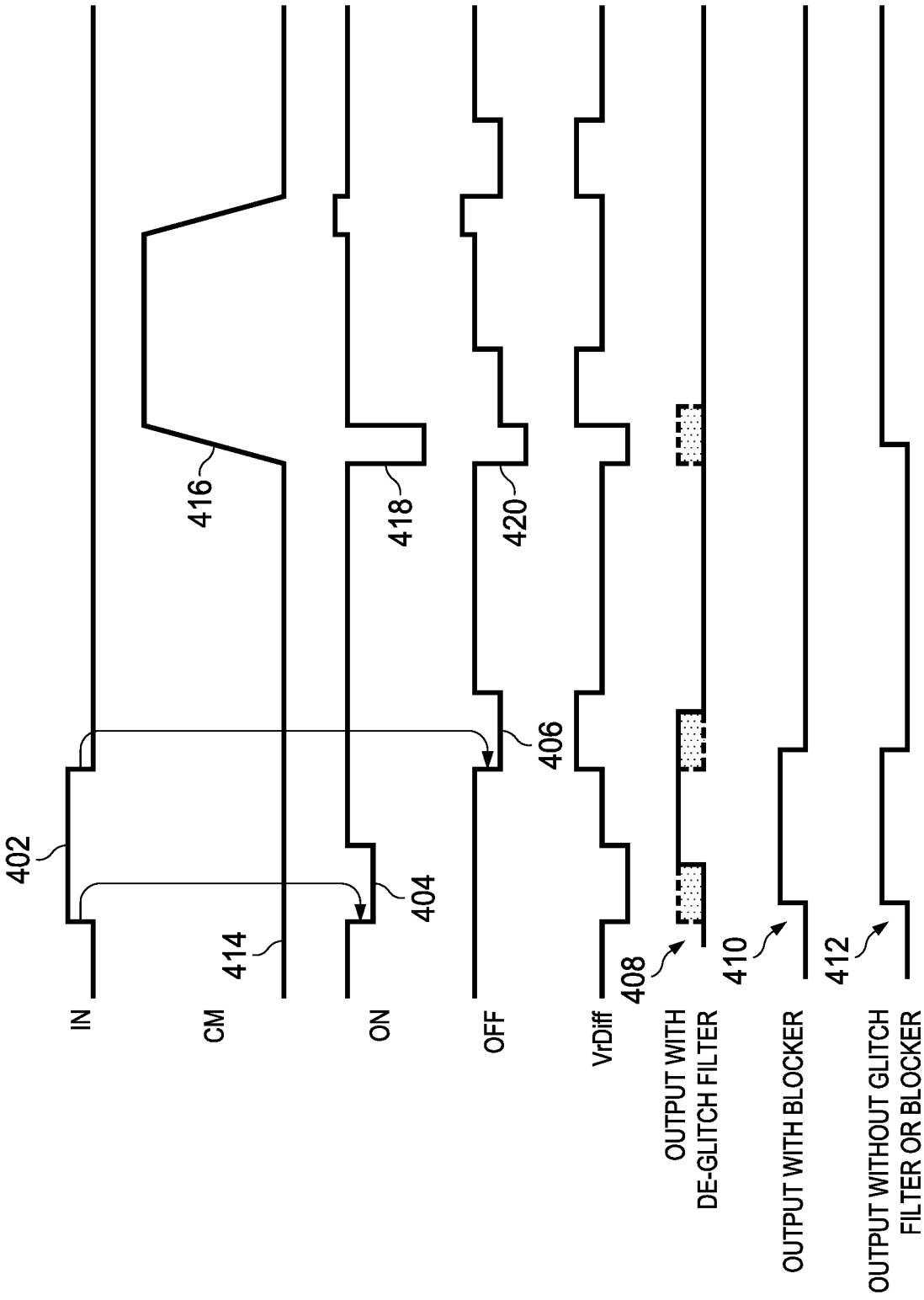

IN
CM
ON
OFF
VrDiff
OUTPUT WITH DE-GLITCH FILTER
OUTPUT WITH BLOCKER
OUTPUT WITHOUT GLITCH FILTER OR BLOCKER
402
404
406
408
410
412
414
416
418
420

FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2016/106443

A. CLASSIFICATION OF SUBJECT MATTER

H03K 19/0185(2006.01)i; H03K 19/0175(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WPI, EPODOC, CNPAT, CNKI: lever shifter, level shifter, driver, pulse, signal, voltage, blocking, compare, detect, on, off, noise

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	CN 101917811 A (XIAN NEW LIGHTING ELECTRONIC TECHNOLOGY CO., LTD.) 15 December 2010 (2010-12-15) description, paragraphs [0022]-[0029] and figures 1-3	1-20
A	CN 103325419 A (LIJING TECHNOLOGY CO., LTD.) 25 September 2013 (2013-09-25) the whole document	1-20
A	CN 103297030 A (NXP BV) 11 September 2013 (2013-09-11) the whole document	1-20
A	US 2010301900 A1 (TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.) 02 December 2010 (2010-12-02) the whole document	1-20

☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
17 July 2017	**27 July 2017**

Name and mailing address of the ISA/CN	Authorized officer
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Facsimile No. **(86-10)62019451**	Telephone No. **(86-10)010-61648502**

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2016/106443

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
CN	101917811	A	15 December 2010	CN	101917811	B	17 April 2013
CN	103325419	A	25 September 2013	JP	5395203	B2	22 January 2014
				US	2013249595	A1	26 September 2013
				CN	103325419	B	17 May 2017
				TW	201340609	A	01 October 2013
				TW	I517579	B	11 January 2016
				US	9076529	B2	07 July 2015
				JP	2013201524	A	03 October 2013
CN	103297030	A	11 September 2013	EP	2634919	A1	04 September 2013
				US	2013222072	A1	29 August 2013
				CN	103297030	B	28 December 2016
US	2010301900	A1	02 December 2010	CN	101908880	A	08 December 2010
				US	8115514	B2	14 February 2012