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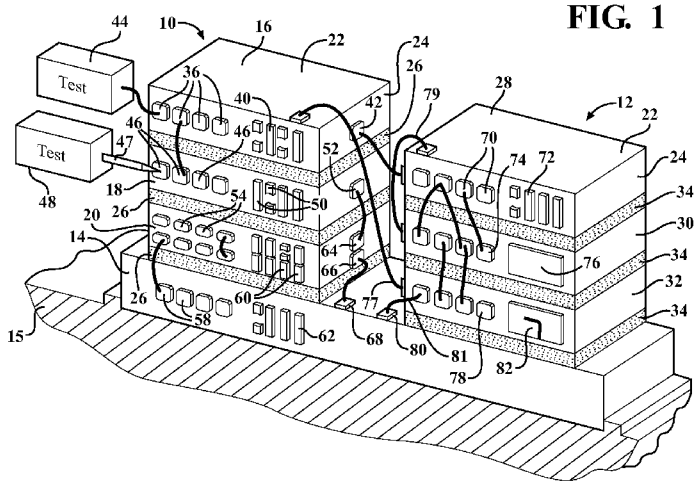
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(54) **Title**: STACKABLE SEMICONDUCTOR CHIP WITH EDGE FEATURES AND METHODS OF FABRICATING AND PROCESSING SAME

FIG. 1




(57) **Abstract**: A method of performing a function on a three-dimensional semiconductor chip package as well as on its individual chips is disclosed. An operative relationship between a function performer and an edge feature on the chip(s) is created. The edge feature is an electrically or thermally conductive pad, a probe pad, a fuse, a resistor, a capacitor, an inductor, an optical emitter, an optical receiver, a test pad, a bond pad, a contact pin, a heat dissipator, an alignment marker and/or a metrology feature. A function performer is a test probe, laser, programming device, interrogation device, loading device and/or tuning device. A chip with edge features is also disclosed, along with a three-dimensional stack of such chips in either of several different configurations. The formation of edge features, singulation of dice having incipient edge features, and stacking and handling of dice with edge features are described.

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# STACKABLE SEMICONDUCTOR CHIP WITH EDGE FEATURES AND METHODS OF FABRICATING AND PROCESSING SAME

## TECHNICAL FIELD

[0001] This disclosure relates to semiconductor chips and more particularly to the fabrication and processing of a stackable semiconductor chip having edge features that facilitate or provide access to circuitry on or in the chip.

## BACKGROUND

[0002] Three-dimensional conductor chip packages comprising a stack of thin semiconductor chips are now being manufactured. The chips in these packages often contain controllers, memories, sensors, analog components, processors and specialty communications components as well as Micro-Electro-Mechanical Systems (MEMS) devices. The cost of these relatively dense, integrated packages is high, so quality control and testing as part of the fabrication, so quality control and testing as part of the fabrication process is all the more important.

[0003] Functions such as testing, trimming, bonding and tuning are typically carried out by accessing the primary surfaces of the semiconductor chips, usually a planar top surface. The accessing step may require bringing, for example, a probe into actual contact with a feature such as a pad or trace on the surface. This becomes complicated or impossible when the primary surfaces of the interior chips are no longer accessible as a result of having been integrated into a stack.

## BRIEF SUMMARY

[0004] In accordance with an aspect of the invention, a method is provided for performing one or more functions on a semiconductor chip that is part of a stack of semiconductor chips without the necessity of contacting or otherwise addressing a top surface feature. This is achieved by providing one or more access features on a chip edge surface and, where necessary, connecting the edge feature or features to a circuit or component carried by the chip. These edge surface features remain accessible after chip stacking.

[0005] In accordance with this aspect, the function which is performed may consist of one or more of testing, altering, repairing, programming, interrogating, loading and tuning as well as bonding one or more conductors into a functional relationship with a circuit or component on the chip.

[0006] In addition, the edge feature may consist of one or more of an electrical conductor, a thermal conductor, a fuse, a resistor, a capacitor, an inductor, an optical emitter, an optical receiver, a test pad, a bond pad, a contact pin, a heat dissipation device, multiples of these and combinations of these.

[0007] In a variation of this aspect, the signal conduit may consist of one or more of an electrical conductor such as a trace or a via, a heat conductor, an optical conductor, multiples of these and combinations of these.

[0008] The method can also comprise the steps of locating the stack containing the semiconductor chip to be processed by way of an edge feature on a fixture wherein the edge feature can be addressed by a function performer and thereafter activating the function performer to address the edge feature. As used herein, a "chip" is a physical object with top and bottom primary surfaces, and one or more peripheral edge surface, the actual number of such edge surfaces being determined by chip geometry.

[0009] The functions of addressing and activating may involve actual physical contact between the function performer and the edge feature but it may also be carried out in a non-contacting way particularly where the edge feature associated with the peripheral edge surface is an optical device or is recessed or buried beneath a surface of material that is transparent to the output of the function performer. The function performer may be one or more of a test probe, a wire bonder, a laser, a programmer contact, a trimmer, a data transfer contact and/or an optical transmitter or receiver and/or multiples or combinations of these elements.

[0010] In accordance with a second aspect of the invention, a stackable semiconductor chip is provided wherein the chip comprises a primary surface and has one or more devices as described above associated with it. This primary surface, although exposed when the die which makes up the semiconductor chip is fabricated both before and after singulation, is no longer exposed once the chip has been integrated into the three-dimensional stack. Accordingly, the die is further provided with an edge feature as well as a signal conduit between the edge feature and the primary surface device and/or devices so that the edge feature can be used in a process as set forth above. This aspect of the invention extends to multiple chips bonded together in a stacked combination.

[0011] In accordance with a third aspect of the invention, a method of fabricating stackable semiconductor chips is provided wherein the fabrication process or method results in chips which can be processed in any of various ways by access to edge surface features after the chips have been integrated into a three-dimensional stack. As hereinafter described in detail, this process may involve the formation of layered integrated circuits in large two-dimensional arrays having what, after singulation, become edge features. During a singulation step, the buried edge features are exposed thus to provide access to a circuit or component integrated into the chips in the primary fabrication process even though the chips are assembled into a three-dimensional package of stacked chips which eliminates access to some or all of the primary surface devices in the stack.

[0012] As used herein, the terms "chip" and "die" are synonymous.

## BRIEF SUMMARY OF THE DRAWINGS

[0013] The description herein makes reference to the accompanying drawings wherein like reference numerals refer to like parts throughout the several views and wherein:

[0014] FIG. 1 is a perspective view of a pair of stacked semiconductor chips loaded on a common foundation chip embodying one or more aspects of the invention;

[0015] FIG. 2 is a perspective view of an alternative arrangement of stacked semiconductor chips on a foundation chip that is fixtured for alignment with a test probe;

[0016] FIG. 3 is a side view of still another semiconductor chip stack embodying one or more aspects of the invention;

[0017] FIG. 4 is a partial side view of a section of a semiconductor chip illustrating various arrangements of edge surface features;

[0018] FIG. 5 is a plan view of two semiconductor chips post-singulation but before stacking;

[0019] FIG. 6 is a plan view of a singulated die or chip having few structures or pads as edge features;

[0020] FIG. 6A is a side view of the device of FIG. 6;

[0021] FIG. 7 is a side view of another chip stack illustrating another way to utilize edge features in the form of bonding pads;

[0022] FIG. 8 is a side view of another chip stack showing a way to perform functions thereon;

[0023] FIG. 9 is a plan view of two singulated chips in contact with one another; and

[0024] FIG. 10 is a side view of the device of FIG. 9.

## DETAILED DESCRIPTION

[0025] When semiconductor chips are bonded together in stacks, the primary surfaces of chips low in the stack are covered up. Therefore, access to features or devices on or associated with the primary surfaces is no longer possible for such functions as testing or wire bonding, or trimming or tuning or configuration change, redundancy, repair and/or encoding or programming. In accordance with embodiments of the invention, these and other functions are carried out by way of features that have been located in such a way as to be associated with one or more of the peripheral edge surfaces of the chips or dice. Thus, a die or chip that is fabricated in accordance with the teachings herein includes one or more edge features that facilitate or enable testing, wiring, repair, reconfiguration, tuning or processing despite the fact that the chip or die has been incorporated into a three-dimensional stack. Also disclosed herein are systems and devices to test, wire bond or otherwise process features on the edges of chips or dice in a stacked array. Also described herein is a method of performing processes on componentry or devices in stacked semiconductor dice, despite the fact that the primary surfaces with which the components or devices are associated are no longer accessible to conventional equipment.

[0026] Referring to FIG. 1, there is shown a pair of three-dimensional semiconductor chip stacks 10, 12 bonded in side-by-side relationship to a semiconductor foundation chip 14. Chip stack 10 comprises semiconductor chips 16, 18 and 20, each of which exhibits planar top and bottom primary surfaces 22 as well as peripheral edge surfaces 24. In this case, because semiconductor chips 16, 18, 20 are essentially rectangular, they each have four peripheral edge surfaces 24. The peripheral edge surface(s) can vary from one to any number depending on geometry. Chips 16, 18, 20 are adhered to one another and to foundation chip 14 by bonding material 26 between primary surfaces 22. As hereinafter described, each of chips 16, 18, 20 is presumed to carry a device or component that is associated with or exposed to one or both of primary surfaces 22. As is apparent from an inspection of FIG. 1, some of those devices or components become inaccessible as a result of the three-dimensional stacking.

[0027] Chip stack 12 comprises semiconductor chips 28, 30 and 32 also bonded to one another as well as to a primary surface of foundation chip 14 by bonding material 34.

[0028] The choice of three chips in each of stacks 10, 12 is arbitrary as the number may vary from two to any practical number as will be apparent to persons skilled in semiconductor fabrication technology.

[0029] Chip 16 exhibits edge features, which in this case are contact pads 36 for testing or wire bonding on the surface closest to the viewer in FIG. 1 as well as alterable edge laser fuses 40. Chip 16 is also provided with a bonding pad 42 on right hand peripheral surface 24 as shown in FIG. 1 for purposes of wire bonding. A test circuit 44 is shown wire bonded to one of pads 36 on top chip 16 of stack 10. In addition, fuses 40 are shown in two different conditions; i.e., some are broken or open-circuited and others remain intact.

[0030] Chip 18 is provided on its forward peripheral edge surface with bonding or probe contact pads 46 as well as laser alterable fuses 50, the former being shown while accessed by a probe 47 that is part of a circuit test device 48. In FIG. 1, foundation chip 14 has been appropriately fixtured at support 15 so as to permit pad 46 to be accurately addressed, in this case "contacted", by the function performer, in this case circuit test device 48.

[0031] Chip 20 is provided with electrically conductive pads 54 and fuses 60 on its foremost peripheral edge surface as well as pads 64, 66 on its right hand peripheral edge surface. The former are used for wire bonding purposes to create conductive interconnections between chips in stack 10 as well as between chip 20 and foundation chip 14, the latter having bonding pads 58 associated with the foremost peripheral surface along with fuses 62. Pads 52, 64 are shown wire bonded together, and pad 66 is shown wire bonded to a pad 68 on foundation chip 14. These uses and interconnections are illustrative rather than limiting.

[0032] Referring to stack 12, the foremost peripheral edge surface 24 of chip 28 is provided with conductive pads 70 as well as laser-alterable fuses 72. The foremost peripheral edge surface 24 of chip 30 is provided with conductive pads 74 and a trimmable structure 76. The foremost peripheral edge surface 24 of chip 32 is provided with pads 78 and a trimmable structure such as resistive film 82. As shown, wire bonding between the pads of the stacked chips is achievable despite the lack of access to the primary surfaces. Wires such as 77, 79 can be connected between chip stacks 10, 12 as well as between two chips in a single stack 10 or 12, and wire 81 can be connected

between one of pads 78 on lowermost chip 32 of chip stack 12 to a pad 80 on a primary surface of foundation chip 14.

[0033] Thus, FIG. 1 illustrates four different kinds of edge features; namely a wire bonding or conductive pad, a probe contact pad, a fuse and a trimmable feature such as a resistive film. In addition, FIG. 1 illustrates the fact that the edge features may be utilized not only for testing purposes but also to create interconnections between chips in the stack as well chips in two adjacent stacks.

[0034] Referring now to FIG. 2, an additional design capability is illustrated, in this case by showing a four-high chip stack 84 adjacent to a three-high chip stack 86, both stacks being bonded to a foundation chip 88 that is fixtured at support 87. Chip stack 84 comprises chips 90, 92, 94, 96, all of which are understood to carry circuit devices such as one or more of the devices described above in association with the primary surfaces, at least one of which in the case of each chip is no longer accessible by reason of the assembly of the chips into stack 84 and the application of bonding material 98 to such primary surfaces. Top chip 90 has edge features such as conductive pads 100 as well as a primary surface features 108 that are possible because the top primary surface and a portion of the bottom primary surface of chip 90 remain exposed. Chip 92, on the other hand, has only edge features, in this case in the form of pads 102, 111 that can be used for testing or wire bonding purposes as shown. Chip 92 also has fuses 103 as an additional edge feature.

[0035] Chip 94 has pads 104 as edge features, such pads being used in association with probe 47 of circuit test device 48 also shown in FIG. 1. Thus, the assembly of FIG. 2 has been properly fixtured at support 87 so as to align pads 104 in such a way as to be addressable; i.e., in this case, contacted by probe 47 at the appropriate time when data is to be gathered and processed. Data may be gathered and processed for various purposes; e.g., for quality control or for alteration to achieve predetermined parametric goals. Chip 94 also has fuses as edge features.

[0036] Chip 96 is provided with edge features in the form of fuses and pads 106, which in this case are used for wire bonding. In this case, for example, FIG. 2 shows wires running between pads 106 on the peripheral edge of chip 96 and similar pads 107 on the edge of foundation chip 88 as well as at least one wire running between pads 106 on the same chip 96.

[0037] Stack 86 of FIG. 2 is identical to stack 12 in FIG. 1 so its description is not repeated here.

[0038] One purpose in illustrating the arrangement of FIG. 2 is to show that the invention is useful not only in stacked semiconductors packages wherein all of the chips are geometrically similar in shape and size so as to fully overlap and overlie one another but also in stack arrangements wherein the chips are of different sizes and/or shapes, thereby providing a stair step effect such that both primary and edge surface features can be utilized albeit to a lesser degree.

[0039] Referring to FIG. 3, there is shown another arrangement of stacked semiconductor chips, in this case comprising semiconductor chip stacks 110, 112 located adjacent to one another and bonded to a semiconductor foundation chip 114. Chip stack 110 comprises semiconductor chips 116, 118, which are essentially identical in size and geometry joined together by bonding material 119. As discussed with reference to FIGS. 1 and 2, chips 116, 118 have peripheral edge surface features, one or which is an optical transmitter 124. The other edge features are shown for purpose of illustration as probe, contact, or wire bonding pads as well as fuses so that the semiconductor chips can be interconnected among themselves as well as between themselves and foundation chip 114.

[0040] Chip stack 112 comprises chips 120, 122 having edge features that in this case include an optical receiver 126 on the left peripheral edge surface of chip 120. Chips 116, 120 are aligned with one another in the stacked direction as well as being arranged in an adjacent position so that optical transmitter 124 is aimed essentially at optical receiver 126 for data communication therebetween. This illustrates the fact that the operative association between edge features on the same or adjacent chips may be non-contacting.

[0041] FIG. 4 illustrates still another variation of aspects of the invention. In FIG. 4, reference numeral 128 denotes dielectric material in any one of the chips illustrated in FIGS. 1 through 3, the material having an exposed peripheral edge surface 129. In this case, a first edge feature in the form of a pad 130 is shown protruding above surface 129 whereas the second edge feature in the form of a pad 132 is shown flush with surface 129. Still a third edge feature in the form of a pad 134 is shown recessed relative to surface 129 but still exposed for contact or wire bonding or other processing purposes. Finally, a pad 136 is shown as a subsurface feature; i.e., below surface 129 but yet accessible for processing purposes by reason of the fact that dielectric material 128 is transparent to whatever function is to be performed by way of access to pad 136. Capacitive, inductive and optical couplings are examples.

[0042] FIG. 4 illustrates still another aspect that is common to the certain article and processing embodiments disclosed herein and that is the use of signal conduits 138 between the edge features, in this case pads 130, 132, 134, 136 and the device or devices associated with the chip that comprises dielectric material 128; i.e., the purpose of the edge surface feature is to provide access to the device associated with the chip and the outside world, and thus signal conduits 138 are used. They may take the form of traces or other forms of electrical conductors, thermal conductors for optical conductors, etc. However, there are instances where no such signal conduits are needed; e.g., where the edge features are alignment marks or metrology features. To catalog the edge features, they may be:

a) pads designed for contact for the probe for electrical testing;

b) pads designed for wire bonding;

c) solder bumps or terminations for electrical contacts through physical contact, solder reflow or solder reflowing;

d) protruding pins for electrical contact purposes;

e) vias that may carry information from one die through to another die;

f) structures such as fuses for redundancy repair, digital repair, encoding of information, circuit reconfiguration, encoding identification parameters, implementing and security encoding, serialization, etc.;

g) trim pads for altering impedance or tuning the value of a circuit element such as a resistor, capacitor, inductor, oscillator and/or other circuit elements;

h) optical devices or optical interface devices such as transmitters; e.g., lasers or LEDs; and/or receivers;

i) alignment marks and metrology features; and/or

j) heat dissipation features such as thermally conductive pads or heat pipes.

[0043] Accordingly, one stacked die may optically transmit information to another nearby die without the need for wiring as illustrated by example in FIG. 3.

[0044] Subsurface feature or pad 136 illustrated in FIG. 4 may, for example, be a metal or phase change fuse that is embedded beneath the surface of dielectric material 128 but alterable through delivery of a laser beam. The wavelength of the light from the

laser can be selected such that the die material is transparent to it; for example, a wavelength of 1.3μm can be used with silicon. Internal trim pads are also possible.

[0045] Signal conduits 138, when used, may be created with vias or vertical aluminum copper or tungsten structures and may also be made with traditional lithography techniques, deep-reactive ion etching followed by refill or by laser formation followed by refill.

[0046] FIG. 5 shows a layout of two dice 150, 152 wherein the signal conduits are metal traces 154 and the edge features are shown as cylindrical vias 156. In this case, traces 154 interconnect edge feature vias 156 to respective circuitry 158, 160 on adjacent dice 150, 152. Dice 150, 152 shown in FIG. 5 have not yet been singulated; i.e., they are all part of a larger array fabricated in a field of material (here, wafer 162) containing many such chips or dice of similar design. The solid lines illustrate where the edge surfaces of the die surfaces will lie after singulation.

[0047] In describing the methodology herein, wafer 162 referred to above in connection with FIG. 5 contains dice 150, 152 and other dice to be singulated with edge features here in the form of cylindrical vias 156 that are to be exposed during singulation. Wafer 162 is then processed by sawing or laser cutting and/or a combination of sawing, cutting and/or routing to define and expose the edge features, in this case vias 156, as shown for die 150 in FIGS. 6 and 6A. Edge vias 156 are now fully exposed so as to be available for processing as described.

[0048] As will be apparent to those skilled in the art, singulation can be performed by straight cuts made by way of straight cuts with a traditional saw. Alternatively, a laser can be used to make non-straight cuts to expose the edge features that are flush with the cut surface. Non-straight singulation with a laser can also be used to rout out protruding edge features or those which are slightly recessed as shown by pad 134 in FIG. 4. Saw cutting followed by laser routing can also be used. Lasers can also be used to make slots or slices or trim lines to expose edge features.

[0049] Another way to expose an edge feature is to perform singulation by sawing laser cuttings or scribing or braking followed by an etching that can remove dielectric material 128 surrounding the features. One preferred etch is a selected etch performed with a chemical such as $XeF_2$ that removes silicon at a much higher rate than metal features.

[0050] Additional structures can be added to etch features after singulation with optional edge exposure. For example, edge features can be plated, passivated, soldered or

reconfigured for mechanical mating. Features can be reformed and reflowed through heating, laser, chemical or mechanical alteration. Edge features can also be added with adhesives. All of these steps can be performed before or after stacking the dice.

[0051] Referring now to FIG. 7, the disclosure turns to the discussion of stacking techniques. A die with edge features as described above can be stacked on another die or chip by picking up the die with a die-attach film already on the lower or upper surface and stacking it with or to another die in either aligned or stair step fashion as described above. The die-attach film is then cured by, for example, exposure to ultraviolet light. Similarly, an adhesive may be applied to the dies without a die-attach film and cured in the stacking process. With respect to dice or chips with edge features, care must be taken during the stacking process not to obscure or damage the edge feature with, for example, bonding materials. Contaminating the edge feature should be avoided and any contamination should be removed using an appropriate technique, such as cleaning, polishing, etching or dissolving. Laser cleaning and debris removal may also be used. Dice or chips with edge features may require alignment during the stacking and bonding process such that the edge features are properly oriented. This is preferably carried out using mechanical positioning as shown in FIGS. 1 and 2 so that the dice are in the intended locations to access edge features for additional processing steps such as wire bonding, testing or laser processing. Edge features may also require alignment to facilitate electrical connections or optical communication as described above with respect to FIGS. 1-3.

[0052] FIG. 7 illustrates another possibility in edge alignment by crimping one die 170 on top of another die 172 where edge connectors 176 already in place mate with edge pads 178 on lower die 172. This crimping process may also be carried out with bonding using either a die-attach film or adhesive. The electrical connections can be conductors that can be crimped together or formed using soldering or wire bonding techniques.

[0053] Bare die and stacked dice with edge features will often require automated handling techniques and these techniques should be selected so as not to damage the edge features. Handling techniques may include such devices as mechanical grippers, vacuum grippers or temporary adhesion onto a carrier plate. Grippers can be designed to allow testing access or to contain an appropriate testing interface.

[0054] Testing or other edge function performance steps can be carried out on individual chips as well as on partial or complete stacks of chips. FIG. 8 shows a single die 180 having a primary surface 182 and four edge surfaces 184. All of edge surfaces

184 have edge features. By way of example, pads 186 are provided on the left peripheral edge surface 184 for access by probes 188 as part of test circuitry 190. Pads 192 are provided on another edge surface 184 for wire bonding purposes. Features 194 are provided on another edge surface 184 and are configured in such a way as to be repairable by a focused laser beam 196. Finally, optical communication devices 198, 200 are provided on another edge surface for appropriate communication with complementary optical communication devices 202, 204 on a laterally-arranged adjacent structure 206. Accordingly, multiple functions can be performed at the same time on a given die.

[0055] The discussion now turns to methods for aligning edges of chips with the edges of other chips as well as to collateral devices. It is necessary to align edge features in order to process them with laser beams, to contact them with electrical probes to perform wire bonding, to optically communicate or to otherwise interact with an edge feature. Alignment may be accomplished by aligning to the physical edges of a die, aligning to features fabricated on the edges of the due, such as bonding, pads or fuses, dedicated alignment features such as targets or fiducials that are located on the edges of the dies, aligning to structures or features located on the bottom primary surfaces of the die or aligning to other or nearby collateral structures. Alignment can be verified and modified during the alignment procedure. For example, electrical conductivity or circuit impedance can be tested and a position adjustment can be made to correct alignment. Alignment may involve determining the relative location of two different dice, thereafter the relative location of die or die features may be used to facilitate proper interfacing such as wire bonding between the two dice.

[0056] Alignment may involve using cameras or optical scans or laser scans to determine feature locations. Machine vision and vision analysis techniques can be employed. The locations of multiple dice may be determined from a single image. It may be necessary to assess and perform alignment differently on different sides of a die containing edge features. Die alignment may be optimized by assessing different sides of a die and the edge features on such dies are oriented, FIG. 8 being an example of a die with different edge features on the various peripheral edge surfaces. An optimal placement can be determined based upon the requirements of the die edges or features on the different edges.

[0057] FIG. 9 introduces the subject of how to produce edge vias and interconnect between die features.

[0058] Interconnect involving edge features may involve wire bonding of an edge feature to any other feature located on an edge, on a primary surface or on another nearby die circuit board, package conductor, foundation chip or test probe. Interconnect may be between features on a die that are stacked and/or laterally arranged.

[0059] As shown in FIG. 9, the edge features of two different dies 210, 212 can be brought into direct contact with one another. In FIG. 9, the edge features of dies 210, 212 located along facing edge surfaces 214, 216 have been brought into contact with one another at contact area 218. This contact area 218 may provide communication between two dice that are located on top of one another as well as beside one another. The edge features on a center die such as die 220 shown in FIG. 10 may function as vias to transmit signals around center die 220 so that lower die 222 can communicate with upper die 224 by way of vias 226 without communicating with center die 220 if that is desired.

[0060] Testing of edge structures may occur before or after stacking. Parametric tests and functional tests can be done to verify that the dice were properly fabricated. Tests may be used to sort and distribute components into bins. Following tests, additional tuning, trimming, reconfiguration, repair, serialization or identification can be performed on edge structures.

[0061] Testing, tuning and trimming and repairing with edge structures can be also used to determine and/or correct for changes and defects during the packaging process. For example, it may be required to tune the electrical impedance to properly mate one die to a different die. Packaging effects can be mitigated using edge tests or alterations.

[0062] Some of the testing, trimming and tuning can be based on properties in the die that are measured before they are stacked. Testing during a die stacking may reveal that the die is cracked or has undergone irreparable damage during handling. Such a die can be removed and replaced with an undamaged substitute. Alternatively, this stack of dice can be discarded before any additional undamaged dies are added by bonding or otherwise. Testing with edge structures can also be used as part of a reliability test, a burn-in and/or during final testing of stacked dies.

[0063] FIGS. 1 and 2 illustrate in schematic terms what is needed to perform some types of testing. A fixture adapted to receive dice of a certain configuration and of a predetermined edge feature type is provided. That fixture automatically aligns dice of appropriate geometry and edge configuration arrangement with function performing devices such as test probes so that the function performing devices properly address the

edge features in space. Thereafter, the function performing devices can be activated; i.e., advanced into contact or into near proximity or simply turned on as necessary to produce a functional relationship with the edge feature being addressed. Data can be collected as necessary and decisions made regarding the viability, operability and/or alteration made in or to the edge feature.

[0064] It will be appreciated that the embodiments illustrated in the drawing and described above are exemplary and that implementation of the invention can be carried out in various other configurations. That is, the above described embodiments have been described in order to allow easy understanding of the present invention, and do not limit the present invention. On the contrary, the invention is intended to cover various modifications and equivalent arrangements included within the spirit and scope of the appended claims, which scope is to be accorded the broadest interpretation so as to encompass all such modifications and equivalent structures as is permitted under the law.

What is claimed is:

1. A method of performing a function on a semiconductor chip that is part of a stack of semiconductor chips wherein said chip has a primary surface and one or more peripheral edge surfaces, a device associated with the primary surface and an edge feature associated with the edge surface wherein:

the function consists of one or more of testing, altering, repairing, programming, interrogating, loading, tuning and data exchange;

the device consists of one or more of a circuit, circuit component, memory and controller;

the edge feature consists of one or more of an electrical conductor, a thermal conductor, a fuse, a resistor, a capacitor, an inductor, an optical emitter, an optical receiver, a test pad, a bond pad, a contact pin, a heat dissipator, alignment marks, and metrology features;

wherein the method comprises the steps of:

(a) locating the stack such that the edge feature can be accessed by a function performer; and

(b) activating the function performer to access the device via the edge feature.

2. The method of claim 1 wherein the function performer is a test probe.

3. The method of claim 1 wherein the function performer is a wire bonder.

4. The method of claim 1 wherein the function performer is a laser.

5. The method of claim 1 wherein the function performer is a programmer contact.

6. The method of claim 1 wherein the function performer is a trimmer.

7. The method of claim 1 wherein the function performer is a data transfer contact.

8. The method of claim 1 wherein the function performer is an optical transmitter.

9. The method defined in claim 1 wherein the chip is also provided with a signal conduit connecting the device to the edge feature.

10. The method of claim 9 wherein the signal conduit is one or more of an electrical conductor, a thermal conductor and/or an optical conductor.

11. A method of testing an integrated circuit chip of the type comprising a dielectric body carrying at least one circuit device, said chip having a primary surface and at least one peripheral edge surface, at least one probe pad associated with said peripheral edge surface and electrically connected to the circuit device comprising the steps of:

bringing a test probe into contact with the test pad; and

generating data derived from the contact of the test probe with the test pad.

12. A method of tuning or otherwise altering circuitry on an integrated circuit chip of the type comprising a dielectric body having a primary surface and at least one peripheral edge surface, said circuitry being at least associated with said primary surface, said chip further having an alterable circuit component on said edge surface and connected by a signal conduit to the circuitry comprising the steps of:

mounting the integrated circuit in a fixture such that an external device can address the component; and

operating the external device to alter the component on the peripheral edge surface.

13. A three-dimensional semiconductor device comprising:

first and second stacked integrated circuit chips, each said chip comprising a body of dielectric material having a primary surface and at least one peripheral edge surface, at least one of the chips having circuitry disposed on a primary surface which is

overlaid by a primary surface of the other chip in the stack, at least one said chip having a conductor test pad disposed on the peripheral edge surface of the chip and electrically connected to the circuitry on the primary surface of the chip;

whereby the circuitry on at least said one chip can be tested by means of a test probe contacting the test pad.

14. A method of fabricating an integrated circuit chip which is adapted to be stacked with other similar integrated circuit chips in a three-dimensional array and tested while in the stacked array comprising the steps of:

(a) forming circuitry on or in the chip;

(b) placing a test pad on a peripheral edge surface of the chip, and

(c) electrically connecting the test pad to the circuitry on or in the chip.

15. A method of fabricating a three-dimensional semiconductor chip stack comprising a plurality of individual semiconductor dice comprising the steps of:

constructing a two-dimensional array of semiconductor dice in a dielectric field material wherein each die has an exposed primary surface, a device associated with said primary surface, at least one buried edge feature and a signal conduit interconnecting the device with the buried edge feature;

singulating the dice to create peripheral edge surfaces and expose said buried edge features; and

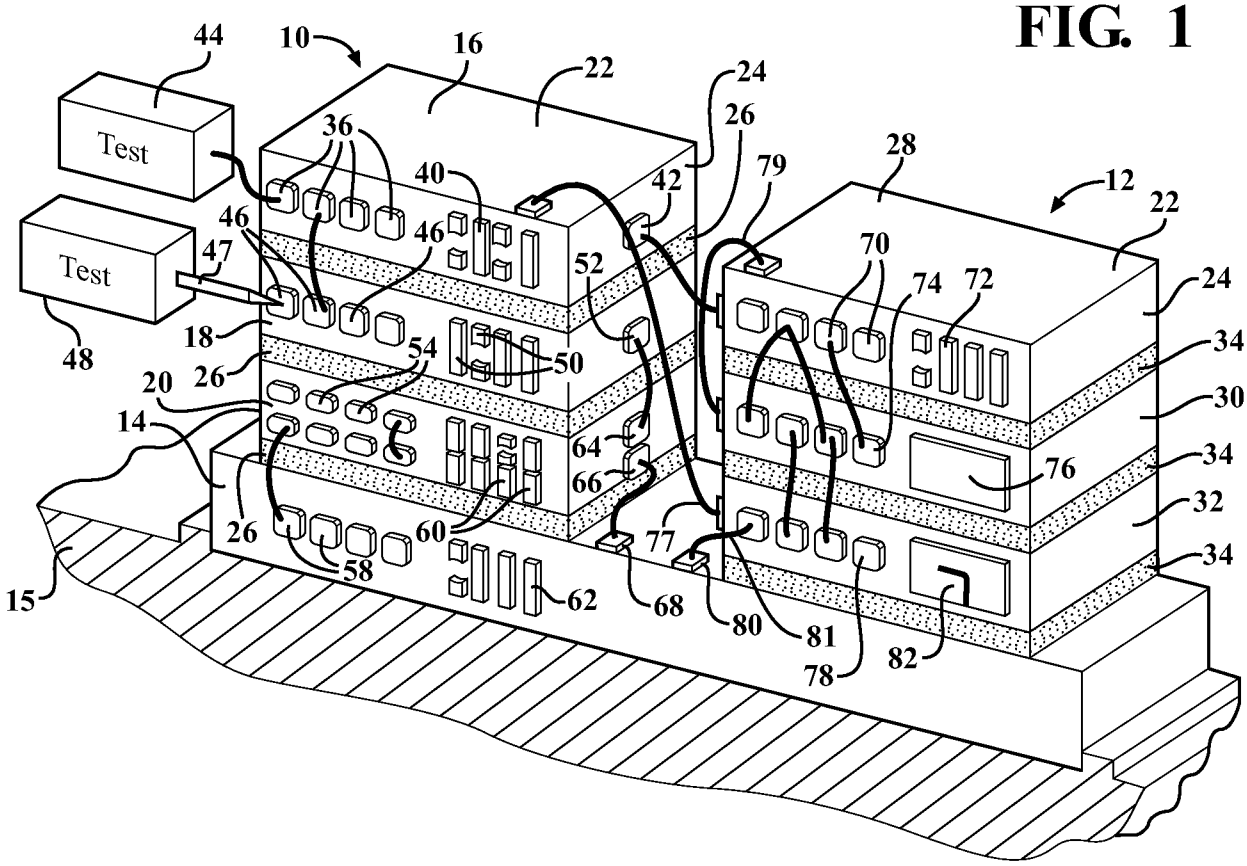
combining dice in a stack so as to de-expose at least some primary surfaces.

16. A method of testing a device on an integrated circuit chip located in a stack of semiconductor chips wherein each chip has a primary mounting surface for one or more integrated circuit devices, at least one peripheral edge surface intersecting the primary surface, and a test probe contact pad on the edge surface and electrically connected to the device on the primary surface, said method comprising the steps of:

placing the stack on a test fixture so as to align the pad with a test probe; and

causing the test probe to come into contact with the pad.

FIG. 1


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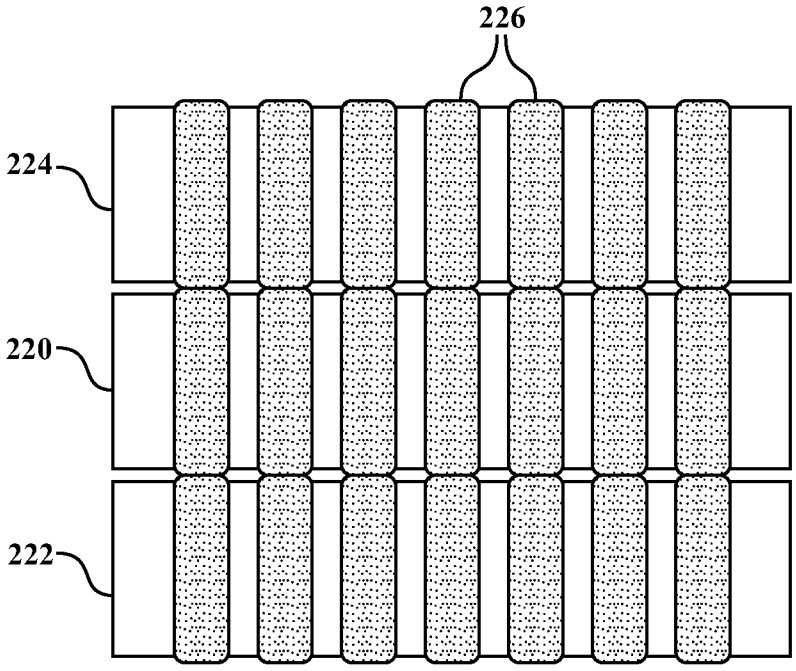

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FIG. 10

FIG. 2

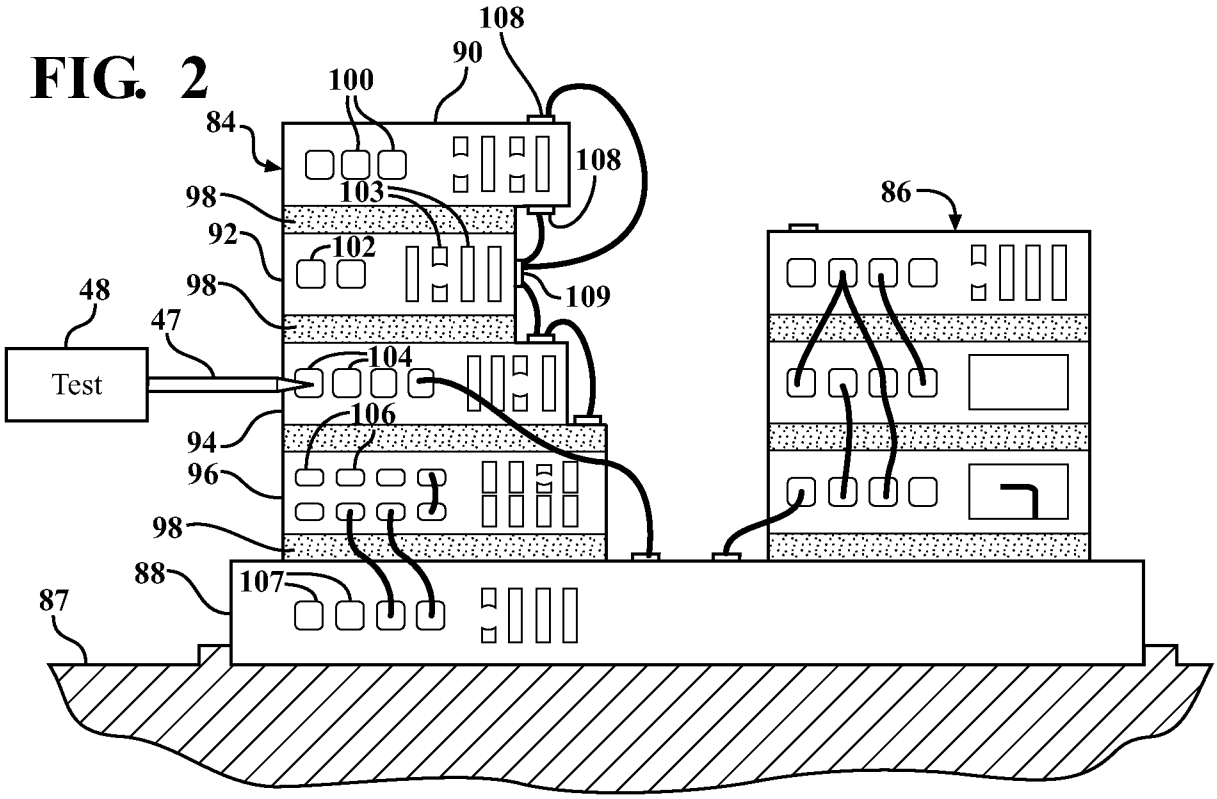
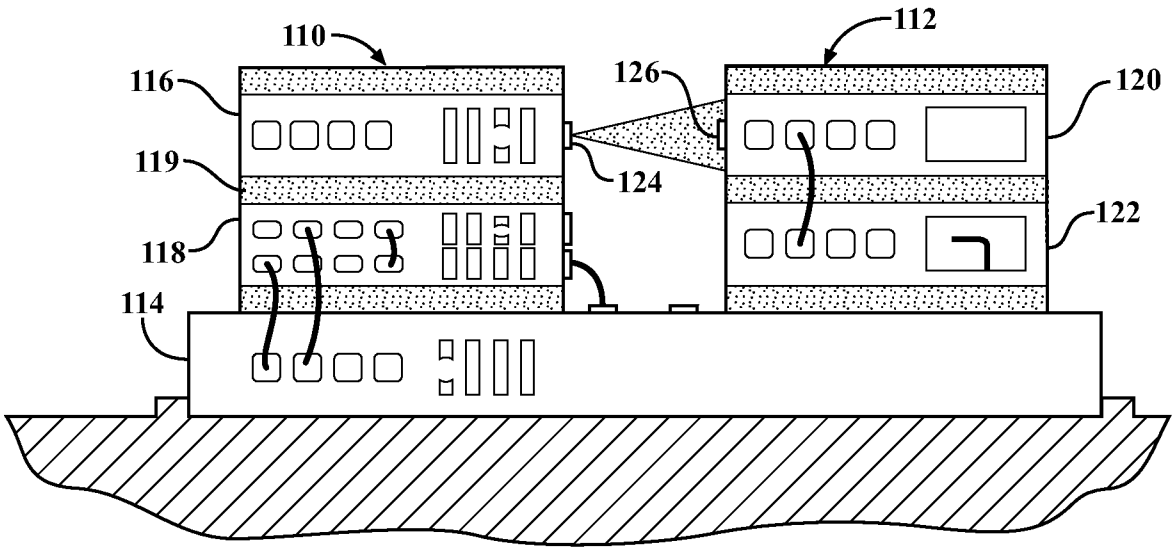

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Test
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FIG. 3


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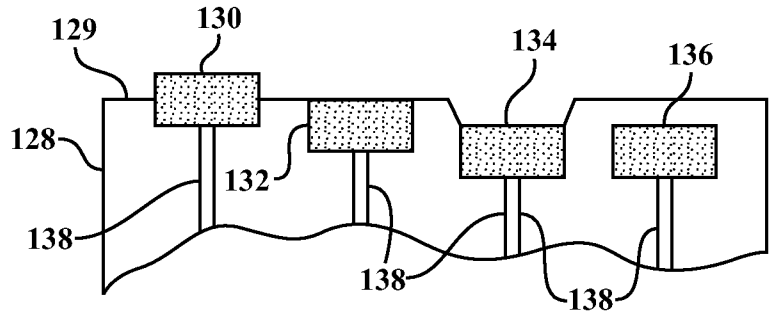

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FIG. 4

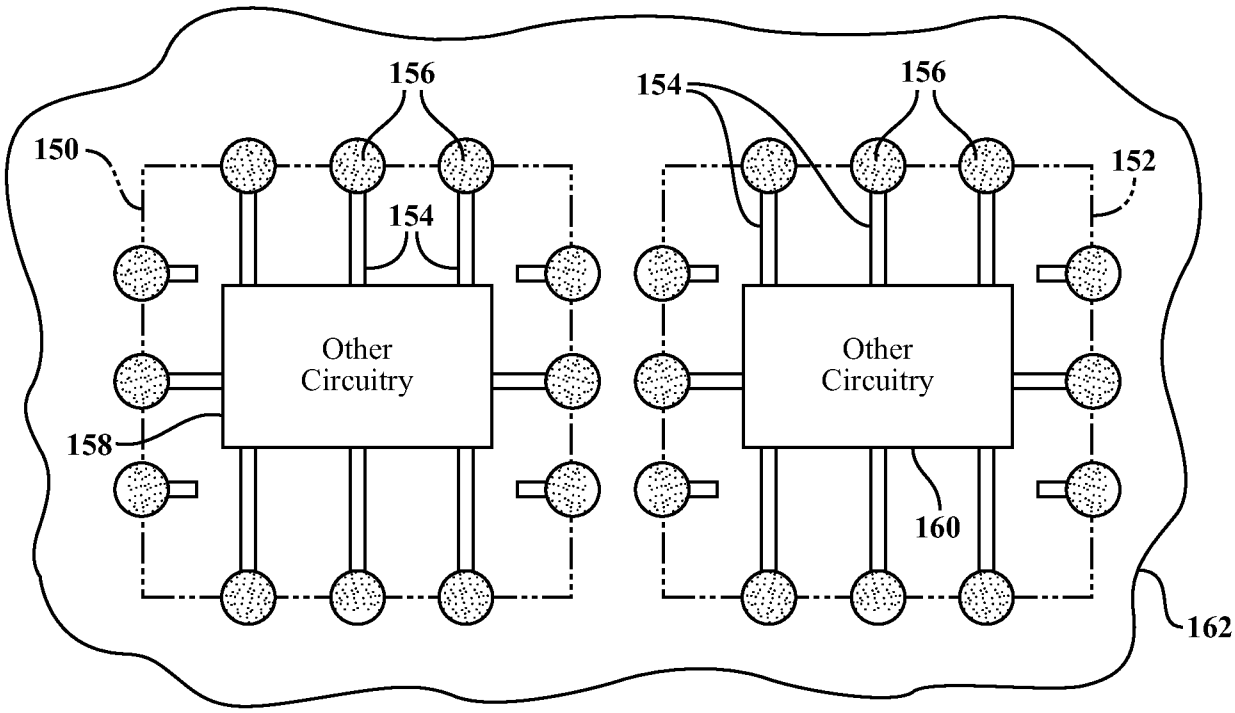

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Other Circuitry
Other Circuitry
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FIG. 5

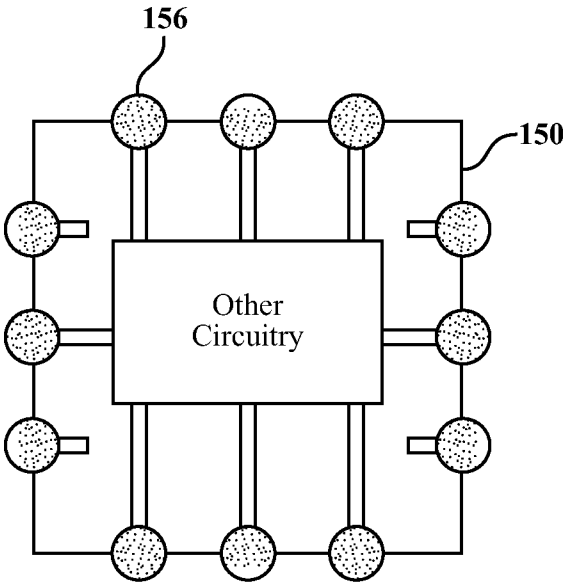



FIG. 6

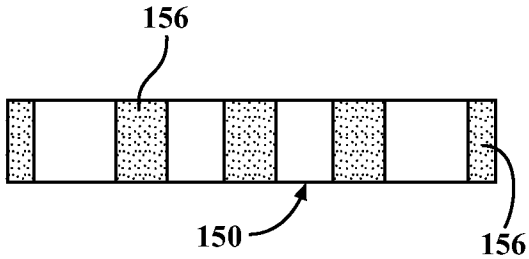



FIG. 6A

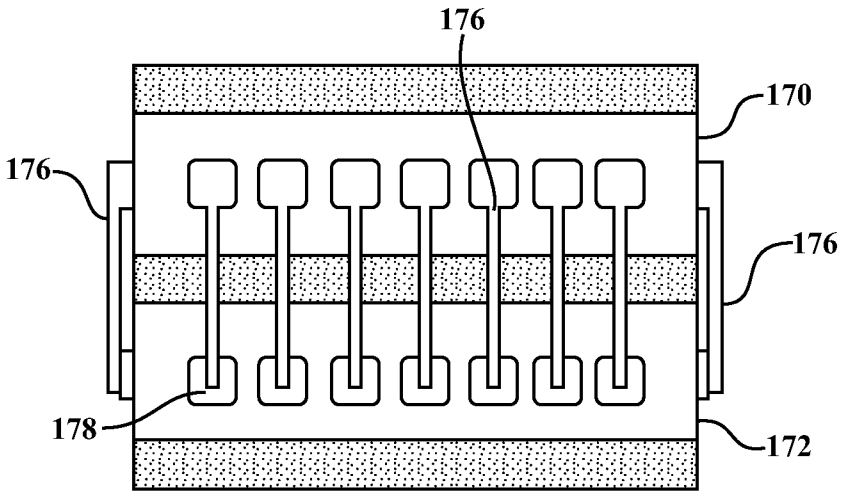



FIG. 7

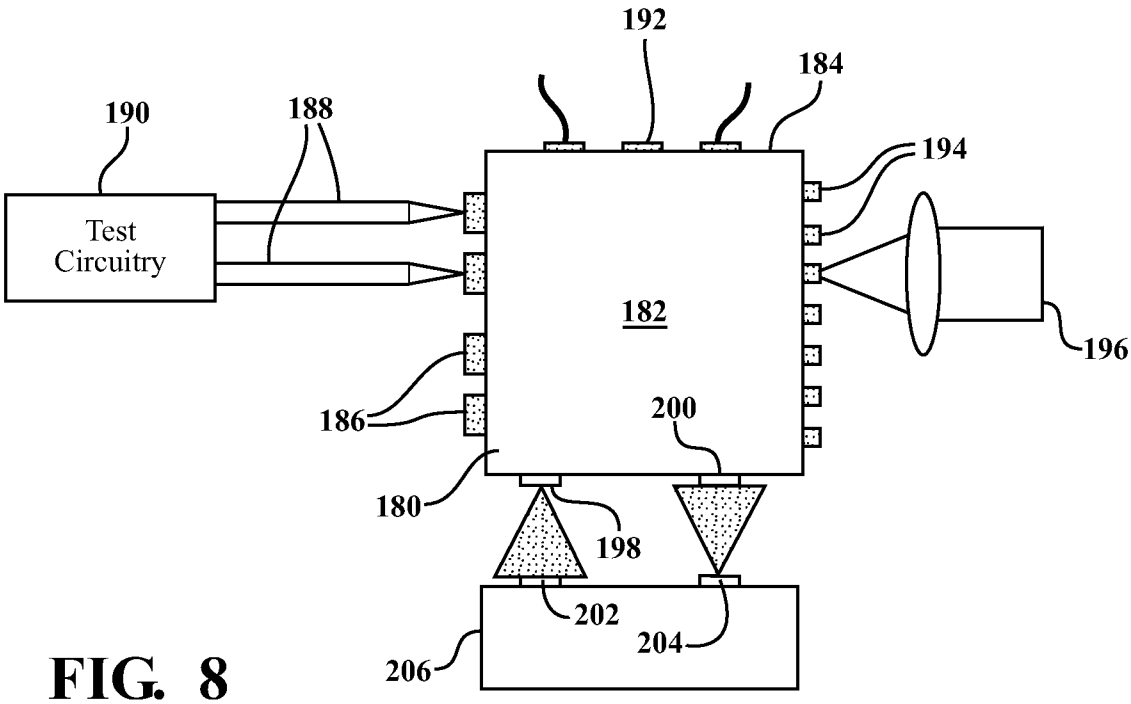

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Test
Circuitry
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FIG. 8

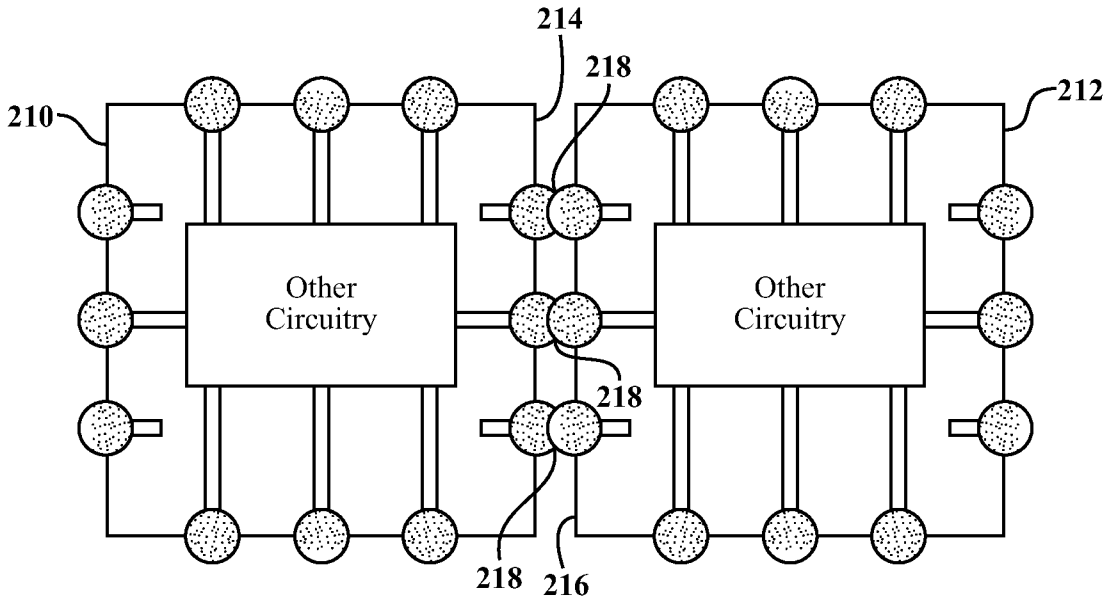

214
218
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Other
Circuitry
Other
Circuitry
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218
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FIG. 9

**INTERNATIONAL SEARCH REPORT**

International application No.
**PCT/US2011/058030**

**A. CLASSIFICATION OF SUBJECT MATTER**

***H01L 25/00(2006.01)i, H01L 23/58(2006.01)i, G01R 31/26(2006.01)i***

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

H01L 25/00; H01L 23/52; H01L 21/60; H01L 29/00; H01L 29/04; H05K 3/36; H01L 23/02; H01L 21/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: integrated, circuit, package, stack, vertical, sidewall, semiconductor, wafer, active, solder, bump, and similar terms.

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X<br>A | US 2008-0006921 A1 (STATS CHIPPAC LTD.) 10 January 2008<br>See abstract, Figures 1-13 and claims 1-20 | 15<br>1-14,16 |
| A | KR 10-2001-0073946 A (삼성전자 주식회사) 03 August 2001<br>See abstract, Figures 1-5 and claims 1-6 | 1-16 |
| A | US 06034438A A (PETERSEN ROBERT W.) 07 March 2000<br>See abstract, Figures 1-5 and claims 1-17 | 1-16 |
| A | US 2007-0023883 A1 (MARKUS BRUNNBAUER et al.) 01 February 2007<br>See abstract, Figures 1-13 and claims 1-34 | 1-16 |

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
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"&" document member of the same patent family

| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 15 MAY 2012 (15.05.2012) | **17 MAY 2012 (17.05.2012)** |


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**INTERNATIONAL SEARCH REPORT**

Information on patent family members

International application No.

**PCT/US2011/058030**

| Patent document cited in search report | Publication date | Patent family member(s) | Publication date |
|---|---|---|---|
| US 2008-0006921 A1 | 10.01.2008 | None | |
| KR 10-2001-0073946 A | 03.08.2001 | None | |
| US 06034438A A | 07.03.2000 | WO 98-18160 A1 | 30.04.1998 |
| US 2007-0023883 A1 | 01.02.2007 | DE 102005030465 A1<br>DE 102005030465 B4<br>US 7429782 B2 | 04.01.2007<br>20.12.2007<br>30.09.2008 |