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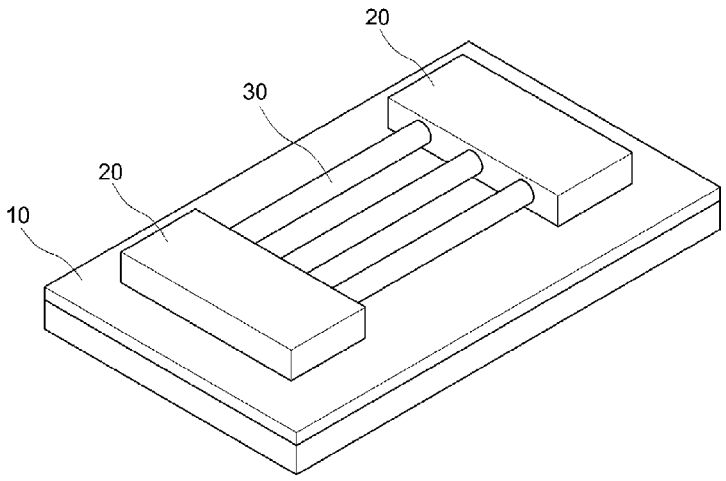
[Continued on next page]

(54) Title: METHOD FOR PRODUCING CARBON NANOTUBE TRANSISTOR AND CARBON NANOTUBE TRANSISTOR THEREBY

[Fig. 1]



(57) Abstract: The present invention relates to a method of manufacturing a carbon nanotube transistor in which a carbon nanotube channel is formed between a source electrode and a drain electrode and a gate electrode is formed at one side of the carbon nanotube channel, the method comprising the steps of: (a) forming the carbon nanotube channel on a substrate; (b) electrically connecting the source electrode and the drain electrode to both ends of the carbon nanotube channel, respectively; and (c) applying a stress voltage across the source electrode and the drain electrode to remove metallicity of the carbon nanotube channel. According to the method of manufacturing a carbon nanotube transistor of the present invention, a metallic part can be selectively removed from a carbon nanotube which is used as a channel of a transistor and has metallic properties and semiconductor properties mixed with each other.

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Description

METHOD FOR PRODUCING CARBON NANOTUBE TRANSISTOR AND CARBON NANOTUBE TRANSISTOR THEREBY

Technical Field

[1] The present invention relates to a method of manufacturing a carbon nanotube transistor and a carbon nanotube transistor manufactured by the same.

Background Art

[2] Carbon nanotubes are expected as a material having industrial applications in a variety of areas including electronic information communication, environment and energy fields because of their excellent electrical, mechanical and chemical characteristics.

[3] Carbon nanotubes are visualized as a graphite sheet rolled having a nanosize-diameter and the conductivity of the carbon nanotubes varies according to the rolling angle and structure of the graphite sheet such that the carbon nanotube has metallic or semiconductor properties.

[4] Furthermore, the carbon nanotubes can be classified into single-walled carbon nanotube (SWNT), double-walled carbon nanotube (DWNT), multi-walled carbon nanotube (MWNT) and rope carbon nanotube according to a degree of lamination of the graphite sheet.

[5] Each of carbon atoms constituting the carbon nanotube is combined with three neighboring carbon atoms according to sp^2 combination method to form a hexagonal honeycomb structure. The carbon nanotube could have metal or semiconductor properties by its diameter and chirality. It is generally known that a third has metal properties and two-thirds has semiconductor properties of which a band gap is inversely proportional to the diameter of the carbon nanotube in SWNT.

[6] The carbon nanotube having the semiconductor properties can be applied to transistors, memory devices and gas sensors and the metallic properties are required for the carbon nanotube to be used as an electrode material.

[7] The carbon nanotube having the semiconductor properties is not required to be additionally doped because it has been doped with impurities. Furthermore, the carbon nanotube can be advantageously used to manufacture a semiconductor chip with high integration because it has a very narrow line width.

[8] However, the metallic properties included with the semiconductor properties in the carbon nanotube must be eliminated in order to use the carbon nanotube as a semiconductor material.

[9] To this end, U.S. Patent Laid-Open Publication No. 2006-223068 discloses a technique of selectively separating a carbon nanotube of semiconductor property from a carbon nanotube of metallic property in fabricated carbon nanotubes in a solution. However, although this technique is suitable for a large quantity of carbon nanotube powder specimen, it is required to spread the separated carbon nanotube on a substrate for making semiconductor device.

[10] Accordingly, there is a need for a method of controlling the property of carbon nanotube to remove only the metallicity of the carbon nanotube in semiconductor device structure, such as a transistor.

Disclosure of Invention

Technical Problem

[11] Accordingly, the present invention has been made to solve the above-mentioned problems occurring in the conventional art, and a primary object of the present invention is to provide a method of manufacturing a carbon nanotube transistor for removing metallicity from carbon nanotubes applied to a channel in a device such that the channel has semiconductor properties.

[12] Another object of the present invention is to provide a carbon nanotube transistor manufactured by removing metallicity of carbon nanotube in a channel of a device.

Technical Solution

[13] According to an aspect of the present invention, there is provided a method of manufacturing a carbon nanotube transistor, in which a carbon nanotube channel is formed between a source electrode and a drain electrode, and a gate electrode is formed at one side of the carbon nanotube channel, the method comprising the steps of: (a) forming the carbon nanotube channel on a substrate; (b) electrically connecting the source electrode and the drain electrode to both ends of the carbon nanotube channel, respectively; and (c) applying a stress voltage across the source electrode and the drain electrode to remove metallicity of the carbon nanotube channel.

[14] The step (c) comprises a process of applying a gate voltage to the gate electrode to deplete carriers in a semiconductor part of the carbon nanotube channel, before the stress voltage is applied or at the same time when the stress voltage is applied.

[15] The method of manufacturing a carbon nanotube transistor may further comprise the steps of: (d) measuring the turn-on current and turn-off current of the carbon nanotube transistor and calculating the ratio of the turn-on current to the turn-off current; and (e) comparing the ratio of the turn-on current to the turn-off current with a reference value to evaluate the performance of the carbon nanotube transistor.

[16] The method of manufacturing a carbon nanotube transistor may further comprise the step of: (f) changing the condition of applying the stress voltage when the ratio of

the turn-on current to the turn-off current is smaller than the reference value, and then repeatedly performing the step (c).

[17] The method of manufacturing a carbon nanotube transistor may further comprise the steps of: (g) measuring and calculating a drain current variation according to a gate voltage variation for the carbon nanotube transistor; and (h) comparing the drain current variation according to the gate voltage variation with a reference value to evaluate the performance of the carbon nanotube transistor.

[18] The method of manufacturing a carbon nanotube transistor may further comprise the step of: (i) changing the condition of applying the stress voltage when the drain current variation according to the gate voltage variation is smaller than the reference value, and then repeatedly performing the step (c).

[19] The step of changing the condition of applying the stress voltage may include changing a stress voltage applying time or the stress voltage. The number of times of changing the stress voltage applying time may be limited to a predetermined number of times and the stress voltage may be changed when the number of times of changing the stress voltage applying time exceeds the predetermined number of times.

[20] The gate electrode may be a silicon substrate or a liquid gate electrode formed by exposing the carbon nanotube channel to a liquid, and then bringing a metal electrode into contact with the liquid or inserting the metal electrode into the liquid, the liquid is a liquid with a low ion concentration such as deionized water. The absolute value of the gate voltage is smaller than 1V.

[21] According to another aspect of the present invention, there is provided a carbon nanotube transistor comprising: a source electrode; a drain electrode; and a carbon nanotube channel for interconnecting the source electrode and the drain electrode, wherein carbon nanotubes corresponding to a metallic part mixed with a semiconductor part are thermally cut and lose its metallicity when the carbon nanotube channel is formed.

Advantageous Effects

[22] As described above, according to the method of manufacturing a carbon nanotube transistor of the present invention, a metallic part can be selectively removed from a carbon nanotube that is used as a channel in a transistor and has both metallic properties and semiconductor properties. Accordingly, the carbon nanotube channel operates in the same manner as a channel formed of only a semiconductor carbon nanotube.

[23] Therefore, according to the method of manufacturing a carbon nanotube of the present invention, the metallicity can be removed from the carbon nanotube channel of the carbon nanotube transistor to strengthen the semiconductor properties so as to

remarkably improve the performance of the carbon nanotube transistor.

[24] Accordingly, transistor performances are improved in application fields such as sensors to which the carbon nanotube transistor is applied, and thus the improvement of property of sensors, such as sensitivity, can be expected.

[25] Furthermore, the method of manufacturing a carbon nanotube transistor of the present invention does not select a semiconductor carbon nanotube and use the selected semiconductor carbon nanotube, manufactures a transistor using carbon nanotubes without using a selecting process, and then removes only metallicity from the carbon nanotubes. Accordingly, a manufacturing process is simple, and thus carbon nanotube transistors having high performance can be manufactured in a great quantity with high yield for a short manufacturing time.

Brief Description of the Drawings

[26] Further objects and advantages of the invention can be more fully understood from the following detailed description taken in conjunction with the accompanying drawings, in which:

[27] FIG. 1 illustrates the concept of a carbon nanotube semiconductor device;

[28] FIG. 2 is a flow chart of a process of removing metallicity from a carbon nanotube channel of carbon nanotube transistors in a method of manufacturing the carbon nanotube transistor according to the present invention;

[29] FIG. 3 illustrates an operation of performing the process of removing metallicity from the carbon nanotube channel illustrated in FIG. 2;

[30] FIG. 4 is a graph showing a turn-on current, a turn-off current and the ratio of the turn-on current to the turn-off current of a carbon nanotube channel of carbon nanotube transistors according to a stress condition applied to the carbon nanotube transistor; and

[31] FIG. 5 is a graph showing a variation in the drain current with respect to the gate voltage of a carbon nanotube transistor after a stress condition is applied to the carbon nanotube transistor.

Best Mode for Carrying Out the Invention

[32] A method of manufacturing a carbon nanotube transistor according to the present invention includes a step of growing carbon nanotubes as a channel between a source electrode and a drain electrode of a transistor, and a step of applying overcurrent to a metallic part of the grown carbon nanotube channel having the metallic part and a semiconductor part, which are mixed with each other, to remove metallicity of the metallic part of the carbon nanotube channel to make the carbon nanotube channel have semiconductor properties, when the transistor is fabricated using the carbon nanotubes.

[33] Here, the overcurrent applied to the metallic part of the carbon nanotube channel changes or destroys the structure of metallic carbon nanotubes to remove the metallicity of the carbon nanotube channel.

[34] It is desirable to apply a predetermined voltage to the gate electrode of the transistor in the step of removing the metallicity of the carbon nanotube channel. When the predetermined voltage is applied to the gate electrode, carriers are depleted in the semiconductor part of the carbon nanotube channel by the gate voltage, and thus the overcurrent applied to the carbon nanotube channel flows through the metallic part rather than the semiconductor part to remove the metallicity in the metallic part of the carbon nanotube channel.

[35] That is, the gate voltage is applied to the transistor to deplete carriers in the semiconductor part of the carbon nanotube channel and change the semiconductor part into a depletion layer so as to increase the electrical resistance of the semiconductor part. Then, a high voltage is applied across the source electrode and the drain electrode such that overcurrent flows through the metallic part of the carbon nanotube channel to efficiently destroy and remove the metallicity of the metallic part. More specifically, the overcurrent applied to carbon nanotubes of the metallic part thermally cuts the structure of the carbon nanotubes to destroy and remove conductivity of the carbon nanotubes, that is, metallicity.

[36] The method of manufacturing a carbon nanotube transistor of the present invention is described in detail with reference to FIGS. 1 and 2.

[37] FIG. 1 illustrates a carbon nanotube transistor manufactured according to the method of manufacturing a carbon nanotube transistor of the present invention.

[38] Referring to FIG. 1, the carbon nanotube transistor of the present invention includes a silicon substrate (Si/SiO_2) 10, electrodes 20, and a carbon nanotube channel 30. The electrodes 20 may be a source electrode or a drain electrode and the carbon nanotube channel 30 electrically connects the source and drain electrodes 20 to each other. A method of manufacturing the carbon nanotube transistor illustrated in FIG. 1 is explained below.

[39] First of all, a pattern corresponding to a channel is formed on the silicon substrate 10 insulated with a SiO_2 layer formed by oxidizing silicon according to a photolithography method of a semiconductor process. The method of forming the pattern uses a method conventionally used in a photolithography process. In the present embodiment, photoresist is coated on the silicon substrate 10, a mask corresponding to the channel is located above the photoresist layer and light is irradiated to the photoresist layer. A portion of the photoresist layer, which is exposed to the light and denatured, is removed by using an etching solution to form the pattern corresponding to the channel. Here, although the photoresist is not limited to a specific material, it is

desirable to use polymethyl methacrylate (PMMA).

[40] Then, a liquid catalyst is introduced in order to form carbon nanotubes in the pattern formed as above. Although Fe/Mo catalyst solution is used as the liquid catalyst in the present embodiment of the present invention, any material capable of promoting the growth of carbon nanotubes can be used as the liquid catalyst. Preferably, transition metals such as Co, Fe, Ni, Mo and Cu, protein including a transition metal, such as Ferritin, reagents containing iron ion, such as $FeCl_3$ and $FeSO_4$, dendrimer containing iron ion or gold nanoparticles can be used as a catalyst for promoting the growth of carbon nanotubes.

[41] Subsequently, the silicon substrate 10 on which carbon nanotubes are reacted with the liquid catalyst is put in acetone solution to completely remove the photoresist layer made of PMMA, and then the catalyst-treated silicon substrate 10 is loaded into a furnace in the ambient of CH_4 and H_2 at the temperature of 900°C and grown for 10 minutes to form single walled carbon nanotubes in the channel.

[42] The electrodes 20 are formed at both ends of the carbon nanotube channel formed as above to fabricate the transistor as illustrated in FIG. 1. The electrodes 20 can be formed using conventional photolithography and thermal evaporation for manufacturing semiconductor devices and detailed explanations thereof are omitted.

[43] It is desirable that the transistor according to the present invention is a MOSFET but it is not limited thereto.

[44] While the carbon nanotube channel of the transistor fabricated as illustrated in FIG. 1 is formed of carbon nanotubes, the carbon nanotube channel includes a metallic part in terms of the property of carbon nanotubes. Accordingly, it is required to remove metallicity in the metallic part of the carbon nanotube channel.

[45] A method of removing the metallicity in the carbon nanotube channel in the method of manufacturing a carbon nanotube transistor according to the present invention is described in detail with reference to FIG. 2.

[46] In the present invention, a process of removing the metallicity in the carbon nanotube channel of the transistor can be performed simultaneously with a wafer probing process for testing whether transistors formed on a wafer are poor through a probe station.

[47] Referring to FIG. 2, first of all, the method of removing the metallicity in the carbon nanotube channel according to the present invention, measures and confirms whether the carbon nanotube channel of a target transistor has metallicity in step S100.

[48] Here, the metallicity of the carbon nanotube channel is confirmed in such a manner that parameters of the transistor, such as the turn-on current, turn-off current and threshold voltage, are measured through a measurement system, and then it is confirmed whether the transistor shows satisfactory performance comparing the

measured parameters with a predetermined reference value in step S200.

[49] Specifically, when metallicity of more than a desired level exists in the carbon nanotube channel of the transistor, the transistor cannot accomplish desired performance. Accordingly, it can be confirmed whether metallicity exists in the carbon nanotube channel of the transistor by measuring the ratio of the turn-on current to the turn-off current, threshold voltage or transconductance of the transistor.

[50] The reference value can use a value previously input by a user and stored and can be controlled to various values according to the desired performance of the transistor.

[51] In a case where the performance of the transistor is satisfied when the parameters are compared with the reference value, the process of removing metallicity is not performed in step S600.

[52] However, when the desired performance of the transistor is not satisfied, that is, when a metallic part of more than a predetermined level exists in the carbon nanotube channel of the transistor, a stress voltage is applied across the source electrode 20 and the drain electrode 20 of the transistor to leave the carbon nanotube channel 30 between the source electrode 20 and the drain electrode 20 under a predetermined stress condition in step S300. Under this stress condition, the predetermined stress voltage is applied for a predetermined period of time. The process of removing metallicity is stopped when the stress condition exceeds a predetermined range and the process is applied when the stress condition is in the predetermined range.

[53] When the stress voltage is applied to the carbon nanotube channel between the source electrode and the drain electrode, overcurrent flows through the carbon nanotube channel according to the applied stress voltage and applies stress to the carbon nanotube structure of the metallic part of the carbon nanotube channel. This stress cuts the carbon nanotube structure to change the carbon nanotube structure, and thus carbon nanotubes of the carbon nanotube channel lose metallicity. When carbon nanotubes in the carbon nanotube channel lose metallicity, the resistance of the carbon nanotube channel increases to result in loss of metallicity of the carbon nanotube channel.

[54] Meanwhile, it is desirable that the stress condition is not applied to the semi-conductor part existing in the carbon nanotube channel. To achieve this, it is desirable that a voltage is applied to one side of the carbon nanotube channel, that is, the gate electrode of the transistor, which is formed in a position to which electric field can be applied, to change the semiconductor part of the carbon nanotube channel into a depletion layer, that is, to deplete carriers in the semiconductor part, when the stress condition is applied.

[55] The stress condition is applied to remove metallicity of the carbon nanotube channel, and then the performance of the transistor is measured again to confirm

whether the desired performance is achieved in step S400.

[56] When the desired performance is not achieved, the stress condition is changed and the changed stress condition is applied to repeat the process of removing metallicity in step S500.

[57] It is desirable to repeatedly apply the stress condition through the following method.

[58] Whenever the same stress voltage is applied, a stress applying time is increased. For example, the stress applying time is increased to 0.01 seconds, 0.05 seconds and 0.25 seconds etc. When the performance of the transistor is not satisfied even after a stress is applied for a predetermined time, it is desirable to limit the number of changing the stress applying time to prevent a process time from excessively increasing.

[59] That is, when the performance of the transistor is not satisfied even after a stress condition corresponding to a predetermined maximum allowable stress applying time (for example, 0.25 seconds) is applied, a method of increasing the stress voltage is used. For example, the stress voltage is increased by 5V.

[60] When it is confirmed that the desired performance of the transistor is achieved according to the measurement of the performance of the transistor after the stress condition is applied in stages, the process of removing metallicity in the carbon nanotube channel of the transistor is finished.

[61] Hereinafter, the method of removing metallicity of a carbon nanotube channel of a corresponding transistor using a semiconductor device measurement system for transistors formed on a substrate is explained with reference to FIG. 3.

[62] Referring to FIG. 3, a plurality of transistors to be tested exist on a substrate 10 and each of the transistors includes a source electrode 20 and a drain electrode 20 connected to each other through a carbon nanotube channel 30.

[63] A process of measuring the performance of the transistor through a probe card 50 which comes into contact with the electrodes 20 and applies a signal and a process of removing metallicity are performed on the transistor. The probe card 50 includes a plurality of probes 40 which come into contact with the electrodes of the plurality of transistors to apply signals.

[64] The probe card 50 is connected to a measurement system 90 through a matrix switching system 70. The probe card 50 is connected to the matrix switching system 70 through signal lines 60.

[65] Here, the matrix switching system 70 controls a plurality of internal switches 80 corresponding to transistors to be tested to apply a stress condition suitable to the transistors.

[66] When the process of measuring the performance of a transistor and a process of removing metallicity from the transistor are finished, the measurement system 90 controls the switches 80 of the matrix switching system 70 to sequentially test

following to-be-tested transistors.

[67] Here, when the process of measuring transistor performance and the process of removing metallicity have been sequentially performed on all the transistors included in a single die, the measurement system 90 moves to another die on the substrate and carries out the transistor performance measurement and metallicity removal processes.

[68] It is also desirable to carry out the transistor performance measurement and metallicity removal process to the whole dies of a wafer simultaneously, with the probe card which covers whole dies to reduce the process time.

[69] Meanwhile, the result of the metallicity removal process, for example, data of transistors included in dies or in each die that have passed standards, is stored and can be used as performance data of transistors even after the substrate is cut into respective dies and wire bonding and packaging are performed.

[70] As described above, it is desirable to apply a predetermined voltage to the gate electrode to deplete carriers in the semiconductor part of the carbon nanotube channel in order to increase the resistance of the semiconductor part of the carbon nanotube channel, when the stress voltage is applied across the source electrode and the drain electrode. Here, a silicon substrate can be used as the gate electrode.

[71] In another preferred embodiment, the gate electrode is not additionally formed and a liquid gate, which is formed by exposing the carbon nanotube channel 40 to a liquid and bringing a metal electrode into contact with the liquid or putting the metal electrode into the liquid, can be used. Here, it is desirable to use a liquid with a low ion concentration, such as deionized water, as the liquid in order to prevent ion current from flowing through the liquid or prevent the liquid from electrolysis.

[72] In a case where the liquid gate is used, it is desirable to form a passivation layer using photoresist to expose only the carbon nanotube channel region in order to protect metal conductor patterns of a source and a drain and the electrodes 20.

[73] When the liquid gate is used, it is desirable that the absolute value of the gate voltage is smaller than 1V that can sufficiently deplete carriers in the semiconductor part of the carbon nanotube channel. When the gate voltage is excessively high, the liquid used for the liquid gate may be electrolyzed, and thus the liquid gate is not suitable for the transistor.

[74] As described above, the present invention can test transistors formed on a substrate such as a wafer by the probe card 50 and, simultaneously, remove metallicity in the carbon nanotube channel of each transistor.

[75] While the present invention is described in more detail below through an example, the scope of the present invention is not limited to the example.

[76] Example

[77] SiO_2/Si substrate is prepared and PMMA layer is formed thereon and patterned to

remove a portion of the PMMA layer, which corresponds to a channel of a transistor. Fe/Mo catalytic solution is coated on the patterned portion corresponding to the channel, and then the PMMA layer is removed through lift-off.

[78] The SiO_2/Si substrate having the portion corresponding to a channel, coated with Fe/Mo catalytic solution is loaded into a furnace in the ambient of CH_4 and H_2 and the furnace is heated to 900°C for 10 minutes to grow carbons on the portion corresponding to the channel to form a single walled carbon nanotube channel.

[79] Electrode patterns are formed on portions of the substrate, which correspond to both sides of the carbon nanotube channel, through photolithography method, and then Ti with a thickness of 5nm and Au with a thickness of 30nm are sequentially deposited using thermal evaporation while maintaining a vacuum to form electrodes. Subsequently, the substrate is put into acetone solution to remove metals such as Ti and Au deposited on an undesired portion to obtain a carbon nanotube transistor.

[80] Subsequently, the performance of the carbon nanotube transistor obtained as above is measured.

[81] To measure the performance of the transistor, the drain current, turn-on current I_{on} and turn-off current I_{off} are measured and the ratio of the turn-on current I_{on} to the turn-off current I_{off}, that is, I_{on}/I_{off}, is calculated. In the present embodiment, a reference value for I_{on}/I_{off} is set to 20.

[82] The measurement of the performance of the transistor is repeated while changing a stress condition in stages until the measured I_{on}/I_{off} exceeds the reference value.

[83] The stress condition is applied in stages in such a manner that a voltage of 10V is applied across the source and drain electrodes while increasing a voltage applying time to 0.01 seconds, 0.05 seconds and 0.25 seconds. After the voltage is applied for 0.25 seconds, the voltage is increased by 5V, and then the stress condition is repeatedly applied while increasing the voltage applying period to 0.01 seconds, 0.05 seconds and 0.25 seconds.

[84] Measurement values according to the aforementioned stress condition are illustrated in FIGS. 4 and 5.

[85] It can be known from FIG. 4 that a drain current value is reduced when a stress voltage 10V is applied for 0.01 seconds, when 20V is applied for 0.25 seconds and when 25V is applied for 0.25 seconds. From this result, it can be known that metallicity of the carbon nanotube channel is reduced but the reduction in the metallicity is not so large as the performance of the transistor is satisfied.

[86] However, when 40V is applied for 0.05 seconds, the turn-off current I_{off} is abruptly decreased as compared to the turn-on current I_{on}, and thus I_{on}/I_{off} is suddenly increased and exceeds the reference value. From this result, it can be confirmed that the carbon nanotube transistor shows satisfactory transistor performance.

[87] It can be confirmed from FIG. 4 that the metallic part of the carbon nanotube channel is removed so that the carbon nanotube channel has semiconductor properties when a stress condition suitable for the carbon nanotube channel of the carbon nanotube transistor is applied.

[88] Meanwhile, FIG. 5 shows a drain current I_D measured as a function of a gate voltage V_G whenever the metallic part is removed from the carbon nanotube channel after a stress condition is applied. It can be confirmed from FIG. 5 that a device, which does not show transistor performance because the drain current is not varied, even though the gate voltage is changed when the stress condition is not applied or when an appropriate stress condition is not applied, shows excellent transistor performance in that the drain current I_D is varied according to a gate voltage variation, after 40V is applied for 0.05 second as stress condition.

[89] Furthermore, it can be confirmed from FIG. 5 that the confirmation of the transistor performance can also be made by measuring a variation in the drain current I_D according to a variation in the gate voltage V_G in the present invention.

[90] Results obtained by applying the method of the present invention to dies including 12 transistors respectively are arranged in Table 1.

[91] Table 1

Experiment	The number of dies	The number of transistors	Before removal of metallicity		After removal of metallicity	Success rate
			The number of carbon nanotube channels	I_{on}/I_{off} is greater than 20	I_{on}/I_{off} is greater than 20	Dies including at least three high-performance carbon nanotube transistors
1	2	24	14	0	14	100
2	9	108	69	6	60	100
3	11	132	65	6	34	100

[92] It can be confirmed from Table 1 that a plurality of transistors having unsatisfied performances achieve desired transistor performances because I_{on}/I_{off} is remarkably increased after the process of removing metallicity in the method of manufacturing a carbon nanotube transistor of the present invention is performed. In particular, it can be known that 100% yield is obtained when a case where at least three carbon nanotube field effect transistors (CNTFETs) corresponding to high-performance carbon nanotube transistors are integrated into a single die is determined as final yield.

[93] While the present invention has been particularly shown and described with reference to exemplary embodiments thereof, it will be understood by those of ordinary skill in the art that various changes in form and details may be made therein without departing from the spirit and scope of the present invention as defined by the following claims.

Claims

[1] A method of manufacturing a carbon nanotube transistor in which a carbon nanotube channel is formed between a source electrode and a drain electrode and a gate electrode is formed at one side of the carbon nanotube channel, the method comprising the steps of:
(a) forming the carbon nanotube channel on a substrate;
(b) electrically connecting the source electrode and the drain electrode to both ends of the carbon nanotube channel, respectively; and
(c) applying a stress voltage across the source electrode and the drain electrode to remove metallicity in the carbon nanotube channel.

[2] The method according to claim 1, wherein a gate voltage is applied to the gate electrode to deplete carriers in a semiconductor part of the carbon nanotube channel, before the stress voltage is applied or at the same time when the stress voltage is applied in the step (c).

[3] The method according to claim 1, further comprising the steps of:
(d) measuring a turn-on current and a turn-off current of the carbon nanotube transistor and calculating the ratio of the turn-on current to the turn-off current; and
(e) comparing the ratio of the turn-on current to the turn-off current with a reference value to evaluate a performance of the carbon nanotube transistor.

[4] The method according to claim 3, further comprising the step of:
(f) changing the condition of applying the stress voltage when the ratio of the turn-on current to the turn-off current is smaller than the reference value, and then performing the step (c) again.

[5] The method according to claim 1, further comprising the steps of:
(g) measuring and calculating a drain current variation according to a gate voltage variation for the carbon nanotube transistor; and
(h) comparing the drain current variation according to the gate voltage variation with a reference value to evaluate performance of the carbon nanotube transistor.

[6] The method according to claim 5, further comprising the step of:
(i) changing the condition of applying the stress voltage when the drain current variation according to the gate voltage variation is smaller than the reference value, and then performing the step (c) again.

[7] The method according to claim 4 or 6, wherein the step of changing the condition of applying the stress voltage comprises varying a stress voltage applying time or the stress voltage.

[8] The method according to claim 7, wherein the number of times of changing the

stress voltage applying time is limited to a predetermined number of times, and the stress voltage is changed when the number of times of changing the stress voltage applying time exceeds the predetermined number of times.

[9] The method according to any one of claims 1 to 6, wherein the gate electrode is a silicon substrate.

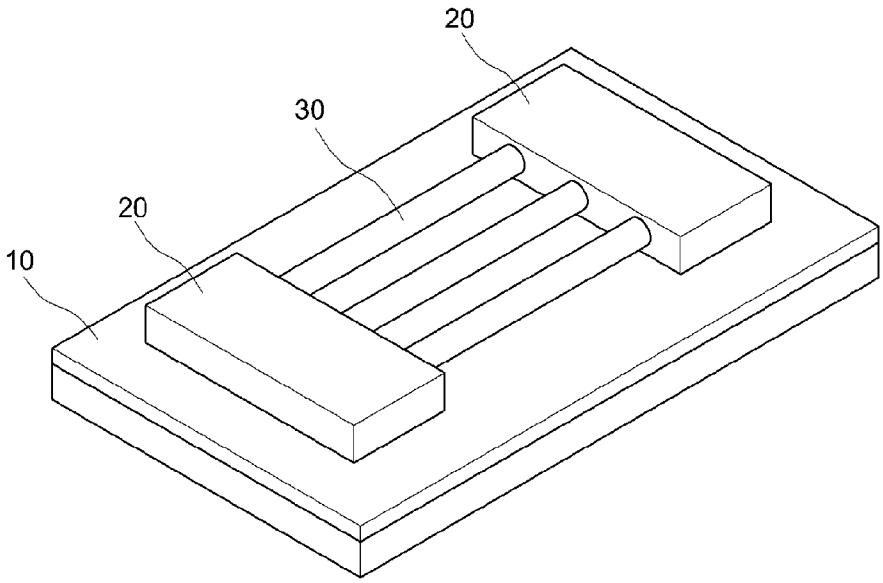
[10] The method according to any one of claims 1 to 6, wherein after the carbon nanotube channel has been exposed to a liquid, a metal electrode is brought into contact with the liquid or inserted into the liquid to form a liquid gate electrode and use the liquid gate electrode.

[11] The method according to claim 10, wherein the liquid is a liquid with a low ion concentration, such as deionized water.

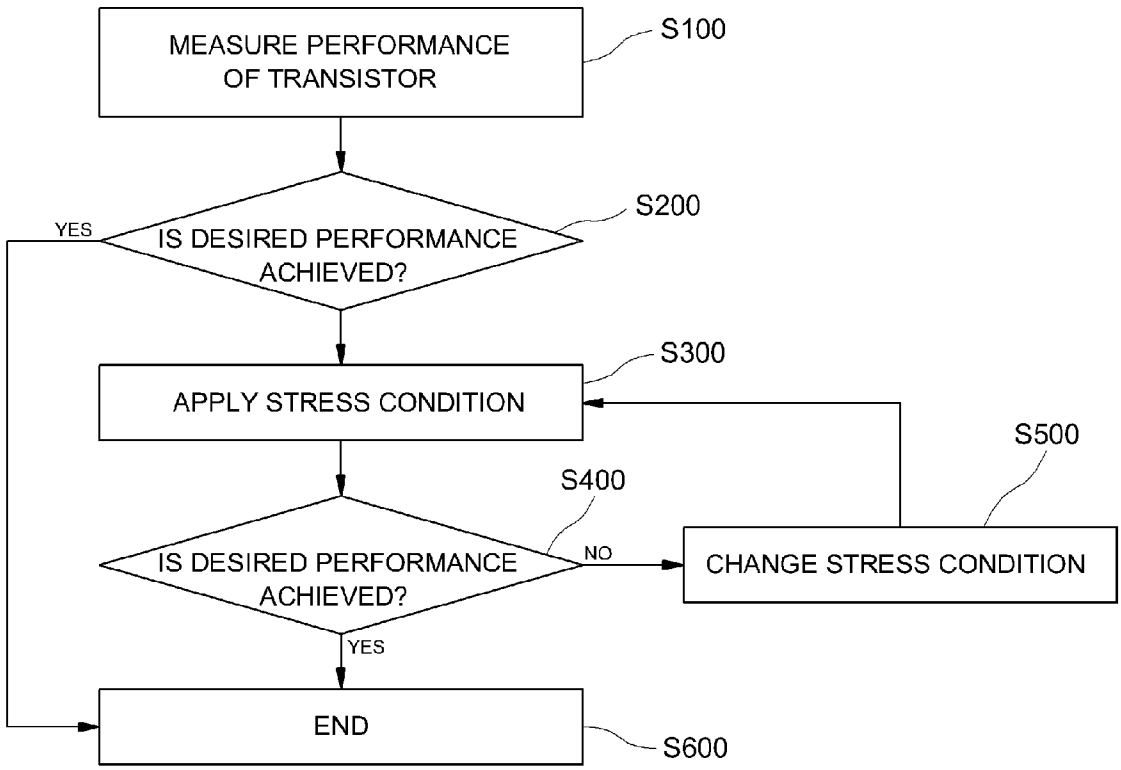
[12] The method according to claim 11, wherein the absolute value of the gate voltage is smaller than 1V.

[13] A carbon nanotube transistor comprising:
a source electrode;
a drain electrode; and
a carbon nanotube channel for interconnecting the source electrode and the drain electrode,
wherein carbon nanotubes of a metallic part mixed with a semiconductor part are thermally cut and lose metallicity when the carbon nanotube channel is formed.

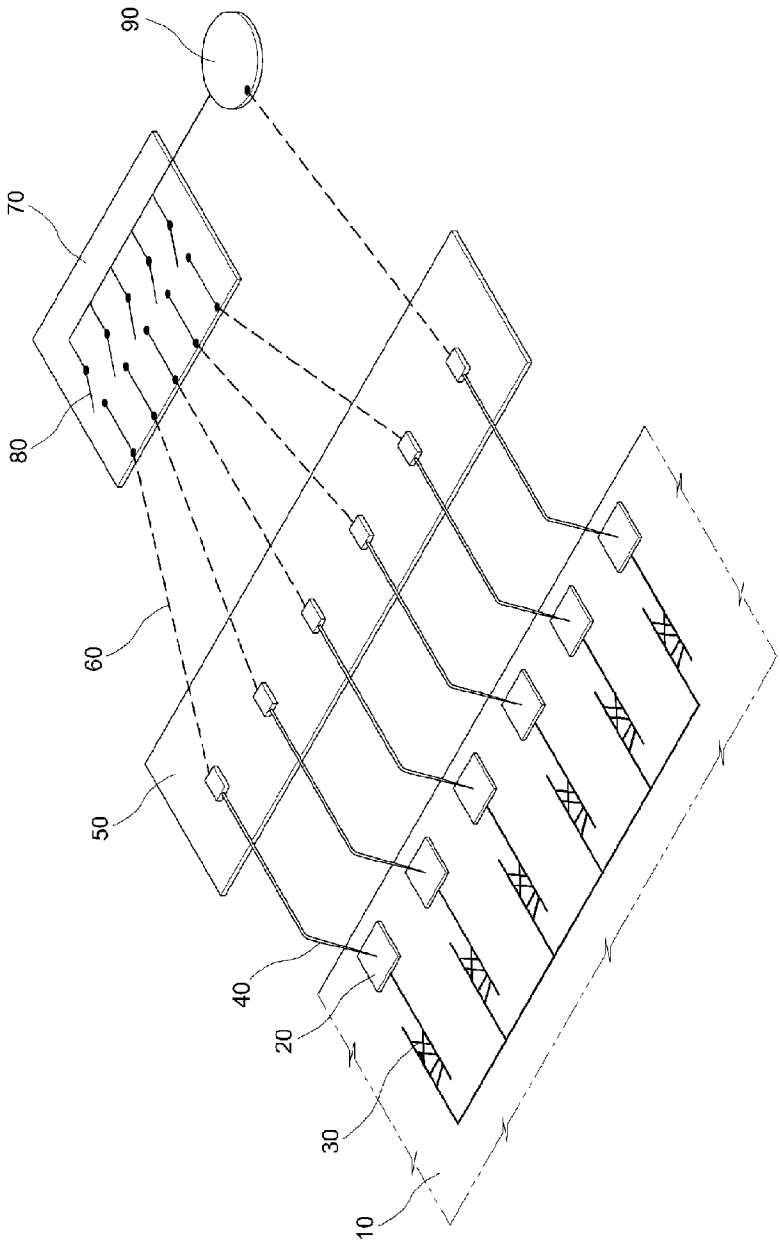
[Fig. 1]


20
30
20
10

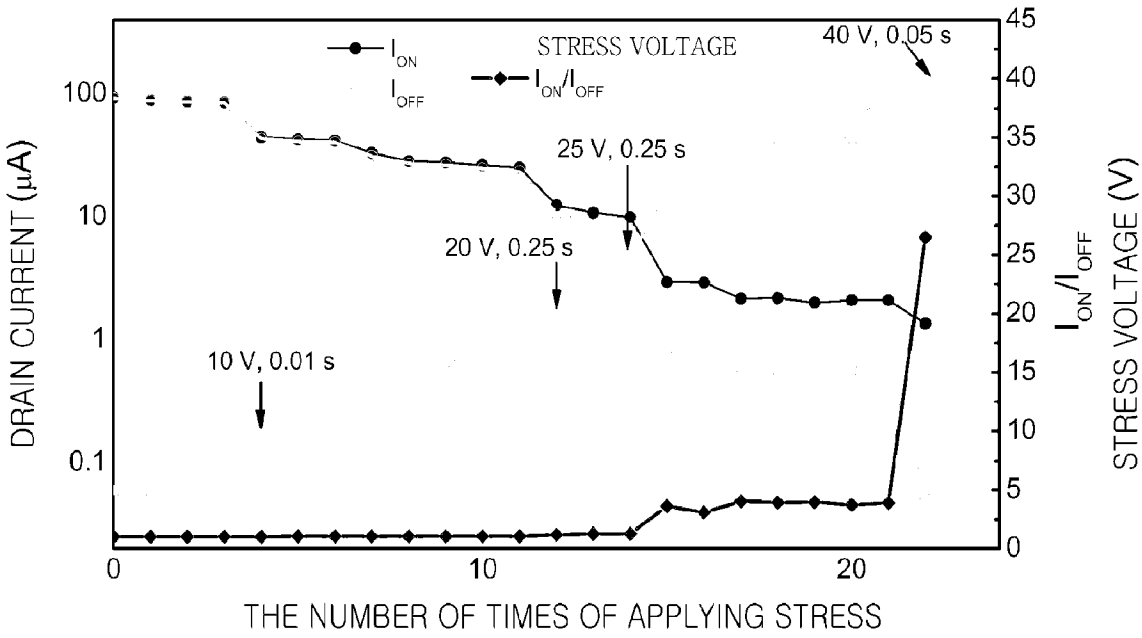
[Fig. 2]


MEASURE PERFORMANCE OF TRANSISTOR
S100
IS DESIRED PERFORMANCE ACHIEVED?
S200
YES
APPLY STRESS CONDITION
S300
IS DESIRED PERFORMANCE ACHIEVED?
S400
NO
CHANGE STRESS CONDITION
S500
YES
END
S600

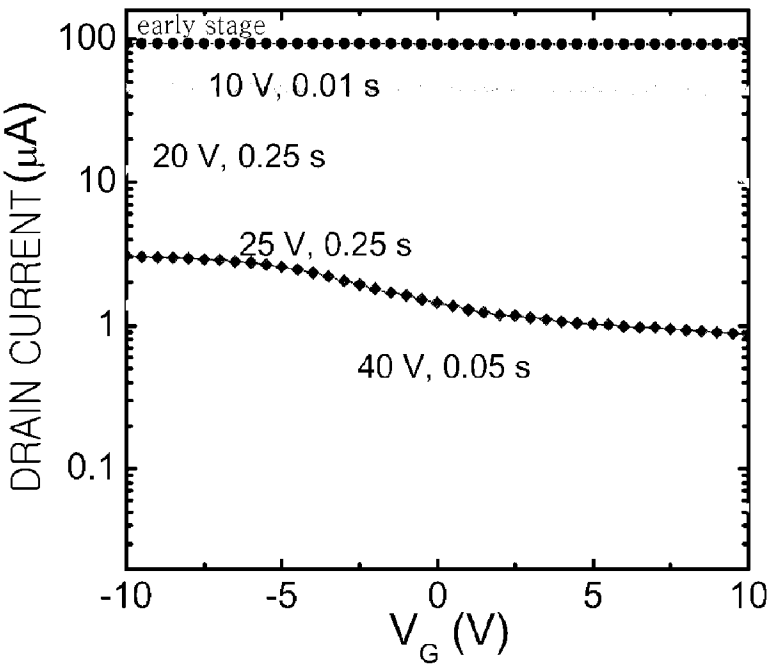
[Fig. 3]



[Fig. 4]


STRESS VOLTAGE
I_{ON}
I_{OFF}
I_{ON}/I_{OFF}
40 V, 0.05 s
25 V, 0.25 s
20 V, 0.25 s
10 V, 0.01 s
DRAIN CURRENT (μA)
100
10
1
0.1
0
10
20
45
40
35
30
25
20
15
10
5
0
I_{ON}/I_{OFF}
STRESS VOLTAGE (V)
THE NUMBER OF TIMES OF APPLYING STRESS

[Fig. 5]


early stage
10 V, 0.01 s
20 V, 0.25 s
25 V, 0.25 s
40 V, 0.05 s
DRAIN CURRENT (μA)
100
10
1
0.1
-10
-5
0
5
10
V_G (V)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR2008/001295

A. CLASSIFICATION OF SUBJECT MATTER

H01L 29/78(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 8 :H01L 29/78, H01L 29/786

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

KOREAN UTILITY MODELS AND APPLICATIONS FOR UTILITY MODELS SINCE 1975

JAPANESE UTILITY MODELS AND APPLICATIONS FOR UTILITY MODELS SINCE 1975

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKIPASS(KIPO internal) "carbon nanotube" , "transistor" , "channel" , "semiconductor"

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 7105851 B2 (DUBIN, VALERY M.) 12 September 2006 See the abstract; column 1, line 53 - column 5, line 63.	1-13
A	US 6891227 B2 (APPENZELLER, JOERG et al.) 10 May 2005 See the abstract; column 4, line 4 - column 7, line 26.	1-13
A	US 7247877 B2 (HAKEY,MARK C. et al.) 24 July 2007 See the abstract; column 3, line 36 - column 7, line 55.	1-13
A	US 4942441 A (KONISHI, NOBUTAKE et al.) 17 July 1990 See the abstract; column 3, line 27 - column 8, line 2.	1-13

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
30 SEPTEMBER 2008 (30.09.2008)	**30 SEPTEMBER 2008 (30.09.2008)**

Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/KR2008/001295

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