PATENT SPECIFICATION (11) 1 594 391

1 594 391

(21) Application No. 8074/78 (22) Filed 1 Mar. 1978 (19)
(31) Convention Application No 773311 (32) Filed 1 Mar. 1977 in
(33) United States of America (US)
(44) Complete Specification Published 30 Jul. 1981
(51) INT. CL.[3] H04Q 3/52
(52) Index at Acceptance
H4K 1A10 1A12 1A2 1A8 1H13 1W SD

(54) IMPROVEMENTS IN OR RELATING TO A TELECOMMUNICATIONS SYSTEM

(71) We, SIEMENS AKTIENGESELLSCHAFT, a German Company, of Berlin and Munich, Federal Republic of Germany, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:-

This invention relates to an electronic telephone switching system having peripheral units such as a plurality of subscriber and line circuits, a plurality of trunk and tie line circuits, at least one attendant line circuit, a plurality of signalling tone receivers and a plurality of link control circuits.

U.S. Patents nos. 3,904,831 and 3,943,297 describe a private automatic branch exchange (PABX) wherein subscriber line circuits signalling receivers, signalling transmitters and connecting sets of attendant stations or consoles and other special junctors are connected as input and output units to the horizontal lines of a switching matrix. Feeding sets, internal junctors or internal feeding sets, as the case may be, are connected to the vertical lines of the switching matrix. A connection between subscriber stations connected to the rows and other input and output units is established by operating the crosspoints at two matrix crossings. As an example, the connection of a subscriber station to a junctor circuit is established by closing the crosspoint switch at only one crosspoint of the switching matrix. The number of crosspoints is dependent on the number of wires to be switched.

Techniques for establishing connections between input/output (I/O) devices connected to the horizontal lines of the switching matrix by using a switching matrix having one or more stages and by through-connecting more than one crosspoint are exemplified by U.S. Patent no. 3,308,242 and British Patent no. 1,058,893. The latter shows that this form of connection may also be established by wires of a single switching stage of the switching matrix, each of which connects at least two crosspoints. In this regard, reference is made to the article, "Le nouveau system telephonique Trachsel-Gfeller a reflecteurs crossbars" in the Swiss publication *TECHNIQUE PTT*, 1955, No. 3, pp. 115-129, and to "Der X/53er-Schweizer Kreuzschienen Hausautomat" published in *HASLER-MITTEILUNGER OF HASLER AG*, Bern, No. 3, 1957, pp. 57-67, as well as to U.S. Patent No. 2,955,165. Various types of arrangements are employed in these known telephone systems, i.e., both directly controlled systems and those using common-control equipment.

In some of the aforementioned facilities, subscriber stations, as well as junctor and feeding circuits are to be scanned in successive cycles in accordance with the last-look principle. For example, it is known from U.S. Patents Nos. 3,904,831 and 3,943,297, when a subscriber originates a call which is to be identified during the scanning cycle, after assignment of a junctor and feeding circuit, to commence the further stages of the operation, such as transmission of the selection signals during the scanning cycle of the relevant junctor and feeding circuit in use. This means that the scan period of a junctor and feeding circuit must be comparatively long so as to be able to perform all the functions involved in the exchange of information between the junctor and feeding circuit and the connecting calling and called peripheral units, such as subscriber stations.

The transmission of signal tones (e.g., dial tone, busy tone or ringback signal) to the peripheral units, such as subscriber stations, is also accomplished during the scan period of the junctor and feeding circuit being used for the connection in question. The appropriate tone is connected by linking the tone generator via appropriate tone crosspoints to a junctor line circuit. Hence, tone-connection and speech-path crosspoints are provided. This prior art arrangement is exemplified by West German Auslegeschriften 1,079,685 and 2,111,787.

West German Auslegeschrift 1,079,685 describes a method of using a central tone generator whose tone signals are connected via tone-connecting crosspoints to a subscriber station; the tone-connecting crosspoints are opened and closed in synchronism with the system clock-pulse pattern for the tone (e.g., busy tone) to be transmitted. It can also be seen from West German Patent No. 2,111,787 (VPA 71/6033, filed March 11, 1971) that the tone signal is connected via a tone connection separated from the speech path connection to a repeater winding of the junctor and feeding circuit. In this patent, it is pointed out that the control circuit for the crosspoints of the tone connection is separated from the access circuit of the tone signal. It is likewise known in the time division multiplex (TDM) switching are to connect the tone during the sampling period for the junctor and feeding circuit.

The principal disadvantages of the known arrangements, such as those described in U.S. Patents Nos. 3,904,831 and 3,943,297 are as follows:

a. Greater complexity as a result of the two-wire switching in the switching network, particularly with regard to switching control, and supervisory means as well as greater complexity of I/O units and junctor and feeding circuits.

b. Since each sampling of peripheral units occurs only during the normal periodic sequence of the scanning cycle, either the quantity of information to be exchanged during each scan or the number of I/O devices that can be connected as well as of the junctor and feeding circuits, is considerably reduced because of the long period required for scanning these circuits.

c. Considerable technical effort is needed to permit the exchange of information, via the junctor and feeding circuits, with the units connected thereto while they are being scanned.

d. This is all the more difficult, since access is possible only via the switching matrix by scanning the horizontal lines of the switching matrix.

e. Since tone connection via the tone switching matrix is likewise a function of the scan period of the junctor and feeding circuits, this means an additional load for the outlay required for establishing the connection during the scan period of a junctor and feeding circuit.

According to this invention there is provided a circuit arrangement for an exchange in an electronic telephone system, said circuit arrangement including a first switching network for establishing connections between selected subscriber circuits and a second switching network for establishing connections between selected tone generators and selected subscriber circuits via said first switching network, each of said switching networks having crosspoint switches, a link control circuit being arranged to control interconnection via said switching networks, crosspoint switches of the second switching network having first electrode lines connected to second electrode lines of crosspoint switches of the first switching network, said first and second electrodes being of opposite polarities so as to provide a series circuit via respective interconnected cross-point switches of the two switching networks, said link control circuit providing a connection to an attenuation point between the first electrode line and said second electrode line of each interconnected pair of lines, said link control circuit having means for determining the attenuation of speech circuits via said second electrode lines by control of said attenuation point, said attenuation determining means being a control input to which a control signal can be applied to determine said attenuation.

Embodiments of the invention will now be described, by way of examples, with reference to the accompanying drawings wherein:-

Figure 1 is a schematic block diagram of a PABX system in which the switching arrangement of the invention is utilised;

Figure 2 is a schematic diagram of a known 4×4×2 switching matrix illustrating crosspoint switching activation in a matrix of this form;

Figure 3 is a schematic diagram of a crosspoint switching module which can be used with the Figure 2 switching matrix;

Figure 4 is a schematic diagram illustrating an 8×4×1 switching matrix achieved through a rearrangement of the 4×4×2 matrix and using the Figure 3 switching modules;

Figure 5 is a schematic diagram of an 8×4×1 switching matrix wherein crosspoint connections are completed through separate activation of thyristors in a thyristor switching module;

Figure 6 is a schematic diagram illustrating the connection arrangement of wires *al*, *sl* and *tl* (Figure 1) to a link control circuit (e.g., J2) in the Figure 1 embodiment;

Figure 7 is a detailed schematic diagram of a trunk line circuit (e.g., TLU) used in the Figure 1 embodiment;

Figure 8 is a schematic block diagram illustrating the connected relationship between the customer and programme memories in the Figure 1 embodiment;

Figure 9 is a detailed schematic diagram of the circuitry for selecting customer memory locations for the performing of "readout", "write-in" and erase operations in connection with the customer memory in the Figure 1 embodiment;

Figure 10 is a detailed schematic diagram of apparatus for applying data signals to the storage locations M1-8 of the customer memory in the Figure 9 embodiment;

Figure 11 is an extension of the circuitry illustrated in Figure 10;

Figure 12 is a detailed schematic diagram of the peripheral conversion and storage device (PC) in the Figure 1 embodiment and of its connections to the faster rise time pulse transmitting bus line group (HSB) and the lower rise time pulse transmitting bus line group (LSB) therein, and

Figure 13 is a detailed schematic view of the attendant's station (AC) and connecting circuitry (ALC) in the Figure 1 embodiment.

Embodiments of the invention will now be described with reference to a preferred embodiment of a programme-controlled PABX which can be assembled from conventional electronic components generally employed in data processing systems and in particular in centrally controlled telecommunications switching systems. However, certain of these commercially available components may need to be modified for use and assembly into the PABX described here, and where necessary the components are described in detail in the following description below.

System Description

The PABX described below and illustrated in Figure 1 operates according to the principles of a system wherein the subscriber line circuits (SLC1 to SLC*n*), the tie line circuits, interexchange trunk line circuits and interoffice trunk line circuits, such as trunk line circuits TLU, tone-frequency signal receivers R-T*f* and connecting circuits ALC of an attendant's station AC are scanned in a periodic sequence so as to determine, on the basis of the last-look principle, if the last operating condition has changed. The last-mentioned four types of circuits and link control circuits J1 to J*m*, tone generators TG1 to TG*x*, and the logic control unit for service SVS are likewise interrogated directly by means of address code (polling) during idle periods, i.e., during time intervals between two scan periods per address code. This is necessary in order to receive data or transmit instructions to any one of the seven types of circuits mentioned above.

The one-at-a-time principle always applies to the reception and transmission of data and instructions and to the scanning of circuits. The circuit to be scanned is selected by a data processing unit CPU on the basis of a conventional programme stored in a programme memory PM, which is a constituent part of central programme control CC. In one scan all peripheral units and other scan devices are scanned one after another. The scan periods are so chosen that there are free times after each period. In these free times for each period each of the peripheral units and also memory spaces will be operated by sending the individual address code of that unit or space via the data bus line, e.g. bus line *d a*; in this specification this is called "polling" a unit or line or memory space.

If more idle time exists in a scan period than is needed, particularly during light-traffic periods, these idle times can be used for performing service and test procedures. This is discussed in greater detail below.

Switching network SM of the system may consist of one or more stages. In the present example, it is assumed that the switching network for switching the speech paths to the subscriber line circuits, to the interexchange trunk line circuits and to the attendant's station as well as to the tone-frequency receivers is single-stage. This means that two crosspoints in a column must be operated in known manner to interconnect two subscriber stations or to connect one subscriber to one interexchange trunk line circuit. In the system under consideration, the switching network for switching the speech path and the speech path itself have one wire. Thyristors are employed as crosspoint switching elements. These thyristor crosspoint elements are operated respectively during the scan periods of the subscriber stations or during the scan periods of the link control circuits, whereby the latter are not scanned in a periodic sequence, but are polled by their addresses.

The crosspoint switches are switched on and off by polling the crosspoints of the crosspoint switch used for connecting a subscriber line circuit to a holding circuit via bus line LSB/*dt*. The switching elements used in the system and the control principle as well as various basic functions will be described below.

The central control unit CC of the system comprises a central data processing unit CPU of conventional construction which controls all necessary processes in the system - particularly those for scanning and polling the peripheral units - necessary to receive and to process information as well as to dispatch and transmit instructions.

To handle these processes, a central data processing unit CPU is provided with a scratch pad memory SPM with variable content. This means that this scratch pad memory SPM is always kept current on the last status of the data concerning the existing conditions of the subscriber line circuits, line circuits, crosspoints, etc. Furthermore, the central data processing unit CPU is provided with the programme memory PM, in which the available programmes are stored, and with a customer memory CM, which at least contains the data specific to the subscribers, various line circuits and other peripheral units and circuits. If necessary, this memory CM may be polled by the central data processing unit CPU. The customer memory CM is variable, i.e., the data for subscribers and other peripheral units and circuits are input manually through selection via a peripheral maintenance circuit MC. These are known circuits and not relevant to this invention so that they are not described in detail herein.

The transmission of data and instructions as well as addresses to or from the central data processing unit CPU, programme memory PM, customer data storage CM, scratch pad memory SPM and test circuit TC can be accomplished on the bus lines HSB which carry faster rise time pulses than on bus lines LSB. The interrogation of the centralised units and decentralised circuits is effected via the bus lines HSB for addresses HSB/*da'*. The speed of data transmission on both kinds of bus lines is equal. The faster rise time pulses have a faster rise time at the leading edge because, in the input circuits of the HSB bus line, TTL components are used. In the LSB bus lines MOS components are used; therefore we have in this case lower rise time pulses. The advantage is that in this case the required performance is lower as are reflections if there are long connecting lines.

With regard to the transmission of data and addresses or the reception of data from the peripheral and other units, it must be stated that these operations are effected by lower rise time pulses as in the central control unit CC. Hence, the peripheral conversion and storage device PC is provided, which establishes the connection between the faster rise time pulse transmitting lines HSB and the lower rise time pulse transmitting bus lines LSB. The construction and operation of these bus lines, units and circuits are described in detail below:

Decimal Dial Pulsing and Voice-Frequency Code Dialling

The PABX system described above employs telephones with decimal dial pulsing, as well as those using voice-frequency code dialling. To be able to distinguish the subscriber stations using different modes of dialling from each other, those stations are identified with a special bit code in the customer memory CM.

The subscriber stations using pushbutton dialling all have a tone signal generator so as to be able to send voice-frequency dial signals. In the present example each dialled digit of a telephone number will be represented by two out of seven or eight frequencies. In each case, regardless of whether dial pulsing or voice-frequency dialling is provided, the first digit of a dialled code is passed to the central data processing unit CPU, which can compare this digit information with the data stored in the customer memory CM so as to find out what type of dialling is needed to extend the call to the desired telephone or interexchange trunk line.

Conventional AND/OR elements are employed as comparator and evaluator circuits. If the interexchange trunk line circuit gives access to a system based on decimal dial pulsing, the selected digit must be converted. This occurs in the occupied interexchange trunk line circuit. In the case of internal calls, no conversion takes place, but the coded signals dispatched from the subscriber station are passed as voice-frequency signals directly from the tone generator of the subscriber station via the speech path and the appropriately operated crosspoints of the speech path network to voice-frequency signalling receiver R-T*f* and the central control unit. The transmission is accomplished in an appropriate signal code of the central data processing unit CPU of the central control unit CC via the data bus lines LSB/*dr* if information for the marking of the crosspoint is complete.

As mentioned earlier, if necessary the two frequencies supplied from a subscriber station using voice-frequency dialling are converted in the interexchange trunk line circuit occupied, but firstly the first code digit will be converted in the voice-frequency signalling receiver R-T*f* and then passed to the central data processing unit CPU for evaluation purposes, and then, for an external connection, the trunk line circuit will be seized. The latter retransmits the further dialled information via the corresponding interexchange trunk line. If necessary, the voice-frequency signals are converted in the interexchange trunk line circuit, e.g., into decimal dial pulses, which are routed via speech wires in known manner. These pulses are functions of the system frequency, i.e., dependent on the system timing device.

The type of conversion of two-frequency signals into decimal dial pulses is effected in a manner as is known for telephone systems with both types of dialling options.

Programme Control Unit PM, Data Processing Unit CPU, Scanning, Polling

The following description relates to the instructions defined in a programme for execution by the central processing unit CPU. These instructions control all functions in the peripheral switching units. The peripheral switching units include, for instance, the subscriber line circuits SLC1 to SLC*n*, the interexchange trunk line circuits TLU, the voice-frequency signal receivers R-T*f*, connecting circuit ALC for attendant's station AC, as well as the tone generators or tone converters TG1 to TG*x* and the crosspoints of switching network SM and the associated link control circuits J1 to J*m* provided in each column. A specific programme listing is not given herein, but it can be readily derived from the functions and operating sequences described hereinbelow.

The central processing unit CPU transmits a number of signals to the peripheral units such as specific clock signals, intermediate information, addresses and class-of-service signals. All these types of data are available in the semi-permanent scratch pad memories SPM and customer memory CM. The central data processing unit CPU receives, at a rate of 80 times a second, the status of each subscriber station (e.g., S1), of each interexchange trunk line circuit (e.g., TLU), of each voice-frequency signal receiver R-T*f* and of each connecting circuit ALC of an attendant's station AC. This means that each unit is scanned 80 times a second, i.e., about once every 12.5 milliseconds, so that after data transmission, the rest of the 12.5 milliseconds can be used for other functions as described below.

When the status of one of the above mentioned peripheral units and circuits has changed in relation to the last status ("last look"), this information is received in the scratch pad memory together with the address of the peripheral unit or circuit. During the next idle period of the scanning cycle the central data processing unit CPU can be interrogated by polling the particular unit or circuit concerned to identify the data stored and dispatch the necessary instructions. Data are received from the central data processing unit CPU via the bus lines LSB/*dr*, LSB/*dt* and the peripheral conversion and storage device PC. If an excessive number of peripheral units or circuits or crosspoints, as well as link control circuits, wait for service by the central processing unit, and the free time in one period of the scanning cycle is not long enough for handling all request stored, the rest of the processing is done in the next idle time of the first following period of the scanning cycle. The central data processing unit in such a case continues its polling operation for the unit waiting for service in a sequence defined by the programme in the programme memory PM. This sequence is based on a predetermined definition, using well known criteria, of the priorities or class-of-service and type of incoming data resulting, for example, from the changes in status of a peripheral unit or circuit.

The following description demonstrates, as mentioned in the preceding paragraph, that the described PABX distinguishes between the normal scanning cycle and the polling of peripheral units and circuits whose addresses are available together with data in scratch pad memory SPM. The central data processing unit CPU must operate on the data of the particular peripheral unit or circuit concerned in order to be able to execute instructions for subsequent operations, e.g., the establishment of a connection for that unit or circuit. This may be the connecting of the calling station S*n* via subscriber line circuit SLC*n* and the speech path network SM to the interexchange trunk TL via an optimum route. The connection via the speech path network SM is established by operating two crosspoint switches in a column, e.g., *k*2 and *k*3 in Figure 1. The speech path network SM is shown as only having one stage, but a greater number of stages may be used.

The polling of peripheral units and circuits by transmitting the address of this unit or circuit via the wires *dt* of the data bus lines LSB in the free time intervals of scan periods in the scanning cycle is a characteristic feature of this embodiment. The advantage of this technique lies in the fact that the entire system can be run with a single micro-computer of known construction. In the case under discussion the computer is the central data processing unit CPU, which processes the incoming data and provides the instructions. Thus, a minimum number of additional modules and circuits are required. These advantages are facilitated by ensuring that the scanning and interrogation operations occur within the time pattern of the clock pulse generator SC.

Another important factor is the single-wire speech path to be switched via the speech path network SM. This single-wire speech path is switched, preferably, by means of thyristors. Such speech path switching has many advantages for the system described herein, as will become apparent from the following description.

From the above it follows that the respective time periods for the scanning and polling may be in either the same of in different time periods in the scan cycles. The central processing unit CPU controls these operations so that first the scanning and then the polling operations are carried out one after another in the same time period of the scan cycle.

Speech-path and Tone Crosspoint Switches

As mentioned earlier, voice communication between two subscriber stations or between one subscriber station and an interexchange trunk line circuit is established by means of the switching speech path matrix SM by operating two of the crosspoint switches in a column. If, in addition, transmitted pulsing signals must be converted, a third crosspoint switch in the same column must be operated with a view to connecting an appropriate voice-frequency signalling receiver T-R*f*. The same is true if, for example, the exchange operator must cut into an existing connection, in which case the necessary connection can be established by additional operation of the contact located in the column which has been occupied for the connection between the calling subscriber and the trunk line circuit. Such interconnection of subscriber stations, interexchange trunk line circuits, receivers and operator's positions by operating two or more crosspoint switches disposed in a column is known and is found, for instance, in time division multiplex systems by simultaneously closing two or more switches having the same pulse position.

The technique of applying tone signals by means of a special tone signal switching matrix is exemplified in West German Patent no. 2,111,787, as mentioned above. However, in the embodiment described herein a special feature of the tone connection mode lies in the particular way of connecting the tone by using single-wire switching matrices, i.e., a single-wire speech path switching matrix as well as a single-wire tone switching matrix. The special nature of this tone-signal connection to the speech path is essentially formed by the control leads for the crosspoint which is to be through-connected.

The general system description shows that the essential current rise needed for through-connecting via the crosspoints is brought about by the current sink for the speech path crosspoints in the subscriber line circuits or interexchange trunk line circuits and for the tone-connection crosspoints in the link control circuits. The through-connection is provided by one of the link control circuits J1 to J*m* for the speech path crosspoints as well as for the tone crosspoints. Each link control circuit is assigned to a column of the crosspoints of the speech path switching matrix and to a row of the tone signal switching matrix. However, only one separate output is provided in the relevant line circuit to achieve the necessary switching.

The tone generators TG1 to TG*x* convert the square wave pulses received from the central clock-pulse generator SC into sinusoidal signals made up of one or more frequencies.

In order to through-connect the crosspoints, the various circuits such as the subscriber line circuits, the interexchange trunk line circuits and the connecting circuit, as well as the link control circuits and tone generators, are polled from the central data processing unit via the address lines during the idle times of scan periods. To disable the crosspoints, new polling with an accompanying disabling instruction is necessary. This is also essential with a view to the tone-signal transmission since in this case, in addition to the tone-signal identification, one must indicate what clock pulse is involved to enable the tone to be removed in conformity with the ON time and OFF time.

Figure 1 shows that via line *t*1, which represents the cathode line for the tone crosspoint switches *tk*1 and *tk*2 disposed in one column and which is polled via the link control circuit J2 (current sink), the connection of the tone to anode line *a*1 of speech path crosspoints *k*4 to *k*7, disposed in the corresponding column of the network SM occurs via a bypass capacitor (e.g., C). If, for example, one views the connection of a tone signal from the tone generator or tone converter TG1 to the line connected to subscriber S1 via the crosspoint switch *k*4, this connection requires operation of the tone crosspoint switch *tk*1.

To achieve this, the cathode line *t*1 must be accessed from the link control circuit J2, the anode line *ag*1 from tone generator TG1, and the control electrode from the tone generator TG1 via the control wire *s*1. The accessing occurs by polling the tone generator TG1 and the holding circuit via the address lines "*da*" of the data transmitting bus line LSB and the address output unit AX of the peripheral conversion unit PC. The latter unit and, thus, the address output unit AX receives the addresses of the tone generator to be accessed and of the line circuit to be accessed from scratch pad memory SPM under the control of the data processing unit CPU. The scratch pad memory SPM receives its data allocated to individual connections from the customer memory CM, in which signal-connection and delay signals for each tone generator are stored. It is there indicated which tone signal must be transmitted to which subscriber and which link control circuit is used. The activation of the crosspoint switches is effected by polling in the same manner as the corresponding transmitting of information.

The information as to which tone signal must be transmitted yields an instruction for the tone connection and removal as a function of a central clock generator SC. This means that the tone crosspoint switch is closed and opened as a function of connection and removal instructions. A tone generator is assigned as a tone converter to each kind of clock pulse.

As will be described below, the data in the customer memory may be altered via a maintenance circuit MC and the bus lines LSB/HSB by keying or dialling in, so that clock pulses assigned to a tone generator, too, can be varied.

In connection with this application of the tone signal, there must be assurance that only one tone signal at a time wll be applied to a specific connection. Double connections are not possible without faulty activation of crosspoints in the circuit arrangement described herein.

Alteration of Clock Pulses for Existing Signals or Initiation of New Signals

The clock pulses of the signals to be transmitted are determined by appropriate control of the tone-connection crosspoint switches. Through-connection, as well as disconnection of the crosspoint switches is dependent on polling of each crosspoint and one of the corresponding transmitting of instruction signals. The clock pulses associated with a given tone signal, e.g., calling signal, busy signal, etc. are stored in the programme memory PM and are polled with each activation of a tone-connection crosspoint for the first (e.g., "ringing tone") connection during a call to be established, as a function of the ringing tone connection instruction from the central data processing unit. In addition to this timing information, i.e., "calling signal", the scratch pad memory SPM will store the further connection data of the calling connection, such as the subscriber address and the tone generator address. The timing information contains data on the initiation and end of the clock pulse and on the different forms of signal, i.e., the purpose of the signal, such as ringing, for example.

In order to have the option of changing the clock pulses (preprogrammed in the system) of specified signals (e.g., ringing) as well as initiating new tone signals, the programme memory PM must either be programmable in a simple manner or the timing of specified signals must be stored in the customer memory CM assigned to the tone generator instead of in the programme memory and have facilities for interrogation there. In any event the customer memory CM is available as a store that can be changed at any time, i.e., a random access memory (RAM) may be used.

It should be noted that each of the tone generators is allocated according to the different frequencies and not to a specific signal (e.g., the ring signal). The connection of special devices, such as tape recorders and also other data devices, may also be effected over one or more special tone generators in the speech path.

Dictating machines, television sets for conferences, data terminals, etc. can be connected with the speech and/or special matrix like the other peripheral units. The relationship of converters containing tone generators to specific clock pulses simplifies the control of the tone-signal crosspoints and leads to savings in memory capacity. The central clock pulse generator SC is employed to synchronize the instructions dispatched from the central data processing unit CPU with the clock pulse available in the system.

Control of Crosspoint Switches in the Case of Single-Wire Switching

Thyristors are preferably employed as crosspoint switches in the system described herein, and these are combined in a switching network to form a switching matrix in the manner to be described below. Referring to Figure 2, the switching matrix shown is a 4×4×2 crosspoint switch, i.e., a matrix having 4×4 dielectrically insulated thyristor modules disposed in 4 rows and 4 columns and with two thyristors per crosspoint. Thus, two-wire switching of speech paths is possible.

If in the described system the same switching matrix is employed for single-wire switching, it must be modified appropriately so as to activate the crosspoints, assuming the use of the same crosspoint switching devices. Thus, the switching matrix is to be modified to form an arrangement with 8 rows and 4 columns and one crosspoint switch per crosspoint, i.e., with 8×4 thyristors with one crosspoint each, or 8×4×1.

Figure 2 illustrates the activation of the crosspoint switches in the known 4×4×2 matrix. The column in which the crosspoints to be activated are disposed is determined by means of one of the two control leads 1 or 2 in columns A, B, C or D, and the row is determined by means of one of the control leads 1 or 2 in rows W, X, Y or Z. Both thyristors disposed at a crosspoint are through-connected, not only in the presence of the corresponding control signals on the control leads for the determination of the row and column, but also only after previously turning on the appropriate cathode and anode potentials.

Figure 3 illustrates the construction of a thyristor module forming a crosspoint switch.

In order to obtain a 8×4×1 matrix for the telephone switching system described herein, the existing 4×4×2 matrix must be rearranged. To achieve this, the thyristors through-connected via the anode A1 (Figure 3) are followed by those disposed in a column coordinate and through-connected via the anode A2. This is shown by a dotted line in Figure 4 between the thyristors T*h*1 and Th5. At the same time, and also connected in parallel with the cathode inputs 15 and 22 of the thyristors Th1 and Th5, a connection to the control lead W is established via the diodes WD1 and WD2. This control lead W is intended for selecting the row in which a crosspoint is to be operated. This is to ensure that only the thyristor which is determined via a cathode input (e.g., 15) and the input (e.g., W) of the control lead, as well as via the column control lead (e.g., A) can be activated or through-connected. To determine the relevant column, input A, B, C or D is provided without change.

Figure 5 shows an arrangement for a switching matrix which does not require correlation between two thyristors and a thyristor module. In Figure 5, the diode arrangements (WD1, WD2) and associated connections (shown in broken line in Figure 4) are omitted for the sake of clarity. It shows that by connecting in parallel the thyristors associated with a column, coupled with the possibility of separately activating the two thyristors associated with a given thyristor module, the existing 4×4×2 matrix can be converted into a 8×4×1 matrix.

To operate a crosspoint switch in this manner, the following processes can be executed: select a subscriber station (e.g., S1), thereby selecting the subscriber line circuit and turning on the cathode potential, e.g., across 22 (the current-sink circuit remains energized even after closing until opened by a separation instruction); at the same time determine the row, then select a holding circuit (e.g., J2) interrogating it and connecting a control signal (e.g., to line E1), and at the same time determine the column. In this way, each through-connection in the switching matrix occurs when the anode potential (e.g., across A1) is turned on (Figure 1).

It is apparent from the above that the connection of the cathode lines W1, W2 via the diodes WD1, WD2 with the control leads W permits single-wire switching via the particular matrix. The diodes WD1 and WD2 prevent crosstalk.

Link Control Circuit

By means of one of the link control circuits (e.g., J1 in Figure 1) there occurs the activation of the speech-path crosspoint switches as well as the connection from the anode line to the cathode line via a through-connected thyristor and the tone-signal connection via an additional (likewise through-connected) tone crosspoint switch and its cathode line (as shown in Figure 1). In addition, the link control circuit facilitates an appropriate regulation of attenuation and when a speech-path crosspoint switch is operated, it signals the corresponding matrix module.

Figure 6 shows the scheme for connecting the wires *a*1, *s*1 and *t*1 to the link control circuit (e.g., J2). The current sink of the link control circuit is labelled CS. As shown, the wire *t*1 is connected to the base of the tone-crosspoint thyristor TK1. The control wire for the speech-path crosspoint is labelled *g*. The point JA2 is the scanning point for the crosspoint; that is, it is the point activated via the interexchange trunk and PBX-power-lead line circuit so as to through-connect or disable the particular crosspoint concerned. In the control connection to the point JA2 there is likewise connected a photo coupler CR intended for signalling the operating condition to a module when the crosspoint is activated. A loss pad TK3/TK5 is connected to the anode line *a*1 of the speech-path crosspoint. This pad TK3/TK5, which activated or not by the common control unit CC as a function of the form (i.e., short or long) of the connected interexchange trunk line, is connected with anode line *a*1 of the speech-path crosspoint. This pad is needed whenever short lines are connected. In the present instance, the attenuator circuit causes an interposition of an additional resistance of about 300 ohm.

A capcitor arrangement CE forms a connection to the anode line over which the tone signal is linked to the speech path (C in Figure 1). It should be noted that the anode line is connected to all speech-path crosspoints disposed in a single column. To establish voice communication at least two such crosspoints must be operated. Hence, it follows that, depending on the number of operated crosspoints a signal can be transmitted via the capacitor and tone-signal connecting point to one or more subscribers, for example not only to the calling or called party, but also to other parties wishing to be invloved in the same connection.

It should also be noted that the activation of the loss pad occurs via the wire EV2 by interrogation via the bus line LSB for signals with lower rise times.

As mentioned earlier, the crosspoint switch of the tone switching network is operated in synchronism with the prescribed clock pulse pattern. This is done through activation via the control wire *s*1 by applying appropriate connection and removal signals from the central data processing unit CPU over the data transmission circuit.

The Trunk Line Circuit (Figure 7)

The following is a description of the functions of a trunk line circuit, such as the circuit TLU in Figure 1. In the trunk line circuit seizure may be effected from the trunk line, i.e., from the general switched telephone network both with a "ground start" and with a "loop start".

Referring to Figure 7, if in the idle condition no potential whatever is applied to the tip conductor *a* an incoming seizure can occur by connecting ground potential ("ground start"). By connecting this ground potential in the case of an outgoing seizure, the acknowledgement signal is received from the exchange side. In the case of the "ground start", a negative potential (−48 volt) is continuously applied across the ring conductor *b*. In the case of a "loop start", ground potential is continuously applied from the exchange side to the tip conductor, while −48 volt is continuously applied to the ring conductor. In such a case, seizure can only occur by transmitting an alternating current ringing signal. The processes in connection with both modes of seizures will be described below. Since it must be possible to connect a PABX trunk link circuit with an external line circuit in an external public telephone network by means of the first mode (ground start) as well as by means of the second mode (loop start), the trunk line circuit must always be connected in such a manner that both seizing modes are equally feasible.

The external line circuit lines enter the PABX trunk line circuit on the right-hand side, both speech wires *a* and *b* (tip and ring) being connected to the trunk line and, therefore, to the external telephone network while the wires shown on the left-hand side represent the address circuits and the data circuits as well as one (*g*) of the two speech wires which are connected to the PABX internal wires. The other wires, particularly the signalling wires 1 to 6, are connected to the data transmission circuit group LSB for the data, address and information exchange with the central data processing unit CPU. The exchange side of the external trunk line is designated as the secondary winding of a transformer LU and must be suitable for any external exchange-side connecting and ringing mode.

Trunk Line Circuit with Ground Start

In the idle condition the transistor T1 is switched on via the signalling wire 4 due to the potential applied and remains energized via a conventional holding circuit not shown in detail. Upon scanning the trunk line circuit, its idle condition is recognised because of the existence of the holding circuit.

If the incoming seizure in the case of a ground start occurs through application of ground potential to the tip conductor, a loop in the trunk line circuit is activated via the ring conductor and is connected from the tip conductor via the bridge rectifier G, not only directly via the photo coupler L1 to the ring conductor, but also via additional circuits connected in parallel in which are disposed, inter alia, a diode D1, a resistor R1 or the transistors T2 to T5. The resistor R2 and a pair of diodes D2 are likewise connected in one of these additional circuits. Due to the activation of the photo coupler L1/T6, the transistor T6, which is under the influence of the photo coupler, is activated via the +12V potential and resistors R3 and R4, as well as via resistors R5, R6, R7 and the amplifier V1 is activated to provide an output signal on control lead 7. Parallel circuits still exist via the capacitor C1 and the resistor R8. The trunk line circuit is indicated as occupied by the data processing unit CPU via wire 7. Transistors T1 and T6 are conductive. This is valid as an indication that a seizure with ground potential has taken place (ground start).

If an alternating current ringing is simultaneously transmitted from the external public network upon application of ground potential to the tip conductor, the transistor T7 in the circuit is also switched on via the resistors R9, R10, R11 and the capacitors C2, C3 as well as the diodes D3 to D5. The detection of the ringing signal in the trunk line circuit is necessary, since the disconnection of the ringing signal, when the called subscriber in the PABX answers, must be controlled by the trunk line circuit. Upon simultaneous transmission of ground potential via the tip conductor and the ringing signal, the evaluation of the ground potential for seizing purposes is likewise effected by the evaluating circuit via the photo coupler L1/T6, thereby activating transistor T6 in the manner specified above.

When the called PABX-subscriber answers, this is detected by the data processing unit CPU upon scanning the trunk line circuit. When the PABX-subscriber answers, the transistor T8, as well as the relay K4, are activated via the wire 1 and the gate G1. Moreover, the transistor T12 is switched on via the wire 6. As a result, the photo coupler L3/T9 is activated and thus, the transistor T9, which is connected to the resistor R12 and the capacitor C4 in the Graetz bridge rectifier G, is switched on. This causes the direct current flowing through the tip and ring conductors to rise more than tenfold (e.g., from 2 mA to 26-35 mA). This D.C. current rise is detected in the external telephone network as answering, causing the ringing signal to be disconnected.

During the conversation, the above mentioned transistors T9, T2, T3, T4 and T5 as well as T1, T8, and T6 remain conductive.

To release the connection initiated by the subscriber to the external telephone network the potentials are turned off from the ring and tip conductors. However, the free indication occurs with a time lag so as to prevent an immediate new seizure and to first ensure an internal full ressetting of all switching elements seized and operated. Subsequently, only if the circuit is switched through via the transistor T1 is a new seizure permitted.

If the connection being established is an outgoing seizure from the trunk line circuit, the transistor T10 is switched on via the wire 5, and the relay K3 is activated upon detection of the off-hook condition of a calling station and concurrent detection of the idle condition of the trunk line circuit after the trunk code has been selected. The current-sink circuit CS is connected to render the ring conductor operative through contact $1k3$ with the result that the current for the ring conductor rises to about 50 mA. At the same time, a potential is applied to the tip conductor by switching the contact $2k3$, that is, a loop established via the photo coupler L1 (T6) and the Graetz bridge circuit G between the tip and ring conductors. If the line circuit of the external public telephone network has detected the increase in current to the ring conductor as a seizure, ground potential will be applied to the tip conductor as an acknowledgement signal, activating the photo coupler L1/T6, so that transistor T6 is again rendered conductive. As a result of this circuit condition (i.e., conducting transistors T1, T6 and T10), a ringing tone is also transmitted to the calling party so as to indicate the seizure of the external telephone network. The dial signals now selected by the subscriber station of the PABX are transmitted via the wire 3 to the photo coupler L3/T9 and from there to the transistor T9, so that appropriate increases in potential corresponding to the transmitted dial signals are sent to the tip conductor. These potential increases are passed to the external telephone network and further evaluated there.

In the case described above, the photo coupler L1/T6 and, hence, also the transistor T6, are controlled during the transmission of the dial signals with the result that the potential applied to the wire 7 would also vary continually. However, in the present case the wire 7 must remain on a sustaining potential, and the diode D is provided to achieve this. With the diode D6 the drawing of continuous current at the end of each dial pulse from the input of the gate G2 coming from the wire 3 is assured. In this way, the unwanted potential change on the wire 7 is avoided.

Upon completion of the call, the connection is released as described above.

Trunk Line Circuit With Loop Start

If, instead of the seizure of the PABX from the external telephone network with application of ground potential to the tip conductor ("ground start"), the seizure from the telephone network is effected with a "loop start", ground potential is continuously applied to the tip conductor, in idle condition, and a negative potential to the ring conductor. The incoming seizure from the telephone network occurs exclusively through the application of the alternating current of the ringing signal. In this case, a current rise occurs in the circuit that detects the application of ground potential in the case of a ground start with the result that, in addition to the photo coupler L1/T6 and the transistors T2, T3, T4, T5 and T6, the transistor T7 is also switched on. The resistor R7 therefore will be lower as for the ground start condition. The increase in current caused by the ringing signal initiates with one half-wave the activation of photo coupler L1/T6 and with the other half-wave that of photo coupler L4/T13, alternately controlling transistors T6 and T13. Thus, an output signal is also applied alternately to wires 7 and 8. It should be noted that the circuit via transistor T7 represents a controlled function for photo coupler L1/T6, ensuring its satisfactory response.

As explained earlier, answering the subscriber of the PABX causes photo coupler L3/T9 and relay K4 to be activated. A speech circuit is established by means of contact K4 via the secondary winding of transformer U, and transistor T9 and hence also T11, are switched on via photo coupler L3/T9. As described earlier, the direct current is increased more than tenfold via the speech wires. This involves the activation of the current sink. In the external telephone network this is detected as an answering by the called party and the ringing signal is cut off. The release occurs after establishment of the call condition, as explained above.

If seizure of the trunk line is effected by the calling party, when data processing unit CPU detectors the removal of the receiver by the calling party during a scanning cycle, the signal is disconnected from wire 4 and, instead, a potential is applied to wire 7. This causes transistor T12 to be switched on, thereby activating photo coupler L3/T9 and transistor T9. As a result, the current through the speech wires is increased, which increase is interpreted in the external telephone network as a seizing signal. This network does not return an acknowledgement signal. The increase in current acts on photo coupler L1/T6, with the result that a signal is applied to wire 7. This is detected by data processing unit CPU during the scanning of the external line circuit. After detection of the seizing signal in the external telephone network, a dial tone is sent to the PABX. As described above, the transmission of the dial signals, e.g. DC dial signals, occurs by generating current rises in the speech wires via transistor T12 and photo coupler L3/T9. Release follows after the connection has been established, as described above.

The Customer Memory CM (Figures 1, 8, 9)

The customer memory comprises a store such as an electrically alterable read only memory EAROM. New data are written into this customer memory CM from the peripheral unit of the maintenance circuit. The storage locations are selected via the existing bus lines HSB with the aid of available addresses which are not utilised further. Random access of central data processing unit CPU to the customer memory (also for testing purposes) is assured by using bus lines HSB. Further, by utilizing bus lines, the number of addresses available for selecting storage locations is so large that data can be placed into and extracted from the memory by a polling process for all subscribers who can be connected to the system.

As shown in Figure 8, customer memory CM is advantageously combined with the existing programme memory PM in such a way that a certain area of the programme memory PM receives higher-level customer data, i.e. group addresses which, like the other storage locations of programme memory PM, are selected and sampled by the central data processing unit CPU via the bus lines HSB and decoder DPM. On the basis of the information available in the programme memory PM, certain storage locations are selected for the purpose of fetching specific (e.g. subscriber-specific or specific to particular peripheral units) individual information via an additional decoder DKDS in the customer memory. The sampling result is routed to the central data processing unit CPU via data output lines *da* of the bus lines HSB and stored as information.

The utilization of idle storage locations of programme memory PM for combination with the selection of storage locations of the customer memory has the advantage that the programme memory can be loaded to full capacity, while the existing bus lines HSB and address repertory can be fully utilized for the selection of the customer memory. In addition, this enables the necessary size of the customer memory to be reduced to a bare minimum.

Figure 9 shows details of the selection circuit for storage locations of the customer memory for reading, writing and erasing information therein.

By means of an address applied to the input of decoder DPM via the address bus lines HSB/*da* a given storage location is selected in one of two address buffer registers AR1 and AR2, with the result that at an output *ar*11 of address register AR1 and at an output *ar*21 of address buffer register AR2 a complete information block is applied to the inputs of memories M1 to M8 dependent on the similar transmitted status and command information which are received via the data bus lines HSB/*dr* in separate bit series. At the same time as the information is supplied to the memories M1 to M8, the storage location address goes to the decoder HS to select the storage location to store, to read out or to erase the customer data assigned, for example to a telephone station.

Parallel to the selection processes described above, storage locations in an instruction register BR, data input register WDR and read register RR are selected by the polling of the address register. The writing of data into or the reading of data from one of the memories M1 to M8 (AU1 to AU9) occurs via the addressing by the decoder HS. These data items are written into store via data bus lines *dr* or are read out via line *dt* and then rerouted. The erase, write or read instructions are a part of the information of the data processing unit CPU that is transmitted via data bus line HSB/*dr*. This information flows by way of the instruction register BR, WDR, RR via the outputs *br*1, *br*2, *br*3, *wdr*, *rr* to the memories M1 to M8. An acknowledgement signal is passed to data processing unit CPU via an output *br*4 of instruction register BR. It is ensured via an input *brs* that if a register module is not plugged in, the ongoing sequence of operations is not executed and that data processing unit CPU recognizes this. The CPU will then either occupy another register and continue the operation or start with a new switching process. Signalling may occur in parallel with the foregoing operation.

For the erasing, writing and reading operations of customer memory portion KDS fast rising pulses are needed. This means that the storage capacitor S*p*C provided in the corresponding circuit (Figure 10) must be charged very rapidly. Current pulses are necessary to achieve this. However, the transistors are endangered by these current pulses. To remove this risk, field effect transistors that can be turned on via a current sink must be employed.

A potential change from +5V to 23V and lasting, for example, for a period approximately equal to or exceeding 100 ms is needed as erase signal. The permissible tolerance range is very narrow (e.g. ± 5 %)

Storage Arrangement for Customer Memory CM

Figures 10, 11 show the special changeover unit for the fast loading and discharging of storage capacitor S*p*C. As mentioned earlier, this storage capacitor S*p* is conditional upon the fast operating time of memories M1 to M8.

The circuit shown in Figure 11 is only to control information supplied to the connecting point EMI shown in Figure 10 and Figure 11.

Dependent on the commands for erasing, writing and reading there will be a different status on the outputs *br*1, *br*2 and *br*3 (Figure 9) of the instruction register BR. For the writing command, on the output *br*1 there will be a sequence of 200 square wave (+) pulses. The voltage alternates between +5V and −23V such that for a period 5 μm there is +5V voltage and for a period of 100 μm a −23V voltage. For the erasing command there will be an inactive status on *br*1, *br*2 and *br*3. For the reading command there will be an on pulse in which the voltage alternates once from +5V to 14V (a period of 1 μs) and back to 5V. Dependent on information from the central processing unit CPU transmitted via the data bus line HSB/*dr*, the capacitor S*p*C must charged and discharged dependent on the information flowing to the memories M1 to M8. This charging and discharging will be effected by changing the voltage on the connecting point EM1 in accordance with the reading, writing and erasing commands. The fast rising pulses are needed by the TTL components (see page 12).

In the first shown in Figure 10 the transistors TT5 and TT6 turn on faster than the transistors TT1 and TT3.

The field effect transistor TT2 and TT4 only work as current sinks to get a limited current on the transistors TT1 and TT3, to protect them from short circuit and they are always in an on state.

If −23V is applied to EMI, the capacitor C2 will be charged and if it is charged the transistor TT6 is turned on for the 100 μs period that the −23V is connected.

Then the transistor TT5 will be turned off, as will transistor TT1, but more slowly. If the transistor TT1 is turned off the transistor TT3 is turned on, and the capacitor S*p*C is loaded.

These operations are effected very rapidly. After the −23V is turned off at EMI, the +5V voltage us turned on for a period of 5 μs. The transistor TT5 is turned on. The transistor TT1 is turned on and the transistor TT3 is turned off. The time for which the transistor TT3 is not already turned off, the field effect transistor TT4 protects the transistor TT3.

The capacitor S*p*C is discharged. These operations are repeated as often as the voltage on EMI is changed.

Allocation of the Scanning Cycle

Figure 12 shows the peripheral conversion and storage unit PC (Figure 1) which is to act as a connecting link between the bus line HSB for pulses with a faster rise time and the peripheral bus line LSB for the pulses with a slower time. Each of the two data transmission line groups can be subdivided into sets depending on their function. The first set comprises circuits *dt*1 over which is transferred the information fetched from specified peripheral units and to be stored in the common control unit CC, e.g. in connection with the charge registration (accounting) or routine testing. The second set comprises outgoing and incoming data circuits *dt*2 or *dr*, over which the instructions are transferred in the outgoing direction to the peripheral units and subscribers and, conversely, the data transmitted from there.

The third set comprises the circuit *un* and *sv* over which the peripheral units and subscribers must be scanned in successive cycles from the common control unit CC and thus, from the central data processing unit relative to its instantaneous condition.

The fourth set comprises various trunk groups provided for scanning the peripheral units, over which trunk groups the particular circuit conditions of peripheral units are interrogated for performing switching processes about to be executed, such as call establishment or changeover (e.g. in the case of a conference or transfer call).

It should be noted that the bus lines communicating with the central control have as many wires as are needed for transmitting the parallel binary code being used. If, for example 256 addresses are needed, there will be 8 wires for carrying 8 parallel bits.

To utilize the address repertory as effectively as possible, the unit must be so selected that it is assigned a group address, an area address and, within the area, a unit address, for example in order to identify the holding circuit group, the area within the group, and the individual line circuits themselves. Figure 12 shows the corresponding address bus lines *gr*, *se* and *dv*.

A periodically completed scanning cycle lasts 12.5 milliseconds if each peripheral unit is scanned 80 times per second, as mentioned above. Since only 1 millisecond is needed by the peripheral unit for transmitting the data to be sampled, the remaining time of 11.5 milliseconds within the scanning cycle is available for other purposes.

For the reasons set forth above, there are provided, in addition to the universal scanning circuits *un* and *sc* for the periodic scanning of the telephone stations, line circuits of every kind (e.g. link control units Jl-Jm) tone generators (e.g. TGl-TGx), connecting circuits ALC for attendant's stations, voice-stations, voice-frequency signalling receivers R-Tf, etc. There are further provided, for the scanning of units assigned to a special testing position for associated units in case of need or also as a matter of routine, lines *fa* that permit a more rapid scanning of specified peripheral units.

More important than the above additional scanning is the fact in the available remaining time of 11.5 milliseconds per scan period telephone stations, units and circuits are polled by means of the central processing unit CPU. Thus the unit CPU gains access to these peripheral units so as to be able to handle instructions and information for processing sequences of operations waiting to be switched. If 11.5 milliseconds are not adequate for such operations, the incomplete switching process and associated polling of the peripheral equipment are continued within the subsequent free time in the scan period of the scanning cycle after completion of the normal scanning of the peripheral equipment.

The idle or free times in each period in the scanning cycle are also utilized for other purposes, for example, as mentioned above, to poll storage locations in the customer memory for the purpose of establishing a connection, i.e. for reading customer-specific data necessary for the call set-up simultaneously with the selection of a peripheral unit to be involved in the call (e.g. link control circuit or interexchange trunk line circuit) depending on the particular call condition.

If data in the customer memory must be erased and written anew, if certain routine test procedures must be performed according to a pre-specified programme or if maintenance operations must be controlled externally, certain units of the system, as well as the test panel involved or the maintenance circuit, must be polled. This is normally done during low-traffic periods in the remaining idle periods of the scan cycle. Processes not performed during an idle period of the cyle are performed in the next available idle period of a subsequent scan cycle.

In the example under discussion, erasing and new writing of data in the customer memory as well as control of testing procedures, take place via the maintenance circuit MC. To accomplish this, the data exchange with the central control unit occurs only via the bus lines HSB.

The ringing signal generator RG for the subscriber stations supplies the maintenance circuit with the clock pulses necessary for routine tests. The ringing signal generator is powerline-operated via line SVS.

The maintenance circuit exchanges data via LSB and HSB bus lines.

Attendant's Station AC - Attendant's Connecting Circuit ALC

Figure 13 shows the circuitry for the transmission of every type of information to the attendant's station and from there to connecting circuit ALC using a minimum number of transmission lines. To accomplish this, the signals to be transmitted are sent as serial-code D.C. signals. Figure 13 shows the transmitter of the attendant station marked S1. This transmitter applies the coded signals to transmission path ADR. These signals consist of potential connections and disconnections of various durations. The same is true for the transmission in the opposite direction by transmitter S2 via transmission path ADT.

The reception of the transmitted signals and, thus, the transmission to the evaluator means, not shown, at the receiving end occur via the corresponding photo couplers OT1 or OT2. Thus the provision of each attendant station with only 1 speech wire and 4 signal transmission wires is assured.

In the embodiments described above the data processing unit of the central control unit effects an attenuation regulation with addressed operation of the speech path crosspoint. This control is achieved by commands received via the data transmission line, employing the appropriate link control unit.

Also, between the anode of each speech path crosspoint and the cathode of each tone connection crosspoint, a scanning connection is provided to the data transmission lines connected to the central control unit and a display indicator is connected between the anode and the scanning connection. In this way it is possible to monitor the addressed operation and transmission of commands via the relevant transmission line.

The embodiments described above are also described and illustrated in our copending application No. 8075/78 (Serial No. 1594392).

WHAT WE CLAIM IS:-

1. A circuit arrangement for an exchange in an electronic telephone system, said circuit arrangement including a first switching network for establishing connections between selected subscriber circuits and a second switching network for establishing connections between selected tone generators and selected subscriber circuits via said first switching network, each of said switching networks having crosspoint switches, a link control circuit being arranged to control interconnection via said switching networks, crosspoint switches of the second switching network having first electrode lines connected to second electrode lines of crosspoint switches of the first switching network, said first and second

electrodes being of opposite polarities so as to provide a series circuit via respective interconnected crosspoint switches of the two switching networks, said link control circuit providing a connection to an attenuation point between the first electrode line and said second electrode line of each interconnected pair of lines, said link control circuit having means for determining the attenuation of speech circuits via said second electrode lines by control of said attenuation point, said attenuation determining means being a control input to which a control signal can be applied to determine said attenuation.

2. A circuit arrangement according to Claim 1 wherein said first electrodes are cathodes and said second electrodes are anodes, the tone generators being connected to anodes of the crosspoint switches of the second switching network and subscriber circuits being connected to cathodes of the crosspoint switches of the first switching network.

3. A telecommunications exchange including a circuit arrangement according to Claim 1 or Claim 2 and also including a central control unit arranged to scan the crosspoint switches in turn to provide enabling or disabling signals and to provide a control signal determining said attenuation.

4. An exchange according to Claim 3 wherein each of said crosspoint switches is provided with means for indicating visually the operative state of the crosspoint switch.

5. An exchange according to Claim 3 or Claim 4 wherein a plurality of said link control circuits are provided and said attenuation control signal includes an address portion associated with the relevant link control circuit.

6. An electronic telephone system including an exchange according to any one of Claims 3 to 5.

7. An electronic telecommunications system with peripheral devices and at least one exchange, a plurality of sound frequency signal receivers, a plurality of link control units, a plurality of sound signal generators, and with a speech path matrix and a tone connection matrix for connecting the peripheral devices to the sound generators, with a central control unit which possesses at least one programme memory and one scratch pad memory, with time pulsing means and with data transmission lines for interconnection within the central control unit and for connecting the central control unit to the peripheral devices for the transmission of data, each of the link control units having a connection point for receiving a control command from the central control unit for setting the attenuation of a speech path between the anode of each speech path crosspoint and the cathode of each tone connection crosspoint, integrated crosspoint modules being used in the speech path matrix.

8. A system as claimed in Claim 1 wherein between the anode of each speech path crosspoint and the cathode of each tone connection crosspoint, a scanning connection is provided to the data transmission lines connected to the central control unit and a display indicator is connected between the anode and the scanning connection.

9. A system as claimed in Claim 1 wherein, for the regulation of the attenuation of the speech path via the central control unit, an addressed operation of the relevant link control unit and thus of the relevant switched-through speech path is carried out.

10. A circuit arrangement for an exchange in an electronic telephone system, said circuit arrangement being substantially as described herein with reference to Figures 1 and 6 of the accompanying drawings.

11. An electronic telecommunications system substantially as described herein with reference to Figures 1 to 4 and 6 to 13 or Figures 1, 2, 3 and 5 and 13 of the accompanying drawings.

G.F. REDFERN & CO.,
Marlborough Lodge,
14 Farncombe Road,
Worthing, West Sussex,
BN11 2BT.

Printed for Her Majesty's Stationery Office, by Croydon Printing Company Limited, Croydon, Surrey, 1981. Published by The Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.

1594391 COMPLETE SPECIFICATION

10 SHEETS *This drawing is a reproduction of the Original on a reduced scale*

Sheet 1

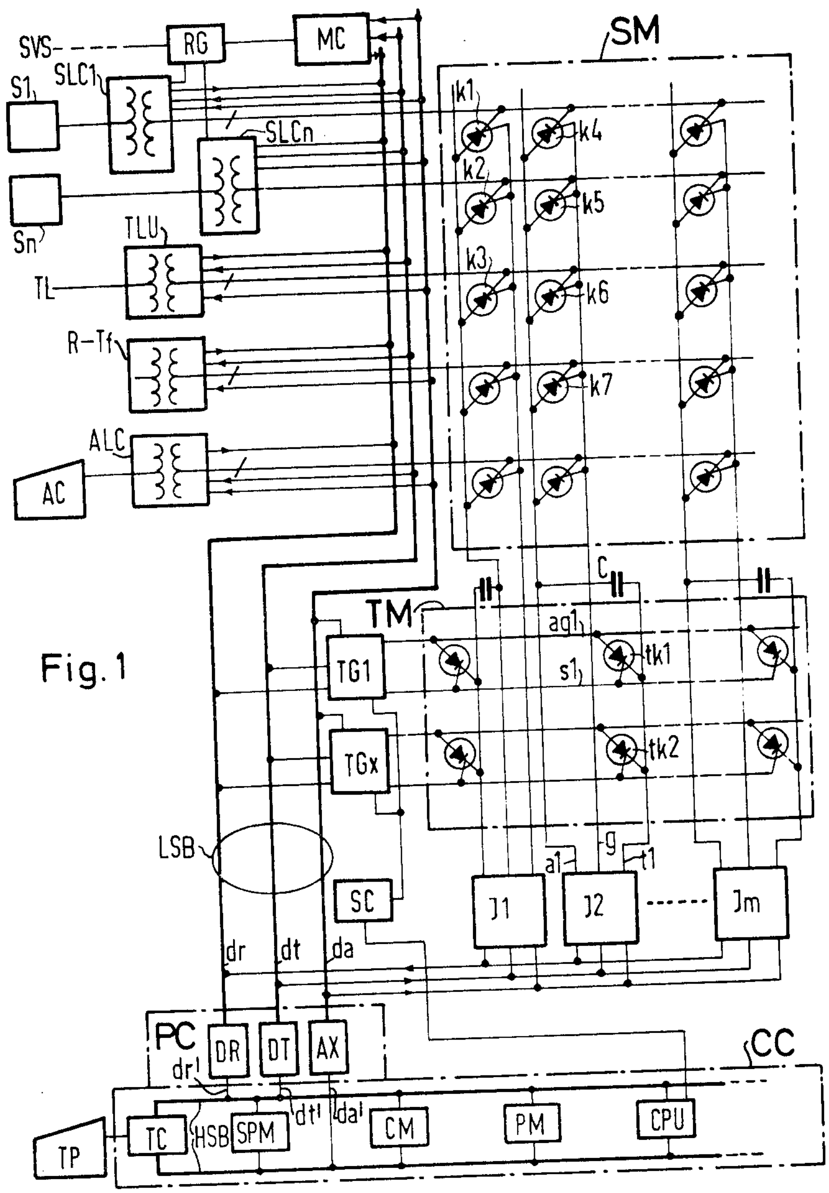


Fig. 1

Fig. 2

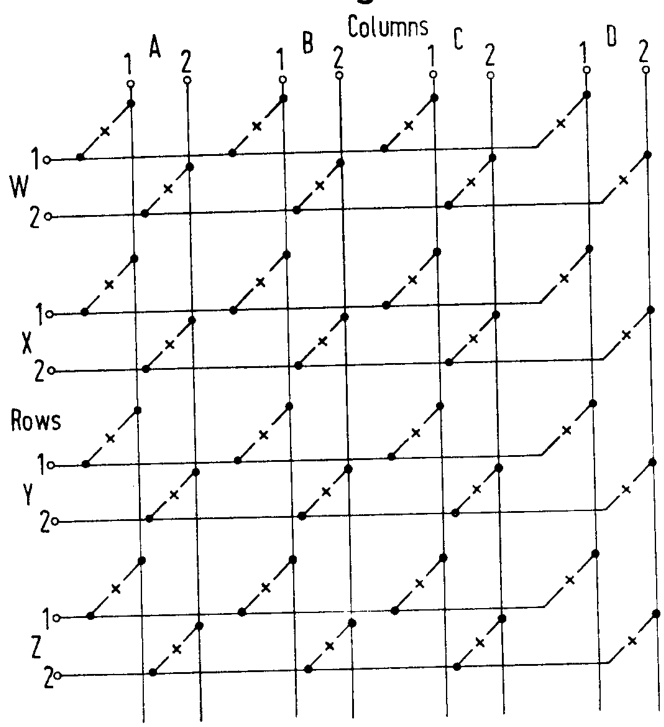
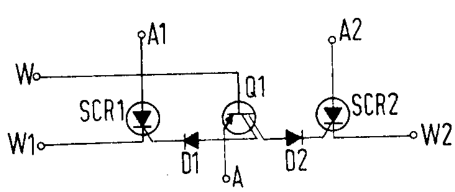


Fig.3



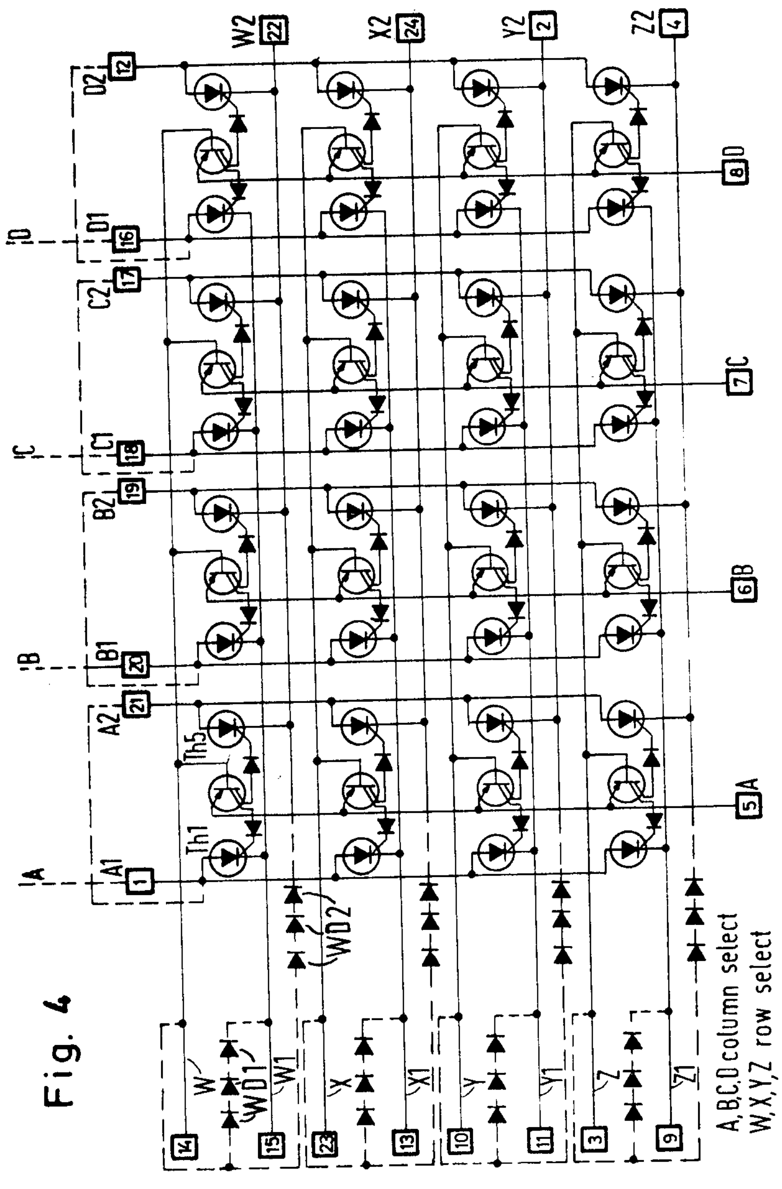

A1
A2
B1
B2
C1
C2
D1
D2
Th1
Th5
W
X
Y
Z
W1
X1
Y1
Z1
W2
X2
Y2
Z2
WD1
WD2
A
B
C
D
A,B,C,D column select
W,X,Y,Z row select

Fig. 4

Fig. 5

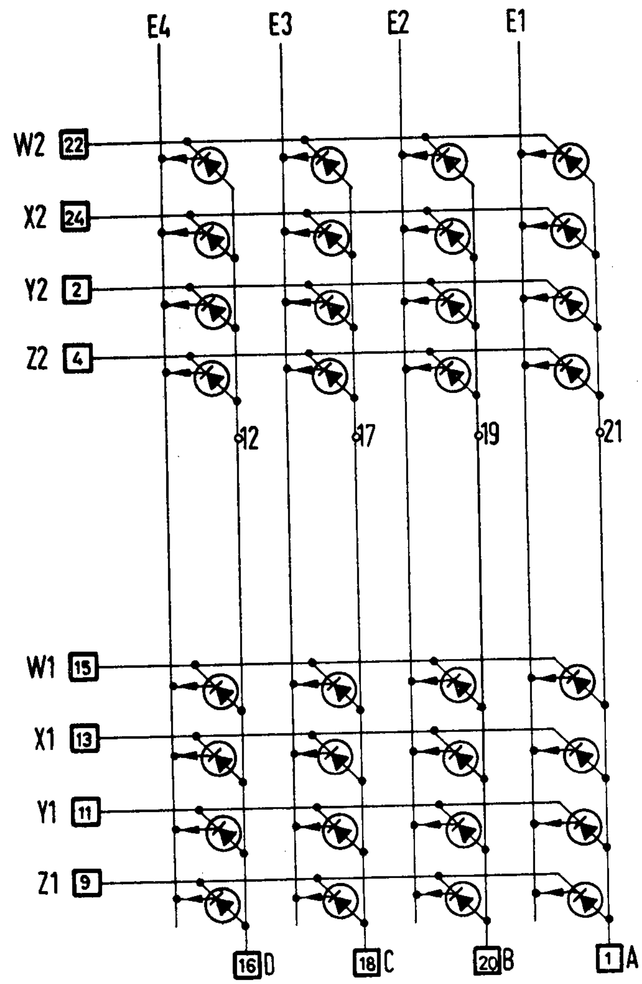
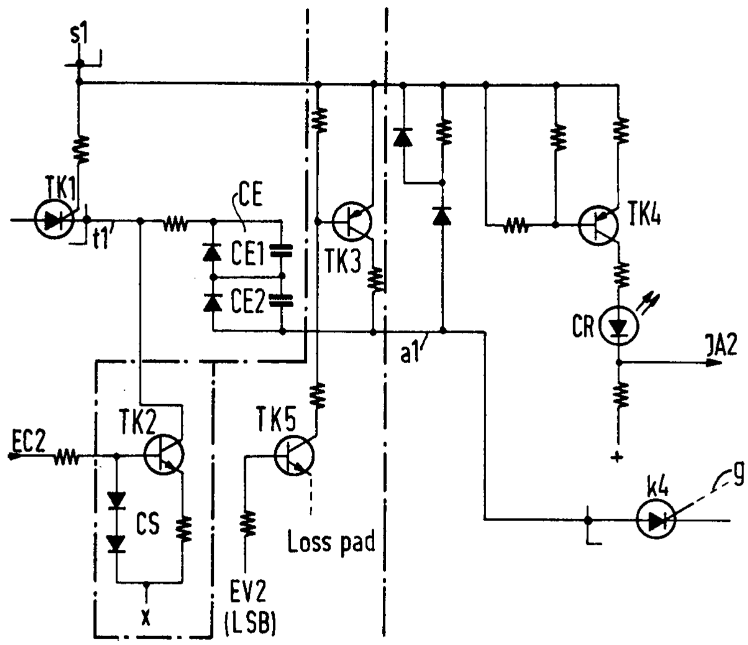

E4
E3
E2
E1
W2 22
X2 24
Y2 2
Z2 4
12
17
19
21
W1 15
X1 13
Y1 11
Z1 9
16 D
18 C
20 B
1 A

Fig.6


s1
TK1
t1'
CE
CE1
CE2
TK3
TK4
CR
JA2
a1'
TK2
TK5
EC2
CS
x
EV2
(LSB)
Loss pad
k4
g
+

1594391 COMPLETE SPECIFICATION

10 SHEETS *This drawing is a reproduction of the Original on a reduced scale*

Sheet 6

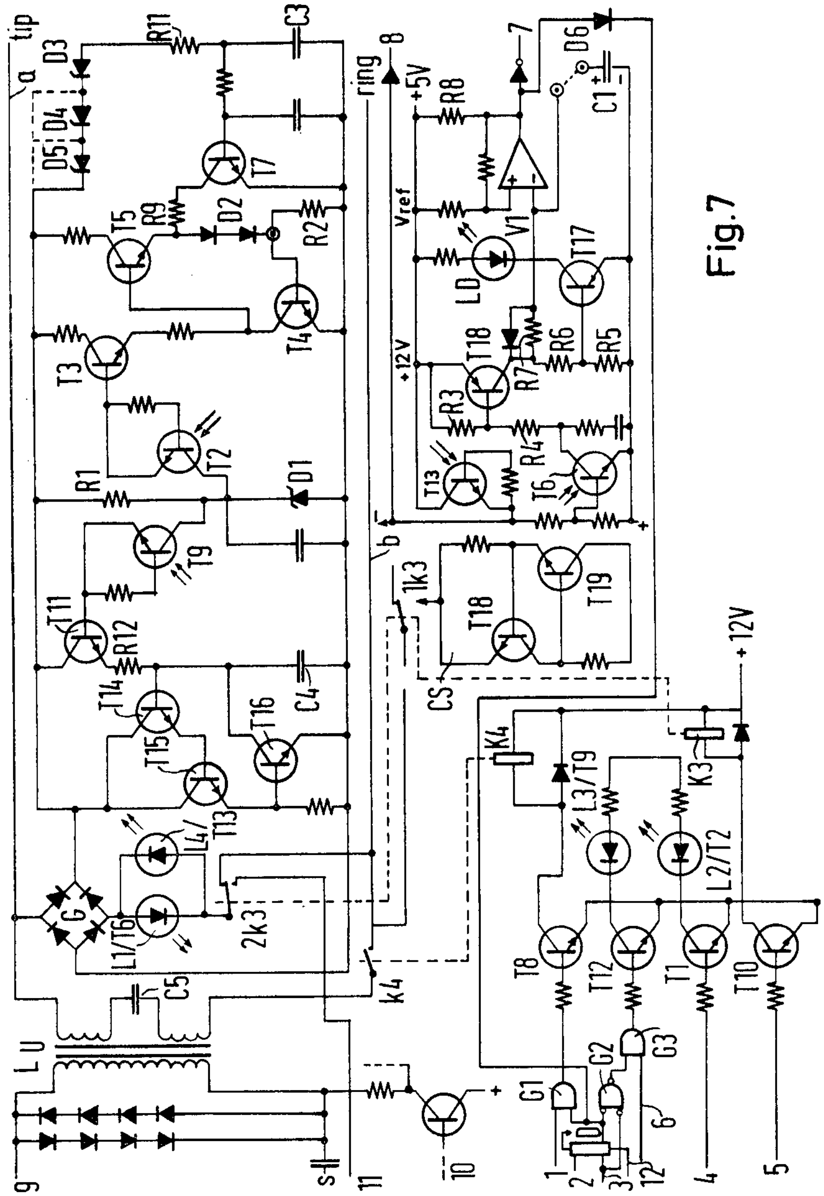


Fig.7

Fig.8

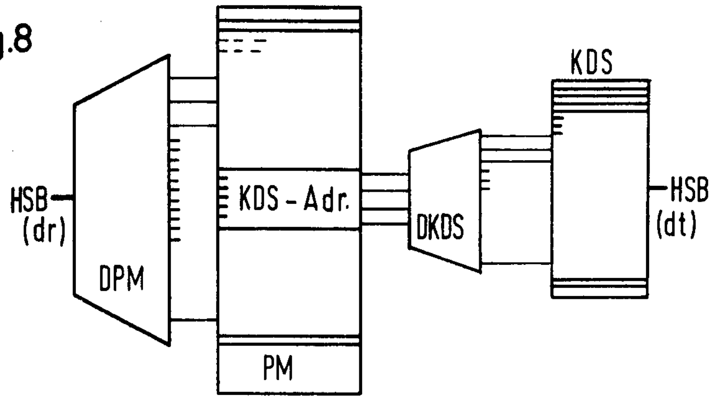
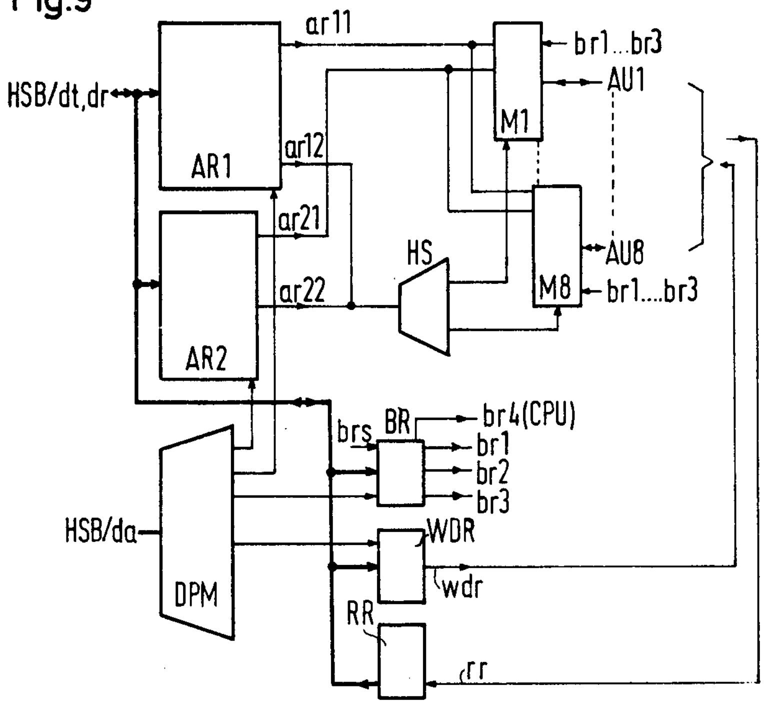

KDS
KDS - Adr.
HSB
(dr)
DPM
DKDS
HSB
(dt)
PM

Fig.9


ar11
br1...br3
AU1
HSB/dt,dr
M1
ar12
AR1
ar21
HS
AU8
M8
ar22
br1....br3
AR2
brs
BR
br4(CPU)
br1
br2
br3
HSB/da
WDR
wdr
DPM
RR
rr

1594391 COMPLETE SPECIFICATION

10 SHEETS *This drawing is a reproduction of the Original on a reduced scale*

Sheet 8

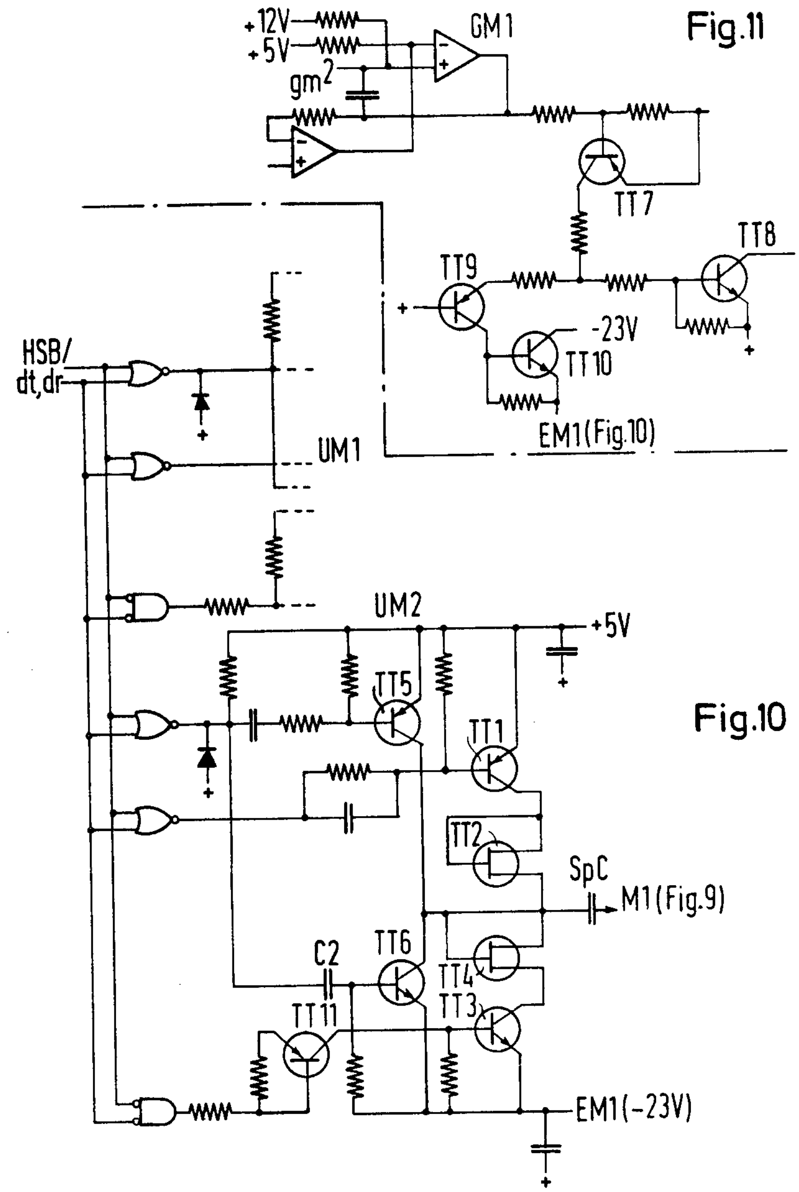


Fig.12

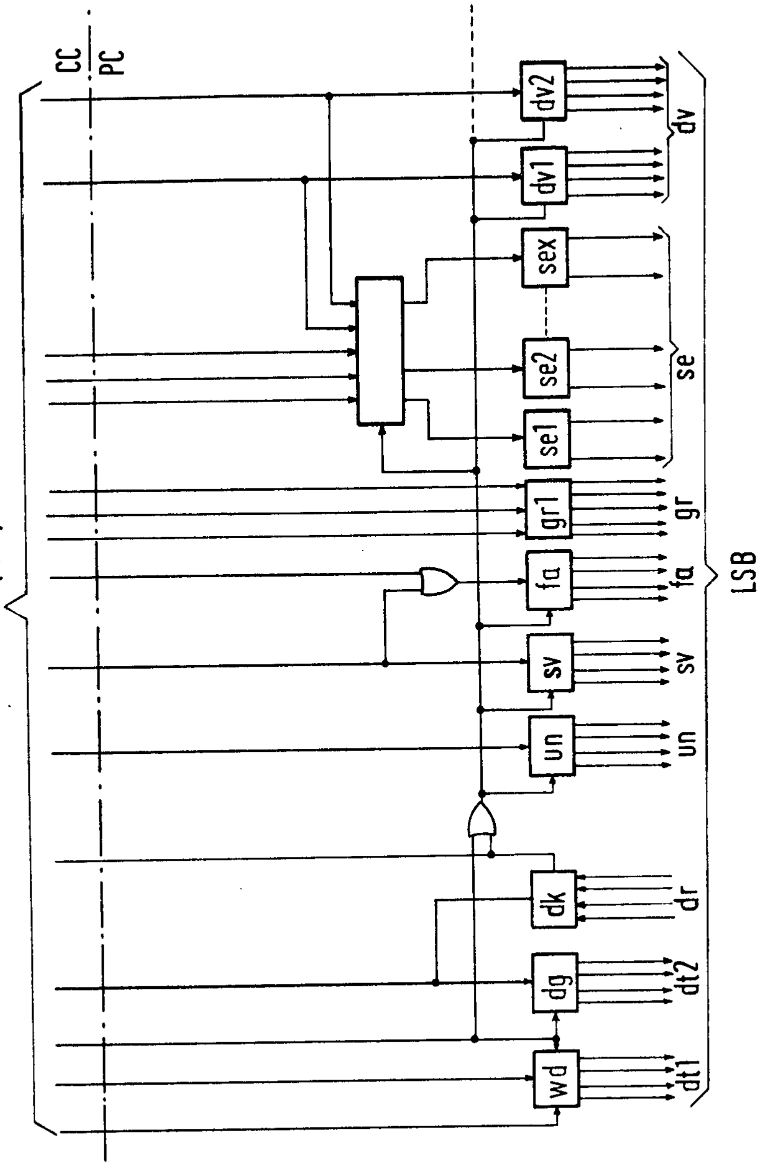

CPU(HSB)
CC
PC
dv2
dv1
sex
se2
se1
gr1
fa
sv
un
dk
dg
wd
dv
se
gr
fa
sv
un
dr
dt2
dt1
LSB

Fig.13