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(54) Title: CVD BASED SPACER DEPOSITION WITH ZERO LOADING

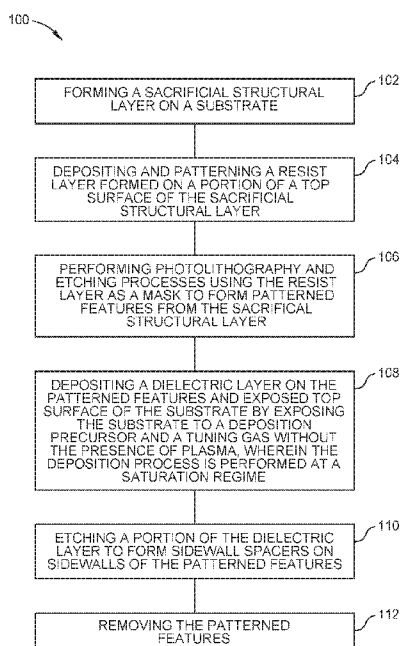


FIG. 1

(57) Abstract: Embodiments of the present disclosure relate to deposition methods for dielectric layers with zero pattern loading characteristics. In one embodiment, the method includes depositing a conformal dielectric layer on the substrate having a patterned area and a blanket area by exposing the substrate to a deposition precursor and a tuning gas simultaneously without the presence of plasma in a process chamber, wherein the deposition precursor is reacted to form a chemical reaction by-product, and the chemical reaction by-product is the same as the tuning gas, and wherein the deposition precursor and the tuning gas are provided at an amount that is more than required for the deposition reaction to occur at the patterned area and the blanket area.

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CVD BASED SPACER DEPOSITION WITH ZERO LOADING

FIELD

[0001] Embodiments of the present disclosure generally relate to methods for semiconductor processing. Specifically, embodiments of the present disclosure relate to methods for deposition of a conformal dielectric film.

BACKGROUND

[0002] Dielectric layers have been used for applications such as barrier layers or spacers in the fabrication of modern semiconductor devices. The dielectric layers can be deposited over features, e.g., trenches or vias, in a patterned substrate using a deposition process, such as atomic layer deposition (ALD) or chemical vapor deposition (CVD). The dielectric layers are then anisotropically etched to form spacers on either side of the features. While methods of depositing spacers using ALD process can provide conformal layers over the features due to the self-limiting nature of the ALD process, it has been challenging to form highly conformal dielectric layers across the patterned substrate and blanket substrate with zero pattern loading using thermal CVD processes due to the reaction mechanism the thermal CVD.

[0003] Therefore, there is a need in the art to provide an improved thermal CVD method for depositing dielectric layers in high aspect ratio trenches with reduced pattern loading.

SUMMARY

[0004] Embodiments of the present disclosure generally relate to deposition methods for dielectric layers with reduced (e.g., zero) pattern loading characteristics. In one embodiment, the method includes depositing a conformal dielectric layer on the substrate having a patterned area and a blanket area by exposing the substrate to a deposition precursor and a tuning gas simultaneously without the presence of plasma in a process chamber, wherein the deposition precursor is reacted to form a chemical reaction by-product, and the chemical reaction by-product is the same as the tuning gas, and wherein the deposition precursor and the tuning gas are provided at an

amount that is more than required for the deposition reaction to occur at the patterned area and the blanket area.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] Embodiments of the present disclosure, briefly summarized above and discussed in greater detail below, can be understood by reference to the illustrative embodiments of the disclosure depicted in the appended drawings. It is to be noted, however, that the appended drawings illustrate only typical embodiments of this disclosure and are therefore not to be considered limiting of its scope, for the disclosure may admit to other equally effective embodiments.

[0006] Figure 1 depicts a flow chart of a process associated with an exemplary self-aligned double patterning (SADP) process according to an embodiment of the present disclosure.

[0007] Figures 2A-2E illustrate cross-sectional views of a structure formed by the process depicted in Figure 1.

[0008] To facilitate understanding, identical reference numerals have been used, where possible, to designate identical elements that are common to the figures. The figures are not drawn to scale and may be simplified for clarity. It is contemplated that elements and features of one embodiment may be beneficially incorporated in other embodiments without further recitation.

DETAILED DESCRIPTION

[0009] Embodiments of the present disclosure provide deposition methods for dielectric layers with zero pattern loading characteristics. These methods use thermal chemical vapor deposition (CVD) of dielectric layers from a deposition precursor and a tuning gas. The deposition process may include exposing a substrate having patterned area and blanket area to the deposition precursor and the tuning gas provided at increased partial pressure and gas velocity at low temperatures. These process conditions allow the dielectric layer to be deposited at the same deposition/reaction rate across the entire surface of the substrate. Because the deposition/reaction rate is the same for both patterned area and blanket area, the variation in the film thickness between these areas is zero or reduced to the minimum. As a result, conformal

dielectric layers can be formed over patterned area and blanket area with zero pattern loading.

[0010] Exemplary chambers that may be used to practice embodiments of the present disclosure may include PRODUCER™ CVD chamber, PRODUCER SACVD™ chamber, PRODUCER® XP PRECISION™ CVD chamber, DXZ® processing chamber, or PRODUCER HARP™ chamber, which are commercially available from Applied Materials, Inc. of Santa Clara, California. Other tools capable of performing CVD processes may also be adapted to benefit from the embodiments described herein. The chambers of this process may be configured individually, but may also be part of an integrated tool. The process may be performed on any substrate, such as a 200 mm, 300 mm, or 450 mm substrate or other medium suitable for semiconductor processing.

[0011] Figure 1 is a flow chart of a process 100 associated with an exemplary self-aligned double patterning (SADP) process according to an embodiment of the present disclosure. Figures 2A-2E illustrate cross-sectional views of a structure formed by the process 100 depicted in Figure 1. The self-aligned double patterning process is chosen for illustration purposes, and variations are contemplated. The concept of the disclosure is equally applicable to other deposition processes or patterning schemes, such as a self-aligned triple patterning (SATP) process, a self-aligned quadruple patterning (SAQP) process, a via/hole shrink process, a back end of line (BEOL), etc., that may use a protective spacer or protective sacrificial layer, as needed in various semiconductor processes such as NAND flash application, DRAM application, or CMOS application, etc.

[0012] The process 100 starts at block 102 by forming a sacrificial structural layer 220 on a substrate 200, as shown in Figure 2A. The sacrificial structural layer 220 may be a silicon-based material such as silicon oxide, silicon nitride, silicon oxynitride, silicon carbides, or polysilicon. It is contemplated that the choice of materials used for the sacrificial structural layer 220 may vary depending upon the etching/ashing rate relative to the resist layer to be formed thereon.

[0013] While the substrate 200 is illustrated as a single body, the substrate 200 may contain one or more materials used in forming semiconductor devices such as metal contacts, trench isolations, gates, bitlines, or any other interconnect features. The substrate 200 may be a material or a layer stack comprising one or more of the

following: crystalline silicon, silicon oxide, silicon oxynitride, silicon nitride, strained silicon, silicon germanium, tungsten, titanium nitride, doped or undoped polysilicon, doped or undoped silicon wafers, silicon on insulator (SOI), carbon doped silicon oxides, silicon nitrides, germanium, gallium arsenide, glass, sapphire, low k dielectrics, and any combinations thereof. In cases where a memory application is desired, the substrate 200 may include the silicon substrate material, an oxide material, and a nitride material, with or without polysilicon sandwiched in between.

[0014] At block 104, a resist layer 230, such as a photoresist material, is deposited on a portion of the top surface 223 of the sacrificial structural layer 220 and patterned with a desired pitch as shown in Figure 2A.

[0015] At block 106, one or more suitable photo-lithography and etching processes are performed, using the resist layer 230 as a mask, to form patterned features 221 from the sacrificial structural layer 220 on the substrate 200. The patterned features 221 can have an aspect ratio of about 1:1 to about 50:1, for example about 3:1 to about 10:1. The term “aspect ratio” in this disclosure refers to the ratio of the height dimension to the width dimension of the patterned feature.

[0016] The patterned features 221 on the substrate 200 provide a patterned area 201, while the open region having no patterned features 221 provides a blanket area 203, as shown in Figure 2B. The patterned features 221 may be used for forming, for example, gate stack or interconnect such as vias or trenches. The patterned features 221 are sometimes referred to as placeholders, mandrels or cores and have specific line width and/or spacing based upon the photoresist material used. The width of the patterned features 221 may be adjusted by subjecting the resist layer 230 to a trimming process. After the pattern has been transferred into the sacrificial structural layer 220, any residual photoresist and hard mask material (if used) are removed using a suitable photoresist stripping process.

[0017] At block 108, a dielectric layer 240 is deposited conformally on the patterned features 221 (patterned area 201) and the exposed upper surface 225 of the substrate 200 (blanket area 203), as shown in Figure 2C. The dielectric layer 240, when deposited using improved process conditions to be discussed below, will achieve good step coverage with substantially zero pattern loading across the surface of the substrate 200. For example, the percentage of film thickness between different surfaces of the characteristic difference is less than 2%. Typically, pattern loading is

high for thermal CVD process, where the deposited layer is often thicker in blanket areas than areas having densely packed patterned features. This is due partly to the differences in exposed surface area of the substrate and mass-dominated reaction related to the supply of reactants. The patterned area, e.g., patterned area 201, has a larger deposition surface than an open or blanket area, e.g., blanket area 203, on which the dielectric layer 240 is deposited.

[0018] In some cases, the patterned area 201 may have an exposed vertical surface area greater than the blanket area 203 by a multiplicative factor greater than or equal to 2, 3, 5, 10, or 20 for region of substantially the same dimensions or area when measured in top down plan view. In some embodiments, the density of features 221 in a patterned area 201 is greater than or equal to 2, 3, 5, 10, or 20 than a density of features 221 in the blanket area 203. The differences in exposed surface area of the substrate can cause the deposition rate to vary between the patterned area 201 and blanket area 203. In spacer applications, since feature critical dimension (CD) is determined by the thickness of the spacer, the pattern loading will lead to a CD variation at different locations. The improved process conditions of the present disclosure allow the dielectric layer 240 to be deposited at substantially the same deposition/reaction rate across the patterned area 201 and the blanket area 203 of the substrate 200. Because the deposition/reaction rate is the same for both the patterned area and the blanket area, the variation in the film thickness between these areas is zero, or can be reduced to a minimum. As a result, conformal dielectric layers can be formed over patterned area 201 and blanket area 203 with zero pattern loading.

[0019] The dielectric layer 240 that can benefit from the present disclosure includes silicon-containing dielectric material, such as silicon oxide, silicon oxynitride, or silicon nitride. The dielectric layer 240 may be carbon doped, hydrogen doped, and/or contain other compounds or elements (such as n-type or p-type dopants) to tailor film properties. In some embodiments, the dielectric layer 240 can be a carbon-based material, such as an amorphous carbon (a-C) layer.

[0020] The deposition of the dielectric layer 240 is performed in a process chamber by exposing the substrate to a deposition precursor at low temperatures. In some embodiments, a tuning gas, which is a chemical reaction by-product in the deposition process of the dielectric layer 240, is flowed concurrently (*i.e.*, co-flow mode) with the deposition precursor during deposition of the dielectric layer 240. No plasma excitation

is present in the substrate processing region during the deposition process. The deposition precursor can be one or more of any suitable precursors depending upon the application. In cases where a silicon-containing dielectric material is desired, the deposition precursor can include a silicon-containing precursor. The process chamber may be a CVD chamber or any suitable thermal process chamber.

[0021] Suitable silicon-containing precursor may include silanes, halogenated silanes, organosilanes, and any combinations thereof. Silanes may include silane (SiH_4) and higher silanes with the empirical formula $\text{Si}_x\text{H}_{(2x+2)}$, such as disilane (Si_2H_6), trisilane (Si_3H_8), and tetrasilane (Si_4H_{10}), or other higher order silanes such as polychlorosilane. Other silicon-containing precursor, such as octamethylcyclotetrasiloxane (OMCTS), methyldiethoxysilane (MDEOS), bis(tertiary-butylamino)silane (BTBAS), tridimethylaminosilane (TriDMAS), trisdimethylaminosilane (TrisDMAS), dichlorosilane, trichlorosilane, dibromosilane, silicon tetrachloride, silicon tetrabromide, or combinations thereof, or organosilicon compounds having a ratio of oxygen to silicon atoms of 0 to about 6, may also be used. Suitable organosilicon compounds may be siloxane compounds, halogenated siloxane compounds that include one or more halogen moieties (e.g., fluoride, chloride, bromide, or iodide), such as tetrachlorosilane, dichlorodiethoxysiloxane, chlorotriethoxysiloxane, hexachlorodisiloxane, and/or octachlorotrisiloxane, and aminosilanes, such as trisilylamine (TSA), hexamethyldisilazane (HMDS), silatrane, tetrakis(dimethylamino)silane, bis(diethylamino)silane, tris(dimethyl-amino)chlorosilane, and methylsilatrane.

[0022] In cases where the dielectric layer 240 is a carbon-based material, the deposition precursor may be a carbon-containing precursor such as hydrocarbon compounds. The hydrocarbon compounds may be partially or completely doped derivatives of hydrocarbon compounds, including fluorine-, oxygen-, hydroxyl group-, and boron-containing derivatives of hydrocarbon compounds. Suitable hydrocarbon compounds may include one or more of the following compounds, for example, alkanes such as methane (CH_4), ethane (C_2H_6), propane (C_3H_8), butane (C_4H_{10}) and its isomer isobutane, pentane (C_5H_{12}) and its isomers isopentane and neopentane, hexane (C_6H_{14}) and its isomers 2-methylpentane, 3-methylpentane, 2,3-dimethylbutane, and 2,2-dimethyl butane, and so on. Additional suitable hydrocarbons may include alkenes such as ethylene, propylene, butylene and its isomers, pentene and its isomers, and

the like, dienes such as butadiene, isoprene, pentadiene, hexadiene and the like, and halogenated alkenes include monofluoroethylene, difluoroethylenes, trifluoroethylene, tetrafluoroethylene, monochloroethylene, dichloroethylenes, trichloroethylene, tetrachloroethylene, and the like. Also, alkynes such as acetylene (C_2H_2), propyne (C_3H_4), butyne (C_4H_6), vinylacetylene and derivatives thereof can be used as carbon precursors. Additionally cyclic hydrocarbons, such as benzene, styrene, toluene, xylene, ethylbenzene, acetophenone, methyl benzoate, phenyl acetate, phenylacetylene (C_8H_6), phenol, cresol, furan, alpha-terpinene, cymene, 1,1,3,3-tetramethylbutylbenzene, t-butylether, t-butylethylene, methyl-methacrylate, and t-butylfurfurylether, compounds having the formula C_3H_2 and C_5H_4 , halogenated aromatic compounds including monofluorobenzene, difluorobenzenes, tetrafluorobenzenes, hexafluorobenzene and the like can be used. Halogenated hydrocarbons such as carbon tetrachloride (CCl_4), diiodomethane (CH_2I_2), chlorofluorocarbon (CFC), bromotrichloromethane ($BrCCl_3$), 1,1-dichloroethylene, bromobenzene, or derivatives thereof may also be used.

[0023] The tuning gas, as discussed above, is a chemical reaction by-product in the deposition process of the dielectric layer 240. Therefore, the tuning gas is chosen depending on the deposition process and chemistry used for the deposition precursor. The tuning gas may or may not participate in the chemical reaction. In cases where the deposition precursor is a silicon-containing precursor using silane, the substrate is exposed to the deposition precursor and the tuning gas, and the deposition precursor is reacted to form a chemical reaction by-product. In such a case, the chemical reaction by-product is the same as the tuning gas. For example, in an example reaction of $SiH_4 + 2O_2 \rightarrow SiO_2 + 2H_2O$, the product is SiO_2 and water (H_2O), and the by-product may include hydrogen gas (H_2). In this case, the tuning gas can be hydrogen gas. One of ordinary skill in the art can select one or more tuning gases based on the application and the deposition precursor used.

[0024] In one example where the deposition precursor uses a silicon-containing precursor, the flow rate for the silicon-containing precursor is controlled to provide a partial pressure of the silicon-containing precursor in the process chamber. The partial pressure of the deposition precursor in the process chamber is an indicator of the concentration of the reacted precursors residing at or near the surface of the substrate. In embodiments where a 300 mm substrate is used, the silicon-containing precursor

may be provided at a flow rate of about 10 sccm to about 10000 sccm, such as about 20 sccm to about 5000 sccm, for example about 50 sccm to about 2000 sccm. The flow rate may be adjusted so that the partial pressure of the silicon-containing precursor is controlled in a range from about 10 Torr to about 100 Torr, for example about 40 Torr to about 80 Torr. The partial pressure of the silicon-containing precursor may be greater (e.g., 100 Torr or above) so long as the partial pressure of the silicon-containing precursor does not negatively impact the mean free path length of the gas molecules and thus affect the diffusivity of precursors into the trenches between the patterned features 221.

[0025] Similarly, the flow rate for the tuning gas is controlled to provide a partial pressure of the tuning gas in the process chamber. The tuning gas may be provided at about the same flow rate as the deposition precursor. The flow rate may be adjusted so that the partial pressure of the tuning gas is controlled in a range from about 10 Torr to about 100 Torr, for example about 40 Torr to about 80 Torr. In various embodiments where the silicon-containing precursor and the tuning gas are co-flowed into the process chamber, the tuning gas and the silicon-containing precursor may be provided at a volumetric flow ratio (tuning gas: silicon-containing precursor) of about 1:2 to about 1:6, for example about 1:4.

[0026] In some embodiments, no carrier/inert gases are used during the deposition process. In such cases, the chamber pressure can be substantially identical to the partial pressure of the silicon-containing precursor, or the combined pressure of the deposition precursor and the tuning gas. In any case, the flow rate and the increased partial pressure of the precursor/tuning gas enable the precursor/gas to diffuse or penetrate into the bottom of the trench between the patterned features 221.

[0027] In some cases, carrier gases may be used to carry the silicon-containing precursor to the process chamber. In some cases, inert gases may be used to help maintain the process chamber at a particular pressure. In some cases, dilution gases may be used to control the density and deposition rate of the dielectric layer 240. Suitable carrier/inert/dilution gases may include helium, argon, hydrogen, ammonia, nitrogen, noble gas such as krypton, xenon, or any combinations thereof. In some cases, a p-type or n-type dopant gas, such as diborane (B_2H_6), phosphine (PH_3), arsine (AsH_3), etc., may be used during the deposition process. In any case, the combination of the precursors (e.g., deposition and tuning gas) and the gases of carrier/inert/dilution

or dopant gases can be used to set the total pressure of the process chamber to a range of about 20 Torr to about 600 Torr.

[0028] During the deposition process, the substrate 200 may be maintained at a temperature of about 550°C or below, for example about 500°C or below, such as about 250°C to about 480°C. In one example, the substrate 200 is maintained at a temperature of about 350°C to about 450°C. The substrate 200 may be spaced about 50 mils to about 300 mils from a showerhead faceplate where the precursors and/or gases enter the process chamber. When the precursor/tuning gas are kept at a constant flow, the spacing between the substrate and the showerhead faceplate can be controlled to increase the gas velocity, which in turn helps diffusion of the precursors into the bottom of the trench between the patterned features 221. In one embodiment, the flow rate and the spacing may be controlled so that the precursor/tuning gas are flowed at a rate of about 0.1 Liter/minute to 1 Liter/minute. In any case, the partial pressure, substrate temperature, and flow parameters may be adjusted such that the dielectric layer 240 is deposited at a rate of about 1 Å/min to about 600 Å/min, for example about 2 Å/min to about 50 Å/min. The deposited dielectric layer 240 may have a thickness of about 50 Å to about 600 Å.

[0029] It is noted that the process conditions described herein can be modified for processing substrates with different sizes. The above process conditions are applicable to other deposition precursor such as the carbon-containing precursor, or can be modified depending upon the material of the dielectric layer 240. A person of ordinary skill in the art can modify the flow rates and/or other parameters to deposit a desired dielectric layer.

[0030] Increasing partial pressure of the deposition precursor(s) and the tuning gas allows the deposition process to proceed in a saturation regime, which means the deposition precursor and the tuning gas are provided at an amount that is more than required for a deposition reaction to occur at the patterned area 201 and the blanket area 203. In one embodiment, the deposition precursor and the tuning gas are provided at an amount that is at least 20% or more, for example about 50% to about 300%, greater than the amount of the deposition precursor and the tuning gas that can be consumed at the patterned area 201 and the blanket area 203. In other words, the patterned area 201 and blanket area 203 are exposed to excessive amount of the deposition precursor and the tuning gas. Without being bounded by any particular

theory, the saturation regime can result in a decreased variation in the thickness between the patterned area 201 and blanket area 203 since the supply of the deposition precursor and the tuning gas is much higher than the consumption of the precursors in both the patterned area 201 and blanket area 203. Since higher concentration of the deposition precursor can lead to an increase of the deposition rate and higher concentration of the tuning gas (*i.e.*, the chemical reaction by-product of the deposition process) can lead to a decrease of the deposition rate at a given temperature, the saturation regime will allow the concentration of the deposition precursor and the concentration of the tuning gas to maintain at the same level across the patterned area 201 and the blanket area 203. Therefore, the deposition rate between the patterned area 201 and blanket area 203 will be substantially identical, thereby achieving reduced, or substantial zero pattern loading for a thermal CVD process.

[0031] At block 110, after the dielectric layer 240 has been deposited conformally on the patterned features 221 using the improved deposition process discussed at block 108, a portion of the dielectric layer 240 is selectively removed from horizontal surfaces of the substrates. For example, the dielectric layer 240 may be anisotropically etched (a vertical etch), leaving the dielectric layer 240 on sidewalls of the patterned features 221. Particularly, the dielectric layer 240 on an upper surface 227 of the patterned features 221 and the dielectric layer 240 on the exposed surface of the substrate 200 (*e.g.*, the blanket area 203) are removed to expose the upper surface 227 of patterned features 221 and the upper surface 225 of the substrate. The remaining dielectric layer 240 thus forms sidewall spacers 241 and protects the sidewall of the patterned features 221, as shown in Figure 2D. Due to the improved deposition process of the dielectric layer 240, the sidewall spacers 241 as formed can have a uniform thickness across the substrate surface and provide a constant CD for multi-patterning applications.

[0032] At block 112, the patterned features 221 are removed using a plasma etching process or other suitable wet stripping process, leaving the sidewall spacers 241 as shown in Figure 2E. The plasma etching process may be performed by bringing the substrate 200 in contact with a plasma generated from a fluorine-based etching chemistry to remove the patterned features 221. The etching chemistry is selective so that the sidewall spacers 241 do not get damaged during the etching/stripping process.

Upon removal of the patterned features 221, the sidewall spacers 241 may be used as a hardmask for etching the underlying layer, layer stack, or structure.

[0033] In summary, embodiments of the present disclosure provide CVD deposition processes for dielectric layers with reduced or zero pattern loading characteristics. The deposition process may include exposing a substrate having patterned area and blanket area to a deposition precursor and a tuning gas provided at increased partial pressure at low temperatures. The deposition process is performed at a saturation regime to provide excessive amount of the deposition precursor and the tuning gas to the substrate. These process conditions allow the dielectric layer to be deposited at the same deposition/reaction rate across the entire surface of the substrate. Because the deposition/reaction rate is the same for both patterned area and blanket area, the variation in the film thickness between these areas is zero or minimized. As a result, conformal dielectric layers can be formed over patterned area and blanket area with zero pattern loading.

[0034] While the foregoing is directed to embodiments of the present disclosure, other and further embodiments of the disclosure may be devised without departing from the basic scope thereof.

Claims:

1. A method for processing a substrate, comprising:
depositing a conformal dielectric layer on the substrate having a patterned area and a blanket area by exposing the substrate to at least a deposition precursor and a tuning gas simultaneously without the presence of plasma in a process chamber, wherein the deposition precursor is reacted to form a chemical reaction by-product, and the chemical reaction by-product is the same as the tuning gas, and wherein the deposition precursor and the tuning gas are provided at an amount that is more than required for a deposition reaction to occur at the patterned area and the blanket area.
2. The method of claim 1, wherein deposition precursor comprises silicon and the tuning gas and the deposition precursor are provided at a volumetric flow ratio (tuning gas: deposition precursor) of about 1:2 to about 1:6.
3. The method of claim 1, wherein the deposition of the dielectric layer further comprises exposing the substrate to a n-type or p-type dopant gas.
4. The method of claim 1, wherein deposition precursor comprises silicon and the tuning gas and the deposition precursor are provided at an amount that is at least 20% greater than the amount of the tuning gas and the deposition precursor that can be consumed at the patterned area and the blanket area.
5. The method of claim 4, further comprising selectively removing the conformal dielectric layer from horizontal surfaces of the substrate to form sidewall spacers on vertical surfaces of a plurality of features extending from the horizontal surfaces.
6. The method of claim 1, wherein the deposition precursor comprises a carbon-containing precursor.
7. The method of claim 6, wherein the carbon-containing precursor comprises hydrocarbon compounds.
8. A method of processing a substrate, comprising:

co-flowing a deposition precursor and a tuning gas into a processing chamber, the tuning gas comprising a reaction by-product of the deposition precursor;

exposing a surface of the substrate to the deposition precursor and the tuning gas; and

depositing a material layer onto the substrate without igniting a plasma of the deposition precursor and the tuning gas.

9. The method of claim 8, wherein the tuning gas and the deposition precursor are provided at an amount that is at least 20% greater than the amount of the tuning gas and the deposition precursor that can be consumed at the surface of the substrate.

10. The method of claim 8, wherein the deposition precursor comprises silicon and the tuning gas comprises hydrogen gas.

11. The method of claim 8, wherein
the substrate comprises a blanket area and a patterned area disposed proximate to the blanket area, and
a difference in a thickness of the material layer deposited in the patterned area and a thickness of the material layer deposited in the blanket area is less 2%.

12. The method of claim 11, wherein the material layer comprises a silicon-containing dielectric material.

13. The method of claim 11, further comprising selectively removing the material layer from horizontal surfaces of the substrate to form sidewall spacers on vertical surfaces of a plurality of features extending from the horizontal surfaces.

14. A method for processing a substrate, comprising:
depositing a conformal silicon-containing dielectric layer on a substrate having a patterned area and a blanket area by exposing the substrate to at least a deposition precursor and a tuning gas simultaneously without the presence of plasma in a process chamber, wherein

the deposition precursor gas is reacted to form a chemical reaction by-product,

the chemical reaction by-product is the same as the tuning gas,
the deposition precursor and the tuning gas are provided at an amount that is at least 20% greater than an amount that can be consumed at surfaces of the patterned area and the blanket area, and

a difference in a thickness of the silicon-containing dielectric layer deposited in the patterned area and a thickness of the silicon-containing dielectric layer deposited in the blanket area is less 2%.

15. The method of claim 14, wherein the tuning gas comprises hydrogen gas (H_2) and the silicon-containing dielectric layer comprises a silicon oxide.

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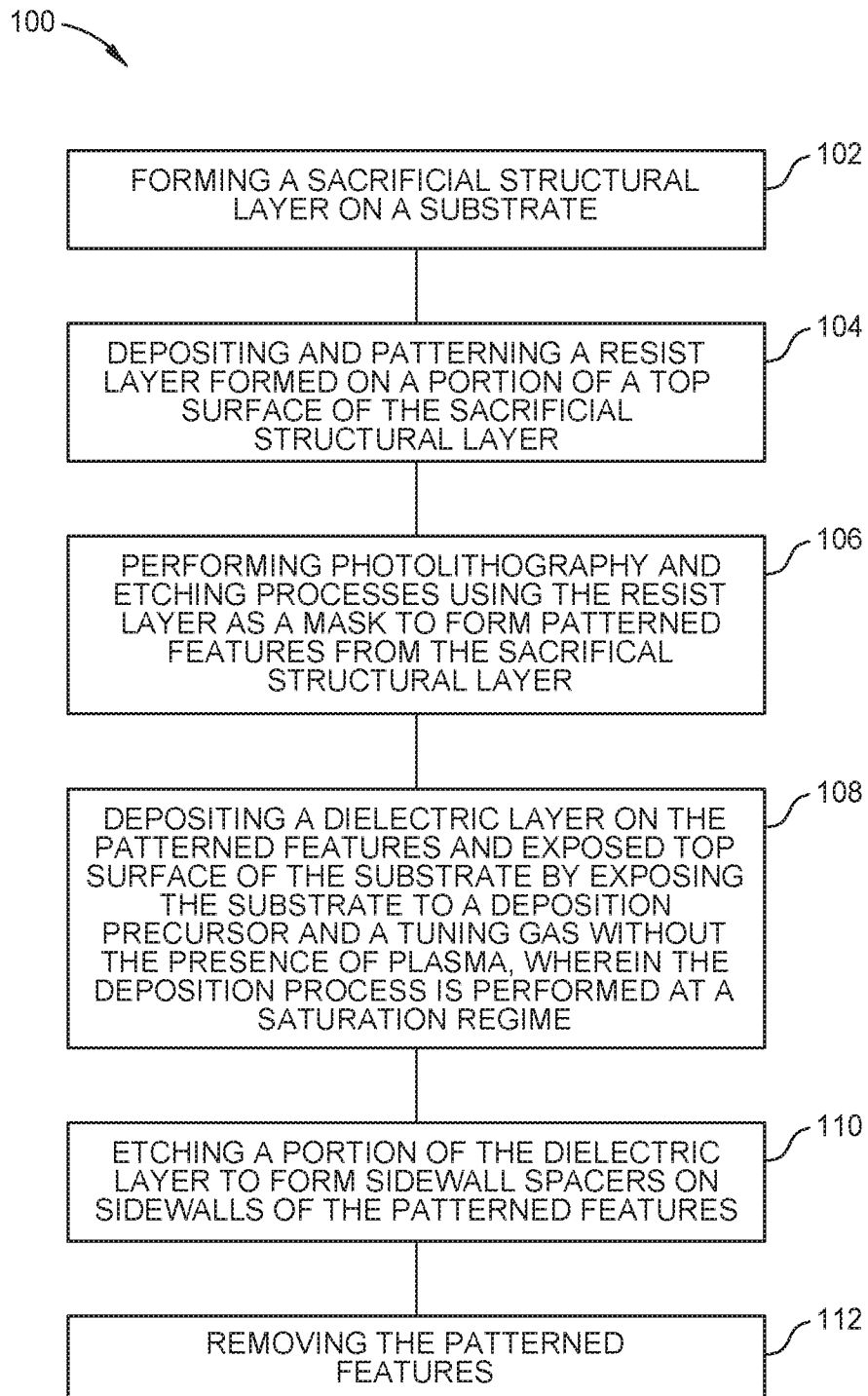


FIG. 1

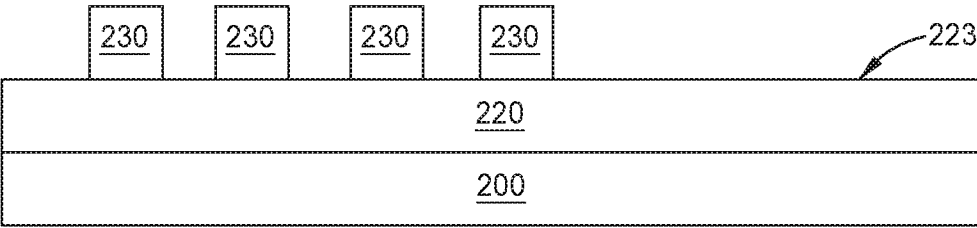


FIG. 2A

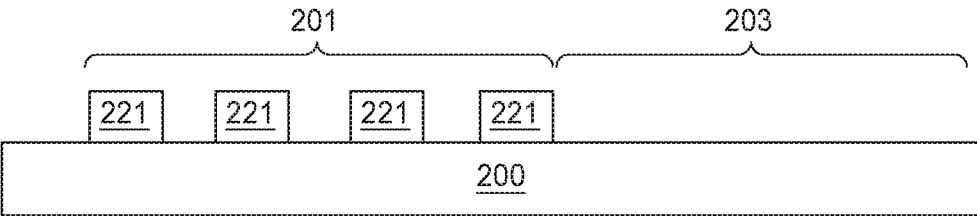


FIG. 2B

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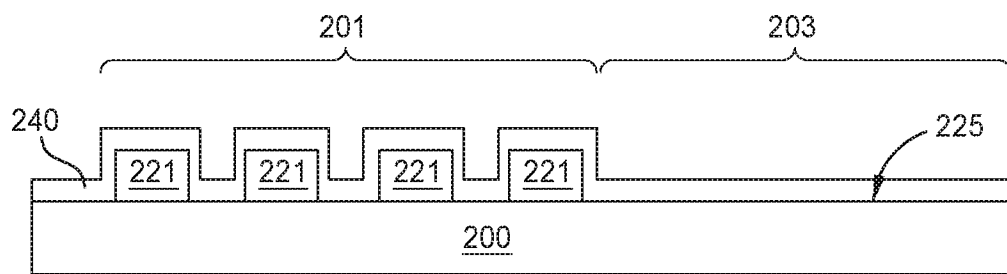


FIG. 2C

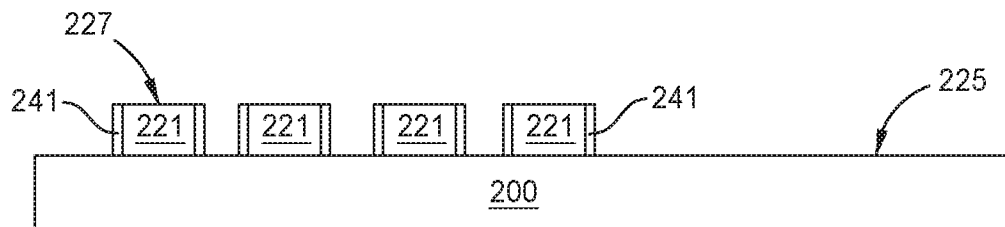


FIG. 2D

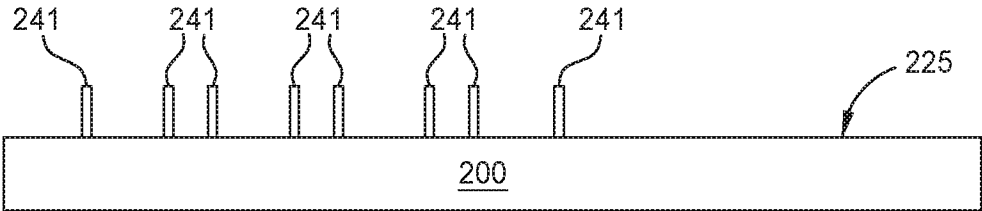


FIG. 2E

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2019/042497**A. CLASSIFICATION OF SUBJECT MATTER****H01L 21/02(2006.01)i, H01L 21/768(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/02; B05C 11/00; C23C 16/34; C23C 16/455; H01L 21/00; H01L 21/316; H01L 21/337; H01L 21/768

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: thermal CVD, conformal dielectric, silicon, hydrogen, tuning gas, byproduct, increase partial pressure

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2012-0142192 A1 (DONGQING LI et al.) 07 June 2012 See claims 1-4 and figures 1-3B.	1-15
A	US 9064684 B1 (COLLIN K. L. MUI et al.) 23 June 2015 See column 11, lines 17-24, column 18, lines 2-5, claim 1 and figure 8.	1-15
A	US 2011-0223774 A1 (SASHA KWESKIN et al.) 15 September 2011 See claims 1-5 and figure 1.	1-15
A	WO 2005-059200 A1 (APPLIED MATERIALS, INC. et al.) 30 June 2005 See claims 24, 38.	1-15
A	US 7919416 B2 (WOO-JIN LEE et al.) 05 April 2011 See claims 1-3.	1-15



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

06 November 2019 (06.11.2019)

Date of mailing of the international search report

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Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2019/042497

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2012-0142192 A1	07/06/2012	CN 103038868 A JP 2013-533639 A KR 10-1847593 B1 KR 10-2013-0093103 A SG 187043 A1 TW 201209920 A US 8318584 B2 WO 2012-015610 A2 WO 2012-015610 A3	10/04/2013 22/08/2013 24/05/2018 21/08/2013 28/02/2013 01/03/2012 27/11/2012 02/02/2012 26/04/2012
US 9064684 B1	23/06/2015	US 8278224 B1	02/10/2012
US 2011-0223774 A1	15/09/2011	TW 201134977 A US 8236708 B2 WO 2011-112330 A2 WO 2011-112330 A3	16/10/2011 07/08/2012 15/09/2011 05/01/2012
WO 2005-059200 A1	30/06/2005	CN 102586757 A CN 102586757 B CN 1906326 A CN 1906326 B EP 1685272 A1 EP 1685272 B1 EP 1788118 A2 EP 1788118 A3 JP 2007-515060 A JP 4801591 B2 KR 10-1216202 B1 KR 10-1216203 B1 KR 10-1254115 B1 KR 10-2006-0113959 A KR 10-2011-0139323 A KR 10-2012-0008074 A US 2005-0109276 A1 US 2006-0102076 A1	18/07/2012 03/09/2014 31/01/2007 16/05/2012 02/08/2006 26/11/2008 23/05/2007 04/07/2007 07/06/2007 26/10/2011 27/12/2012 27/12/2012 12/04/2013 03/11/2006 28/12/2011 25/01/2012 26/05/2005 18/05/2006
US 7919416 B2	05/04/2011	JP 2011-054968 A KR 10-1732187 B1 KR 10-2011-0025086 A US 2010-0143609 A1 US 2010-0144162 A1 US 2010-0184302 A1 US 2010-0221925 A1 US 7972980 B2 US 8142862 B2 US 8765233 B2	17/03/2011 02/05/2017 09/03/2011 10/06/2010 10/06/2010 22/07/2010 02/09/2010 05/07/2011 27/03/2012 01/07/2014