(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
9 August 2012 (09.08.2012)

WIPO | PCT

(10) International Publication Number
WO 2012/106471 A1

(51) International Patent Classification:
H03K 19/096 (2006.01)

(21) International Application Number:
PCT/US2012/023545

(22) International Filing Date:
1 February 2012 (01.02.2012)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
13/019,950 2 February 2011 (02.02.2011) US

(71) Applicant *(for all designated States except US)*: **SYNOPSYS, INC.** [US/US]; 700 East Middlefield Road, Mountain View, CA 94043 (US).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: **FERREIRA DE FIGUEIREDO, Pedro, Miguel** [PT/PT]; Rua Helena Felix No. 68 2o Dto, P-2785-504 S. Domingos De Rana (PT).

(74) Agent: **BARNES, Glenn, D.**; Murabito Hao & Barnes LLP, Two North Market Street, Third Floor, San Jose, CA 95113 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

(54) **Title**: MULTIVOLTAGE CLOCK SYNCHRONIZATION

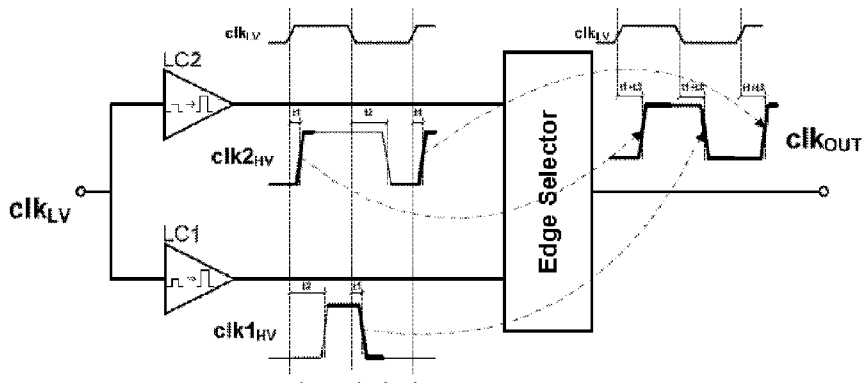

FIG. 5

(57) **Abstract**: A level converter circuit is disclosed. The level converter circuit includes a first level converter that generates a first output signal, and a second level converter that generates a second output signal. The level converter circuit further includes an edge selector coupled to the first level converter and the second level converter that selects a rising edge of either the first output signal or the second output signal, and selects a falling edge of either the first output signal or the second output signal to generate an optimized output signal.

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MULTIVOLTAGE CLOCK SYNCHRONIZATION

FIELD OF THE INVENTION

[001] The present invention is generally related to digital computer systems.

BACKGROUND OF THE INVENTION

[002] Analog circuits often need to distribute a clock signal to multiple voltage domains through the course of their operation. A common situation is in CMOS Analog-to-Digital Converters (ADCs) used in communication and video systems, where the input sampling switch is on 2.5/3.3 Volt domain and the core of the ADC is on 1.2 Volt domain. These two clock domains must be well aligned to allow high frequency operation with low sampling jitter and distortion. In fact, this misalignment is often one of the major sources of distortion on a high-speed ADC. In certain conditions, it may even be the dominant factor.

[003] The circuit of Fig. 1 is typically used for transferring the clock signal from the 1.2 V domain (LV – Low Voltage) to 2.5 V or 3.3 V domain (HV - High Voltage). PMOS transistors (M3/M4) must be weaker than the lower NMOS (M1/M2), to ensure correct operation. One of the transitions depends on the positive feedback of the upper PMOS transistors, and so it is always slower.

[004] In the circuit of Fig. 1, the minimum input-to-output delay is when clk_{LV} goes low, which makes M2 push $clk1_{HV}$ to low. On the other transition, M1 must first push its drain voltage down, and then M4 pushes $clk1_{HV}$ to high, which takes more time.

[005] As shown in Fig. 2, this effect distorts the output duty cycle (38%-47% with 1GHz clock), thereby misaligning the output clock at HV from the original LV one.

[006] The level converter shown in Fig. 3 operates on the complementary output, and its minimum input-to-output delay is when clk_{LV} (and thus when $clk2_{HV}$) goes high. The output duty cycle is also distorted, but in the opposite direction (56%-67% with 1GHz clock, as shown in Fig. 4).

[007] Several improved level converter circuits have been proposed in literature, but none addresses the fundamental asymmetry, described above, that generates transition dependent delay times.

[008] This is a serious problem, because to align the LV clocks with the HV clocks, a delay must be added to the LV clock. For this alignment to be effective the level converter must present a similar propagation delay in the two edges - this is achieved by maintaining the duty-cycle in the LV-to-HV conversion. Furthermore, to enhance the alignment robustness across process, temperature and supply voltage variations, it is also important to minimize the propagation delay of the level converter.

SUMMARY OF THE INVENTION

[009] Embodiments of the present invention solve the problem whereby in order to align low-voltage clocks with high voltage clocks, a delay must be added to the low-voltage clock. Furthermore, embodiments of the present invention also ensure that the duty-cycle is maintained on the low-voltage to high voltage conversion in order to maintain an effective alignment.

[010] In one embodiment, the present invention is implemented as a level converter circuit. The level converter circuit includes a first level converter that generates a first output signal, and a second level converter that generates a second output signal. The level converter circuit further includes an edge selector coupled to the first level converter and the second level converter that selects a rising edge of either the first output signal or the second output signal, and selects a falling edge of either the first output signal or the second output signal to generate an optimized output signal.

[011] In one embodiment, the present invention is implemented as an improved low-to-high level converter, where the output clock is constructed from the best edge of two complementary level converters. Additionally, embodiments of the present invention utilize the outputs of the 2 problem entry level converters, wherein the first has the minimum propagation delay in the high to low transition, and wherein the second has the minimum propagation delay in the low to high transition.

[012] In this manner, embodiments of the present invention solve the duty cycle distortion problem that occurs with conventional implementations and offers minimum delay. When used in high-speed/high-resolution ADCs, embodiments of the present invention improve the distortion at the sampling network significantly. This improvement occurs because embodiments of the present invention advantageously maximize the sampling time which, in conventional implementations, is significantly reduced.

[013] The foregoing is a summary and thus contains, by necessity, simplifications, generalizations and omissions of detail; consequently, those skilled in the art will appreciate that the summary is illustrative only and is not intended to be in any way limiting. Other aspects, inventive features, and advantages of the present invention, as defined solely by the claims, will become apparent in the non-limiting detailed description set forth below.

BRIEF DESCRIPTION OF THE DRAWINGS

[014] The present invention is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings and in which like reference numerals refer to similar elements.

[015] Figure 1 shows a conventional level converter circuit in accordance with the prior art.

[016] Figure 2 shows an output diagram of a level converter circuit in accordance with the prior art.

[017] Figure 3 shows a second conventional level converter circuit in accordance with the prior art.

[018] Figure 4 an output diagram of a level converter circuit in accordance with the prior art.

[019] Figure 5 shows a level converter circuit generating aligned clock signals in accordance with one embodiment of the present invention.

[020] Figure 6 shows a level converter circuit used as building block in one embodiment of the present invention.

[021] Figure 7 shows a level converter circuit implementation in accordance with one embodiment of the present invention.

[022] Figure 8 shows an output diagram of a level converter circuit in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[023] Although the present invention has been described in connection with one embodiment, the invention is not intended to be limited to the specific forms set forth herein. On the contrary, it is intended to cover such alternatives, modifications, and equivalents as can be reasonably included within the scope of the invention as defined by the appended claims.

[024] In the following detailed description, numerous specific details such as specific method orders, structures, elements, and connections have been set forth. It is to be understood however that these and other specific details need not be utilized to practice embodiments of the present invention. In other circumstances, well-known structures, elements, or connections have been omitted, or have not been described in particular detail in order to avoid unnecessarily obscuring this description.

[025] References within the specification to "one embodiment" or "an embodiment" are intended to indicate that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the present invention. The appearance of the phrase "in one embodiment" in various places within the specification are not necessarily all referring to the same embodiment, nor are separate or alternative embodiments mutually exclusive of other embodiments. Moreover, various features are described which may be exhibited by some embodiments and not by others. Similarly, various requirements are described which may be requirements for some embodiments but not other embodiments.

[026] Some portions of the detailed descriptions, which follow, are presented in terms of procedures, steps, logic blocks, processing, and other symbolic representations of operations on data bits within a computer memory. These descriptions and representations

are the means used by those skilled in the data processing arts to most effectively convey the substance of their work to others skilled in the art.

[027] A procedure, computer executed step, logic block, process, etc., is here, and generally, conceived to be a self-consistent sequence of steps or instructions leading to a desired result. The steps are those requiring physical manipulations of physical quantities. Usually, though not necessarily, these quantities take the form of electrical or magnetic signals of a computer readable storage medium and are capable of being stored, transferred, combined, compared, and otherwise manipulated in a computer system. It has proven convenient at times, principally for reasons of common usage, to refer to these signals as bits, values, elements, symbols, characters, terms, numbers, or the like.

[028] It should be borne in mind, however, that all of these and similar terms are to be associated with the appropriate physical quantities and are merely convenient labels applied to these quantities. Unless specifically stated otherwise as apparent from the following discussions, it is appreciated that throughout the present invention, discussions utilizing terms such as "processing" or "accessing" or "writing" or "storing" or "replicating" or the like, refer to the action and processes of a computer system, or similar electronic computing device that manipulates and transforms data represented as physical (electronic) quantities within the computer system's registers and memories and other computer readable media into other data similarly represented as physical quantities within the computer system memories or registers or other such information storage, transmission or display devices.

[029] Figure 5 shows a level converter in accordance with one embodiment of the present invention. As depicted in figure 5, an exemplary operating circuit is shown, where there are 2 level converters, one of each kind, followed by a circuit that “constructs” the output clock using the best edge. As used herein, the term "best edge" the one edge having the lowest delay time of each level converter.

[030] Figure 6 shows a level converter in accordance with an alternative embodiment of the present invention. As depicted in the figure 6 embodiment, it should be seen that clk1HV has the minimum input-to-output delay is when clkLV goes from high to low, and clk2HV has the minimum input-to-output delay is when clkLV goes from low to high.

[031] Figure 7 shows an implementation of a level converter in accordance with one embodiment of the present invention. The figure 7 embodiment illustrates an implementation of the concept depicted in figure 5, using the level converter of figure 6. In the figure 7 embodiment, the clkLV rising edge clk2HV goes high first, which makes the S (set) input of the latch go high, thus causing clkOUT to go high. The feedback through the delays ΔT and the AND gates causes the set input to go low a bit after, and the latch memorizes the previous state (clkOUT = high).

[032] In one embodiment, in the clkLV falling edge clk1HV goes low first, which makes the R (reset) input of the latch go high, thus causing clkOUT to go low. As in the other edge, due to the feedback through the delays ΔT and the AND gates, the R input goes low a bit after, which causes the latch to memorize clkOUT = low.

[033] In one embodiment, for proper operation, the delays ΔT need to be high enough so that the modification of the output state, due to the set/reset of the latch, only reaches the input of the AND gates after transition from the slowest level converter has occurred.

[034] Figure 8 shows a timing output diagram depicting the operation of an exemplary level converter circuit in accordance with one embodiment of the present invention. Specifically, figure 8 illustrates the output clock using the solution of figure 7, which, in the present embodiment, has a duty cycle in the 48%-52% range.

[035] It should be noted that symmetrical duty-cycle and minimum delay allow efficient synchronization with the LV clock by adding matching delays.

[036] In this manner, embodiments of the present invention implement an improved low-to-high level converter, where the output clock is constructed from the best edge of two complementary level converters. Additionally, embodiments of the present invention utilize the outputs of the 2 complementary level converters, wherein the first has the minimum propagation delay in the high to low transition, and wherein the second has the minimum propagation delay in the low to high transition.

[037] In this manner, embodiments of the present invention solve the duty cycle distortion problem that occurs with conventional implementations and offers minimum delay.

When used in high-speed/high-resolution ADCs, embodiments of the present invention improve the distortion at the sampling network significantly. This improvement occurs because embodiments of the present invention advantageously maximize the sampling time which, in conventional implementations, is significantly reduced.

[038] A number of different applications would benefit immensely from the above-described advantages. Such applications include, for example, a number of different systems where it is necessary to convert digital signals to different voltage domains, and where it is important that they are maintained with the same duty cycle, and aligned with each other. Examples include, but are not limited to, various ADC architectures (e.g., Pipeline, Sigma-Delta, SAR ADCs, etc.), and also Digital-to-Analog Converters (DACs).

[039] The foregoing description, for the purpose of explanation, has been described with reference to specific embodiments. However, the illustrated discussions above are not intended to be exhaustive or to limit the invention to the precise forms disclosed. Many modifications and variations are possible in view of the above teachings. Embodiments were chosen and described in order to best explain the principles of the invention and its practical applications, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as may be suited to the particular use contemplated.

CLAIMS

What is claimed is:

1. A level converter circuit, comprising:

a first level converter that generates a first output signal;

a second level converter that generates a second output signal;

an edge selector coupled to the first level converter and the second level converter that selects a rising edge of either the first output signal or the second output signal, and selects a falling edge of either the first output signal or the second output signal to generate an optimized output signal.

2. The level converter circuit of claim 1, wherein the first output signal and the second output signal are at a higher voltage than an input signal of the first level converter and an input signal of the second level converter.

3. The level converter circuit of claim 1, wherein a first delay element and a second delay element are coupled to the edge selector to maintain a symmetrical duty-cycle of the optimized output signal.

4. The level converter circuit of claim 1, wherein the first delay element and the second delay element are coupled to the edge selector and are sized to impose a minimum delay to the optimized output signal.

5. The level converter circuit of claim 1, wherein the first output signal, the second output signal, and the optimized output signal comprise clock signals.

6. The level converter circuit of claim 1, wherein the first output signal, the second output signal, and the optimized output signal comprise clock signals from a first voltage domain, and wherein an input signal of the first level converter and an input signal of the second level converter comprise clock signals from a second voltage domain that is different from the first voltage domain.

7. The level converter circuit of claim 1, wherein the edge selector further comprises a latch that selects the rising edge of either the first output signal or the second output signal, and selects the falling edge of either the first output signal or the second output signal to generate the optimized output signal.

8. An integrated circuit device, comprising:

a first level converter that generates a first output signal;

a second level converter that generates a second output signal;

an edge selector coupled to the first level converter and the second level converter that selects a rising edge of either the first output signal or the second output signal, and selects a falling edge of either the first output signal or the second output signal to generate an optimized output signal.

9. The integrated circuit device of claim 8, wherein the first output signal and the second output signal are at a higher voltage than an input signal of the first level converter and an input signal of the second level converter.

10. The integrated circuit device of claim 8, wherein a first delay element and a second delay element are coupled to the edge selector to maintain a symmetrical duty-cycle of the optimized output signal.

11. The integrated circuit device of claim 8, wherein the first delay element and the second delay element are coupled to the edge selector and are sized to impose a minimum delay to the optimized output signal.

12. The integrated circuit device of claim 8, wherein the first output signal, the second output signal, and the optimized output signal comprise clock signals.

13. The integrated circuit device of claim 8, wherein the first output signal, the second output signal, and the optimized output signal comprise clock signals from a first voltage domain, and wherein an input signal of the first level converter and an input signal of

the second level converter comprise clock signals from a second voltage domain that is different from the first voltage domain.

14. The integrated circuit device of claim 8, wherein the edge selector further comprises a latch that selects the rising edge of either the first output signal or the second output signal, and selects the falling edge of either the first output signal or the second output signal to generate the optimized output signal.

15. A CMOS integrated circuit device, comprising:

a first level converter that generates a first output signal;

a second level converter that generates a second output signal;

an edge selector coupled to the first level converter and the second level converter that selects a rising edge of either the first output signal or the second output signal, and selects a falling edge of either the first output signal or the second output signal to generate an optimized output signal.

16. The CMOS integrated circuit device of claim 15, wherein the first output signal and the second output signal are at a higher voltage than an input signal of the first level converter and an input signal of the second level converter.

17. The CMOS integrated circuit device of claim 15, wherein a first delay element and a second delay element are coupled to the edge selector to maintain a symmetrical duty-cycle of the optimized output signal, and wherein the first delay element and the second delay element are coupled to the edge selector and are sized to impose a minimum delay to the optimized output signal.

19. The CMOS integrated circuit device of claim 15, wherein the first output signal, the second output signal, and the optimized output signal comprise clock signals.

20. The CMOS integrated circuit device of claim 15, wherein the edge selector further comprises a latch that selects the rising edge of either the first output signal or the

second output signal, and selects the falling edge of either the first output signal or the second output signal to generate the optimized output signal.

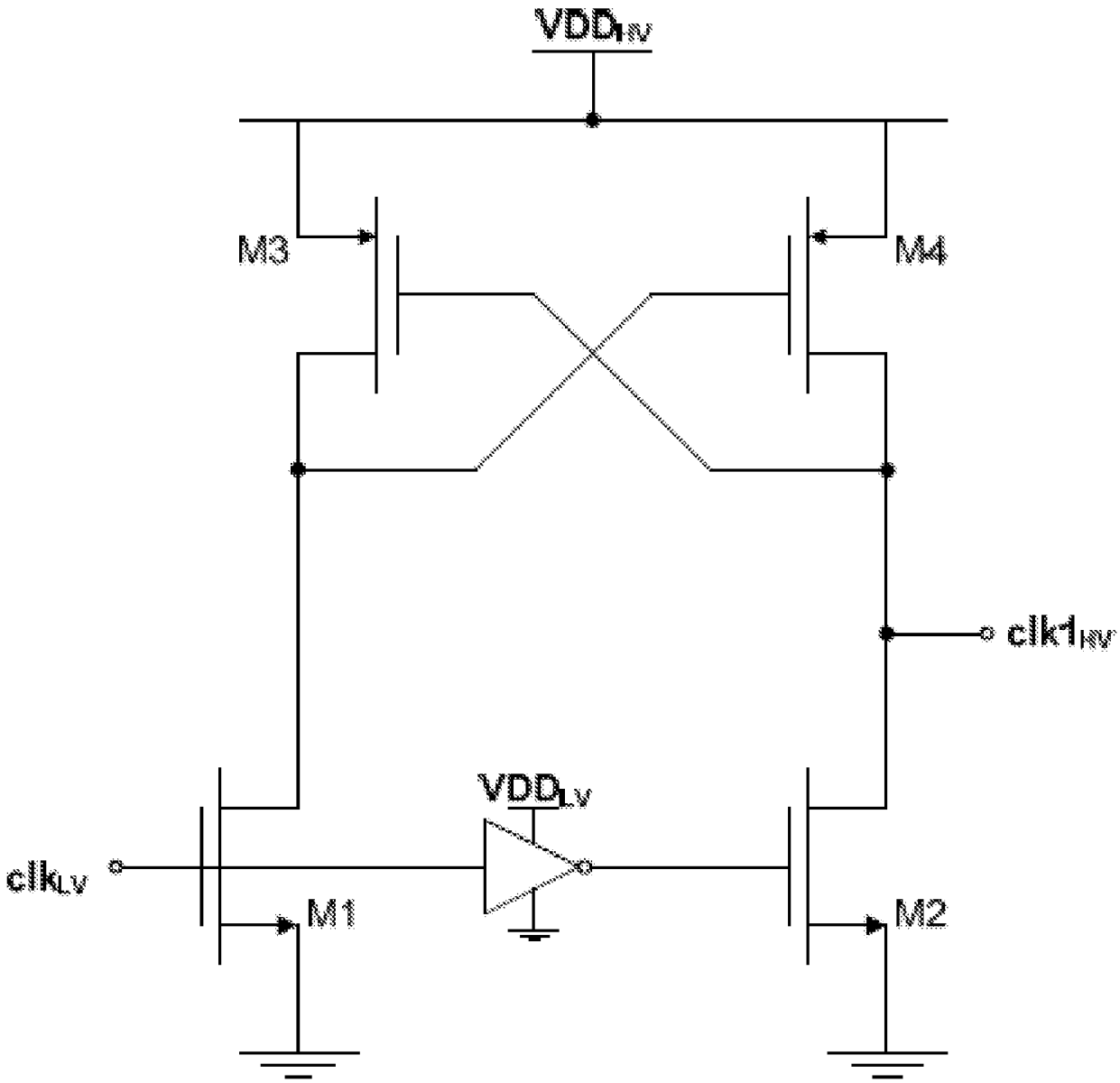


FIG. 1
(Prior Art)

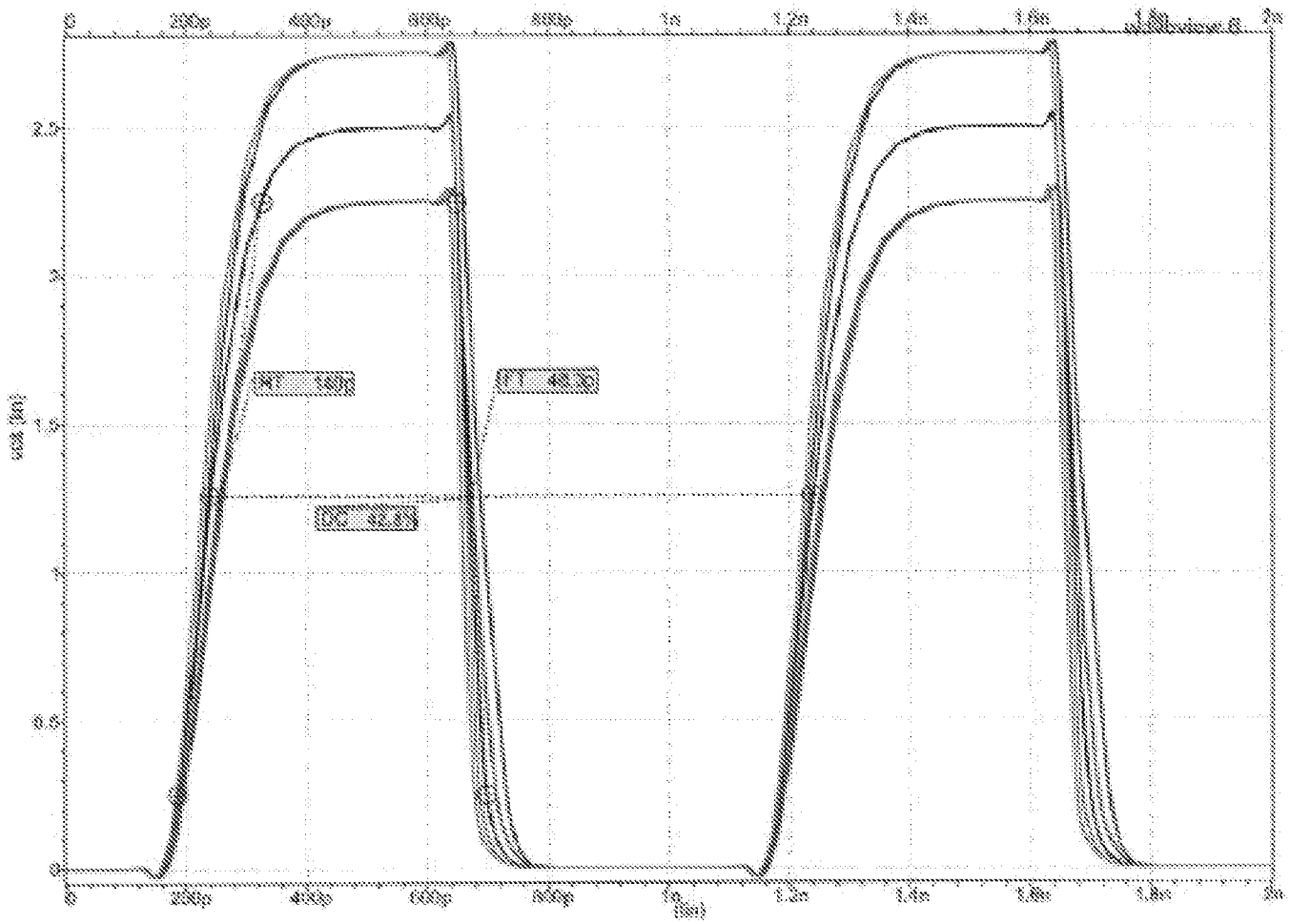


FIG. 2
(Prior Art)

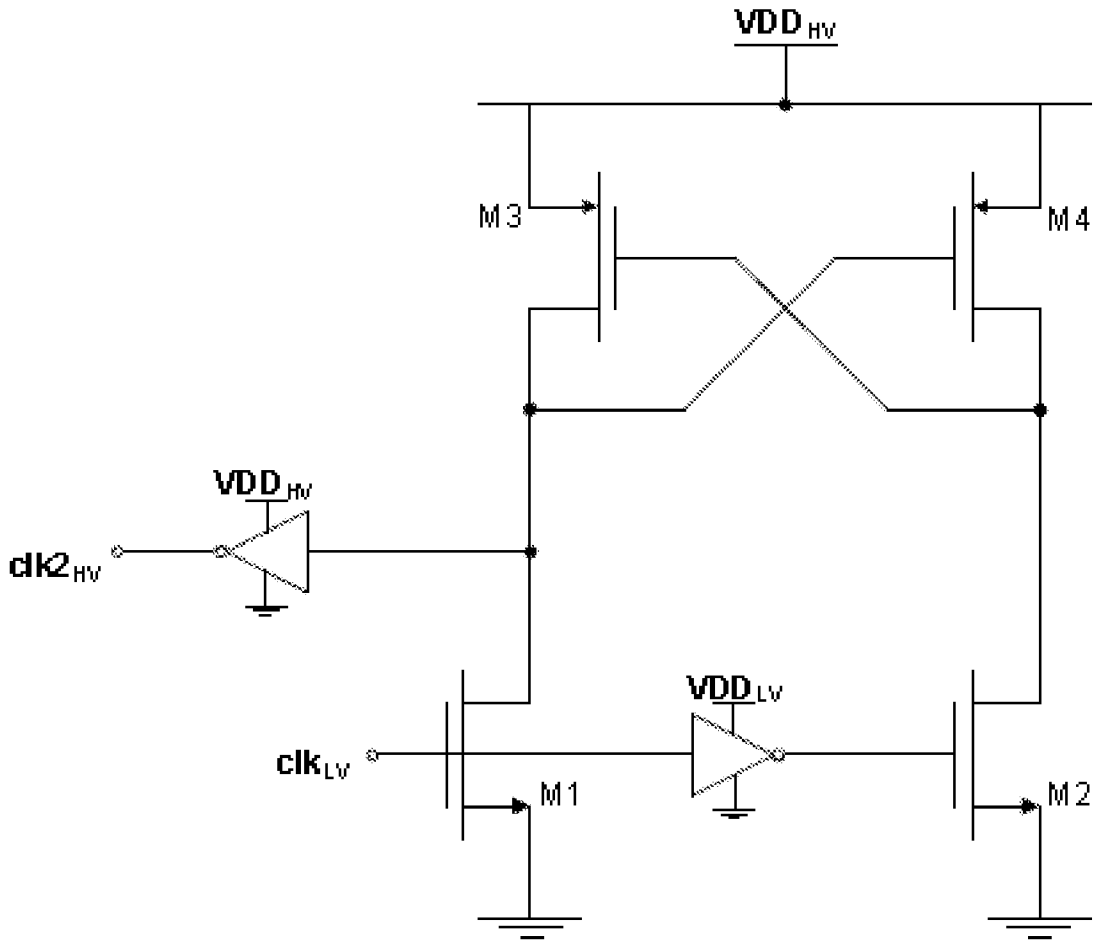


FIG. 3
(Prior Art)

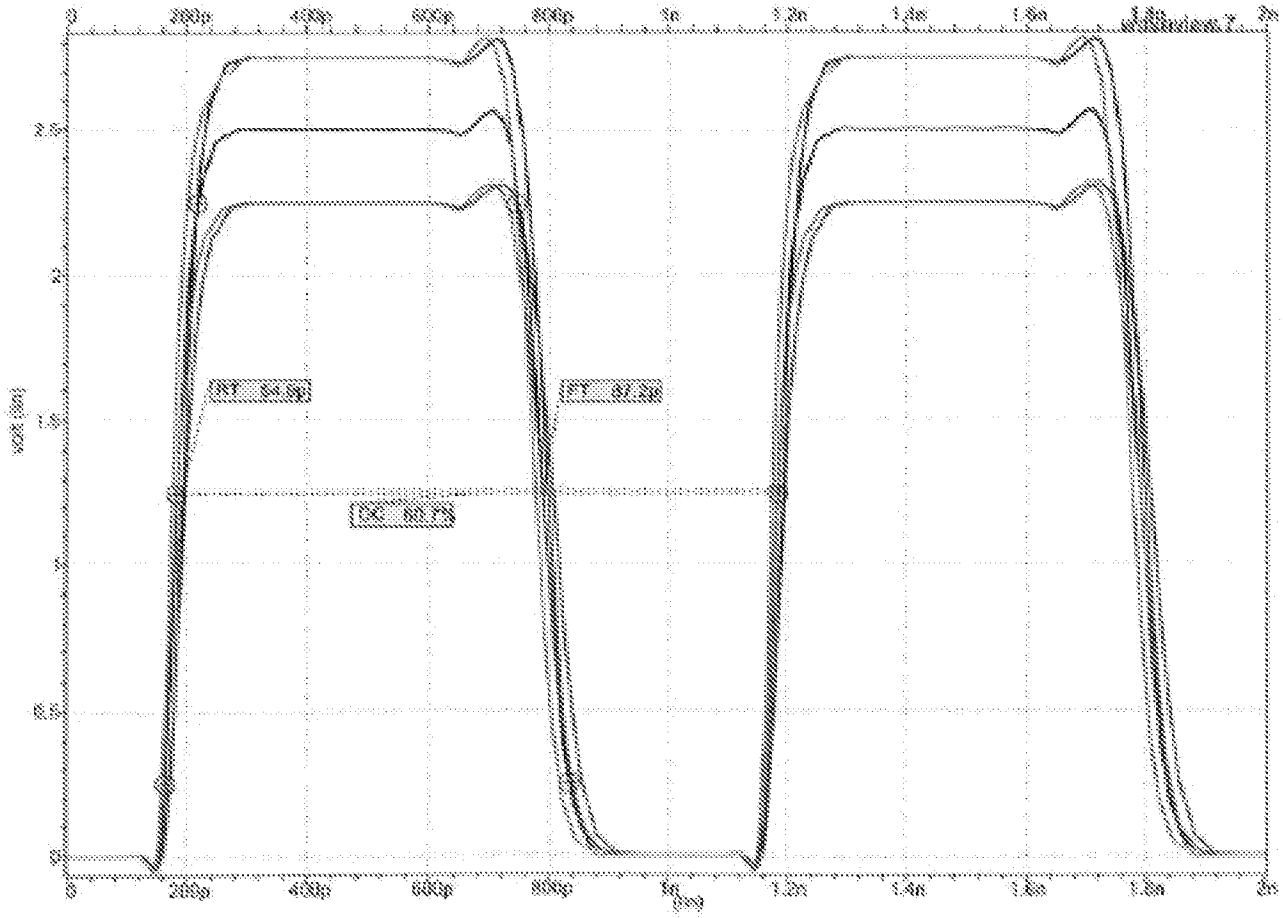


FIG. 4
(Prior Art)

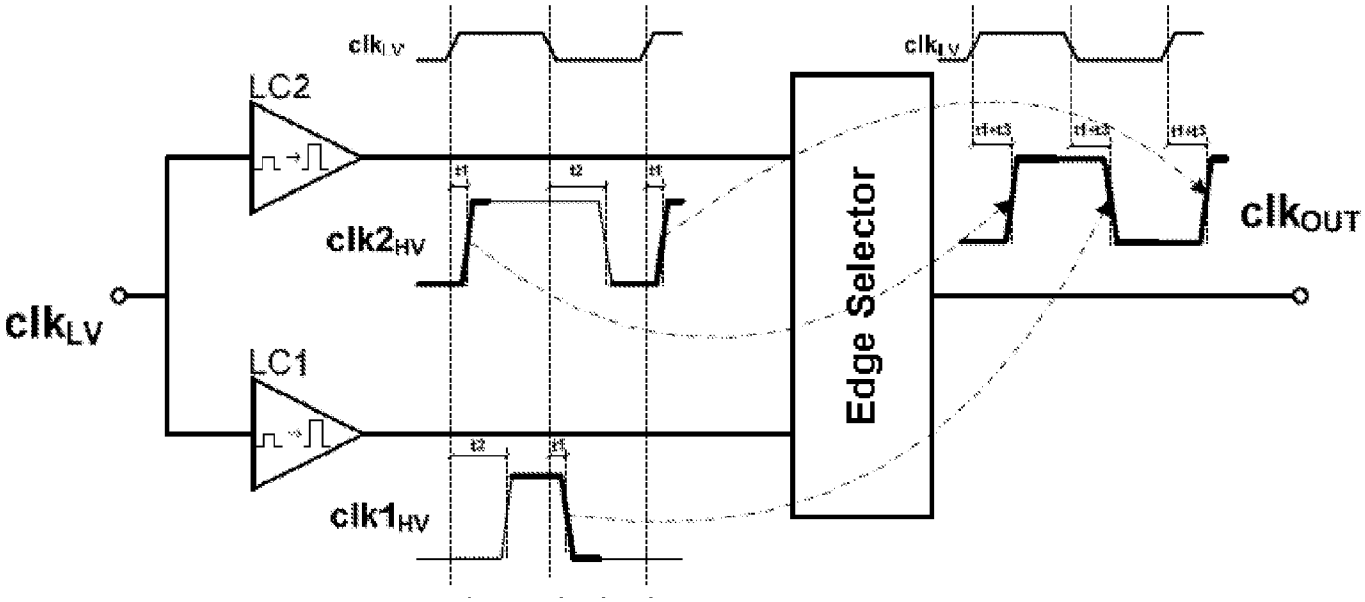


FIG. 5

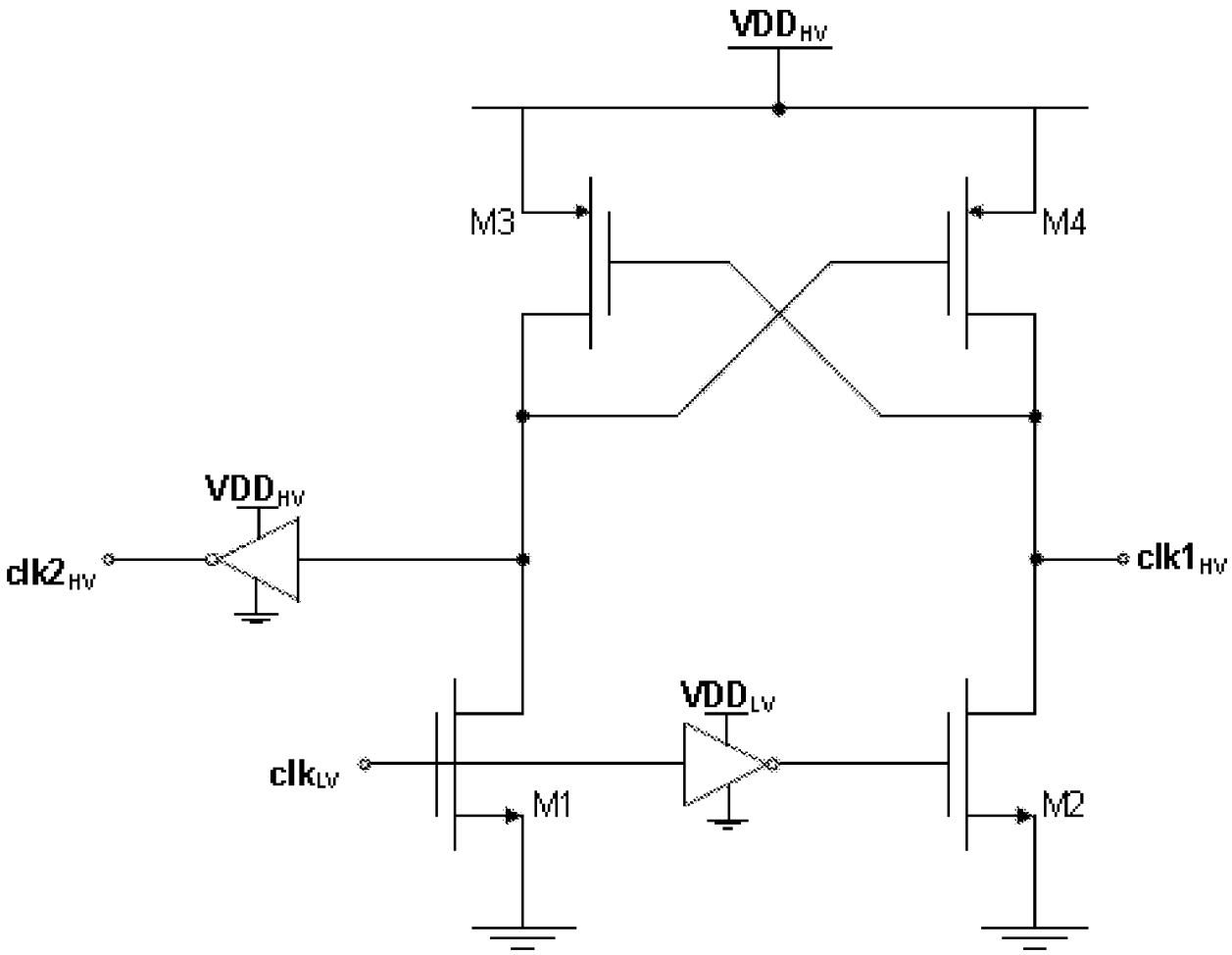


FIG. 6

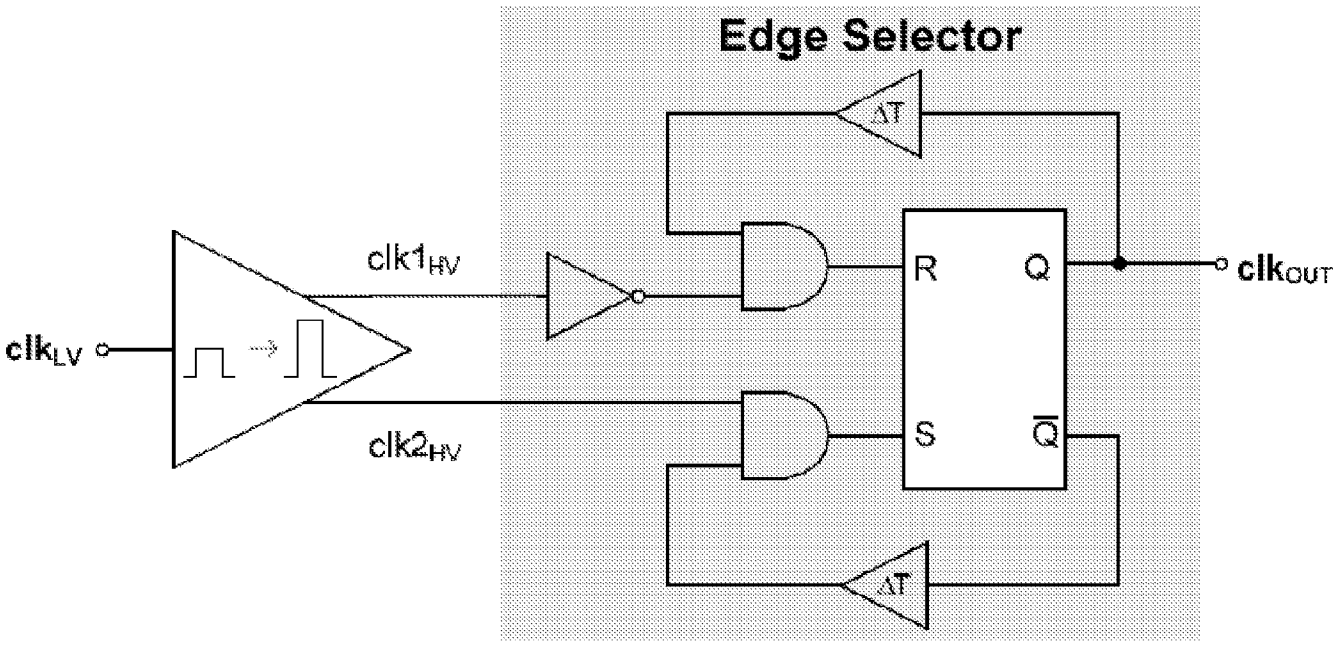
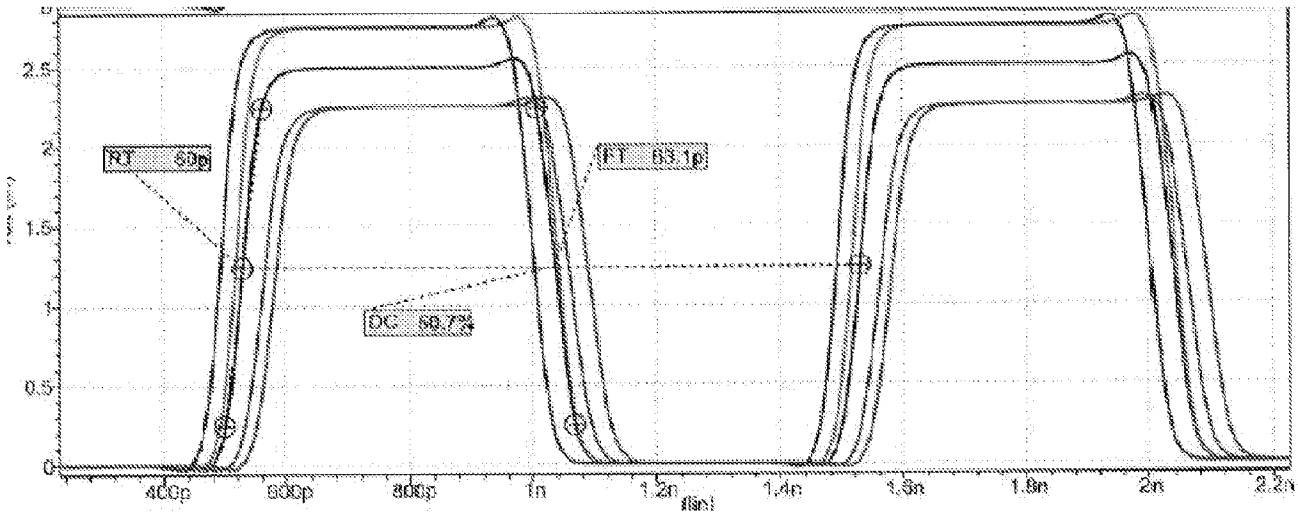


FIG. 7


RT 63p
FT 63.1p
DC 50.7%
2.5
2
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1
0.5
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400p
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2n
2.2n

FIG. 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 2012/023545

A. CLASSIFICATION OF SUBJECT MATTER ***H03K 19/096*** *(2006.01)*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H03K 19/00-19/12, 3/00, H03F 3/00-3/45, G11C 5/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch (RUPTO internal), Esp@cenet, PAJ, DWPI, USPTO

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2003/0189477 A1 (ANDRE SCHAFER et al.) 09.10.2003, par. [0002]-[0007], [0009]-[0015], [0031]-[0036]	1, 2, 8, 9, 15, 16
A	US 5805005 A (EXAR CORPORATION) 08.09.1998	1-19
A	RU 2104601 C1 (PILKINGTON MIKROELEKTRONIKS LIMITED) 10.02.1998	1-19
A	RU 2085030 C1 (BELENKY YURY VENIAMINOVICH et al.) 20.07.1997	1-19

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
19 April 2012 (19.04.2012)	17 May 2012 (17.05.2012)
Name and mailing address of the ISA/ FIPS Russia, 123995, Moscow, G-59, GSP-5, Berezhkovskaya nab., 30-1 Facsimile No. +7 (499) 243-33-37	Authorized officer V. Sagitov Telephone No. 499-240-25-91

Form PCT/ISA/210 (second sheet) (July 2009)