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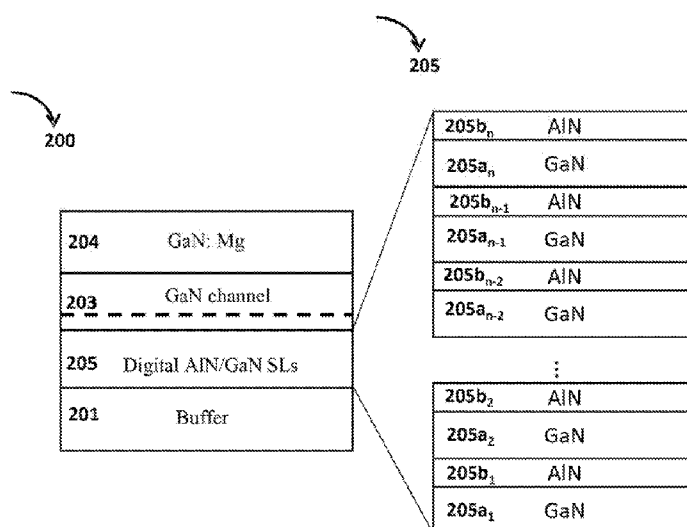


Figure 2

(57) Abstract: A III-nitride power handling device and the process of making the III-nitride power handling device are disclosed that use digital alloys as back barrier layer to mitigate the strain due to lattice mismatch between the channel layer and the back barrier layer and to provide increased channel conductivity. An embodiment discloses a GaN transistor using a superlattice binary digital alloy as back barrier comprising alternative layers of AlN and GaN. Other embodiments include using superlattice structures with layers of GaN and AlGa_xN_{1-x} as well as structures using AlGa_xN_{1-x}/AlGa_yN_{1-y} stackups that have different Aluminum concentrations. The disclosed device has substantially increased channel conductivity compared to traditional analog alloy back barrier devices.

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DIGITAL ALLOY BASED BACK BARRIER FOR P-CHANNEL NITRIDE TRANSISTORS

TECHNICAL FIELD

[0001] The present disclosure is directed in general to the area of III-Nitride transistors and in particular to the design and fabrication of P-Channel GaN Transistors.

BACKGROUND OF THE DISCLOSURE

[0002] GaN power integrated circuits (IC) have the potential of dramatically reducing the size and weight of power electronic systems, thereby substantially reducing the cost of power electronic devices. P-channel GaN-transistor is a critical component for making GaN power ICs. Such power electronic systems are widely needed in electric/hybrid vehicles, more-electric aircrafts, as well as many consumer electronic products.

[0003] A variety of GaN transistors are known and they include P-Channel transistors in conjunction with N-Channel transistors using an analog alloy to improve conductivity. The use of a tertiary alloy such as AlGa_xN_{1-x} (Aluminum-Gallium-Nitride) is often referred to as analog alloy in the art. To increase power handling capacity of GaN transistors, several techniques have been exploited to increase channel conductivity.

[0004] It is important to achieve low channel resistance so that the total power consumption can be reduced as well as the device speed can be improved. Increasing the carrier density is one common option that is exploited often. This can be achieved by using high Aluminum (Al) compositions such as AlGa_xN_{1-x} as back barrier beneath the GaN channel. Higher the aluminum content, higher is the channel conductivity. However thick analog AlGa_xN_{1-x} with high Al content cannot be grown on GaN buffer due to the lattice mismatch. This is a fundamental limit of using analog AlGa_xN_{1-x} alloys as the back-barrier.

[0005] The proposed technology overcomes this limitation by proposing a new way to increase channel conductivity while managing the stress related to lattice mismatch.

SUMMARY OF THE DISCLOSURE

[0006] To address one or more of the above-deficiencies of the prior art, one embodiment described in this disclosure provides for a power handling device comprising, a III-

nitride channel layer, a III-nitride cap layer on the channel layer, where the cap layer has higher level of p-type doping than the channel layer, and a III-nitride digital alloy back barrier below the channel layer comprising a superlattice or superlattice structure. According to an embodiment of the present disclosure, a superlattice is a layer consisting of at least three alternating layers of a material A and a material B; each layer of material A and each layer of material B having a thickness of less than 10 nanometer.

[0007] Another embodiment described in this disclosure provides for a process of making a power handling device comprising the steps of depositing a buffer layer on a substrate, depositing a digital alloy back barrier layer on the buffer layer, depositing a III-nitride channel on the digital alloy layer, depositing a III-nitride p-doped cap layer on the channel layer, etching a gate recess in the cap layer exposing the channel layer, depositing a gate dielectric inside the gate recess and depositing a gate metal inside the gate recess and on the gate dielectric wherein, the digital alloy layer is made up of superlattice structure.

[0008] An embodiment of this disclosure comprises a power handling device having: a III-nitride channel layer, a III-nitride cap layer on the channel layer, where the cap layer has higher level of p-type doping than the channel layer, and a III-nitride digital alloy back barrier below the channel layer; the III-nitride digital alloy back barrier comprising a superlattice structure.

[0009] According to an embodiment of this disclosure, the power handling device further comprises a buffer layer below the digital alloy back barrier layer.

[0010] According to an embodiment of this disclosure, the III-nitride channel layer is a Gallium Nitride (GaN) channel layer.

[0011] According to an embodiment of this disclosure, the cap layer is a Magnesium (Mg) doped GaN.

[0012] According to an embodiment of this disclosure, the digital alloy back barrier is a binary alloy.

[0013] According to an embodiment of this disclosure, the superlattice structure comprises alternating Aluminum Nitride (AlN) and GaN layers.

[0014] According to an embodiment of this disclosure, the superlattice structure comprises ternary alloys.

[0015] According to an embodiment of this disclosure, the superlattice structure comprises alternating GaN and Aluminum-Gallium-Nitride (AlGa_N) layers.

[0016] According to an embodiment of this disclosure, the superlattice structure comprises alternating AlGa_N and AlGa_N layers with different Aluminum percentages.

[0017] According to an embodiment of this disclosure, the digital alloy is designed to

mitigate strain due to lattice mismatch between the channel layer and the digital alloy back barrier layer.

[0018] An embodiment of this disclosure also comprises a of making a power handling device comprising: depositing a buffer layer on a substrate; depositing a digital alloy back barrier layer on the buffer layer; depositing a III-nitride channel on the digital alloy layer; depositing a III-nitride p-doped cap layer on the channel layer; etching a gate recess in the cap layer exposing the channel layer; depositing a gate dielectric inside the gate recess; and depositing the gate metal inside the gate recess and on the gate dielectric, wherein the digital alloy layer is made up of superlattice structure.

[0019] According to an embodiment of this disclosure, the III-nitride channel is GaN and the cap layer is a Magnesium (Mg) doped GaN.

[0020] According to an embodiment of this disclosure, the digital alloy back barrier is a binary alloy.

[0021] According to an embodiment of this disclosure, the superlattice structure comprises alternating Aluminum Nitride (AlN) and GaN layers.

[0022] According to an embodiment of this disclosure, the superlattice structure comprises ternary alloys.

[0023] According to an embodiment of this disclosure, the superlattice structure comprises alternating GaN and Aluminum-Gallium-Nitride (AlGaN) layers.

[0024] According to an embodiment of this disclosure, the superlattice structure comprises alternating AlGaN and AlGaN layers with different Aluminum percentages.

[0025] According to an embodiment of this disclosure, the digital alloy is designed to mitigate the strain due to lattice mismatch between the channel layer and the digital alloy back barrier layer.

[0026] According to an embodiment of this disclosure, the digital alloy layer is between 1 micrometer and 2 micrometer thick.

[0027] An embodiment of this disclosure comprises a P-channel III-nitride transistor having: a III-nitride channel layer, and a III-nitride digital alloy back barrier below the channel layer; the III-nitride digital alloy back barrier comprising a superlattice structure.

[0028] Certain embodiments may provide various technical advantages depending on the implementation. For example, a technical advantage of some embodiments may include the use of binary digital alloy such as stacked up layers of Aluminum Nitride and Gallium Nitride. Other embodiments may use stack up of ternary digital alloys.

[0029] Although specific advantages have been enumerated above, various embodiments may include some, none, or all of the enumerated advantages. Additionally, other technical advantages may become readily apparent to one of ordinary skill in the art after review of the following figures and description.

BRIEF DESCRIPTION OF THE DRAWINGS

[0030] For a more complete understanding of the present disclosure and its advantages, reference is now made to the following description taken in conjunction with the accompanying drawings, in which like reference numerals represent like parts:

[0031] Figure 1 illustrates a conventional p-channel GaN structure with analog AlGaIn back barrier;

[0032] Figure 2 illustrates a p-channel GaN device containing digital AlN-GaN super lattice structure alloys as the back barrier, according to an embodiment of the present disclosure;

[0033] Figures 3a, 3b and 3c illustrate the first set of steps involved in the fabrication of a p-channel GaN transistor containing digital AlN-GaN super lattice alloys as the back barrier, according to an embodiment of the present disclosure;

[0034] Figures 4a, 4b and 4c illustrate the next set of steps involved in the fabrication of a p-channel GaN transistor containing digital AlN-GaN super lattice alloys as the back barrier, according to an embodiment of the present disclosure;

[0035] Figure 5a illustrates a p-channel GaN transistor structure according to an embodiment of the present disclosure;

[0036] Figure 5b illustrates the channel conductivity characteristics for the p-channel GaN transistor structure illustrated in Figure 5a;

[0037] Figure 5c illustrates a p-channel GaN transistor structure according to an embodiment of the present disclosure;

[0038] Figure 5d illustrates the channel conductivity characteristics for the p-channel GaN transistor structure illustrated in Figure 5c;

[0039] Figure 6a illustrates a p-channel GaN transistor structure according to an embodiment of the present disclosure;

[0040] Figure 6b illustrates the channel conductivity characteristics for the p-channel GaN transistor structure illustrated in Figure 6a;

[0041] Figure 6c illustrates a p-channel GaN transistor structure according to an embodiment of the present disclosure; and

[0042] Figure 6d illustrates the channel conductivity characteristics for the p-channel GaN transistor structure illustrated in Figure 6c.

DETAILED DESCRIPTION

[0043] It should be understood at the outset that, although example embodiments are illustrated below, the present technology may be implemented using any number of techniques, whether currently known or not. The present technology should in no way be limited to the example implementations, drawings, and techniques illustrated below. Additionally, the drawings are not necessarily drawn to scale.

[0044] Recently, GaN transistors have revolutionized high power and high speed switching electronics and there is a constant push, driven by the application demands, for higher and higher power handling capacities. GaN transistor's power handling capacity depends directly on the channel conductivity.

[0045] III-Nitride semiconductor materials (Aluminum, Indium, Gallium)Nitride are excellent wide band gap semiconductors very suitable for modern electronic and optoelectronic applications. Though this disclosure describes the technology using GaN, the proposed technology applies to any of the III-Nitride semiconductor materials.

[0046] Figure 1 illustrates a conventional p-channel GaN transistor structure. It contains a ternary alloy (102) Aluminum-Gallium Nitride (AlGa_N), which is normally referred to as analog AlGa_N, as the back barrier. This back barrier 102 is directly under the GaN channel 103 as the back barrier layer helps to improve the p-type carrier concentration in the GaN channel, utilizing the polarization effect introduced by the back barrier AlGa_N layer 102. In other words, the higher conduction band energy in the large bandgap AlGa_N barrier layers improves the confinement of carriers in the low bandgap GaN channel compared to the same structure without the AlGa_N barrier underneath the GaN channel. The AlGa_N layer 102 is built on top of a buffer layer 101 and the buffer layer helps introducing more holes from the p-type GaN. A layer of GaN can serve as the buffer layer 101 and can be mounted on a substrate such as a Sapphire (not shown). A layer 104 of p-doped GaN, (such as Magnesium (Mg) doped GaN) on top of the GaN channel 103 completes the formation of a device that can be used to make a typical GaN transistor. A typical GaN transistor using the structure illustrated in Figure 1 uses the polarization effect of the back barrier 102 to increase the channel conductivity. Polarization

induced hole density is a known phenomenon in the art, as the p-type carriers tend to crowd near the polarized barrier.

[0047] To improve the GaN channel conductivity, there are typically two approaches: either increase the carrier density or improve the carrier mobility. The carrier mobility depends the interface roughness, film quality, and other fundamental material properties which are hard to modify. Thus, increasing the carrier density is a more promising approach. The polarization effect in the AlGaN back barrier has a direct effect over the carrier density in the GaN channel. The density increases with increasing the polarization in AlGaN, which can be realized by increasing the percentage of Aluminum in the back barrier.

[0048] To provide enough polarization effect, AlGaN with reasonable thickness is required. However, most of the time the AlGaN back barrier is grown on GaN buffer, which has a larger lattice constant compared to AlGaN. This introduces a tensile strain in the AlGaN film. Increasing the percentage of Aluminum leads to larger tensile strain, which eventually results in cracks in the AlGaN film. Thus, the higher the aluminum concentration in the AlGaN, smaller the AlGaN thickness would be, to provide the needed polarization effect. The use of AlGaN as a back barrier is often referred to as analog back barrier alloy.

[0049] To overcome this limitation due to lattice mismatch and increased strain as we increase the aluminum concentration in the back barrier, this disclosure proposes a new technology, where the back-barrier layers use digital alloy instead of the analog alloy to improve the channel conductivity while minimizing the stress related to the lattice mismatch. Super lattices such as comprised of stacked up AlN/GaN (Aluminum nitride / Gallium Nitride) alternating layers are referred to as digital alloys.

[0050] Figure 2 illustrates a GaN device 200, according to an embodiment of the present disclosure. It uses alternating AlN/GaN layers forming a superlattice structure 205, which is referred to as a digital AlGaN alloy, to serve as the back barrier. Superlattice structures help reduce the cracking issues due to lattice mismatches. At the same time, superlattice structures can provide a polarization effect similar to what the p-type carrier requires to be formed in the GaN channel.

[0051] The GaN device 200 comprises of a buffer layer 201, typically about 1.5 micrometer thick and a digital superlattice alloy 205 back barrier mounted over the buffer layer 201. The super lattice back barrier 205 comprises alternating layers of AlN (205b_{1:n}) and GaN (205a_{1:n}). This structure is also called as binary alloy. Each of the AlN layers (205b_{1:n}) are typically about 2 to 3 nanometer thick, while the GaN layers (205a_{1:n}) can each be typically 2 to 10 nanometer thick. The superlattice (SL) back barrier 205 typically has more than two; preferably 30 to 40

pairs of alternating AlN and GaN layers. An alternative SL structure is an alternating AlGaN and GaN stack up 205 or AlGaN/AlGaN stack up 205 where the AlGaN layers have different amount Aluminum percentages (by weight or volume).

[0052] According to an embodiment of the present disclosure, the superlattice comprises at least three alternating layers of AlN and GaN; each layer having a thickness of less than 10 nanometer.

[0053] The GaN channel layer 203 is fabricated over the digital alloy layer 205. In a typical device, the GaN channel layer can be 50 nanometer to 300 nanometer thick. The Magnesium (Mg) doped GaN cap layer 204 serves to supply the holes to the channel and is fabricated on top of the GaN channel 203. The p-doped GaN cap layer 204 is typically about 100 nanometer to 200 nanometer thick. In this embodiment, the cap layer 204 can have much higher Mg doping due to the higher polarization effect of the digital alloy layer 205. The overall total device thickness is typically less than 3 micrometer.

[0054] The buffer layer 201 can be GaN or AlGaN. The AlGaN/GaN high-electron-mobility transistor requires a thermally conducting, semi-insulating substrate to achieve the best possible performance. The semi-insulating SiC substrate is currently the best choice for this device technology; however, fringing fields which penetrate the GaN buffer layer at pinch-off introduce significant substrate conduction at modest drain bias if channel electrons are not well confined to the nitride structure. The addition of an insulating buffer on the semi-insulating SiC substrate suppresses this parasitic conduction, which results in dramatic improvements in the AlGaN/GaN transistor performance. A pronounced reduction in both the gate-lag and the gate-leakage current are observed for structures with the buffer layer.

[0055] The digital SL alloy back barrier layer 205 provides the necessary polarization effect along the interface with the GaN channel layer 203. Holes crowd along this interface to provide for the necessary channel conductivity. The digital alloy helps providing a thick back barrier with a strong polarization maintained, which helps introduce more holes into the GaN channel layer 203. A transistor made using GaN device 200 was evaluated for performance and found to have substantially higher switching speeds, lower switching loss and a substantially reduced parasitic value.

[0056] The process of making a transistor using the GaN device 200 can comprise fabricating the layers as structured in Figure 3b, followed by the process steps illustrated in Figure 3c and 4a through 4c. The digital alloy 305 can be fabricated as illustrated in Figure 3a.

The alloy 305 can either be fabricated first or alternatively fabricated as part of fabricating the stack as illustrated in Figure 3b.

[0057] The digital alloy 305 can be formed by stacking up alternative layers of GaN and AlN. A GaN layer is formed using one of many known techniques in the art. One such technique is molecular beam epitaxy (MBE). Alternatively, a GaN layer can also be formed by a sputtering process at a high substrate temperature — for example greater than 700-degree Celsius. Since Gallium is a liquid at around 30-degree Celsius, initial nitridation of Gallium liquid metal surface needs to be done in this sputtering process using pure Ga as target surface. A horizontal water cooled stainless steel trough can be used for the growth of GaN epilayer. A reactive Direct Current (DC) magnetron sputter epitaxy can be used. In fabricating the digital alloy 305, a GaN layer is first formed to the required thickness of between 2 nanometer to 10 nanometer, followed by an AlN (Aluminum Nitride) layer formed on top of this GaN layer by several known techniques, such as sputtering, electroplating or MBE. Typically, a 2 nanometer to 3 nanometer thick AlN layer is formed. The process is repeated for subsequent pair of GaN and AlN layers. It is not unusual to form 30 to 40 pairs of GaN/AlN layers by repeating this process, yielding a digital alloy that is less than 3 micrometer thick.

[0058] The process of making the device 200 comprises forming a buffer layer 301 on a substrate 306 of choice, such as Silicon Carbide (SiC) or Sapphire, as illustrated in Figure 3b. The buffer layer 301 can be any suitable material, such as GaN or AlGaIn. The buffer layer is typically about 1 to 2 micrometer thick and preferably 1.5 micrometer thick. The digital alloy 305 is formed on top of this buffer layer as described earlier. Alternatively, the digital alloy can be fabricated separately and deposited on top of the buffer layer by any known techniques such as MBE or a sputtering process. Typically, the digital alloy will be between 1 to 2 micrometer thick and preferably about 1.5 micrometer thick. The GaN channel is fabricated on top of the digital alloy using techniques described earlier. The GaN channel is typically between 50 nanometer to 300 nanometer thick, and preferably 100 nanometer thick. The p-doped GaN layer is formed on top of the GaN channel by any known process, such as MBE or sputtering. In a preferred embodiment, Magnesium (Mg) is used as the p-dopant.

[0059] The next step in the process is to etch a gate recess 307 that exposes the GaN channel 303 as illustrated in Figure 3c. This etching process typically comprises masking the area around and exposing the etching area and using known etching techniques (such as using chemical or gas or laser / molecular beams) to etch out the gate area and exposing a part of the GaN channel 303. Next, a suitable gate dielectric 408 such as Silicon dioxide is deposited as illustrated in Figure 4a by any known techniques, such as depositing Silicon by sputtering followed by

oxidation or any other suitable technique depending on the chosen gate dielectric.

[0060] Figure 4b illustrates the next step of forming the ohmic contacts 409a and 409b on the p-channel. This step comprises of depositing the contact electrode of the device, such as gold, copper or silver and is typically done using electroplating or sputtering process. The final step is to form the gate metal in the cavity of the dielectric as illustrated in Figure 4c. The gate metal can be gold, silver or copper or any other suitable gate material. Depending on the chosen gate material, process such as electroplating or sputtering can be used. The surfaces can be polished, cleaned and separated from the substrate to form the device 200.

[0061] In the process steps described above, any of the steps illustrated can be changed, modified or eliminated to better suit the materials chosen or as known to one in the art. Additional steps may be added as needed to perfect the device fabrication per specification.

[0062] Several test fabrications and characterization of the proposed technology were carried out to characterize and quantify the benefits of the proposed technology. Since the density of hole along the channel is one of the prime factor deciding the power handling capacity of the device, the tests measure current flow as a function of applied voltage for various device structures. Figures 5a-5d and Figures 6a-6d illustrate the results of this study. The structures are illustrated on the left (Figures 5a, 5c, 6a and 6c) while the performance characteristics of the respective structures are illustrated on the right (Figures 5b, 5d, 6b and 6d).

[0063] Figure 5a illustrates a GaN transistor structure having an epi structure without the back barrier. It comprises of the Buffer layer 501 and having a GaN channel 503 on top. The p-doped GaN layer 504 using Mg as the dopant is deposited on top of the GaN channel 503. The ohmic contacts 509a and 509b is used to apply a voltage to the device and current through the structure is measured. On the right is the measured performance characteristics of this structure as shown in Figure 5b. The X-axis 512 is the voltage applied in Volts between the ohmic contacts 509a and 509b. The Y-axis 511 is the measured current through the device in μ amps. It can be noted that as the voltage is varied between -10v to +10v, the current through the device as shown by the curve 521 linearly increases between -150 μ amps to + 150 μ amps. This baseline performance can be compared with the performance of the subsequent improvements in the device structure.

[0064] Figure 5c illustrates a revised device structure where an analog alloy 502 is added to the device. This analog alloy 502 creates the polarization effect along the GaN channel boundary causing hole crowding and increased current flow. Figure 5d illustrates the performance of this structure in Figure 5c. For the same range of applied voltage (-10v to +10v), the current increases to -410 μ amps to + 410 μ amps as shown by the performance curve 522. This is almost

a threefold increase in the device conductivity, primarily caused by the introduction of the analog alloy 502.

[0065] Next, we compare the performance of having a AlN spacer 612, which is primarily introduced between the GaN channel 503 and the AlGaIn layer 502 as illustrated in Figure 6a, to mitigate the stress due to the lattice mismatch. This spacer 612 marginally increases the current flow as shown by the curve 623 to about -580 μ amps to +580 μ amps as the applied voltage between the ohmic contacts is varied in the same range of -10v to +10v. The structure in Figure 6a has a marginally better performance 623 in Figure 6b compared with the performance curves 521 and 522. The spacer 612 also helps mitigate the stress due to lattice mismatch between the GaN layer 503 and the analog alloy 502.

[0066] Finally, we illustrate the substantial performance improvement of the proposed technology. Figure 6c illustrates the digital alloy layer 605 replacing the analog alloy 502, located between the Buffer layer 501 and the GaN channel 503. The corresponding performance curve 624 in Figure 6d shows the current through the device in the range of -1.0 milliamps to +1.0 milliamps as the applied voltage is varied between the same voltage range of -10v to +10v, as shown by Figure 6d. This is almost a 3X performance in device conductivity compared to the analog alloy performance 522 in Figure 5d. One can titrate the thickness of the digital alloy 605 and / or the material and / or individual alloy material thicknesses of the alloy compositions to increase the conductivity further, while mitigating the stress due to lattice mismatch between the GaN channel 503 and the digital alloy layer 605.

[0067] In particular configurations, it may be desirable to have the AlN/GaN alloy to create the polarization effect to enhance hole crowding. In other configurations, one can use AlGaIn/GaN alloy to create the polarization effect. The device stack up can be varied to suit the intended applications. Thickness of each layers as well as the digital alloy thickness can be varied to meet particular performance needs. Though this disclosure describes the technology using GaN, the proposed technology applies to any of the III-Nitride semiconductor materials (Al, In, Ga)N or the combinations thereof.

[0068] Modifications, additions, or omissions may be made to the systems, apparatuses, and methods described herein without departing from the scope of the inventive concepts. The components of the systems and apparatuses may be integrated or separated. Moreover, the operations of the systems and apparatuses may be performed by more, fewer, or other components. The methods may include more, fewer, or other steps. Additionally, steps may be performed in any suitable order. As used in this document, "each" refers to each member of a set or each member of a subset of a set.

[0069] To aid the Patent Office, and any readers of any patent issued on this application in interpreting the claims appended hereto, applicants wish to note that they do not intend any of the appended claims or claim elements to invoke paragraph 6 of 35 U.S.C. Section 112 as it exists on the date of filing hereof unless the words "means for" or "step for" are explicitly used in the particular claim.

[0070] All elements, parts and steps described herein are preferably included. It is to be understood that any of these elements, parts and steps may be replaced by other elements, parts and steps or deleted altogether as will be obvious to those skilled in the art.

[0071] Broadly, this writing discloses at least the following: A III-nitride power handling device and the process of making the III-nitride power handling device are disclosed that use digital alloys as back barrier layer to mitigate the strain due to lattice mismatch between the channel layer and the back barrier layer and to provide increased channel conductivity. An embodiment discloses a GaN transistor using a superlattice binary digital alloy as back barrier comprising alternative layers of AlN and GaN. Other embodiments include using superlattice structures with layers of GaN and AlGaIn as well as structures using AlGaIn/AlGaIn stackups that have different Aluminum concentrations. The disclosed device has substantially increased channel conductivity compared to traditional analog alloy back barrier devices.

This writing also presents at least the following Concepts:

1. A power handling device comprising:
 - a III-nitride channel layer,
 - a III-nitride cap layer on the channel layer, where the cap layer has higher level of p-type doping than the channel layer, and
 - a III-nitride digital alloy back barrier below the channel layer; the III-nitride digital alloy back barrier comprising a superlattice structure.
2. The power handling device of Concept 1, further comprising a buffer layer below the digital alloy back barrier layer.
3. The power handling device of Concept 1, wherein the III-nitride channel layer is a Gallium Nitride (GaN) channel layer.
4. The power handling device of Concept 1, wherein the cap layer is a Magnesium (Mg) doped GaN.
5. The power handling device of Concept 1, wherein the digital alloy back barrier is a binary alloy.
6. The power handling device of Concept 1, wherein the superlattice structure comprises alternating Aluminum Nitride (AlN) and GaN layers.
7. The power handling device of Concept 1, wherein the superlattice structure comprises ternary alloys.
8. The power handling device of Concept 1, wherein the superlattice structure comprises alternating GaN and Aluminum-Gallium-Nitride (AlGaN) layers.
9. The power handling device of Concept 1, wherein the superlattice structure comprises alternating AlGaN and AlGaN layers with different Aluminum percentages.
10. The power handling device of Concept 1, wherein the digital alloy is designed to mitigate strain due to lattice mismatch between the channel layer and the digital alloy back

barrier layer.

11. A process of making a power handling device comprising:
depositing a buffer layer on a substrate;
depositing a digital alloy back barrier layer on the buffer layer;
depositing a III-nitride channel on the digital alloy layer;
depositing a III-nitride p-doped cap layer on the channel layer;
etching a gate recess in the cap layer exposing the channel layer;
depositing a gate dielectric inside the gate recess; and
depositing the gate metal inside the gate recess and on the gate dielectric wherein,
the digital alloy layer is made up of superlattice structure.
12. The process of making the power handling device of Concept 11, wherein
the III-nitride channel is GaN and wherein the cap layer is a Magnesium (Mg) doped GaN.
13. The process of making the power handling device of Concept 11, wherein the
digital alloy back barrier is a binary alloy.
14. The process of making the power handling device of Concept 11, wherein the
superlattice structure comprises alternating Aluminum Nitride (AlN) and GaN layers.
15. The process of making the power handling device of Concept 11, wherein the
superlattice structure comprises ternary alloys.
16. The process of making the power handling device of Concept 11, wherein the
superlattice structure comprises alternating GaN and Aluminum-Gallium-Nitride (AlGa_N)
layers.
17. The process of making the power handling device of Concept 11, wherein the
superlattice structure comprises alternating AlGa_N and AlGa_N layers with different Aluminum
percentages.
18. The process of making the power handling device of Concept 11, wherein the
digital alloy is designed to mitigate the strain due to lattice mismatch between the channel layer

and the digital alloy back barrier layer.

19. The process of making the power handling device of Concept 11, wherein the digital alloy layer is between 1 micrometer and 2 micrometer thick.

20. A P-channel III-nitride transistor comprising:
a III-nitride channel layer, and
a III-nitride digital alloy back barrier below the channel layer; the III-nitride digital alloy back barrier comprising a superlattice structure.

What is claimed is:

1. A power handling device comprising:
a III-nitride channel layer,
a III-nitride cap layer on the channel layer, where the cap layer has higher level of p-type doping than the channel layer, and
a III-nitride digital alloy back barrier below the channel layer; the III-nitride digital alloy back barrier comprising a superlattice structure.
2. The power handling device of Claim 1, further comprising a buffer layer below the digital alloy back barrier layer.
3. The power handling device of Claim 1, wherein the III-nitride channel layer is a Gallium Nitride (GaN) channel layer.
4. The power handling device of Claim 1, wherein the cap layer is a Magnesium (Mg) doped GaN.
5. The power handling device of Claim 1, wherein the digital alloy back barrier is a binary alloy.
6. The power handling device of Claim 1, wherein the superlattice structure comprises alternating Aluminum Nitride (AlN) and GaN layers.
7. The power handling device of Claim 1, wherein the superlattice structure comprises ternary alloys.
8. The power handling device of Claim 1, wherein the superlattice structure comprises alternating GaN and Aluminum-Gallium-Nitride (AlGa_N) layers.
9. The power handling device of Claim 1, wherein the superlattice structure comprises alternating AlGa_N and AlGa_N layers with different Aluminum percentages.
10. The power handling device of Claim 1, wherein the digital alloy is designed to mitigate strain due to lattice mismatch between the channel layer and the digital alloy back

barrier layer.

11. A process of making a power handling device comprising:
depositing a buffer layer on a substrate;
depositing a digital alloy back barrier layer on the buffer layer;
depositing a III-nitride channel on the digital alloy layer;
depositing a III-nitride p-doped cap layer on the channel layer;
etching a gate recess in the cap layer exposing the channel layer;
depositing a gate dielectric inside the gate recess; and
depositing the gate metal inside the gate recess and on the gate dielectric wherein,
the digital alloy layer is made up of superlattice structure.
12. The process of making the power handling device of Claim 11, wherein
the III-nitride channel is GaN and wherein the cap layer is a Magnesium (Mg) doped GaN.
13. The process of making the power handling device of Claim 11, wherein the
digital alloy back barrier is a binary alloy.
14. The process of making the power handling device of Claim 11, wherein the
superlattice structure comprises alternating Aluminum Nitride (AlN) and GaN layers.
15. The process of making the power handling device of Claim 11, wherein the
superlattice structure comprises ternary alloys.
16. The process of making the power handling device of Claim 11, wherein the
superlattice structure comprises alternating GaN and Aluminum-Gallium-Nitride (AlGa_N)
layers.
17. The process of making the power handling device of Claim 11, wherein the
superlattice structure comprises alternating AlGa_N and AlGa_N layers with different Aluminum
percentages.
18. The process of making the power handling device of Claim 11, wherein the
digital alloy is designed to mitigate the strain due to lattice mismatch between the channel layer

and the digital alloy back barrier layer.

19. The process of making the power handling device of Claim 11, wherein the digital alloy layer is between 1 micrometer and 2 micrometer thick.

20. A P-channel III-nitride transistor comprising:
a III-nitride channel layer, and
a III-nitride digital alloy back barrier below the channel layer; the III-nitride digital alloy back barrier comprising a superlattice structure.

AMENDED CLAIMS

received by the International Bureau on 11 April 2018 (11.04.2018)

1. A P-channel power handling device comprising:
a III-nitride channel layer,
a III-nitride cap layer on the channel layer, where the cap layer has higher level of p-type doping than the channel layer and supplies holes to the channel layer for the channel conductivity, and
a III-nitride digital alloy back barrier below the channel layer; the III-nitride digital alloy back barrier comprising a superlattice structure.
2. The P-channel power handling device of Claim 1, further comprising a buffer layer below the digital alloy back barrier layer.
3. The P-channel power handling device of Claim 1, wherein the III-nitride channel layer is a Gallium Nitride (GaN) channel layer.
4. The P-channel power handling device of Claim 1, wherein the cap layer is a Magnesium (Mg) doped GaN.
5. The P-channel power handling device of Claim 1, wherein the digital alloy back barrier is a binary alloy.
6. The P-channel power handling device of Claim 1, wherein the superlattice structure comprises alternating Aluminum Nitride (AlN) and GaN layers.
7. The P-channel power handling device of Claim 1, wherein the superlattice structure comprises ternary alloys.
8. The P-channel power handling device of Claim 1, wherein the superlattice structure comprises alternating GaN and Aluminum-Gallium-Nitride (AlGa_N) layers.
9. The P-channel power handling device of Claim 1, wherein the superlattice structure comprises alternating AlGa_N and AlGa_N layers with different Aluminum percentages.
10. The P-channel power handling device of Claim 1, wherein the digital alloy is

designed to mitigate strain due to lattice mismatch between the channel layer and the digital alloy back barrier layer.

11. A process of making a P-channel power handling device comprising:
depositing a buffer layer on a substrate;
depositing a digital alloy back barrier layer on the buffer layer;
depositing a III-nitride channel on the digital alloy layer;
depositing a III-nitride p-doped cap layer on the channel layer, such that said cap layer supplies holes to said channel for the channel conductivity [0053] & [0055];
etching a gate recess in the cap layer exposing the channel layer;
depositing a gate dielectric inside the gate recess; and
depositing ~~at~~ the gate metal inside the gate recess and on the gate dielectric wherein, the digital alloy layer is made up of superlattice structure.
12. The process of making the P-channel power handling device of Claim 11, wherein the III-nitride channel is GaN and wherein the cap layer is a Magnesium (Mg) doped GaN.
13. The process of making the P-channel power handling device of Claim 11, wherein the digital alloy back barrier is a binary alloy.
14. The process of making the P-channel power handling device of Claim 11, wherein the superlattice structure comprises alternating Aluminum Nitride (AlN) and GaN layers.
15. The process of making the P-channel power handling device of Claim 11, wherein the superlattice structure comprises ternary alloys.
16. The process of making the P-channel power handling device of Claim 11, wherein the superlattice structure comprises alternating GaN and Aluminum-Gallium-Nitride (AlGaN) layers.
17. The process of making the P-channel power handling device of Claim 11, wherein the superlattice structure comprises alternating AlGaN and AlGaN layers with different Aluminum percentages.

18. The process of making the P-channel power handling device of Claim 11, wherein the digital alloy is designed to mitigate the strain due to lattice mismatch between the channel layer and the digital alloy back barrier layer.

19. The process of making the P-channel power handling device of Claim 11, wherein the digital alloy layer is between 1 micrometer and 2 micrometer thick.

20. A P-channel III-nitride transistor comprising:
a III-nitride channel layer, and
a III-nitride digital alloy back barrier below the channel layer; the III-nitride digital alloy back barrier comprising a superlattice structure.

104	GaN: Mg
103	GaN channel
102	AlGaN
101	Buffer

Figure 1

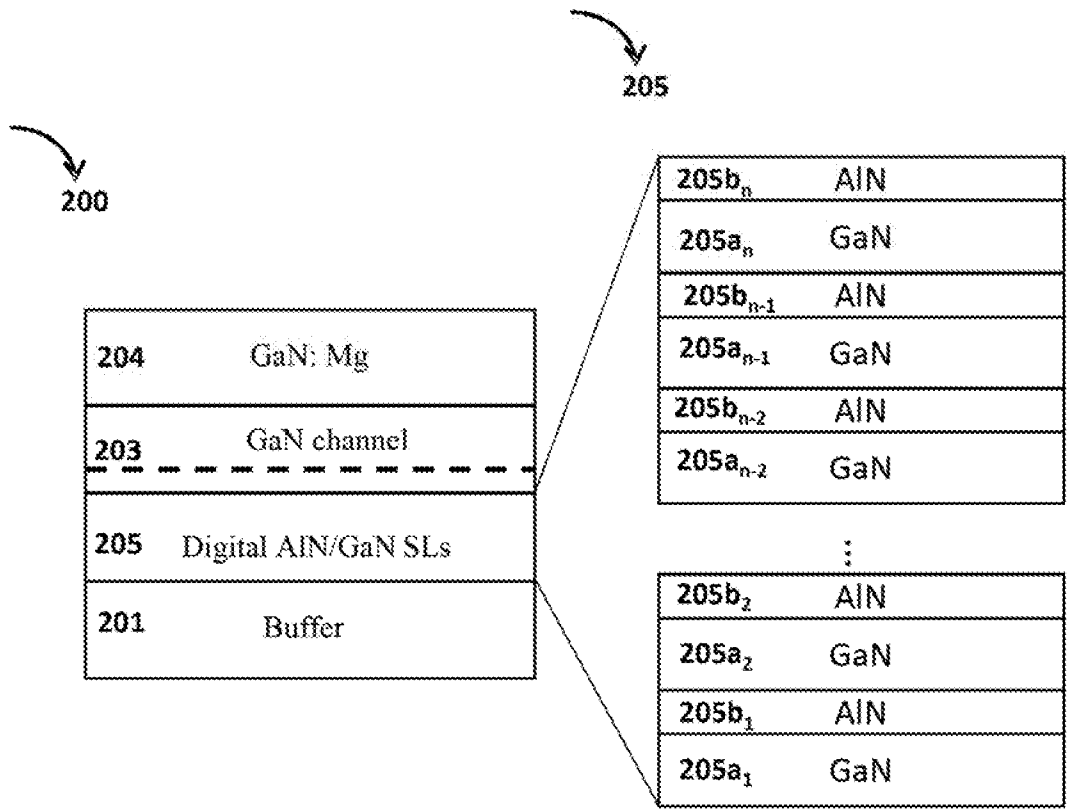


Figure 2

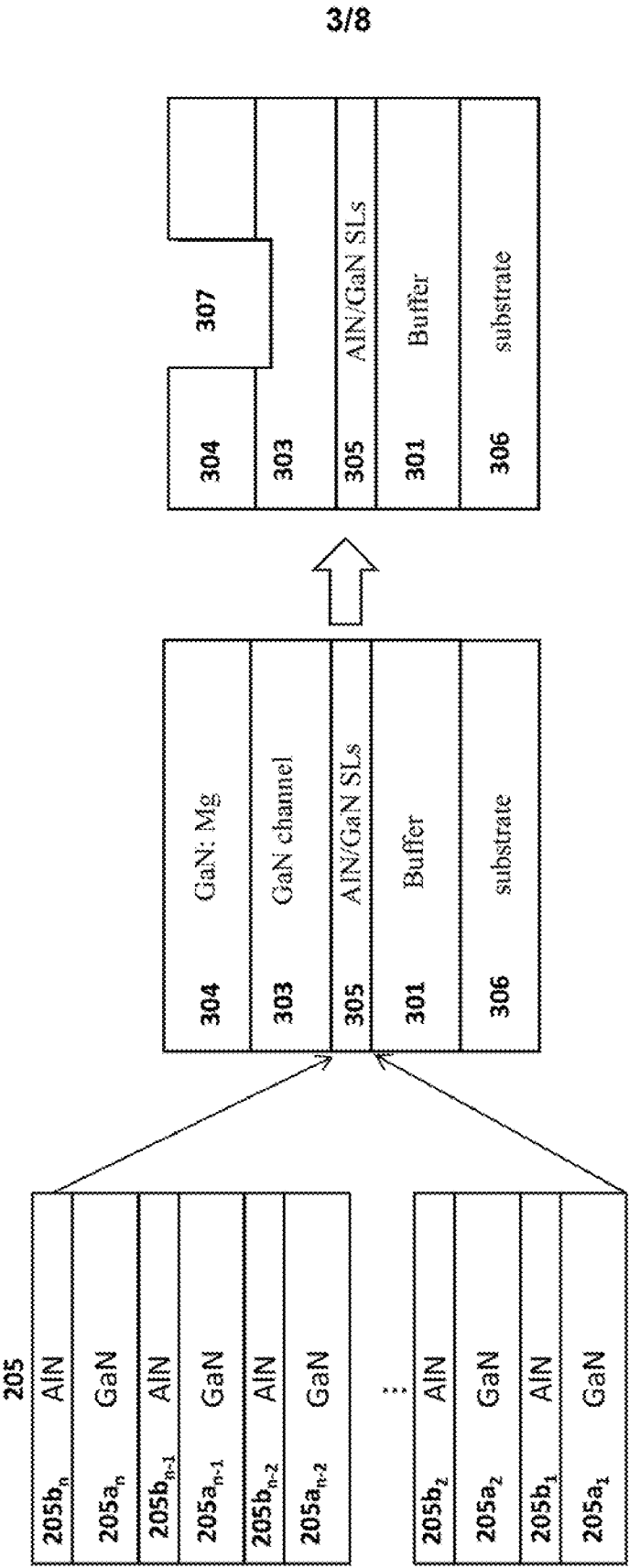


Figure 3c

Figure 3b

Figure 3a

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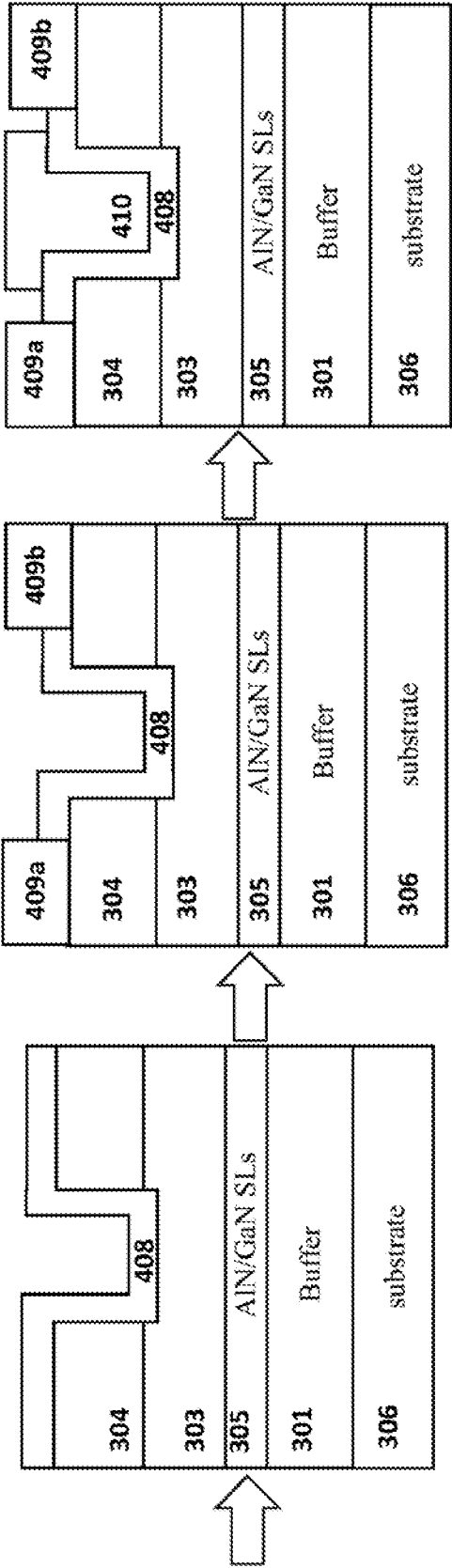


Figure 4c

Figure 4b

Figure 4a

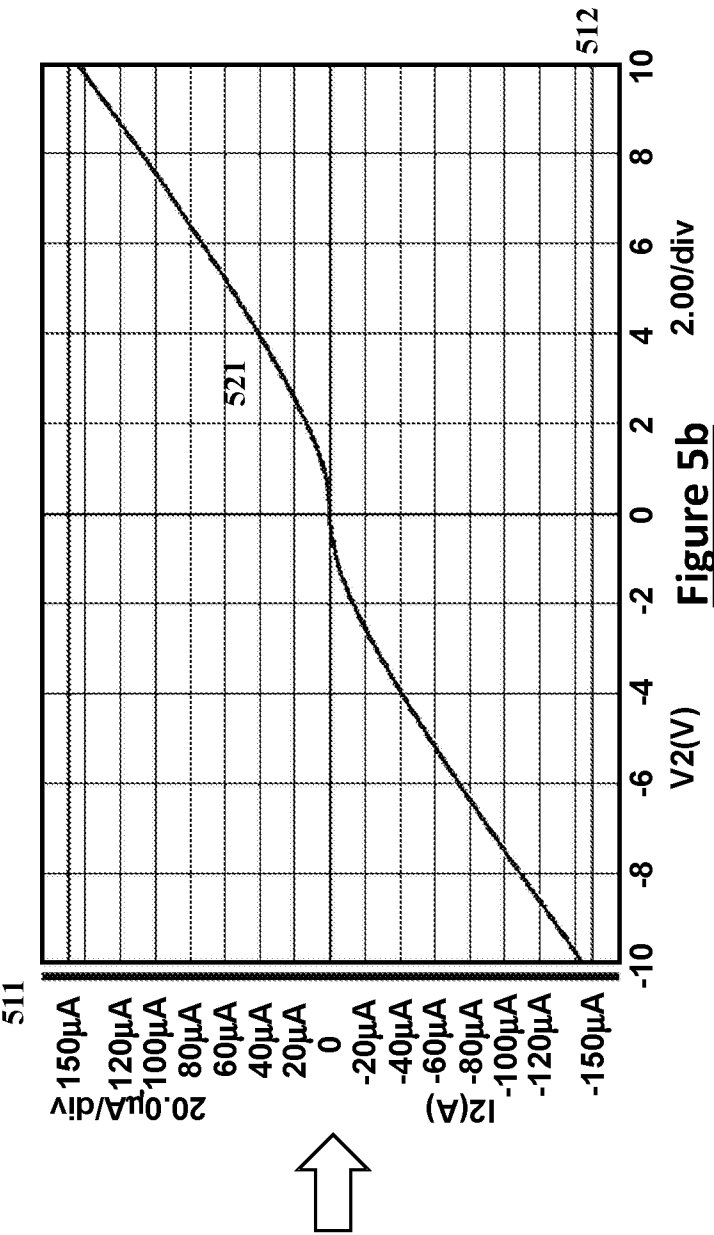


Figure 5b

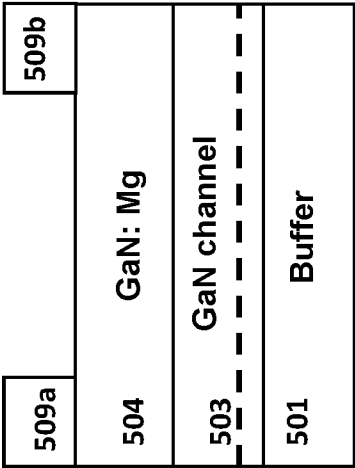


Figure 5a

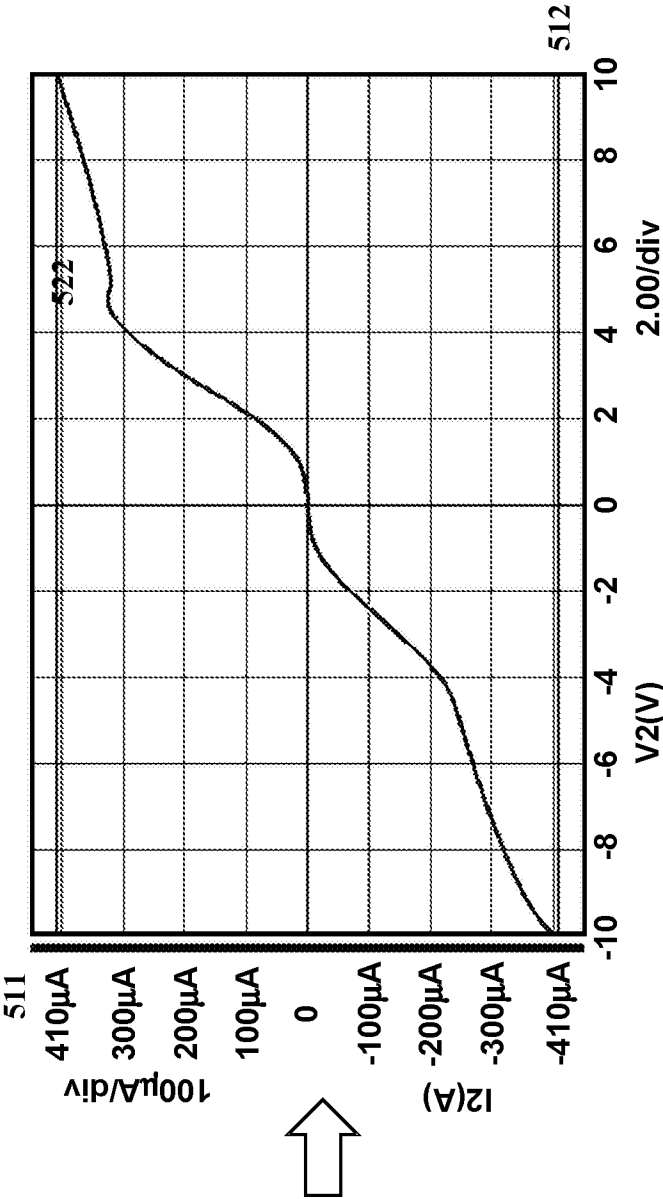


Figure 5d

509a	509b
504	GaN: Mg
503	GaN channel
502	Analog AlGaN
501	Buffer

Figure 5c

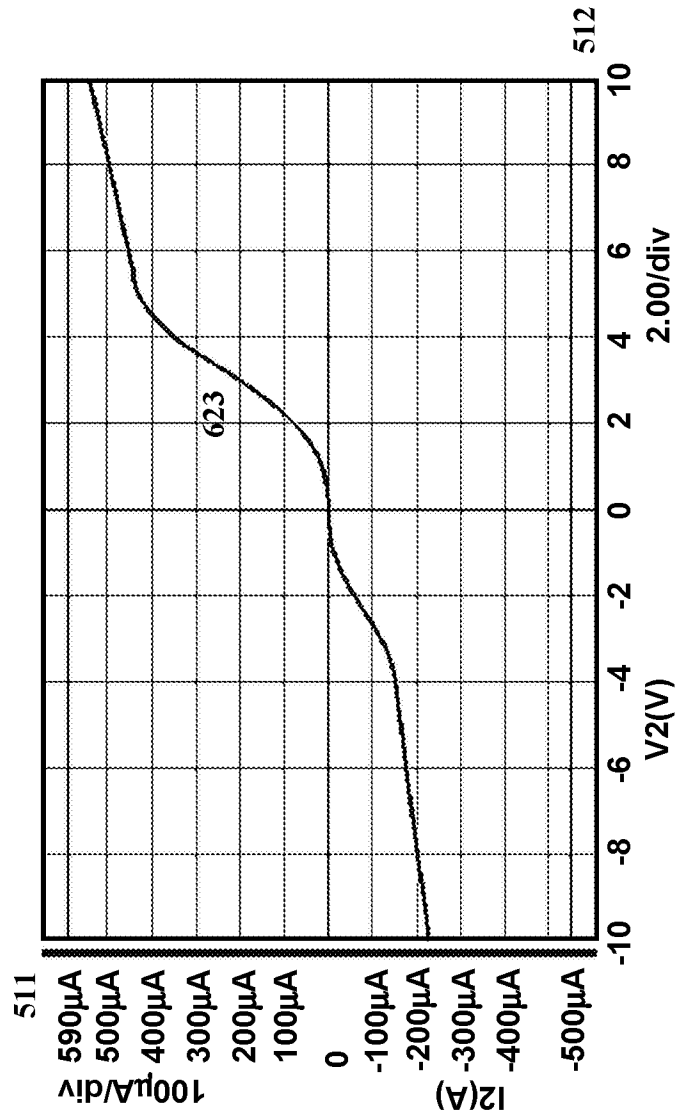


Figure 6b

509a	509b
504	GaN: Mg
503	GaN channel
612	AlN spacer
502	Analog AlGaN
501	Buffer

Figure 6a



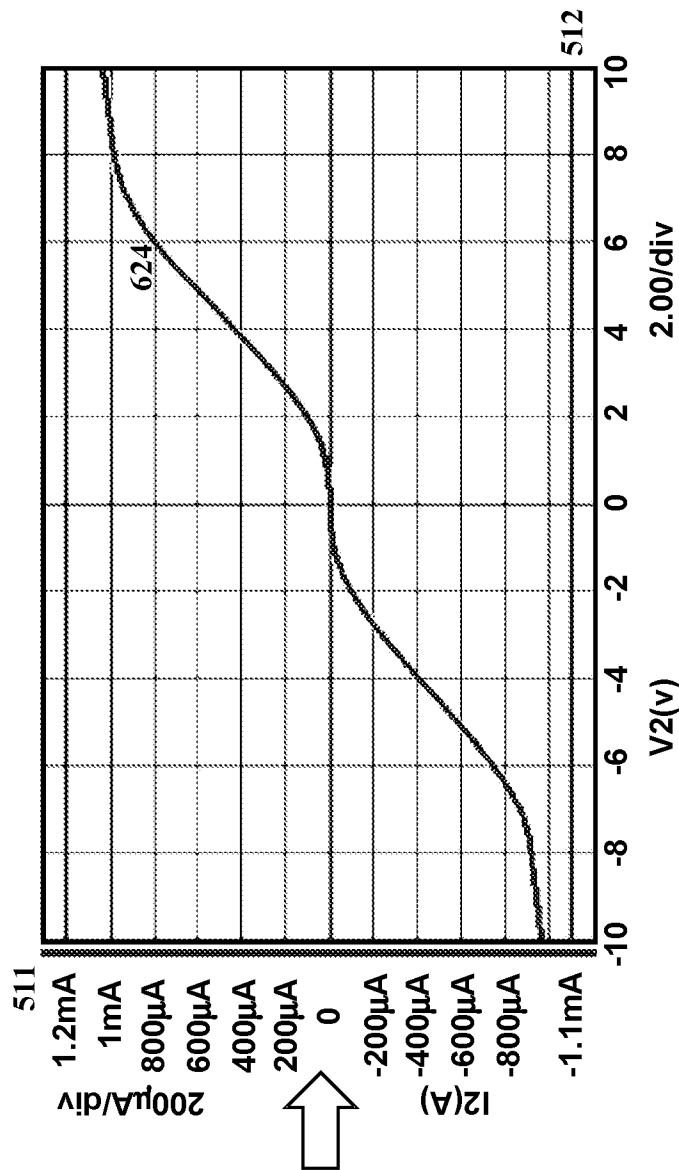


Figure 6d

509a	509b
504	GaN: Mg
503	GaN channel
605	Digital AlGaN
501	Buffer

Figure 6c

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2017/048753**A. CLASSIFICATION OF SUBJECT MATTER****H01L 29/10(2006.01)i, H01L 29/51(2006.01)i, H01L 21/02(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 29/10; H01L 29/778; H01L 29/737; H01L 29/739; H01L 21/338; H01L 29/20; H01L 31/00; H01L 29/51; H01L 21/02

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: transistor, digital-AlN/GaN, super-lattice, III-nitride-channel, polarization-effect, carrier-density

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 9202905 B1 (TRIQUINT SEMICONDUCTOR, INC.) 01 December 2015 See column 2, line 25 - column 8, line 32; claims 1, 8; and figures 1, 6.	20
Y		1-19
Y	US 2007-0164315 A1 (SMITH et al.) 19 July 2007 See paragraphs [0081]-[0108]; claim 1; and figures 1A, 2A-2B, 7.	1-19
A	US 2015-0287785 A1 (TRANSPHORM INC.) 08 October 2015 See figures 3A-3B.	1-20
A	US 2011-0057232 A1 (SHEPPARD et al.) 10 March 2011 See figures 1A-1E.	1-20
A	US 2006-0255364 A1 (SAXLER et al.) 16 November 2006 See figure 1.	1-20



Further documents are listed in the continuation of Box C.



See patent family annex.

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

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Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2017/048753

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