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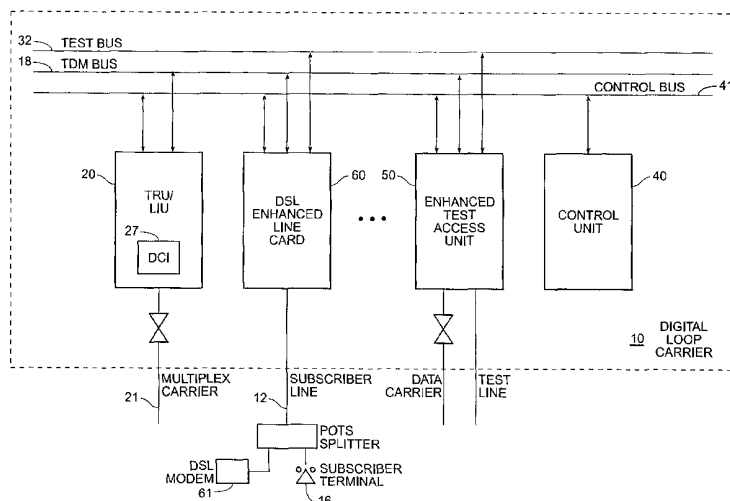
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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: SYSTEM AND METHOD FOR OVERLAYING DSL ACCESS MULTIPLEXER ONTO EXISTING ACCESS SYSTEMS



(57) Abstract: A digital subscriber line access multiplexer (Fig. 3) overlay onto a digital loop carrier system (10) for transporting high speed digital data over an existing backplane (32) which carries voice, data, and test signals between voice line cards (60) and a carrier line (12). The voice signals are time division multiplexed into frames. The system includes a data bus interface (61) for impressing the high speed data on a subset of existing backplane buses (70) for transport along the backplane (32) and for retrieving high speed digital data from the backplane buses (32). The system further includes a plurality of data line cards (60) for connecting to the backplane (32) and backplane subset conductors, the data line cards (60) being adapted to couple the high speed data between the subscriber line (12) and the backplane (32), whereby the high speed digital data can be routed over the backplane subset to any of the digital data line cards (60) without interfering with the voice signals routed to voice line cards.



WO 02/060129 A1

SYSTEM AND METHOD FOR OVERLAYING DSL ACCESS MULTIPLEXER ONTO EXISTING ACCESS SYSTEMS

The present invention relates generally to the field of Digital Subscriber Lines (DSLs), and particularly to a system and method for implementing DSL technology at remote access terminals.

BACKGROUND OF THE INVENTION

In order to relieve the shortage of copper subscriber lines from a telephone central office to a telephone subscriber residence, and also to reduce the length of such lines, access concentrators are frequently employed. Access concentrators employing a digital multiplex carrier to carry many individual voice conversations on a single, or several, multiplex carriers are known as Digital Loop Carriers (DLCs).

FIG. 1 illustrates a block diagram of typical DLC represented generally by the numeral 10. A number of individual twisted pair subscriber lines 12 are terminated by line cards 14. In the case of typical residential telephone service, the lines 12 are terminated by plain-old telephone service (POTS) line cards 14, which provides a number of functions required to operate a telephone or other terminal 16 connected to the line 12 at the subscriber's residence. These functions usually include, but are not limited to:

- Battery -- supplying power to the subscriber terminal;
- Overvoltage -- protecting the line card against environmentally caused overvoltages;
- Ringing -- supplying a ringing signal;
- Supervision -- detecting when a subscriber lifts the telephone receiver;
- Coding -- converting the analog line signal into digital representation;
- Hybrid -- separating the received from the transmitted signals; and
- Termination -- terminating the line with a required standard electrical impedance.

These functions are often collectively referred to as BORSCHT.

Each line card produces a signal in a format suitable for being multiplexed with other line card signals onto a common Time Division Multiplexed (TDM) bus 18 although other buses may be employed. Typically, each line signal is sampled at an 8 kHz

rate and each sample is converted into a digital codeword, each usually consisting of 8 bits using one of several standard coding formats known as μ -law Pulse Coded Modulation (PCM) or A-law PCM. The resulting bit rate per terminated line is, therefore, 64 kb/s.

The codewords from one terminated line 12 or line card 14 are interleaved
5 with those of other lines 12 and line cards 14 onto the TDM bus 18. The codewords are then commonly transmitted over a backplane to a common element, herein called a Transmit and Receive Unit/Line Interface Unit (TRU/LIU) 20 by assigning one or several timeslots to each line card. The TRU/LIU 20 performs two main functions:

1. Electrically driving and receiving signals to/from the TDM bus 18,
10 clock generation, timeslot control, and the like; and
2. Interfacing to a digital multiplex carrier 21, by means of a Digital Carrier Interface (DCI),²² which possibly includes but is not limited to line coding, line quality monitoring, clock recovery, synchronization, loopbacks, framing, alarm detection, multiplexing of signaling bits, maintenance channel termination, and maintenance and remote
15 monitoring functions. Common digital multiplex line interfaces include electrical (T1, E1) and optical (OC-3, OC-12) interfaces.

In order to allow for the electrical testing of subscriber lines 12 and line cards 14, a Test Access Unit (TAU) 30 is typically provided. The TAU 30 is connected to all line cards 14 in the DLC 10 by means of a test bus 32. Test bus implementations and
20 characteristics vary widely depending on the particular embodiment and design of the DLC 10. Typically, in a DLC 10 designed and intended primarily for multiplexing voice services, the test bus 32 characteristics are intended to be electrically suitable for voice signals, but not necessarily for high speed digital signals, such as digital logic or DSL signals.

The TAU 30 is typically controlled by a control unit 40, which may
25 communicate with the TAU 30 and other units in the DLC 10 by means of a control bus 41.

FIG. 2 illustrates the TAU 30 and line card 14 in greater detail. Here a plurality of line cards 14 and the TAU 30 are interconnected for line and circuit testing purposes by the test bus 32.

The test bus 32 typically groups a number of independent conductors together
30 into one or more logical buses. Without loss of generality, the test bus 32 in FIG. 2 has been shown to be logically grouped into four subsets herein labeled, with no intended loss of generality, TestOut2, TestIn2, TestOut4, and TestIn4. This illustrates two relevant concepts:

1. Some line cards communicate with a subscriber terminal using four or more wires and may consequently require 4-wire test buses; and

2. The capability to simultaneously test the subscriber line (known as the test out function) and the Line Interface Circuit (LIC) 11 of the line card 14 (known as the test in function) may be provided by means of distinct subsets of the test bus 32.

FIG. 2 also shows the constituent functional blocks of a 2-wire line card 14. The TDM and Control Interface (TCI) 13 contains circuitry to electrically interface to the TDM bus 18 and the control bus 41, as well as provide general control functions for the line card 14. The LIC 11 provides the BORSCHT functions described above. The test relay 15 provides a means for electrically isolating the LIC 11 from the subscriber line 12, connecting the LIC 11 to the TestIn2 bus, and connecting the subscriber line 12 to the TestOut2 bus.

Operation of 4-wire line cards (not shown) is a logical extension of the above with respect to test relay connectivity with corresponding 4-wire test buses.

FIG. 2 also shows constituent functional blocks of the test access unit 30. A terminations block 34 contains a plurality of electrical terminations required in order to enable meaningful electrical tests of the LIC 11 or the subscriber line 12 to be performed via the test bus 32. A switch matrix 33 provides appropriate means (typically relays or other electrically controllable switches) to electrically connect one or more subsets of the test bus 32 to one or more of a set of line terminations in the terminations block 34 and/or to the external test line 31 (typically twisted pair), either individually, jointly, or severally. A Control Interface 132 contains circuitry to electrically interface with the control bus 41, provide general control functions, and provide specific control functions to actuate the appropriate relays (or other interconnection devices) in the switch matrix 33. The control interface 132 may also function to relay communications to and from the control unit 40 (see FIG. 1) by means of the control bus 41 to and from an external device connected by means of a control interface port 35. An example of such an external device might be a keyboard and display enabling a craftsman to control the testing of lines of line cards by means of keyboard commands.

Both the test relay 15 and the switch matrix 33 are responsive to the control unit 40, which in turn may be responsive to commands from a test controller (not shown).

In many instances, it is desirable to upgrade an existing DLC 10 to enable the provision of new services, specifically for Digital Subscriber Line (DSL) services, and especially asymmetric DSL (ADSL). Besides ADSL, there are a variety of DSL services (e.g., symmetric DSL, high rate DSL, very high rate DSL, etc.) that are generally referred to collectively as xDSL. Since the bit rate per subscriber line for such a service is many times

that for which a voice DLC was engineered and requires the processing of data protocols, such an upgrade becomes problematic.

In order to provide DSL service to a subscriber already served by a voice-only DLC 10 requires changes to hardware. This change may necessitate the physical
5 reconnection of a subscriber's line to a completely different DSL-capable DLC, if one is available at the site. If a DSL-capable DLC is not available, one may need to be installed to serve that subscriber, if space is available in the remote cabinet. If there is insufficient unused space in the cabinet or there is another reason why a new DLC cannot be installed, the subscriber may be denied DSL service altogether.

10 It is an object of the present invention to obviate or mitigate some of the above disadvantages.

BRIEF SUMMARY OF THE INVENTION

In accordance with one embodiment of the present invention, there is provided
15 an overlay system for routing high speed data in a digital loop carrier system. The overlay system impresses and retrieves high speed data on a subset of existing backplane buses without interference among voice, high speed data and test signals.

In accordance with another embodiment of the present invention, there is provided a data bus interface for impressing the high speed data on a subset of existing
20 backplane buses for transport along the backplane and for retrieving high speed digital data from the backplane buses, wherein the existing backplane carries voice, data, and test signals between voice line cards and a carrier line. In one aspect the voice signals are time division multiplexed (TDM) into frames.

In accordance with yet another embodiment of the present invention, there is
25 provided a plurality of data line cards for connecting to the backplane and backplane subset conductors, the data line cards being adapted to couple the high speed data between the subscriber line and the backplane, wherein the high speed digital data can be routed over the backplane subset to any of the digital data line cards without interfering with the voice signals routed to voice line cards.

30 These embodiments are further detailed with reference to the following figures and detailed description.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a typical digital loop carrier according to the prior art.

FIG. 2 is a schematic diagram of a test access unit and line card of FIG. 1.

FIG. 3 is a block diagram of a digital loop carrier with overlaid DSL access multiplexer according to an embodiment of the present invention.

FIG. 4 is a schematic diagram showing another interconnection of an enhanced test access unit and an enhanced line card with a subset of the test bus.

DETAILED DESCRIPTION OF THE INVENTION

For convenience, like structures in the drawings are referred to using like numerals.

FIG. 3 shows the architecture of the DSL access multiplexer (DSLAM) overlay on an existing DLC 10. An enhanced test access unit 50 and DSL enhanced line card 60 provide DSL service to DSL modems 61 while maintaining POTS service to existing voiceband subscriber lines 12 and subscriber terminals 16.

Important components of the operation of the DSLAM overlay, and noteworthy aspects of the present invention, include:

1. The reuse of a subset of the test bus 32, hereinafter called and shown in FIG. 4 as the data bus 70, for the transport of data streams to and from the DSL enhanced line cards 60, in lieu of its previous function of the carriage of test signals; and
2. The combining of functionality of the test access unit 30 with a data aggregation and multiplexing function.

Without intending a loss of generality, FIG. 4 illustrates the use of the test bus 32 subsets TestOut4 and TestIn4 as the data bus 70 for the transport of the data bit streams. The previous functions of the TestOut4 and TestIn4 buses are, in general, no longer available when used as a data bus, and may consequently result in the loss of some line and line card testing capabilities. For example, and with no loss of generality intended, the use of the TestOut4 and TestIn4 buses might result in the loss of testing capability for 4-wire interfaces, but not of testing capability for 2-wire interfaces. The provision of adequate data bit rates for the aggregation and multiplexing of data streams from a plurality of DSL enhanced line cards 60 requires the data bus to carry signals of a significantly higher bandwidth than the voiceband test signals previously carried. There exist a wide variety of DLC system implementations for which the above described overlayment is possible, including (but not

limited to) SLC Series 5 Carrier System (a trademark of Lucent Technologies Inc.), SLC-2000 Access System (a trademark of Lucent Technologies Inc.), and SLC Series 96 Carrier System (a trademark of Lucent Technologies Inc.). Details of implementation, such as the number of test buses conductors, their arrangement, the assignment of these conductors to various testing and test access functions, and their electrical characteristics may differ from system type to system type.

FIG. 4 illustrates the enhanced test access unit 50, the enhanced line card 60, and their interconnection by means of a subset of the test bus 32 in greater detail. The enhanced test access unit 50 expands the functionality of the previously-described TAU 30 by adding the following functions: a Master Data Bus Interface (MDBI) 36; a Cell Aggregation Multiplexer (CAM) 37; a Digital Carrier Interface (DCI) 38; and a control processor 39. Details of the CAM 37, DCI 38, and control processor 39 are well known in the art and need not be discussed here in detail. The MDBI 36 is the master element in the transmission, reception, and protocol implementation for the data bus 70. The MDBI 36 contains all the functions required to communicate over the data bus 70 with the data bus interface (DBI) 61 in the DSL enhanced line card 60. It provides clocking, framing, cell address translation, data recovery, cell queuing, and other functions required for the appropriate operation of the data bus 70. The MDBI 36 and DBI 61 together embody and implement the data bus access protocols and design considerations previously described. The MDBI 36 also provides a suitable interface to effect data or cell transfer to the CAM 37.

The CAM 37 receives and transmits data to and from the MDBI 36. This data may exist in the format of Asynchronous Transfer Mode (ATM) cells, Ethernet packets, or other data packets or formats which are contained in the combined data streams from a plurality of DSL enhanced line cards 60. Without limiting the generality of the discussion, the descriptions that follow will refer to ATM cell handling only. The CAM 37 buffers cells in queues, alters cell headers, controls the sequence of the outflow of cells as required to provide ATM multiplexing, cell flow control, quality of service management, policing, shaping, etc. suitable for ATM access multiplexer functionality as is well known in the art. The CAM 37 then forwards the cells/packets on to a data network through the DCI 38.

The DSL enhanced line card 60 expands the functionality of the previously described line card 14 by adding the following functions: a Data Bus Interface (DBI) 61, a DSL Termination Unit-Central (DTU-C) 62, and a broadband line interface 63. Certain types of DSL signals, such as Asymmetric DSL (ADSL) conforming to ITU-G.922 standards, may coexist on a single line with POTS analog signals. It is, therefore, desirable to provide a line

card capable of simultaneously communicating DSL and POTS signals between the subscriber line 12 and the DLC 10 backplane buses.

The DBI 61 consists of all functions required to communicate over the data bus 70 with the MDBI 36 of the enhanced test access unit 50. These may include, but are not limited to, data bus protocol implementation, clock recovery and synchronization circuitry, electrical drivers, receivers, and timing circuits. The DBI 61 implements the necessary circuitry to conform to the data bus protocol requirements of fair access of multiple line cards to a single shared bus, ATM cell queuing and buffering with multiple qualities of service, and other functions. The DBI 61 is used for impressing a digital signal at a high rate onto the existing conductors of the backplane data bus 70, and for providing elastic stores to match the burst transmission characteristics of the data bus 70 to the continuous bit stream transmitted and received from the DTU-C 62.

The DTU-C 62 (also referred to as a data pump) consists of all circuitry normally required to convert a bit stream to/from signals which can be transmitted on a twisted pair subscriber line according to standard or proprietary protocols and modulation algorithms including (but not limited to) CAP, G.lite, and ANSI T1.413. Such devices are well known in the art and do not need to be described in detail.

The broadband line interface 63 performs all the functions of the line interface circuit 11 for both POTS signals as well as for the DSL signals transmitted and received by the DTU-C 62. The broadband line interface 63 may include a separate POTS line interface, DSL line interface, and POTS splitter, or may be implemented as unified circuitry not requiring a POTS splitter. Such devices are well known in the art and do not need to be described in detail.

Although the invention has been described with reference to certain specific embodiments, various modifications and equivalents thereof will be apparent to those skilled in the art without departing from the spirit and scope of the invention as outlined in the claims appended hereto.

WHAT IS CLAIMED IS:

1 1. A test access unit for coupling high speed data in a digital loop carrier
2 system having a plurality of voice line cards, a plurality of digital line cards, and a backplane
3 including a time division multiplexed bus for routing voice data and a test bus, said test
4 access unit comprising:

5 a data bus interface circuit coupled to route said high speed data to and from
6 said plurality of digital line cards over a subset of said test bus, whereby said high speed data
7 is routed over said backplane to or from said plurality of digital line cards without interfering
8 with said voice data routed over said backplane;

9 an aggregation multiplexer circuit coupled to aggregate and multiplex said
10 high speed data from, and to demultiplex and deaggregate said high speed data to, said
11 plurality of digital line cards via said data bus interface circuit; and

12 a digital carrier interface circuit coupled to interface said high speed data
13 between said aggregation multiplexer circuit and a high speed digital network.

1 2. The test access unit of claim 1, wherein said subset of said test bus
2 comprises a 4-wire test bus.

1 3. The test access unit of claim 1, further comprising:
2 a plurality of electrical terminations coupled to test at least one of said digital
3 loop carrier system and a component associated therewith.

1 4. The test access unit of claim 3, wherein said plurality of electrical
2 terminations are coupled via another subset of said test bus to test at least one of said digital
3 loop carrier system and said component associated therewith.

1 5. The test access unit of claim 4, wherein said another subset of said test
2 bus comprises a 2-wire test bus.

1 6. A data line card for coupling high speed data in a digital loop carrier
2 system having a backplane including a time division multiplexed bus for routing voice data
3 and a test bus, said data line card comprising:

4 a data bus interface circuit coupled to route said high speed data over a subset
5 of said test bus, whereby said high speed data is routed over said backplane without
6 interfering with said voice data routed over said backplane;

7 a digital subscriber line termination unit coupled to convert between said high
8 speed data and twisted pair data; and

9 a broadband line interface circuit coupled to convert between said twisted pair
10 data and information received from a subscriber line.

1 7. The data line card of claim 6, wherein said subset of said test bus
2 comprises a 4-wire test bus.

1 8. The data line card of claim 6, further comprising:
2 a test relay configured to isolate said broadband line interface circuit from said
3 subscriber line and to couple said broadband line interface circuit and said subscriber line to
4 another subset of said test bus.

1 9. The data line card of claim 8, wherein said another subset of said test
2 bus comprises a 2-wire test bus.

1 10. The data line card of claim 6, further comprising:
2 a voice interface circuit coupled to interface said voice data between said time
3 division multiplexed bus and said broadband line interface circuit.

1 11. An overlay system for routing high speed data in a digital loop carrier
2 system, said digital loop carrier system having a backplane including a time division
3 multiplexed bus for routing voice data and a test bus, said overlay system comprising:
4 a plurality of data line cards, each coupled to a subscriber line, and each
5 coupled to route said high speed data between said subscriber line and a subset of said test
6 bus, whereby said high speed data is routed over said backplane without interfering with said
7 voice data routed over said backplane; and
8 a test access unit coupled to route said high speed data to and from said
9 plurality of digital line cards over said subset of said test bus, and to interface said high speed
10 data with a high speed digital network.

1 12. The overlay system of claim 11, wherein each of said plurality of data
2 line cards comprises:
3 a data bus interface circuit coupled to route said high speed data over said
4 subset of said test bus;

5 a digital subscriber line termination unit coupled to convert between said high
6 speed data and twisted pair data; and

7 a broadband line interface circuit coupled to convert between said twisted pair
8 data and information received from said subscriber line.

1 13. The overlay system of claim 11, wherein each of said plurality of data
2 line cards further comprises:

3 a test relay configured to isolate said broadband line interface circuit from said
4 subscriber line and to couple said broadband line interface circuit and said subscriber line to
5 another subset of said test bus.

1 14. The overlay system of claim 13, wherein said another subset of said
2 test bus comprises a 2-wire test bus.

1 15. The overlay system of claim 11, wherein said subset of said test bus
2 comprises a 4-wire test bus.

1 16. The overlay system of claim 11, further comprising:
2 a voice interface circuit coupled to interface said voice data between said time
3 division multiplexed bus and said broadband line interface circuit.

1 17. The overlay system of claim 11, wherein said test access unit
2 comprises:
3 a data bus interface circuit coupled to route said high speed data to and from
4 said plurality of digital line cards over said subset of said test bus;
5 an aggregation multiplexer circuit coupled to aggregate and multiplex said
6 high speed data from, and to demultiplex and deaggregate said high speed data to, said
7 plurality of digital line cards via said data bus interface circuit; and
8 a digital carrier interface circuit coupled to interface said high speed data
9 between said aggregation multiplexer circuit and said high speed digital network.

1 18. The overlay system of claim 17, wherein said test access unit further
2 comprises:

3 a plurality of electrical terminations coupled to test at least one of said digital
4 loop carrier system and a component associated therewith.

1 19. The overlay system of claim 18, wherein said plurality of electrical
2 terminations are coupled via another subset of said test bus to test at least one of said digital
3 loop carrier system and said component associated therewith.

1 20. A method of routing high speed data in a digital loop carrier system,
2 said digital loop carrier system having a backplane including a time division multiplexed bus
3 for routing voice data and a test bus, said method comprising the acts of:
4 receiving said voice data and said high speed digital data from a subscriber
5 line;
6 routing said voice data over said time division multiplexed bus and said high
7 speed digital data over a subset of said test bus, whereby said high speed data is routed over
8 said backplane without interfering with said voice data routed over said backplane;
9 interfacing said high speed data with a high speed digital network; and
10 sending said voice data and said high speed digital data to said subscriber line.

1 21. The method of claim 20, further comprising:
2 testing at least one of said digital loop carrier system and a component
3 associated therewith via another subset of said test bus.

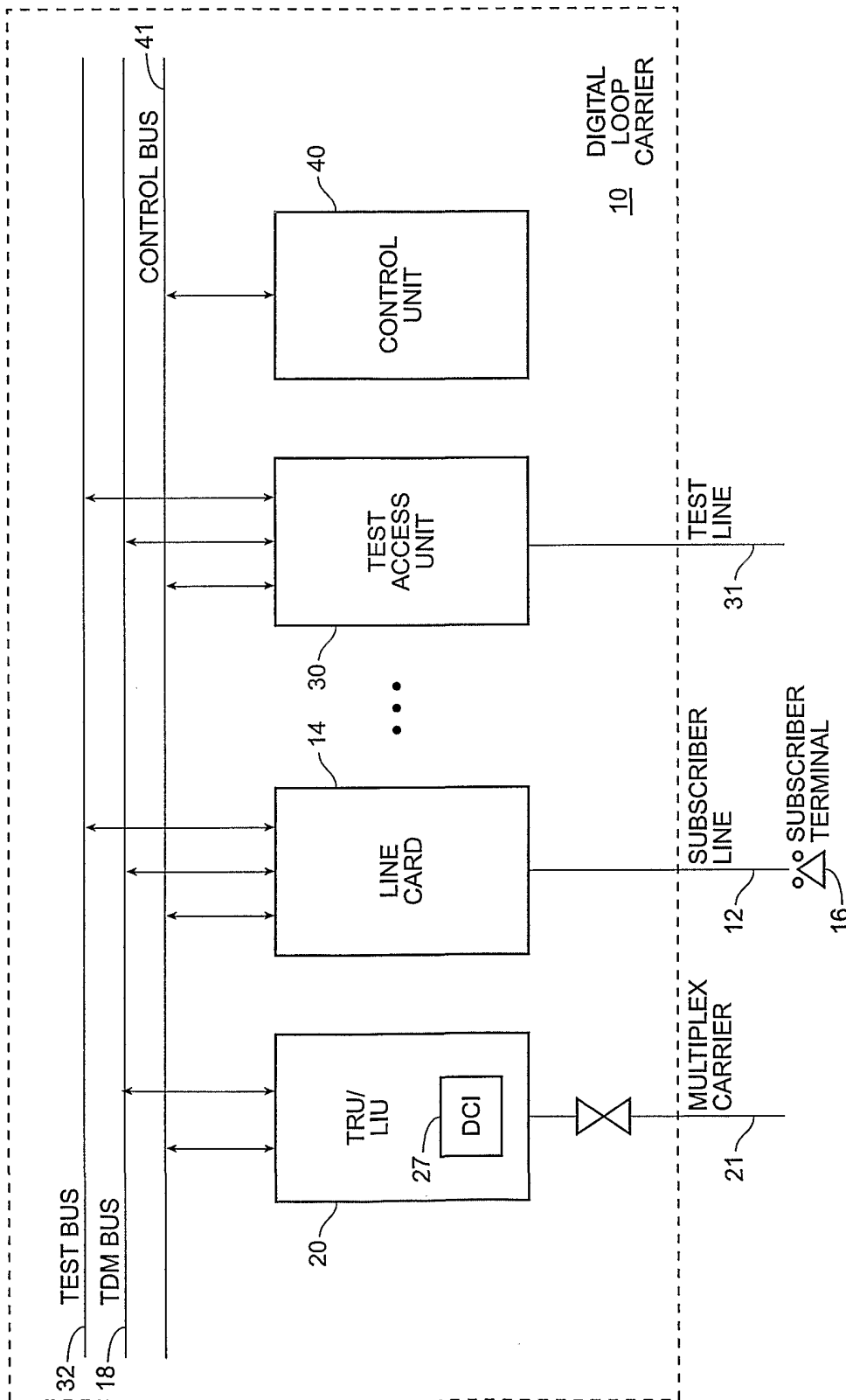


FIG. 1
(PRIOR ART)

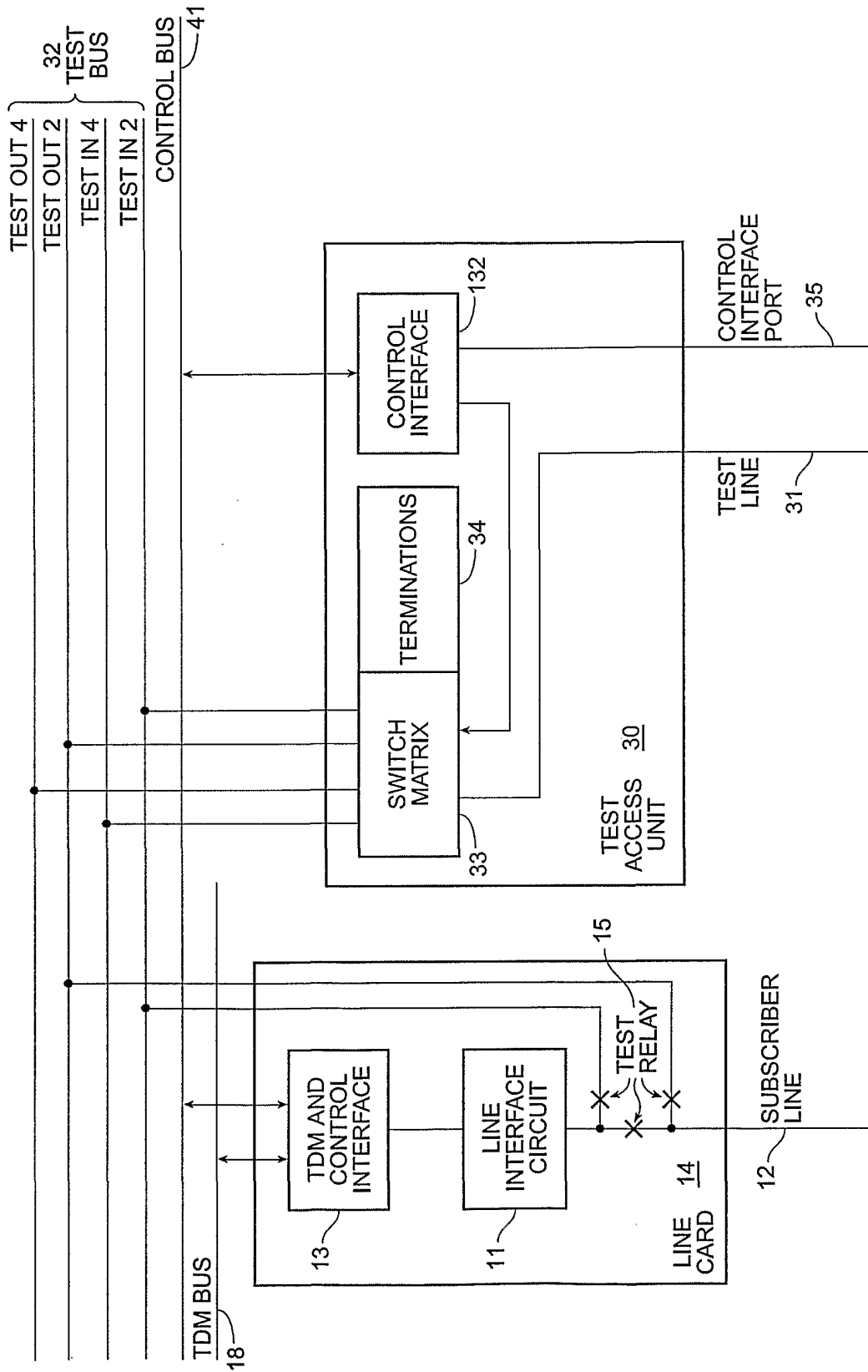


FIG. 2
(PRIOR ART)

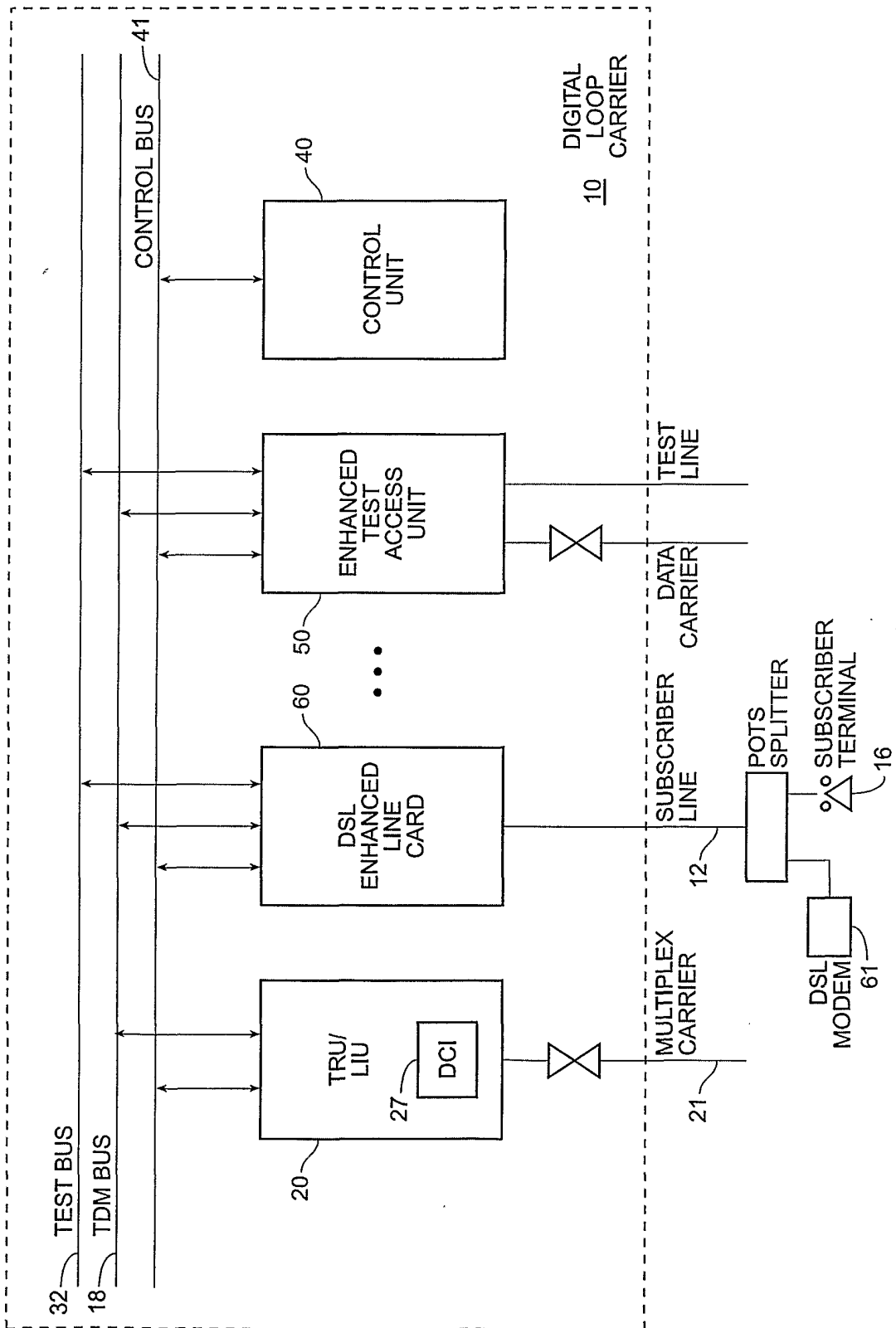


FIG. 3

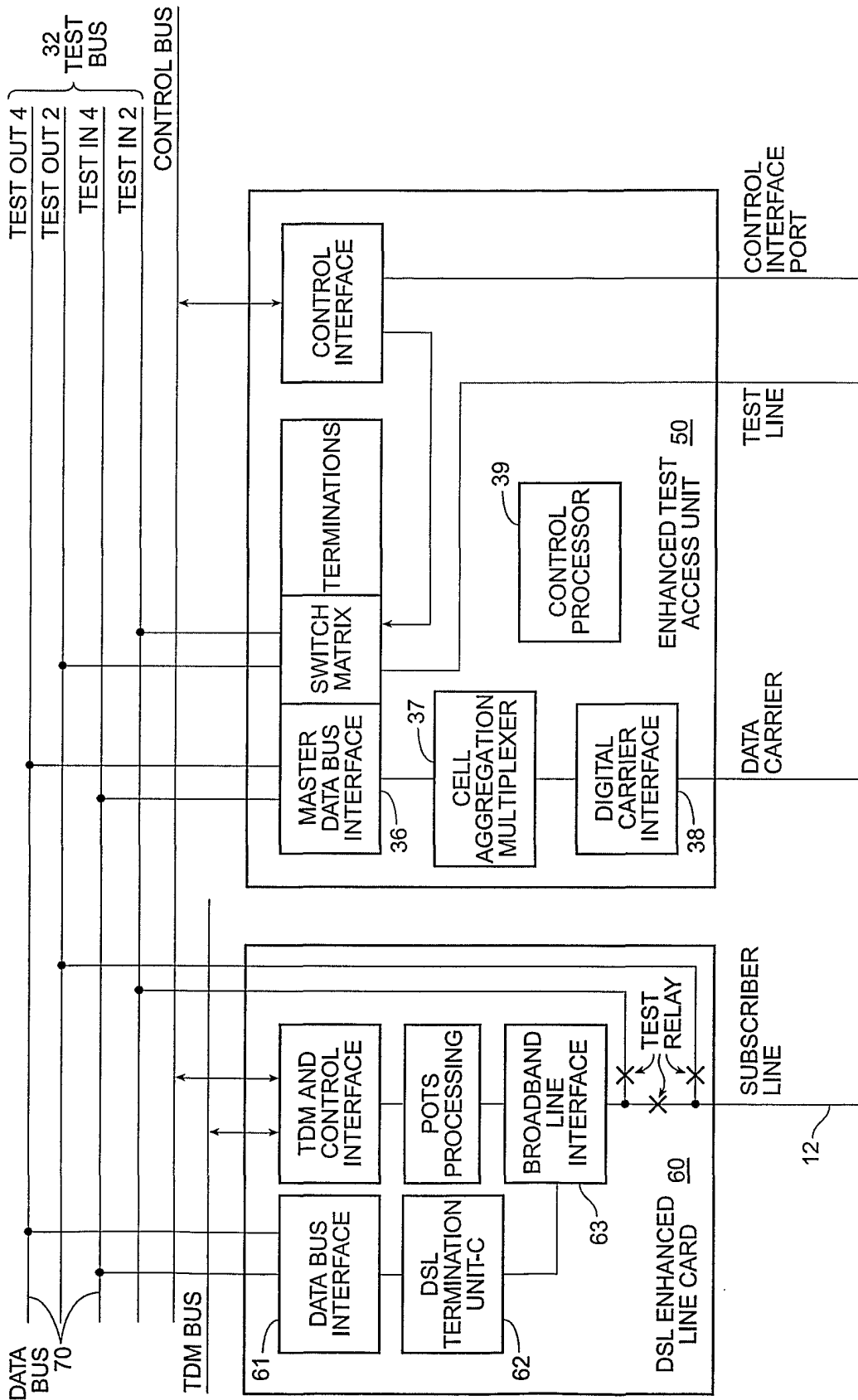


FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US01/17848

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) :H04L 12/28; H04J 3/16

US CL : 370/241, 401, 420, 489

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 370/241, 252, 401, 420, 480, 485, 489, 490

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6,081,517 A (LIU et al) 27 June 2000, abstract.	1-21
A,P	US 6,236,664 B1 (ERREYGERS) 22 May 2001, abstract.	1-21
A	US 6,130,879 A (LIU) 10 October 2000, abstract.	1-21

 Further documents are listed in the continuation of Box C.
 See patent family annex.

* Special categories of cited documents:		"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
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Date of the actual completion of the international search

13 AUGUST 2001

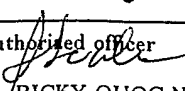
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