United States Patent [19]

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[11] **3,736,868**

[45] **June 5, 1973**

[54] **APPARATUS FOR PRINTING SERIALLY RECEIVED DATA**

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[22] Filed: **Mar. 1, 1972**

[21] Appl. No.: **231,049**

Related U.S. Application Data

[63] Continuation of Ser. No. 25,535, April 3, 1970.

[52] **U.S. Cl.** ..... **101/93 C,** 340/172.5

[51] **Int. Cl.** **B41j 1/34,** G06f 7/00, G06f 15/00

[58] **Field of Search** ..... 101/93 C; 340/172.5; 197/1, 133

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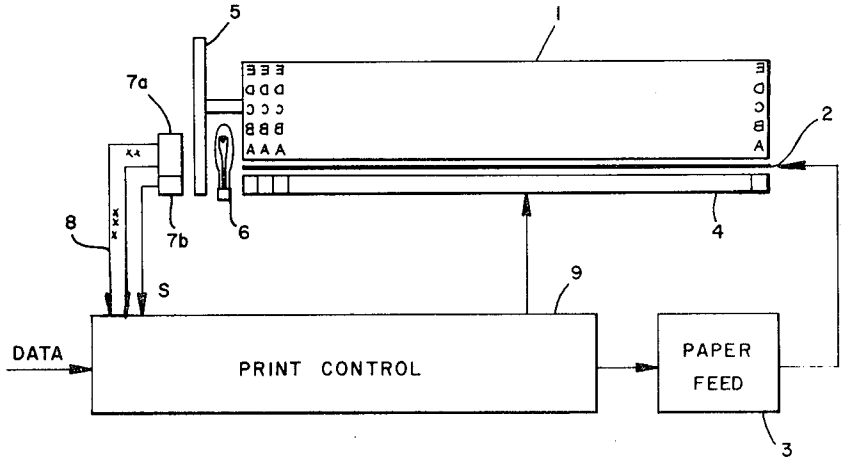
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[57] **ABSTRACT**

A printer and method for printing continually received serially arranged data in which those characters to be printed in a group of columns at the beginning of each line are individually stored in single-character storage registers during operations performed to initiate the line as line feed and carriage return. A separate control circuit is associated with each of these beginning columns and causes the stored character to be printed by an individual print hammer dedicated to the column. The hammers for printing in the remaining columns of the line share control circuits and storage registers. The printer has a moving type carrier and the number of control circuits and storage registers for the remaining columns is substantially equal to the ratio of the time the carrier requires to present a complete font of type characters to the document to the time interval at which successive characters are received from the data source. This allows printing of all those characters to be printed in the remaining columns with a minimum number of storage registers and control circuits.

3 Claims, 8 Drawing Figures



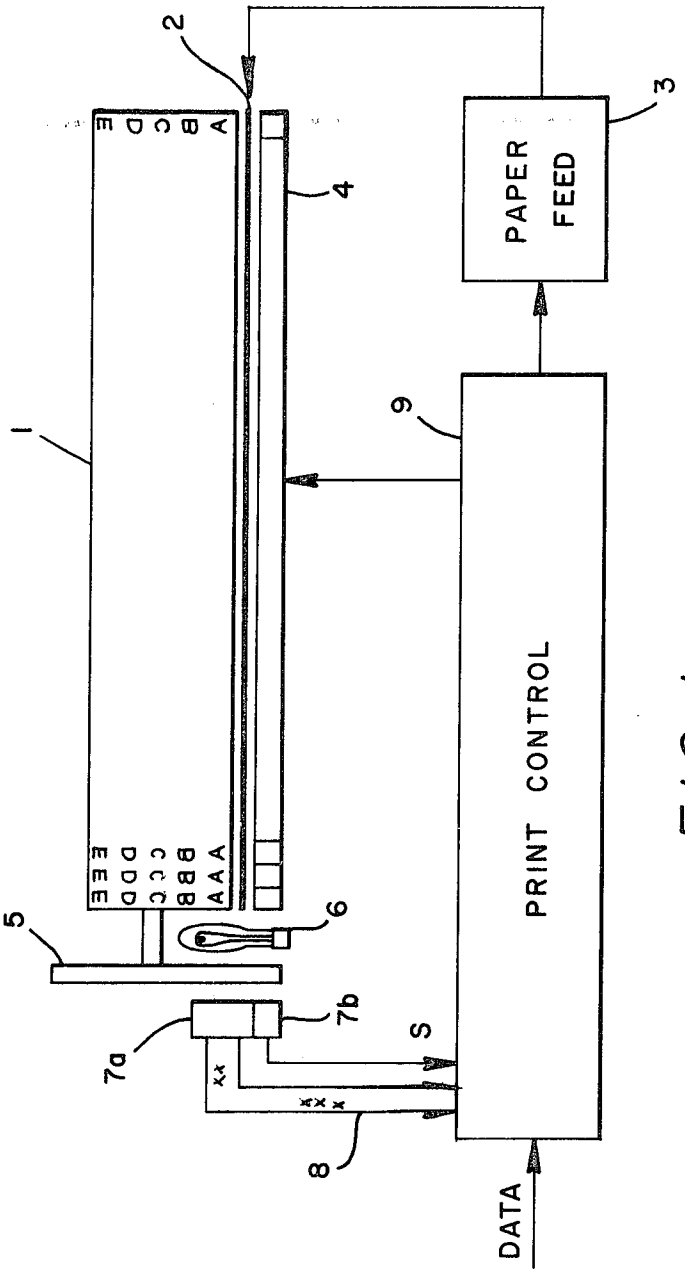


FIG. 1

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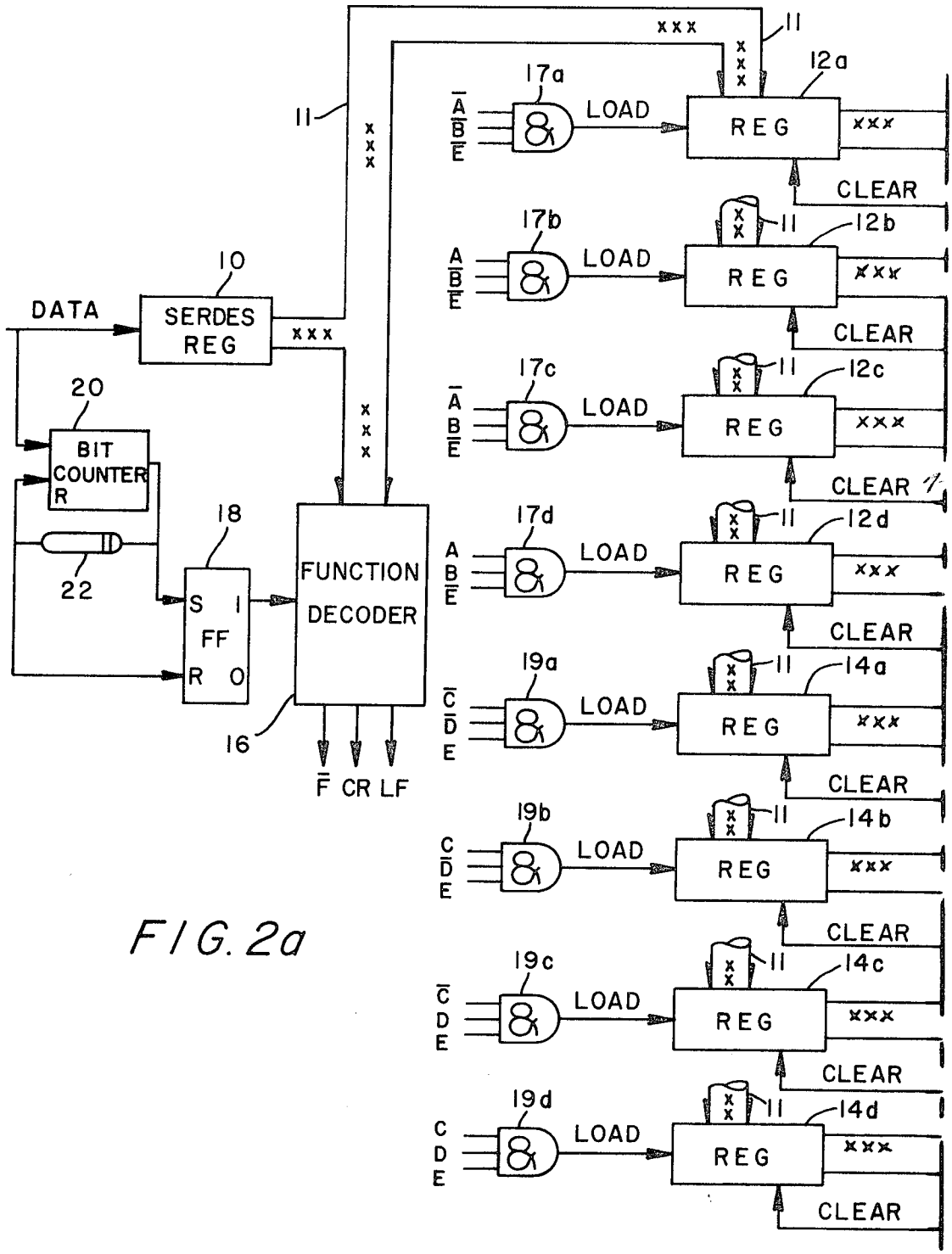


FIG. 2a

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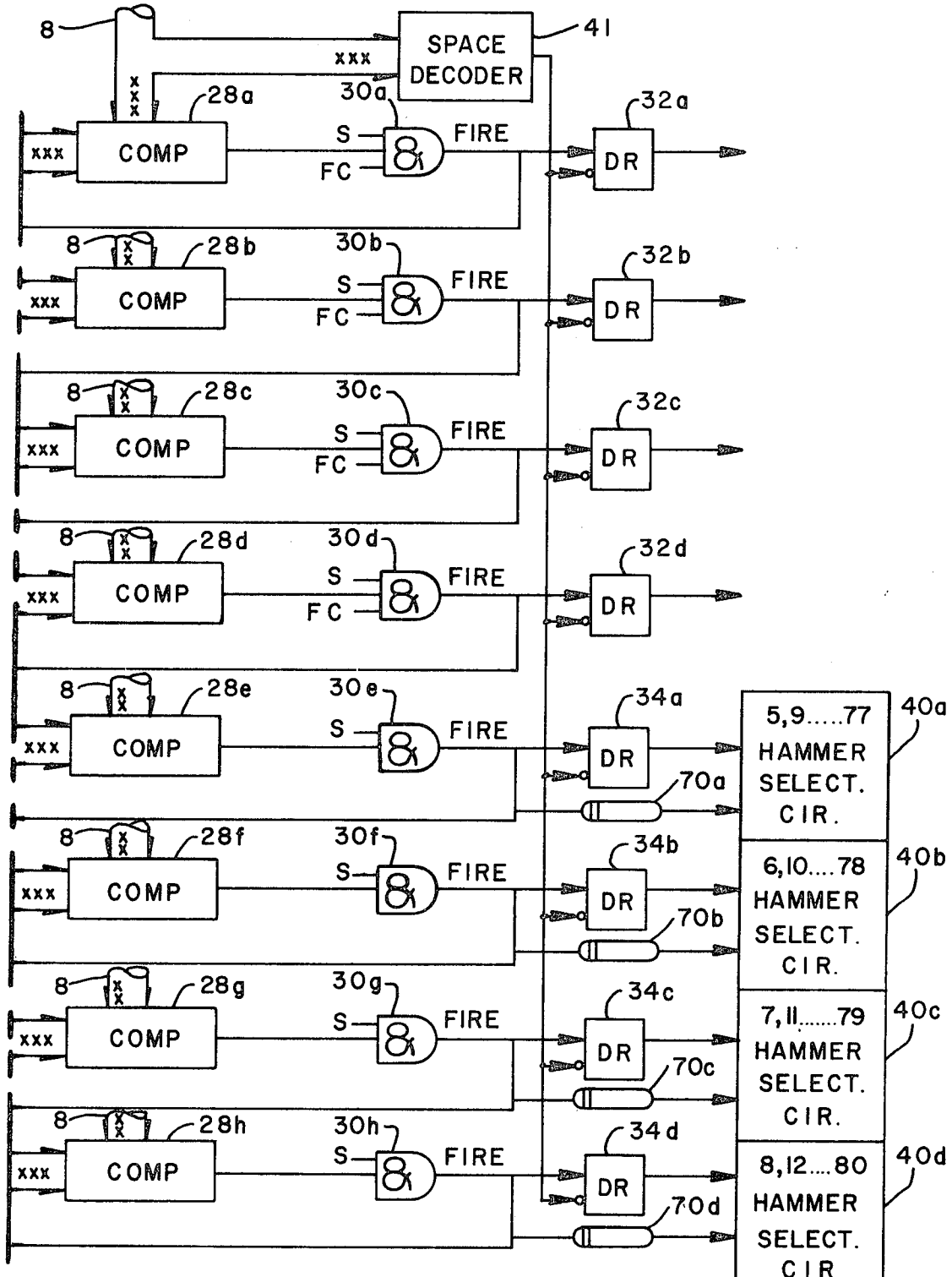


FIG. 2b

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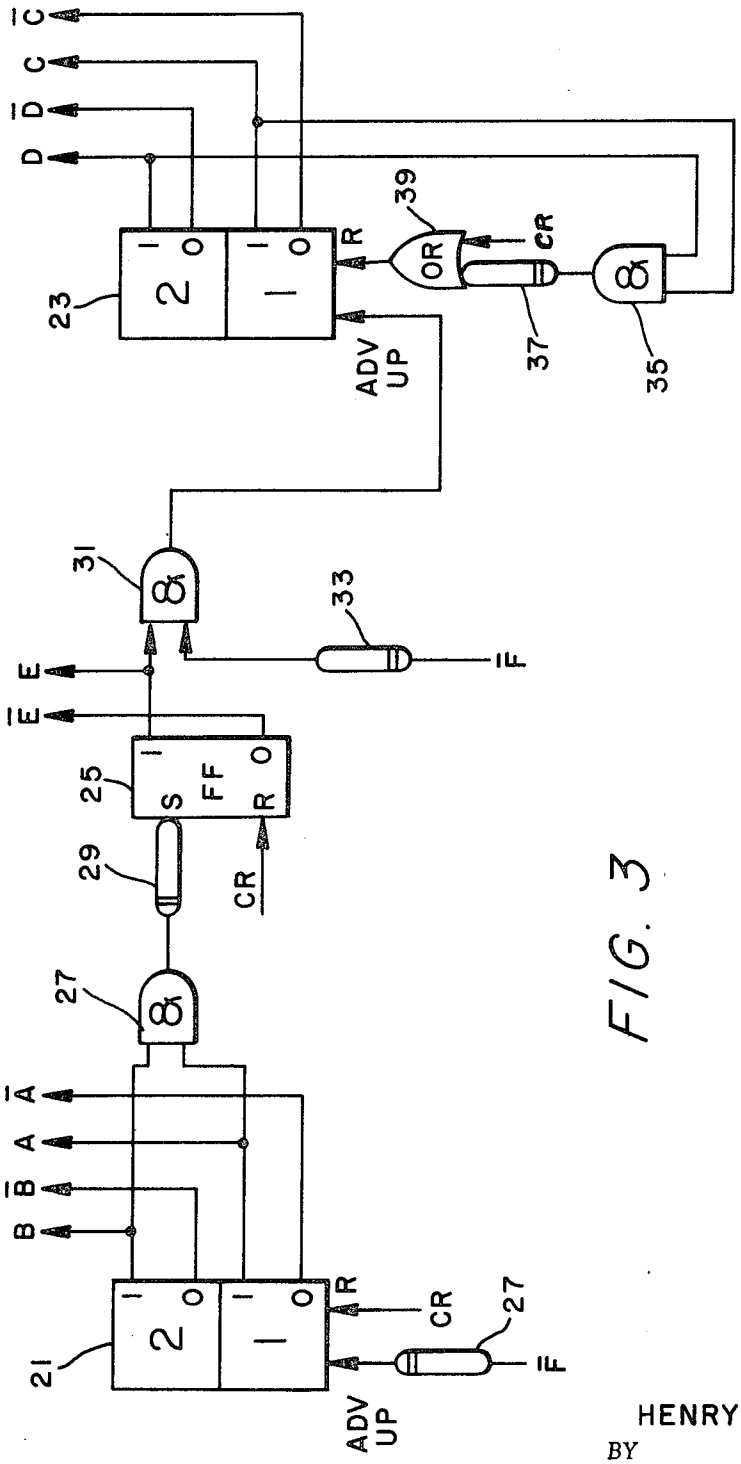


FIG. 3

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FIG. 4

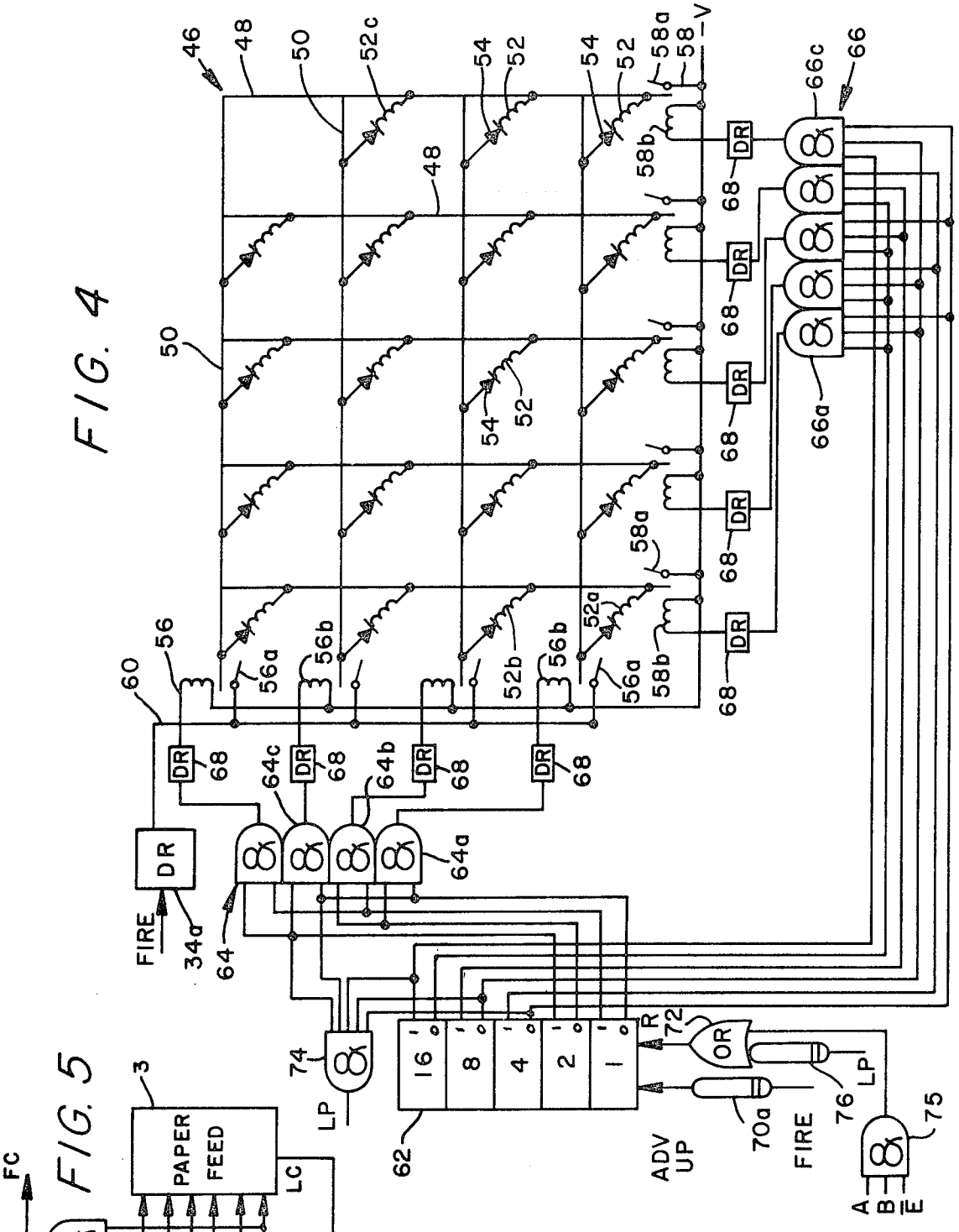
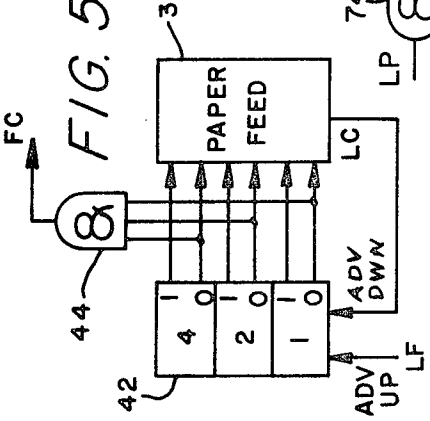


FIG. 5



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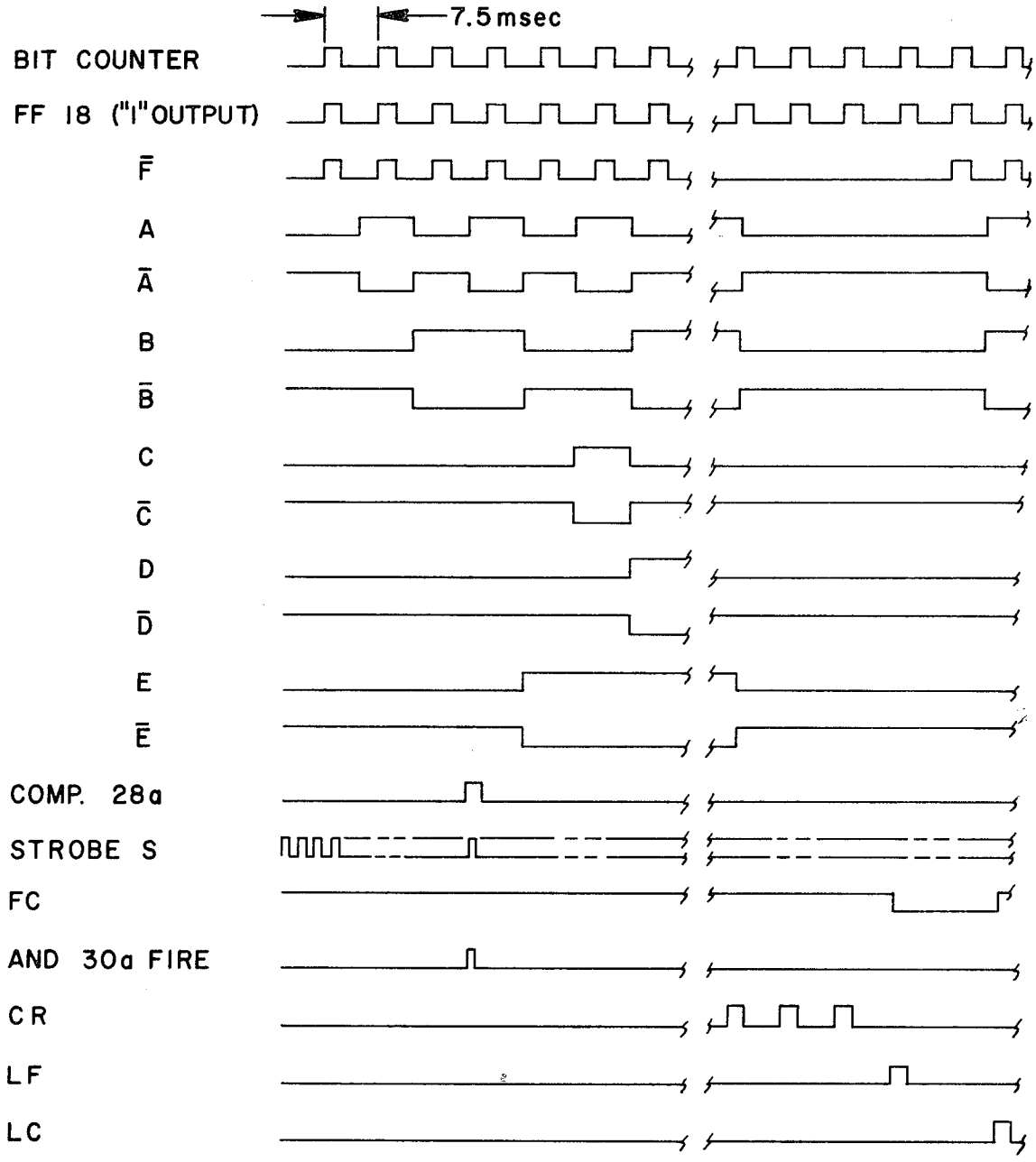


FIG. 6

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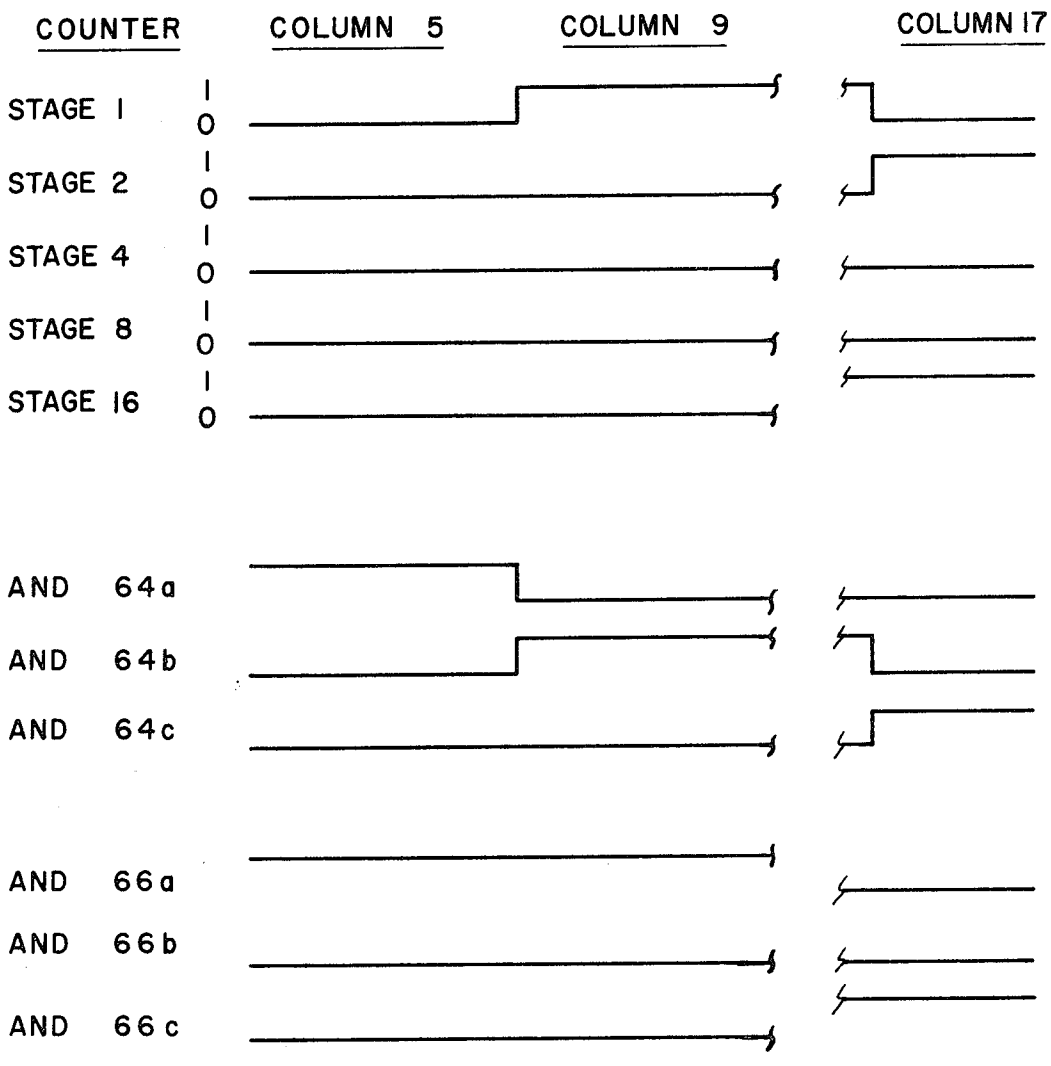


FIG. 7

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APPARATUS FOR PRINTING SERIALLY RECEIVED DATA

This is a continuation of application Ser. No. 25,535, filed Apr. 3, 1970.

BACKGROUND OF THE INVENTION

This invention relates to printing and, more particularly to printing in successive lines serially arranged input information.

Numerous printers have been developed for printing, line-by-line, information in the form of coded electrical signals serially fed to the printer from data processing apparatus. Such printers, generally termed "teleprinters," are extensively used to print information transmitted over communication lines. Their printing mechanism is usually mounted on a carriage which is moved from left to right across the document being printed upon as the data is received. However, the carriage must return to the left side of the document to begin a new line. Since printing cannot occur during this operation, the input data received at this time must be stored somehow or be lost. Storage or "buffer" registers are conventionally provided for this purpose.

Other teleprinters do not utilize a moving carriage but instead provide a stationary printing mechanism for each column in the line being printed. These printers thereby avoid the time and problem caused by "carriage return." However, when beginning a new line, the document being printed upon must be moved to present a blank space to the printing mechanisms. This "line feed" operation, like carriage return requires a period of time. Thus, characters fed to the printer at this time must also be stored or they too are lost.

OBJECTS AND SUMMARY OF THE INVENTION

It is the primary object of this invention to provide a method of printing and a teleprinter requiring minimal storage circuitry for printing serially arranged, continually received input data.

According to the invention continuous input data containing serially-arranged characters is printed in successive lines on a document. Those characters to be printed in a predetermined group of columns at the beginning of each line are stored so that the printer may perform its line feed and carriage return operations when beginning a new line without losing the characters. Individual printing means, each of which is associated with one of the beginning columns, are provided to print the stored characters upon completion of such operations.

For the remaining columns one or more storage circuits are provided, each storage circuit successively storing the characters to be printed in a plurality of the remaining columns. A moving type carrier for presenting type characters to the document is also provided. Preferably, the storage circuitry for the remaining columns only stores a number of characters substantially equal to the ratio of the time the carrier requires to present a complete font of characters to the time interval between successive input characters. This minimizes the storage circuitry required to print in the remaining columns.

BRIEF DESCRIPTION OF THE DRAWING

FIG. **1** is a schematic diagram of a printer incorporating a preferred embodiment of the invention.

FIGS. **2***a* and **2***b*, taken together are a schematic logic diagram of a portion of the print control circuit shown as a block in FIG. **1**.

FIG. **3** is a schematic logic diagram of that portion of the print control circuit which loads characters into the registers shown in FIG. **2**.

FIG. **4** is a schematic logic diagram of a typical hammer selecting circuit shown as a block in FIG. **2**.

FIG. **5** is a schematic logic diagram of that portion of the print control circuit which controls the paper feed.

FIG. **6** is a waveform diagram illustrating the operation of portions of the print control circuit shown in FIGS. **2**, **3** and **5**.

FIG. **7** is a diagram illustrating the operation of the hammer selecting circuit shown in FIG. **4**.

DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG. **1** schematically illustrates a printer having a conventional print drum **1** with type characters on its periphery. The type characters are arranged in rows paralleling the drum's axis and in eighty columns corresponding to the columns to be printed in a line on a document **2**. Each column of the drum contains one complete font of type characters and a space where no character occurs. The drum is rotated at a constant speed by a driving means not shown. The document **2** is stepped by a schematically illustrated paper feed **3**, line-by-line, out of the plane of the drawing. The paper feed moves the document after each line is printed so that the succeeding line may be printed. Any of the usual paper feed devices may be used such as those having a pair of tractors with movable endless chains supporting sprocket pins which engage edge perforations in the document **2**. A bank of eighty hammers **4** is positioned adjacent the drum and the paper **2** passes between it and the drum. A hammer is provided for each column of type characters on the drum. The hammers may consist of any of the variety used in on-the-fly impact printing. When a hammer is actuated it forces a ribbon (not shown) and the document **2** against the type character on the drum which is to be printed.

For ascertaining which row on the drum is approaching the hammers at each instant, a circular code disk **5** of conventional construction is mounted on a shaft extending from the drum to rotate therewith. The code disk is interposed between a light source **6** and a photosensing device **7**. As is conventional, the code disk **6** contains radial rows of coded apertures. The rows correspond to different character rows on the drum and each contains a sufficient number of apertures to represent one character according to a binary code. An additional radial row is included within the code disk; the apertures in this row do not represent a character on the drum but rather the space where no character occurs. Light passes from the light source, through the coded apertures, and onto a portion **7***a* of the photosensing device. In response, this portion of the photosensing device provides unique binary coded signals representing the particular rows of type characters or the row of spaces on the drum. This output is fed over a cable **8** which contains sufficient leads for transmitting binary coded signals.

As is also conventional, the code disk **5** contains a series of radially spaced apertures, each located at one of the disks coded rows of apertures. Light passing through these apertures on to a second portion **7***b* of

the photosensing device causes it to provide a series of strobe pulses S. Each strobe pulse S indicates when a row on the drum is passing the bank of hammers.

Both the row-indicating outputs and strobe pulses S from the photosensing device **7** are fed to a print control circuit **9.** The circuit **9** receives the input data to be printed and provides output signals for controlling the hammers **4** and paper feed **3.**

Before proceeding with a description of the logic diagrams, the meaning of the more extensively used logic circuit symbols is given. Of course, the logic circuit elements in FIGS. **2***a* **2***b*, **3**, **4** and **5** operate in a conventional manner on a binary voltage level basis wherein the inputs to the elements and outputs therefrom always exist at either of two discreet voltage levels, the positive voltage level or the negative voltage level of the system.

An AND circuit is represented by a D-shaped block containing an "&" symbol. The input lines are always connected to the straight side of the block and the output line is always connected to the curved side. The function of this circuit is to provide a positive output voltage only when all input lines exist at the positive level.

An OR circuit is represented by an arrow-shaped block containing the symbol "OR." Input lines are always connected to the concave side of the block and the output line is always connected to the point. The function of this circuit is to provide a positive level output only when any one or more of the input lines is at the positive level.

A delay circuit is represented by an elongated oval-shaped block with a pair of stripes nearest the input end. The function of this circuit is to generate an output level which follows the input level but which changes state at some fixed period of time after the input changes state.

A flip-flop circuit is represented by a block labeled FF. This circuit is any type of bi-stable circuit arrangement wherein a positive level signal at the S (set) input causes the 1 output to go positive and stay positive while the 0 output simultaneously goes negative and stays negative. A positive level signal at the R (reset) input causes the 0 output to go positive and stay positive while the 1 output simultaneously goes negative and stays negative. A flip-flop, once set, will thereafter change its output state only in response to a positive signal at the R input. When it is in the reset state, it will respond only to a positive signal at the S input.

A block labeled "COMP." represents a comparator which is a well-known circuit element for providing a positive level signal at its output when the coded signals applied to its inputs represent identical data.

A block subdivided into sections **1, 2, 4,** etc. represents a binary counter. Each stage of the counter has two outputs (only one of which is energized at a time) and the outputs of each stage represent one bit of a binary number. A positive level signal at the ADV UP input causes the binary number represented on the output lines to advance by a count of one. Conversely a positive level signal at an ADV DWN input causes the binary number represented on the output lines to decrease by a count of one. A positive signal at a RESET input causes the output state of the counter to revert to 0 (positive signals on all 0 output lines).

Referring to FIG. **2***a*, the input data to be printed is fed to the print control circuit, serial by character, serial by bit. Such input may be provided from a telecommunication line. This input data is initially fed to a "serdes" register **10** (serializing-deserializing) which converts the serially arranged bits of each character to parallel-arranged bits. Each character, in parallel bit form, is thereafter fed to eight single-character storage registers, **12***a–d* and **14***–d*, over cable **11** as well as to a function decoder **16.**

In general, a function decoder is any type of circuit arrangement which, when enabled, provides positive signals on one or more outputs when the coded signals fed to it represent functions to be performed by the printer rather than characters to be printed, e.g., signals commanding that the printer begin a new line of print. The function decoder **16** illustrated has two such function-indicating output lines: a positive CR (carriage return) signal for initiating a new line of print, and a positive LF (line feed) signal for stepping the paper an increment equalling one line. When the signals fed to the function decoder do not indicate a function but rather a character to be printed, the function decoder provides a signal $\overline{F}$ at another of its outputs.

It should be noted that the teleprinter disclosed is not of the type having a print mechanism carriage which moves across the document when printing a line. A separate stationary hammer is provided for each column. Thus, the CR carriage return signal is only a command to begin a new line of print and need not also initiate the return of an actual print mechanism carriage to the first column.

The function decoder is enabled by the 1 output of a flip-flop **18.** The flip-flop **18** receives its set input signal from the output of a bit counter **20.** The bit counter receives as its input the data to be printed represented as serially arranged bits. It is chosen to provide a positive level signal when sufficient bits are sensed in the data input to indicate that a character has been fed to the printer, e.g., a positive level signal is provided for every 6 bits if the data fed to the printer is coded according to a code which utilizes 6 bit characters. Thus, for each character the bit counter provides an output signal to cause the 1 output of flip-flop **18** to go positive and enable the function decoder **16.** The output of the bit counter is also passed through a delay **22** to its reset input R so that the bit counter resets itself after sensing each character. The output of the delay **22** is also fed to the reset input of flip-flop **18** to thereby terminate the positive signal at the flip-flop's 1 output and reset the flip-flop.

As previously noted, each character, represented by parallel bits is fed to the registers **12***a–d* and **12***a–d*. Each of these registers is adapted to store coded data representing one character. The characters are sequentially loaded into the registers by AND gates **17***a–d* and **19***a–d*.

Each of these AND gates has three enabling inputs which it receives from the circuit illustrated in FIG. **3.** Each of the AND gates **17***a–d* receives two of its input from a binary counter **21** and its third from the 0 output of a flip-flop **25.** Each of the AND gates **19***a–d* receives two of its inputs from the binary counter **23** in FIG. **3** and its third from the 1 output of flip-flop **25.**

When initiating a printing operation, both counters are reset at their zero states with positive signals $\overline{A}$, $\overline{B}$, $\overline{C}$ and $\overline{D}$ on their 0 output lines. The flip-flop **25** is in its reset state with its 0 output line being positive and providing the signal $\overline{E}$. The output lines of counter **21**

are connected to AND gate **17***a* such that the gate is conditioned by the $\overline{A}$ and $\overline{B}$ signals. Since AND gate **17***a* receives its other input from the 0 output of flip-flop **25** which initially provides the $\overline{E}$ signal, the AND gate **17** is originally enabled and loads the first character to be printed in register **12***a*.

In response to this first character, the function decoder **16** (FIG. 2) provides an $\overline{F}$ signal. After a period of time (determined by delay **27**) sufficient for the first character to be loaded into register **17***a*, this $\overline{F}$ signal is applied to advance the counter **21.** The counter then provides A and $\overline{B}$ output signals. AND gate **17***b* is connected to the counter **21** such that it is enabled by these signals along with an $\overline{E}$ signal from the 0 output of flip-flop **25.** Since the flip-flop still continues to provide the $\overline{E}$ signal, AND gate **17***b* is activated to load the second character into register **12***b*.

Similarly, the succeeding $\overline{F}$ signal provided in response to the second character steps the counter **21** so that it now provides $\overline{A}$ and B outputs to enable AND gate **17***c* and load the third character into register **12***c*. Register **12***d* is loaded in a similar manner when the counter provides signals A and B.

However, as shown in FIG. **3,** the outputs of counter **21** which provide the A and B signals are also fed to enable an AND gate **27.** After a period of time (determined by delay **29**) sufficient for the fourth character to be loaded into register **12***d*, the output of AND gate **27** is applied to the set input of flip-flop **25** to terminate the $\overline{E}$ signal from its 0 output and initiate an E signal from the flip-flop's 1 output. Since AND gates **17***a–d* are not conditioned by the E signal to load registers **17***a–17d*, succeeding characters in the line cannot be loaded into these registers.

However, AND gates **19***a–d* have as one of their conditioning inputs the E signal from flip-flop **25.** The output lines of counter **23** are connected to AND gate **19***a* such that the gate is conditioned by the $\overline{D}$ and $\overline{C}$ signals occurring when the counter is at its 0 state. Since the counter **23** is initially in its 0 state, AND gate **19***a* is enabled when flip-flop **25** changes state to provide its E signal. Thus, the fifth character is loaded into register **19***a*. Like counter **21,** counter **25** is stepped by successive $\overline{F}$ signals. These are fed through AND gate **31** which is conditioned by the E signal from the 1 output of flip-flop **25.** The delay **29** is also chosen so that the F pulse occurring in response to the fourth character has terminated before AND gate **31** is conditioned by the E signal. An unwanted advance of the counter **23** would otherwise occur.

The $\overline{F}$ signal occurring in response to the fifth character passes through delay **33** to advance the counter **23** so that it now provides C and $\overline{D}$ outputs. The output lines of the counter are connected to AND gate **19***b* so that the gate is activated to load the sixth character into register **14***b*.

Similarly, the seventh and eighth characters are loaded into registers **14***c* and **14***c* respectively.

When the eighth character has been loaded, the counter **23** provides D and C signals which are fed via AND gate **35,** delay **37** and OR gate **39** back to its reset input. The delay **37** is provided to allow AND gate **19***d* to become energized and load register **14d** before the D and C signals are terminated. Delay **37** also is chosen so that the $\overline{F}$ pulse occurring in response to the eighth character terminate before the counter is reset to its **0** state.

Since the flip-flop **25** continues to provide an E and not $\overline{E}$ signal, AND gates **19** and not AND gates **17** remain conditioned. Upon returning to its 0 state, the counter **23** loads the next (ninth) character into register **19***a* as it did previously with the fifth character. The 10th 11th and 12th character are loaded into registers **19***b*, **19***c* and **19***d* respectively. Similarly, the 13th, 14th 15th, 16th and subsequent characters are sequentially loaded into registers **14***a–d*.

Thus, the 5th, 9th . . . 77th characters in the line are sequentially loaded into register **19***a*. The 6th, 10th . . . and 78th characters are sequentially loaded in register **19***b*. The 7th, 11th . . . 79th characters are loaded into register **14***c*. The 8th, 12th . . . 80th characters are sequentially loaded into register **14***d*. Every fourth character (beginning with the fifth) is loaded into the same register **14***a–d*.

As shown in FIG. **3,** upon beginning a new line, the CR signal from the function decoder **16** (FIG. **2***a*) is applied to the RESET inputs of flip-flop **25** and counters **21** and **23.** This sets these elements so that they cause the characters in the new line to be loaded into registers **12***a–d* and **14***a–d* as previously described.

Referring to FIGS. **2***a* and **2***b*, each of the registers **12** and **14** is associated with and feeds coded data indicating its stored character over a cable to a comparator **28***a–28h* (FIG. **2***b*). Each of these comparators receive the coded signals over cable **8** from the photosensing device **7** (FIG. **1**). The comparator thus receives signals indicative of the particular row of type characters (or the row of spaces) on the rotating drum which is approaching the hammers. When the coded signals from a register **12** or **14** and from the photosensing device **7** represent an identical type character, the drum is in a position such that the particular type character on the drum which corresponds to the character in the register will be impacted by a hammer upon energization of the hammer at that time. Each comparator then provides a positive signal at its output. The period of delay occurring between the time when the photosensitive device **7** (FIG. **1**) senses light indicative of a character to be printed and the time when the hammer actually impacts the character is compensated for by having the disk **5** lead the characters on the drum by an appropriate distance.

When the inputs to a comparator are identical and a match occurs, the comparator feeds its output signal to one of eight AND gates **30***a–30h*. Each of these AND gates **30** is associated with one of the registers, **12** or **14,** as are the comparators **28.** When one of these AND gates **30** is enabled it provides a FIRE pulse to a hammer driver **32** or **34** to activate a hammer.

Since the voltage levels used in conventional logic systems are relatively low (typically, + 4 volts and − 2 volts) the outputs of AND gates **30** (the FIRE pulses) cannot be used to drive the hammers directly. Thus, a driving circuit arrangement is required to provide an output of sufficient magnitude to drive the hammers in response to the output signals from the AND gates **30.** The driving circuits illustrated as blocks **32** and **34** in FIG. **2** provide a negative to positive to negative square pulse output of fixed duration when energized by a FIRE pulse. The drivers designated **32***a–d* are associated with registers **12***a–d* and, therefore, columns **1–4.** The driving circuits designated **34***a–d* are associated with registers **14***a–d* and therefore columns **5** to **80** in the sequence by which the registers **14** store the char-

acters to be printed in these columns. The hammers associated with columns **5–80** share the four driving circuits **34** through four hammer selecting circuits **40***a–d* which will be described below.

Each of the AND gates **30** receive as conditioning inputs the strobe pulses from the photosensitive device **7** (FIG. **1**) as well as the output of a comparator **28.** A strobe pulse S is fed to each AND gate **30** so that it will provide its FIRE signal only when the rotating drum **1** is in a position such that a row of type characters are adjacent the hammers when the hammers strike the drum.

Each of the AND gates **30***a–d* which provide FIRE pulses for the first four columns has an FC signal as an additional enabling input. The FC ("feed complete") signal indicates that the paper feeding operation occurring just before the printer initiates a new line has been completed. Obviously it is not desired to fire the hammers in the columns at the beginning of the line (Columns **1** to **4** in the embodiment illustrated) until the paper has been stepped to present a new line to be printed. The FC signal is not fed to AND gates **30***e–h* since it is assumed that the document will have already been stepped before printing is to be performed in column **5.**

The function decoder provides an LF signal when it is desired to step the document. Each LF signal is fed to the ADV UP input of a binary counter **42** shown in FIG. **5** to advance it by 1. The number of LF signals are counted by the counter and this information fed to the paper feed which steps the document the specified number of times. Upon each step, the paper feed provides an LC signal ("line complete") indicating that the paper has been advanced a one line space. This LC signal is applied to the ADV DWN input of the counter **42** to decrease its count by 1. Thus, the paper feed **3** is instructed via the counter **42** to advance the required number of one line spaces and when the counter **42** is again decreased to 0 (positive signals on all 0 output lines) the paper feed **3** has stepped the document by the required amount. This condition is sensed by an AND gate **44** having its input lines connected to the three 0 output lines of the counter. When positive signals occur on all the 0 output lines, the AND gate **44** provides the FC enabling signal to the AND gates **30***a–d* associated with columns **1–4.**

Referring again to FIG. **2***b*, each of the driving circuits **32** and **34** have an input connected to a "space decoder" **41.** The space decoder receives as its input the coded signals over cable **8** from the photosensing device **7** which indicate the positions of the various rows of characters and the row of spaces on the drum. When these coded signals indicate that the row of spaces on the drum is approaching the hammers, the space decoder provides a positive output signal. This signal is fed to inhibit all the drivers **32** and **34** (this inhibiting function being illustrated in FIG. **2***b* by a small circle where the space decoder's output line joins each driver's inputs). Thus, when the coded signals in a register **12** or **14** represent a space within the line being printed and the signals over cable **8** also represent a space, the drivers are inhibited and printing does not occur even though a match occurs in one of the comparators **28** and a FIRE pulses is supplied by one of the AND gates **30.**

FIGS. **2***a* and **2***b* also indicate that the FIRE pulse from each AND gate **30** is fed back to its associated register, **12** or **14.** The FIRE pulse clears the data stored within the register once the AND gate has provided a FIRE pulse to print the character. With a space "character," although printing does not occur, the AND gate still provides a FIRE pulse to clear the register of its space-indicating data. Clearing the register in this manner prevents duplicate printing of the characters.

Referring now to FIG. **4,** the circuit **40***a* shown as a block in FIG. **2***b* for sequentially connecting driving circuit **34***a* to the hammer mechanisms in Columns **5, 9 . . . 77** is schematically illustrated. Similar circuits shown as blocks **40***b*, **40***c* and **40***d* in FIG. **2** are provided for sequentially connecting driving circuits **34***b*, **34***c* and **34***d* to those hammer mechanisms which print in columns: **6, 10 . . . 78**; **7, 11 . . . 79**; and **8, 12 . . . 80,** respectively. Each driving circuit **34** is sequentially connected to every fourth hammer in columns **5–80.**

The hammer selecting circuits form no part of the invention and are the subject matter of a copending application titled "Printer and Control Circuit Therefor" by Thomas M. Kearns, executed Jan. **26, 1970,** and assigned to the assignee of the present application.

The hammer selecting circuit **40***a* comprises a network **46** having two sets of leads **48** and **50** arranged to intersect each other and form a matrix. The activating coils **52** in the hammers which print in columns **5, 9, . . . 77** are each connected between a different pair of leads, the leads of each such pair being from different sets. Of course the hammer coils **52** are physically parts of the hammers **4** and are actually located along the length of the drum **1** as indicated in FIG. **1.** However, for ease of illustration, the coils **52** are shown as physically located within the matrix **46** in FIG. **3.** Each coil **52** is connected to a lead in the matrix with an isolation diode **54.** The diodes **54** perform a conventional function of blocking current flow in unwanted directions within the matrix network **46.**

As illustrated, there are four leads in the set designated **50** and five leads in the set designated **48.** There are 19 coils **52** connected to the matrix **46.** Since the hammer selecting circuits **40***c–d* are similar, they too have 19 coils each. Thus, each of the drivers **34** sequentially energizes 19 coils.

Two groups of relays **56** and **58,** are provided. The relays in group **56** have their contacts **56***a* adapted to be connected to a lead in set **50.** The relays in group **58** have their contacts **58***a* adapted to be connected to a lead in set **48.** The relays, of course, may be of any suitable conventional construction. Preferably, they consist of the well-known "reed contact" variety. The relays in group **56** are commoned to a lead **60** over which the driving circuit **34***a* feeds its output pulse when actuated. When one of the relays in group **56** is closed, the output pulse from the driving circuit **34***a* on lead **60** is applied to one of the leads in the set designated **50.** The relays in group **58** are commoned to a negative voltage potential −V such that this potential is applied to one of the leads in the set **48** when one of the relays in this group is closed.

When one relay from each of the groups **56** and **58** is closed, a conductive path is provided for any pulse from the driving circuit **34***a* on lead **60,** along one of the leads in set **50,** across a particular isolation diode **54,** across a particular coil **52,** along one of the leads in set **48,** and to the negative reference potential −V. Therefore, by closing a selected pair of relays (one in

each group) a conductive path is provided from the driving circuit **34***a*, through one particular hammer coil **52**, to the negative reference potential. In this manner, selectively closing a pair of relays operates a selected hammer.

The relays (and therefore the hammer coils **52**) are sequentially energized by a five-stage binary counter **62** and two groups of AND gates **64** and **66**. There are four AND gates in the group designated **64**. Each AND gate in this group has its output connected to one of the relays in group **56** such that actuation of the gate energizes a relay coil **56***b* to close its associated contact **56***a*. The AND gates in group **64** have two inputs each. Each of the inputs is connected to one of the outputs from the low order stages, **1** and **2**, of the binary counter. The connections between these AND gates and the counter **62** are such that each gate is actuated by a particular combination of the two low order bits in the binary coded number represented by the outputs of the counter. Thus, AND gates **64** are activated by the two low order stages of the counter **62** in a manner similar to the one by which AND gates **17** *a–d* and **19** *a–d* (FIG. **2***a*) are activated by counters **21** and **23** (FIG. **3**). With different combinations of the two low order bits, different AND gates in group **64** are actuated. Advancement through the 1 and 2 states of the counter sequentially actuates the AND gates in group **64**. Since each of the AND gates in this group closes a relay in the group designated **56**, sequential advancement of the counter sequentially closes the relays in group **56**.

The other group of AND gates **66** consists of five gates. Each AND gate in this group has its output connected to one of the relays whereupon activation of an AND **66** energizes a relay coil **58***b* and closes its associated contact **58***a* to connect a lead **48** to the voltage source − V. The AND gates in this group **66** have three inputs which are connected to the outputs from the high order stages (**4**, **8** and **16**) of the counter **62**. Similar to the connections between the AND gates in group **64** and the counter, the connections between the AND gates in group **66** and the counter are such that each gate is actuated by a particular combination of the three high order bits in the binary coded number represented by the output of the counter. Different combinations of the three high order bits actuate different AND gates. Advancement of the counter sequentially actuates the AND gates in group **66**. Sequential actuation of these AND gates sequentially operates the relays in group **58**.

Each setting of the counter actuates an AND gate in each of the groups **64** and **66**. Advancement of the counter by successive pulses at its ADV UP input sequentially actuates selected pairs of the gates, the gates of each pair being in different groups. Each of these pairs of AND gates closes one relay in each of the groups **56** and **58** to provide a current path from the driving circuit **34**a, through a selected hammer coil **52**, to the reference potential.

Each of the AND gates in group **64** and **66** has a small driving circuit **68** associated with it and connected to its output. These act in a conventional manner to connect the low output of the AND gates to a sufficiently high voltage to operate the relays.

As illustrated in FIG. **2***b* and **4**, the pulses for advancing the counter **62** are applied via a delay **70***a* from the AND gate **30**e which provides the FIRE pulses for the driving circuit **34***a* and hammer selecting circuit **40***a*. Thus, after each FIRE pulse energizes the driver **34***a* to energize one of the nineteen hammer coils **52** in the hammer selecting circuit **40***a* that FIRE pulse steps the counter **62** so that a new hammer coil **52** is selected in the circuit **40***a*. This new hammer coil will be energized by the next successive output of the hammer driver **34***a*. Similarly, the FIRE pulses from AND gates **30** *f–h* are applied through delays **70** *b–d* to advance the counters in hammer selecting circuits **40** *b–d*.

The counter **62** in FIG. **4** is reset by the output of an OR gate **72** which is energized by the output of either of two AND gates **74** or **75**. The AND gate **74** has five inputs. These are connected to those output lines of the counter **62** which will be energized when the counter represents the binary number 10010. When the counter represents this number, the 19th hammer (i.e., the hammer located in column no. **77**) is actuated. These output lines of the counter will energize the AND gate **74** which will provide an LP signal and after a period of time determined by delay **76**, energize the OR gate **72** to reset the counter. Thus, AND gate **74** and delay **76** cause the counter to be reset after all the hammers in its hammer selecting circuit have been energized.

AND gate **75** has three inputs and is activated by simultaneously receiving the A, B and $\bar{E}$ signals from the counter **21** and flip-flop **25** shown in FIG. **3**. These signals occur when the fourth character of a line is loaded into register **17***d* (FIG. **2**). Since the hammer selecting circuit **40***a* of FIG. **4** is used for printing in Column **5**, the A, B and E signals reset the counter **62** so that the hammer coil for Column **5** is connected to driver **34**a in sufficient time for printing in the fifth column. Similarly, the A, B and E signals are applied to the counters (not shown) in the hammer selecting circuits **40***b–d* to reset them in sufficient time for printing in the sixth, seventh and eighth columns.

OPERATION

An example of the operation of the printer will now be described. Assume that the type drum **1** (FIG. **1**) rotates at 2,000 RPM. Since each column of the drum contains one font, 30 milliseconds are required to pass a complete font past the hammers **4**. Assume that a complete input character is received by the printer every 7.5 milliseconds. Further assume that, under the system of telecommunication used, new line commands fed to the printer consist of CR CR CR LF, i.e., three carriage return commands and one line feed command.

The photosensing device **7** shown in FIG. **1** continually provides both the periodic strobe pulses S and the signals identifying the rows of type characters or the row of spaces as they approach the hammers. The series of strobe pulses is fed to the AND gates **30** shown in FIG. **2***b* while the character or space identifying signals are fed to the comparators **28**.

In reference to FIGS. **2***a*, **2***b* and **6**, the first character of the line being printed enters the serdes register **10** (FIG. **2***a*) in serial bit form. The serdes register converts the bits representing the character from serial to parallel form and feeds this data to registers **12** and **14** and the function decoder **16**. The input dats is fed to the bit counter **20** as well as to the serdes register. When sensing sufficient bits to indicate that a character has been fed to the printer (e.g., six bits under a six-bit code), the bit counter sets flip-flop **18** which enables the function decoder **16**. The output of the bit counter

is also used to reset it and flip-flop **18** after a delay caused by the delay element **22.** The function decoder, assumeing that a character is to be printed in column **1** of the line, provides an $\overline{F}$ signal.

As illustrated in FIGS. **2***a*, **3** and **6,** when beginning a new line the counters **21** and **23** are initially in their 0 states and flip-flop **25** in its reset state. Thus, signals $\overline{A}$, $\overline{B}$. $\overline{C}$. $\overline{D}$ and $\overline{E}$ initially occur. AND gate **17***a* is enabled by the $\overline{A}$, $\overline{B}$ and $\overline{E}$ signals to load the first character of the line into register **12***a*.

Of course, AND gate **30***a* in FIG. **2***b* is receiving its FC conditioning signal since the counter **42** (FIG. **5**) which indicates line feed (LF) commands not yet completed is representing zero.

Thus, with the character to be printed in column **1** stored in register **12***a* and the AND gate **30** receiving its conditioning input, the character will be printed when a match occurs in comparator **28***a* and the strobe pulse S is applied to AND gate **30.** The match in the comparator occurs when the photosensing device **7** provides a coded output identical to the coded signals representing the character stored in register **12***a*. Upon this occurrence, the character for column **1** is printed by AND gate **30**a providing a FIRE pulse to energize the driver **32***a* appropriate to column **1.** This FIRE pulse thereafter is applied to the clear input of register **12***a*.

Referring again to FIGS. **2***a* and **3**, the $\overline{F}$ signal provided by the function decoder **16** is applied via delay **27** to the ADV UP input of counter **21** after AND gate **17***a* has been unabled to load the first character into register **12***a*. This advances the counter so that it now provides A and $\overline{B}$ signals to enable AND gate **17***b* and load the second character into register **12***b*. Comparator **28***b*, AND gate **30***b* and driver **32***b* in FIG. **2***b* then print the second character in the same manner as described above with reference to the first character.

Subsequently, the characters to be printed in the rest of the beginning columns(columns **3** and **4**) will be fed to the printer and printed in the same manner as were the characters in columns **1** and **2.**

Of course, since the drum only passes a complete font past each column every 30 milliseconds and characters are fed to the printer every 7.5 milliseconds, the characters may not be printed the instant they are received. A period of delay may occur until that character on the drum which is to be printed reaches the hammers. The characters will be stored in the registers **12***a–d* until a match is indicated in the appropriate comparator **28***a–28d*.

With respect to columns **5–8,** the hammer selecting circuits **40***a–d* are initially set so that when drivers **34***a–d* are energized they will activate hammers **5, 6, 7** and **8** respectively. When the fourth character is loaded into register **12***d*, the counter **21** (FIG. **3**) provides A and B signals which enable AND gate **27** and set flip-flop **25** so that it provides an E signal. The output of AND gate **27** is passed through delay **29** so that flip-flop **25** can continue to provide its $\overline{E}$ signal until the fourth character is loaded into register **12**d. When the E signal occurs it enables AND gate **19***a* since this gate already is receiving its conditioning $\overline{C}$ and $\overline{D}$ inputs from counter **23** which is in its 0 state. Thus, AND gate **19***a* loads register **14***a* with the next or fifth character.

The $\overline{F}$ signal occurring in response to the fifth character is applied to advance the counter **23** so that it will provide C and $\overline{D}$ signals, enable AND gate **19***b* and load the sixth character into register **14***b*. This $\overline{F}$ signal is applied via AND gate **31** (which has been conditioned by the E signal from flip-flop **25**) and delay **33** which delays advancement of the counter **23** until it has provided its $\overline{C}$ and $\overline{D}$ signals.

Registers **19***c* and **19***d* are loaded with the seventh and eighth characters in the same manner as were registers **19***a* and **19***b*. The characters to be printed in columns **5–8,** after being loaded in registers **19***a–d*, are printed in the manner described with reference to columns **1–4.**

After each of the driving circuits **34***a–d* are energized by the FIRE pulses from AND gates **30** *e–h*, the FIRE pulses are applied via delays **70** *a–d* to the hammer selecting circuits **40** *a–d*. Each FIRE pulse advances the hammer selecting circuit so that upon completion of printing in column **5** the hammer selecting circuit **40***a* has now selected the hammer to be printed in column **9.** Similarly, upon completion of printing in columns **6, 7** and **8** the hammer selecting circuits **40***b*, **40***c* and **40***d* have now selected those hammers which print in columns **10, 11** and **12** respectively.

When the eighth character is loaded into register **19***d*, the counter **23** provides C and D signals which enable AND gate **35** (FIG. **3**). After a period of time determined by delay **37** and sufficient for the eighth character to be loaded, the output of AND gate **35** is fed via OR gate **59** to the reset input of counter **23.** Thus, counter **23** is again at its reset or 0 state and provides $\overline{C}$ and $\overline{D}$ signals. With flip-flop **25** continuing to supply an E signal, AND gate **19***a* is enabled to load the next or the ninth character in the line into register **14***a*. The character for column number **9** is then printed via the appropriate comparator **28***e*, flip-flop **36***e*, AND gate **30***e*, driving circuit **34***a* and hammer selecting circuit **40***a*. These elements perform as already disclosed when describing printing in previous columns.

Subsequent columns, that is, columns **10, 11** and **12** are printed in the same manner as were the previous columns **6, 7** and **8.**

As for the character to be printed in column **13,** it is printed as were the characters in columns **5** and **9.** The hammer selecting circuit **40**a having selected column **13** after being advanced by the FIRE pulse which effected printing in column number **9.**

All the remaining subsequent columns are printed in a similar manner.

Whenever data indicating a space is fed to the printer it is treated as any usual character to be printed. The data is loaded into a register (**12** or **14**) and fed to a comparator **28.** When cable **8** feeds identical data to the comparator, the comparator conditions an AND gate **30** which, in turn, provides a FIRE pulse to activate a driver **32** or **34.**

However, the data fed over cable **8** at this time is also fed to the space decoder **41** which provides a signal to inhibit the driver. Thus, printing does not occur in this column and a space is left.

There are four single-character registers designated **14** and associated with columns **5–80.** These allow one character to be received by the printer each 7.5 milliseconds even though the print drum **1** only presents a complete font to the hammers every 30 milliseconds. That is, four characters may be stored and accommodated at one time and thus no data is lost. The characters are stored within the four registers until the drum rotates sufficiently to present the character to be

printed to the hammers. The amount of storage circuitry required (i.e., enough to accommodate four characters) is ascertained by dividing the time the drum **1** requires to present a complete font of characters to the hammers by the time interval at which successive input characters are received.

When a new line is to be printed, the document is fed to present a new area to the hammers. Additionally, the printer control circuit must cause the next character received to be printed in column number **1.** Conventionally, a new line is initiated by three successive CR (carriage return) signals on the incoming data line followed by one LF (line feed) signal. These four signals require 7.5 milliseconds each and a total of 30 milliseconds. Therefore, they provide sufficient time for a character to be printed in the last column of the previous line since this printing will require no more than 30 milliseconds (the time required for the drum to present a complete font).

With such CR and LF signals initiating a new line, each of the CR signals will reset and maintain the counters **21** and **23** (FIG. **3**) as well as resetting the flip-flop **25** at 0. The LF signal advances the binary counter **42** (FIG. **5**) so that its output lines will represent 1. This signal is fed to the paper feed **3** which, upon completion of the paper feed operation, provides an LC signal to decrease the counter **42** down to 0. The AND gate **44** senses that the counter **42** is at 0 and provides the FC signal to the AND gates **30***a–d* associated with the beginning four columns.

Of course, operation of the paper feed **3** requires a period of time. During this period, characters are still continually received by the printer and thus storage is required to accommodate them since printing cannot occur during the paper feed operation. These characters at the beginning of the new line are sequentially loaded into registers **12***a–d* in the same manner as were the characters for columns **1** to **4** in the previous line. Upon completion of paper feed, the AND gates **30***a–d* will receive their feed complete (FC) signal. Thus, when enabled, they will provide the FIRE pulses necessary to energize the drivers **32** for columns **1–4** of this new line. In this manner, those characters in the beginning columns (i.e., columns **1–4**) are not lost during the paper feed operation. They are stored within the registers **12***a–d*. However, in any case sufficient storage circuitry is provided to store each character which is to be printed in one of the beginning columns.

Those characters to be printed in the remaining columns—columns **5** to **80** of the new line are printed in the same manner as in the previous line.

Referring now to FIGS. **4** and **7,** the operation of the hammer selecting circuit **40***a* will be described. As previously noted, circuit **40***a* sequentially connects driving circuit **34***a* with hammers in columns **5, 9 . . . 77.** Although only operation of hammer selecting circuit **40***a* is described, the other selecting circuits **40***b–d* operate in an identical manner. For printing in column **5,** the counter **62** will have been reset to 0 by the output of the OR gate **72** which was activated by the A, B and $\bar{E}$ signals occurring when the fourth character was loaded into register **12***d* (FIG. **2***a*). Alternatively, provided that the last column (column **77**) associated with the hammer selecting circuit **40***a* had a character printed therein, the AND gate **74** will be activated to reset the counter **62** with an LP signal via delay **76** and OR **72.** In either case, positive signals now appear on all five of the counter's 0 output lines. The AND gates designated **66***a* and **64***a* in groups **66** and **64** are enabled by these outputs and will be active to energize their associated relays. A conductive path is thereby provided across the hammer coil associated with column **5** which is designated **52***a*. Thus, the first output from driving circuit **34***a* after beginning a new line energizes the hammer for printing in column **5.** The FIRE pulse from the AND gate **30***e* (FIG. **2**b) which first energized the driving circuit **34***a* is applied to the ADV UP input of the counter **62** via a delay **70***a*. Of course, the delay **70***a* is chosen to provide sufficient time so that the counter **62** is not advanced until the hammer in column **5** has been activated.

This FIRE pulse advances the counter **62** so that it now energizes AND gates **64***b* and **66***a*. These AND gates energize their associated relays to provide a conductive path across the hammer coil associated with column **9** (designated **52***b*) which is thereby energized when the driving circuit **34***a* provides its next output pulse.

The remaining hammer coils connected to the hammer selecting circuit **40***a* are energized in a similar sequential manner. FIG. **5** illustrates the time relationships between the bits represented on the output lines of the counter **62** and the AND gates **64** and **66.** Only some of the AND gates are indicated since they are illustrative.

As previously disclosed, the 0 outputs of the counter **43** are all positive, representing the binary number 000000 (decimal 0) for printing in column **5.** Thus, for column **5,** FIG. **5** indicates that the outputs of all stages in the counter represent 0 bits. These outputs enable AND gates **64***a* and **66***a*.

For printing in the ninth column, the binary number 000001 (decimal 1) is represented by the outputs of the counter; the outputs of all stages except stage number **1** represent 0 bits. This activates AND gates **64***b* and **66***a* to thereby provide a conductive path across the hammer coil associated with the ninth column.

For the 77th column, the counter will have advanced until it represents the binary number 10010 (decimal 18). This activates AND gates **64***c* and **66***c* which provide a conductive path across the hammer coil (designated **52***c*) associated with the 77th column.

In summary, therefore, it may be seen that the printer and method described prints all of the continually fed serially arranged characters with a minimum amount of storage circuitry. Characters to be printed in the beginning columns, columns **1–4,** are not lost during the line feed operation. Registers **12***a–d*, each of which is dedicated to one of these beginning columns, are provided for this purpose. For the remaining columns, columns **5–80,** only four single-character storage registers **14***a–d* are needed since storage circuitry for only storing four characters is required. The number of characters which must be stored, that is "four," being obtained by dividing the time required by the drum to present a complete font to the hammers divided by the time interval between successive input characters.

Although the teleprinter described above utilizes a separate fixed hammer for each column, the invention may be practiced with a teleprinter having a hammer mechanism which moves on a carriage across the document to print a line. In such a printer, the columns at the beginning of each line (e.g., the first four columns) each have individual fixed hammers and the moving

hammer mechanism only effects printing in the remaining columns. This allows characters to be printed in the beginning columns without waiting for carriage return. Storage circuitry is provided for the characters to be printed in the beginning columns to avoid their loss during the line feed operation occurring at the beginning of each line. Preferably, this storage circuitry comprises single character registers as in the preferred embodiment described.

The moving carriage contains several hammers and effects printing in the remaining columns in cycles, several columns being printed by the several hammers during each cycle. The number of characters which must be stored at one time is substantially equal to the ratio of the time required by the drum to present a font of characters to the time interval between successive input characters. Also, preferably, a number of single-character storage registers are used, each register storing one character to be printed in each cycle and successively storing characters to be printed in successive cycles. Thus, as with the teleprinter described in detail above, this teleprinter also requires only minimum storage circuitry.

It will be appreciated that various changes in the form and details of the above described preferred embodiment may be effected by persons of ordinary skill without departing from the true spirit and scope of the invention.

I claim:

1. An apparatus for continually receiving coded, serially arranged signals representing line feed control characters and data characters and printing type characters representing said data characters in successive print lines on a document, each said print line having an initial group of type characters printed in a plurality of initial print positions in said line and a following group of type characters printed in the print positions following said initial print positions, said apparatus comprising:

first storage means for receiving and storing an initial group of data character signals;

control means for generating a print control signal;

a plurality of first printing means concurrently operable in response to said print control signal to print type characters representing the data characters stored by said first storage means in the initial positions of a print line on said document;

second storage means for receiving and storing a following group of data character signals;

second printing means for printing type characters representing the data characters stored by said second storage means in the print positions following said initial print positions in said print line on said document, said second printing means being operable to commence the printing of each respective type character in said following group as its related data character signal is serially received by said second storage means; and,

positioning means for receiving said line feed control signals, said positioning means being operable in response to received line feed control signals to align the first and second printing means with a new print line position on the document in preparation for printing the next print line, said positioning means being constructed and arranged to inhibit the generation of said print control signal during said aligning operation.

2. The apparatus set forth in claim **1** wherein:

said second storage means includes fewer character storage locations than the number of type characters printable in said print positions following said initial print positions in said print line;

said second printing means includes clearing means operable as each type character is printed to clear the corresponding data character out of said second storage means; and,

said second storage means further includes loading means for loading each newly received data character signal of said following group of data character signals into a cleared character storage location.

3. The apparatus set forth in claim **2** wherein:

said second storage means includes plural character locations; and,

said second printing means includes a separate printing element for each of said character storage locations, each said printing element being adapted to print in one or more of said print positions following said initial print positions in said print line.

* * * * *