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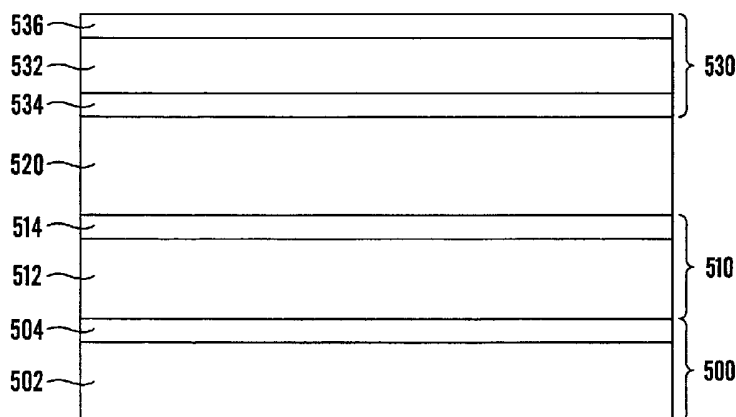
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(54) Title: A METHOD FOR MAKING A FERROELECTRIC MEMORY CELL IN A FERROELECTRIC MEMORY DEVICE, AND A FERROELECTRIC MEMORY DEVICE



(57) Abstract: In a method for making ferroelectric memory cells in a ferroelectric memory device a first electrode comprising at least one metal layer and optionally at least one metal oxide layer is formed on a silicon substrate which has an optional insulating layer of silicon dioxide. A ferroelectric layer consisting of a thin film of ferroelectric polymer is formed on the top of the first electrode layer and at least a second electrode comprising at least one metal layer and at least one metal oxide layer is formed on the ferroelectric layer. The second electrode is deposited by thermal evaporation of a high-purity evaporation source from an effusion cell onto the ferroelectric layer in a vacuum chamber filled with a gas or a gas mixture. A ferroelectric memory device wherein the memory cell has been made with the above method, comprises at least a first and a second set of respectively parallel electrodes (510; 530), wherein the electrodes (510; 530) in a set are provided orthogonally to the electrodes (530; 510) of a nearest following set and with memory cells formed in a ferroelectric layer (520) provided between successive electrode sets, such that memory cells are defined in the crossings between the electrodes (510; 530) which contact the ferroelectric layer (520) on each side thereof.



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A method for making a ferroelectric memory cell in a ferroelectric memory device, and a ferroelectric memory device

The present invention concerns a method for making a ferroelectric memory cell, comprising steps for

- 5 (a) providing a substrate consisting of a silicon layer, and optionally a silicon dioxide isolation layer;
- (b) forming a first electrode comprising at least one metal layer and at least one metal oxide layer, and providing said first electrode adjacent to said substrate and in contact with said silicon layer or said optional silicon
- 10 dioxide isolation layer;
- (c) forming a first ferroelectric layer consisting of a polymer ferroelectric thin film, and providing said first ferroelectric layer adjacent to and in contact with said first electrode; and
- (d) forming a second electrode comprising at least one metal layer and at
- 15 least one metal oxide layer, and providing said second electrode adjacent to and in contact with said first ferroelectric layer.

The present invention also concerns a ferroelectric memory device comprising ferroelectric memory cells capable of storing data in either one of at least two polarization states when no electric field is applied to the

20 memory cells, wherein the ferroelectric memory device comprises at least one ferroelectric layer formed by a polymer ferroelectric thin film and at least a first set and a second set of respective parallel electrodes, wherein the electrodes of the first set are provided in substantially orthogonal relationship to the electrodes of said second set, said first set and second set of electrodes

25 contacting ferroelectric memory cells at opposite surfaces of said at least one polymer ferroelectric layer, and wherein at least the first set and second set of electrodes are adapted to read, refresh or write ferroelectric memory cells by applying appropriate voltages thereto.

Ferroelectrics are electrically polarizable materials that possess at least two

30 equilibrium orientations of the spontaneous polarization vector in the absence of an external electrical field, and in which the spontaneous polarization vector may be switched between those orientations by an electric field. The memory effect exhibited by materials with such bistable states of remanent polarization can be used in memory applications. One of the polarization

35 states is considered to be a logic "1" and the other state a logic "0". Typical passive matrix-addressing memory applications are implemented by letting

two sets of parallel electrodes cross each other, usually in an orthogonal fashion, in order to create a matrix of cross-points that can be individually accessed electrically by selective excitation of the appropriate electrodes from the edge of the matrix. A layer of ferroelectric material is provided
5 between the electrode sets in a capacitor-like structure such that memory cells are defined in the ferroelectric material between the electrode crossings. When applying potential differences between two electrodes, the ferroelectric material in the cell is subjected to an electric field which generates a polarization response generally tracing a hysteresis curve or a portion
10 thereof. By manipulating the direction and the magnitude of the electric field, the memory cell can be left in a desired logic state. The passive addressing of this type of arrangement leads to simplicity of manufacture and allows a high density of cross-points or memory cells.

Sputtering is a method commonly used for depositing different types of
15 layers in ferroelectric memory devices. The bottom and upper electrode sets are often deposited by sputtering and sometimes the ferroelectric memory layer as well. Published International Patent Application No. WO 00/01000 (Hayashi & al.) discloses the use of a direct current magnetron reactive sputtering process for creating a smooth bottom electrode made of e.g.
20 platinum. A gas mixture of a noble gas and either oxygen gas or nitrogen gas is used. This reduces the amount of surface irregularities such as sharp hillocks and leads to improved fatigue endurance, polarization and imprint characteristics. While there are relatively few problems with performing such methods on devices with perovskite ferroelectric cells, e.g. lead zirconium
25 titanate (PZT) which is a very popular alternative, another type of problem needs to be addressed, however, for ferroelectric memory devices with polymer as a memory material. The sputtering of the upper electrode may damage the polymer ferroelectric cells, and hence another method for providing the upper electrode is required.

30 U.S. Patent No. 6,359,289 (Parkin) discloses the making of a magnetic tunnel junction device, wherein an insulating tunnel barrier is preferably thermally evaporated onto a fixed ferromagnetic layer. Similar to the way ferroelectric memory devices function, the two ferromagnetic layers on either side of the insulating tunnel barrier can assume different magnetization directions, i.e. a
35 relative orientation of the magnetic moments, and consequently be operated as a non-volatile random access memory. The insulating tunnel barrier is

primarily made of gallium and/or indium oxide or nitride. Additionally, an oxide or nitride of aluminum can form part of the barrier material in the form of an extra layer. The preferred method of preparing gallium oxide is by depositing gallium from an effusion source in the presence of oxygen gas or
5 in the presence of more reactive oxygen provided by an atomic oxygen source or other source. However, the problem addressed herein is that of high resistance-area values, i.e. large tunnel barrier energy height. Therefore, the solution for thermally evaporating gallium and/or indium oxide or nitride does not address the problem present when electrode material shall be
10 deposited or formed on an underlying polymer layer.

Further there is from EP patent application No. 567 870 A1 (Puffmann, assigned to Ramtron Int. Corp.) known a ferroelectric capacitor for use in a ferroelectric memory device. Generally this publication discloses a composite bottom electrode comprising an additional layer of palladium and a contact
15 layer of e.g. platinum metal, or an alloy of platinum and other metals. The ferroelectric memory material is here an inorganic material, e.g. lead zirconium titanate (PZT) which is well-known in the art. The top electrode on the opposite side can be similarly composite and consist of platinum or an alloy of platinum and other metals. As the ferroelectric material in any case
20 is an inorganic material such as PZT, thermal incompatibility between this material and the process for depositing the top electrode does not constitute a problem.

Thus it is a primary object of the present invention to provide a method for making an electrode layer for memory cells in a ferroelectric memory device,
25 and particularly it is an object of the present invention to provide a method for making an upper electrode layer for memory cells in a ferroelectric memory device. Even more particularly it is an object of the present invention to provide a method for depositing the electrode metal for an upper electrode onto a ferroelectric memory layer in the form of a ferroelectric
30 polymer.

A further object of the present invention are to provide a ferroelectric memory device made with the method according to the invention.

The above-mentioned objects as well as further features and advantages are realized according to the invention with a method which is characterized by
35 step (d) further comprising forming one metal oxide layer by placing said

- substrate, said first electrode and said first ferroelectric layer in a vacuum chamber, providing a high-purity evaporation source in an effusion cell, said effusion cell being provided in said vacuum chamber, evaporating thermally said high-purity evaporation source from said effusion cell onto the surface of said first ferroelectric layer while supplying a working gas at a first gas pressure; and forming one of said at least one metal layer by evaporating thermally said high-purity evaporation source from said effusion cell onto the surface of said at least one metal oxide layer while maintaining a second gas pressure.
- 10 Preferably the high-purity evaporation source is high-purity titanium. Further preferably at least one metal layer of the second electrode is a layer of titanium and the at least one metal oxide layer of the second electrode a layer of titanium oxide, titanium dioxide and a combination of titanium oxide and titanium dioxide.
- 15 Preferably the working gas is oxygen gas or a gas mixture of at least oxygen gas or nitrogen gas. In the latter case the oxygen gas constitutes less than 50% by volume of the working gas and the nitrogen gas more than 50% by volume of the working gas and preferably the oxygen gas then constitutes 15 to 25% of the working gas by volume.
- 20 Advantageously the gas pressure in the vacuum chamber is between -10^3 and -10^6 Torr.
- Advantageously the effusion cell comprises a crucible made of carbon in its graphite form, and the crucible can then preferably be heated to between 1600 and 1900°C during the thermal evaporation of the high-purity of
- 25 evaporation source.
- A preferable embodiment according to the invention further comprises steps for
- (e) forming a second ferroelectric layer consisting of a polymer ferroelectric thin film, said second ferroelectric layer being provided adjacent to and in contact with said second electrode;
- 30 (f) forming a third electrode comprising at least one metal layer and at least one metal oxide layer by thermal evaporation, said third electrode being provided adjacent to and in contact with said second ferroelectric layer;
- (g) forming a first dielectric interlayer consisting of a dielectric material, said

first dielectric interlayer being provided adjacent to and in contact with said third electrode; and

(h) repeating steps (a) through (g) at least once.

5 In this connection it is preferred that step (h) is repeated three times, and further comprises a step for (i) forming a thirteenth electrode comprising at least one metal layer and at least one metal oxide layer, the thirteenth electrode being electrically connected with at least two of the other electrodes.

10 The invention also concerns a ferroelectric memory device characterized in that said first set of electrodes comprises at least one metal layer and at least one metal oxide layer, said first set of electrodes being provided adjacent to a substrate and in contact with a silicon layer, or optionally a silicon dioxide isolation layer, that said second set of electrodes comprises at least one metal layer and at least one metal oxide layer, said second set of electrodes being
15 provided adjacent to and in contact with a ferroelectric layer, and that said second set of electrodes is formed in a vacuum chamber by thermally evaporating a high-purity evaporation source from an effusion cell onto the surface of said ferroelectric layer while providing a working gas at respectively a first and a second gas pressure.

20 In a preferred embodiment the ferroelectric memory device comprises three or more set of electrodes and at least two ferroelectric layers each set of electrodes being provided adjacent to and in contact with at least one ferroelectric layer and each ferroelectric layer being provided between and in contact with two sets of electrodes.

25 The present invention shall now be explained in greater detail by means of a discussion of exemplary embodiments thereof and in conjunction with the appended drawing figures, of which

fig. 1 shows a schematic hysteresis curve of a ferroelectric memory material;

30 fig. 2a schematically a principle for a passive matrix-addressing device with orthogonally crossing first and second electrodes provided in parallel in respective electrode sets;

fig. 2b the device in fig. 2a with memory cells comprising ferroelectric material provided between the crossing electrodes;

fig. 3 a block diagram of a memory device according to a preferred embodiment of the invention;

fig. 4 schematically a partial cross section of an effusion cell as used with an embodiment of the method according to the invention;

5 fig. 5 schematically a cross section of a ferroelectric memory cell as used with an embodiment of the memory device according to the invention; and

fig. 6 schematically a cross section of four stacked ferroelectric memory cells in another embodiment according to the invention.

10 Before the present invention is explained with reference to preferred embodiments a brief review of its general background shall be given with particular reference to the structure of matrix-addressable ferroelectric memories and how they generally are addressed for readout.

Fig. 1 shows a hysteresis curve 100 for a ferroelectric material. Here the polarization P is rendered as a function of the voltage V . The positive saturation polarization is denoted by P_S and the negative saturation polarization by $-P_S$. P_R and $-P_R$ denote respectively the positive and negative remanent polarization, i.e. the two permanent polarization states which can be present in a ferroelectric memory cell and which can be used for representing logic "1" or "0" as is the case. V_S and $-V_S$ denote respectively the positive and negative coercive voltage. It is to be understood that when a polarization is given as a function of voltage, is this based on practical considerations. Generally voltage could be replaced by the electric field strength E and equally generally shall then E_C and $-E_C$ respectively denote the positive and the negative coercive field strength for the ferroelectric material. The voltage can then be calculated by multiplying the field strength with the thickness of the ferroelectric layer for a specific memory cell. The saturation polarizations P_S and $-P_S$ will be attained each time a memory cell is subjected to respectively nominal switching voltages V_S and $-V_S$ which exceed a coercive voltage V_C respectively $-V_C$. As soon as the applied electric field is removed, the ferroelectric material will relax and return to respectively one of the two remanent polarization states P_R and $-P_R$, herein also rendered as respectively the points 110 and 112 on the hysteresis curve. A change of the polarization direction, e.g. from the remanent positive polarization at point 110, takes place by applying a negative electric field

$-E_S$ or a negative voltage $-V_S$ which then respectively can be denoted as the switching field or the switching voltage, and the ferroelectric material will then be driven to the negative saturation polarization $-P_S$ and afterwards relax to the opposite polarization state $-P_R$. Correspondingly a positive switching field E_S or switching voltage V_S might change the negative polarization state $-P_R$ to P_R . The use of switching protocols of this kind which also is known as pulse protocols, determines the electric field by applying voltages to the electrodes in the memory matrix during the write and read operations.

Fig. 2 shows a matrix orthogonally crossing electrodes. According to standard terminology the horizontal electrodes of the row electrodes shall hereinafter be denoted as word lines 200, abbreviated WL, and vertically electrodes or column electrodes as bit lines 210, abbreviated BL. As shown in fig. 2a the matrix can be a matrix with m word lines WL and n bit lines BL such that it appears as an $m \cdot n$ matrix with of course then a total of $m \cdot n$ memory cells defined in the cross points between the word lines WL and bit lines BL. In fig. 2b there is shown a section of the matrix in fig. 2a and wherein memory cells 220 is indicated between the crossing word lines WL and bit lines BL. The ferroelectric material in the memory cell 220 then forms a dielectric capacitor-like structure with respectively a word line WL and bit line BL, e.g. 200 and 210, as electrodes. During the driving and detecting operation word lines 202 and bit lines 212 are activated to respectively active word lines AWL and active bit lines ABL. It can then be applied a voltage which is sufficiently high to switch the polarization direction of a given memory cell as shown in fig. 2b either to define a specific polarization direction in the cell, which conforms to a write operation, or for detecting or monitoring the set polarization direction, something which constitutes a read operation. The ferroelectric material or the ferroelectric layer located between the electrodes functions as mentioned above as a ferroelectric capacitor 222. The memory cell 220 is thus selected by setting the potentials of the associated word line 202 and bit line 212, i.e. the active word line AWL and the active bit line ABL such that the difference conforms to the nominal switching voltage V_S . Simultaneously it must be seen to that the remaining word lines and bit lines, for instance represented by 200 and 210 in fig. 2a and which crosses at memory cells 220, which are not to be addressed, shall be controlled in regard of electric

potential, such that so-called disturb voltages at non-addressed memory cells 220 are kept at a minimum.

As the method according to the present invention concerns ferroelectric memory devices and particularly wherein the ferroelectric memory material is a polymer, an example of a ferroelectric memory device of this kind shall be given in order to ease the understanding of its function.

Fig. 3 shows in a simplified block diagram form the structure and the functional elements of a matrix-addressable ferroelectric memory device which can be adapted for the purposes of the present invention and wherein e.g. the method according to the invention can be applied. The memory macro 310 comprising of a memory array or matrix 300, row and column decoders 32;302, sense amplifiers 306, data latches 308 and redundant word and bit lines 304;34. The row and column decoders 32;302 decode the addresses of memory cells, while sensing is performed by the sense amplifiers 306. Data latches 308 hold the data read until part or all of the data are transferred to the memory control logic or logic module 320. The data read from the memory macro 310 will have a certain bit error rate (BER) which can be reduced by replacing defective word and bit lines in the memory array 300 with redundant word and bit lines 304;34. In order to perform error detection the memory macro 310 may have data fields containing error correction code (ECC) information. The memory control logic 320 provides a digital interface for the memory macro 310 and controls the write and read operations on the memory array 300. Memory initialisation and logic for replacing defective bit and word lines with redundant word and bit lines 304;34 will be found in the memory control logic 320 as well. The device controller 330 for the memory device connects the memory control logic 320 to external bus standards. A voltage generator or charge pump mechanism 340 generates some of the voltages needed for writing and reading the memory cells. A separate clock input to the charge pump 340 from the device controller 330 via an oscillator (not shown), will be used by the charge pump 340 for generating voltages or perform charge pumping independently of the bit rate of the application using the memory macro 310.

As the method according to the present invention applies to the making of an electrode layer by thermal evaporation of an electrode material from an effusion cell, an example of how such an effusion cell is realized and works

shall now be given. In that connection an effusion cell shall be discussed in a generalized fashion, with reference to figure 4.

Fig. 4 shows an effusion cell 410 which comprises, among other, a crucible 420, heating elements 422, a housing 424, supports 426 and a cover 428.

5 During a work operation the crucible is filled with an evaporation source 430 of high-purity which is then evaporated onto the substrate 440. The crucible 420 may be of any desired shape and may be composed of any suitable refractory material such as graphite, tantalum, molybdenum or pyrolytic boron nitride. A set of supports 426 secures the crucible 420 inside the
10 housing 424. In order to evaporate the evaporation source 430 heating elements 422 are used. The number and location of the heating elements 422 may vary between various arrangements. Sometimes the heating elements 422 are placed in proximity to the opening of the crucible 420 such that condensation of evaporation source 430 in this area is avoided. The housing
15 424 and the cover 428 shield the surroundings from heat radiation. A thermoelement can be included within the housing 424 to keep track of the temperature and its development. The effusion cell 410 as well as the substrate 440 are here located within a vacuum chamber 400 which can be filled with a working gas, but also can be used for providing a vacuum
20 environment. The substrate 440 is mounted on a holder 442 which can be rotatable or not depending on the needs of the particular situation. This simplistic description may be complemented, if so desired, by the more detailed descriptions which are found in e.g. U.S. Patent No. 6,011,904 (Mattord) or U.S. Patent No. 6,162,300 (Bichrt), to which reference is made
25 without any of them having a limiting effect on the present invention in any way.

Specific and preferred embodiments of the method according to the invention for making an electrode layer in a ferroelectric memory device embodied as discussed in the foregoing, shall now be described in relation to the more
30 general problem connected with defects and deficiencies in the properties arising when an electrode layer is sputtered on the top of a memory layer made of a polymer material. Particularly these defects and deficiencies in the properties shall appear in the form of a memory material with poor polarization properties and poor fatigue endurance, i.e. a tendency of loosing
35 polarization and that the remanent polarization value decreases (for instance with an increasing number of switching cycles, reversal of the polarization

directions and generally due to disturb voltages and stray capacitances in the memory cell array).

According to the invention it is generally proposed to solve the problem with damages on a ferroelectric memory layer, above all a memory layer of ferroelectric polymer, by thermally evaporating the electrode metal from an effusion cell onto the ferroelectric memory layer. This presupposes that the ferroelectric memory device can be made by different depositing methods. Spin coating is the best-suited and usual method for applying a ferroelectric memory layer of polymer material. The bottom electrode set can still be sputtered, as the silicon substrate can be regarded as being thermally compatible with the process and hence shall not be damaged. However, the upper electrode set must be evaporated to avoid damaging the memory material, e.g. a ferroelectric polymer material which has a relatively low melting point, typically in the order of about 200°C.

Fig. 5 shows schematically in cross section a ferroelectric memory cell. It is formed on a substrate 500 and comprises a first or bottom electrode 510, a first ferroelectric layer 520, and a second or upper electrode 530. In a first preferred embodiment the substrate 500 consists of a silicon layer 502 and on this a silicon dioxide isolation layer 504 which are made in an as per se known manner. Sputtering is used to deposit the first or bottom electrode 510. A number of metals is suitable as electrode material, but titanium is preferably used. In order to deposit the polymer ferroelectric layer 520 by spin coating as usually employed, the device, i.e. the substrate and the electrodes, must be transferred from one manufacturing equipment to another. During this transfer oxidization of the electrodes takes place and the electrode 510 shall thereby consist of a first metal layer 512 and a first metal oxide layer 514 thereon. This is, however, a not unwanted effect, since the first metal oxide layer 514 may function as a barrier layer, preventing diffusion, or as an adhesion layer preventing separation that might lead to a reduced fatigue endurance or contact faults. The first ferroelectric layer 520 is then formed by spin-coating a polymer on top of the bottom electrode 510. Following this, a method according to the present invention is used to deposit the second or upper electrode 530 by means of thermal evaporation. Again a number of metals is suitable, but titanium is preferably used. In order to form a second metal oxide layer 534 in the second electrode layer 530 and similar to the first metal oxide layer 514 in the first electrode layer 510 such that the

second metal oxide layer 534 contacts the first ferroelectric layer 520 and functions as adhesion layer or offers other functionalities, the vacuum chamber 400 is filled with a working gas during the operation. This working gas includes at least either oxygen or nitrogen. In the case of oxygen used as
5 a working gas there will be formed, on top of the first ferroelectric layer 520, a layer of titanium oxide, titanium dioxide or a combination of titanium oxide and titanium dioxide. Once the second metal oxide layer 534 has reached a sufficient thickness the gas pressure is reduced and the thermal evaporation process continues resulting in a pure metal layer 532 being formed on the
10 oxide layer 534. Again, the device is transferred to another manufacturing equipment and a second metal oxide layer 536 is formed on the top of the metal layer 532.

The working gas is kept at a pressure between 10^{-3} and 10^{-6} Torr when forming the second metal oxide layer 534. The gas pressure during the
15 remainder of the thermal evaporation process is sufficiently low to avoid the formation of oxides, but high enough to allow for a fast deposition rate in the process step for forming the second metal layer 532. There is a trade-off between the required purity of the second metal layer 532 and the time required to evacuate the vacuum chamber 400 or reduce the pressure therein
20 to achieve the desired low gas pressure. As mentioned, the working gas may include either oxygen or nitrogen gas. One option is to use only oxygen gas. Another option is to use a mixture of oxygen and nitrogen gas. In the case of a mixture, the oxygen content is kept below 50% by volume and the nitrogen content consequently above 50% by volume. Preferably the oxygen content
25 of the mixture is between 15% to 25% by volume. In certain embodiments the working gas may have further gaseous components.

For thermal evaporation a crucible 420 preferably made from carbon in its graphite form is used. It is filled with an evaporation source 430 which can be selected among a number of suitable metals, but preferably titanium of
30 high purity is used. During the evaporation operation the crucible 420 will be heated to between 1600 and 1900 degrees centigrade.

The method according to the first preferred embodiment can be implemented with different variants. It is possible to use a substrate 500 with a silicon layer 502, but without the silicon dioxide layer 504. Similarly, the first
35 electrode 510 can consist of more than one first metal layer 512 or more than

one first metal oxide layer 514 if necessary, and these layers 512, 514 then can be provided in any suitable order. This can be achieved by successive deposition processes with different metals or by changing the working gas of e.g. an effusion process. Corresponding processual considerations may also be applied to the second electrode 530.

A second preferred embodiment is based on the same process steps as in the first preferred embodiment and comprises in addition some further steps. After depositing the first electrode 510, the first ferroelectric layer 520 and the second electrode 530 in succession on the substrate 500, the deposition process can continue, as shown in figure 6, with a second ferroelectric layer 600, a third electrode 602 and a first dielectric interlayer 604. A ferroelectric memory device with stacked memory cells can be built in this manner with as many memory cells as desired or as practical to realize. The first electrode 510 and the second electrode 530 are arranged such that potential differences can be applied between them and hence influence the polarization response of the first ferroelectric layer or memory material 520. Likewise the second electrode 530 and the third electrode 602 are provided such that potential differences applied between them can be used for influencing the polarization response of the second ferroelectric layer 600. Insulation before depositing further sets of electrodes and ferroelectric layers is provided by the dielectric interlayer 604. Now further ferroelectric memory cells in the stack can be formed, e.g. by continuing with the fourth electrode 606, a third ferroelectric layer 608, a fifth electrode 610, a fourth ferroelectric layer 612, a sixth electrode 614 and another dielectric interlayer 616. The fourth electrode 606 and the fifth electrode 610 are arranged in such a manner that potential differences may be applied therebetween and effect a polarization response of the third ferroelectric layer 608, while correspondingly the fifth electrode 610 and the sixth electrode 614 being formed such that potential differences can be applied therebetween and the polarization response of the fourth ferroelectric layer 612 influenced. Again, a required insulation is provided by the second dielectric interlayer 616 in case further memory cells are deposited and formed in the stack.

Particularly and in a third preferred embodiment it is regarded as practical that the steps of the method according to the present invention are repeated until the ferroelectric memory device comprises 12 electrodes, 8 ferroelectric layers and 4 insulation layers in the form of dielectric interlayers. Then a

thirteenth electrode can be deposited in order to provide electrical contact between different locations in the ferroelectric memory device.

By employing the method according to the present invention it will be possible to manufacture a memory device with a high integration density in a volumetric or three-dimensional architecture. In commonly known
5 embodiments there are for each ferroelectric memory layer used two sets of electrodes, viz. bottom and top electrodes, and in addition insulating dielectric interlayers. For a memory device with 8 ferroelectric layers of memory layers this implies 16 electrode layers and 8 dielectric layers or
10 insulation layers, a total of 32 layers. By using an embodiment wherein the top electrode of the first memory layer forms the bottom of the second memory layer etc., 8 ferroelectric layers shall only require 9 electrode layers and possibly an insulating layer on the top, a total of eighteen layers. Thus a device with a total of 18 layers is obtained, but with the disadvantage that
15 addressing of memory cells cannot take place to all ferroelectric layers simultaneously i.e. in parallel, but at most to every second, and further with the additional disadvantage that the possibility of sneak currents and undesired capacitive couplings increases. The memory device according to the present invention provides a compromise and shall for 8 memory layers
20 comprise a total of 24 layers, but with improved addressing possibilities as the use of 4 isolation layers or interlayers offers a better protection against undesired couplings, e.g. stray capacitances, between the memory layers in the volumetric structure. Realized with the method according to the present invention there is further achieved that the top electrodes of the ferroelectric
25 layer or a memory layer can be deposited without damaging the ferroelectric memory material in the deposition process, something which is of essential importance when it is formed of a low melting point material such as a ferroelectric polymer.

CLAIMS

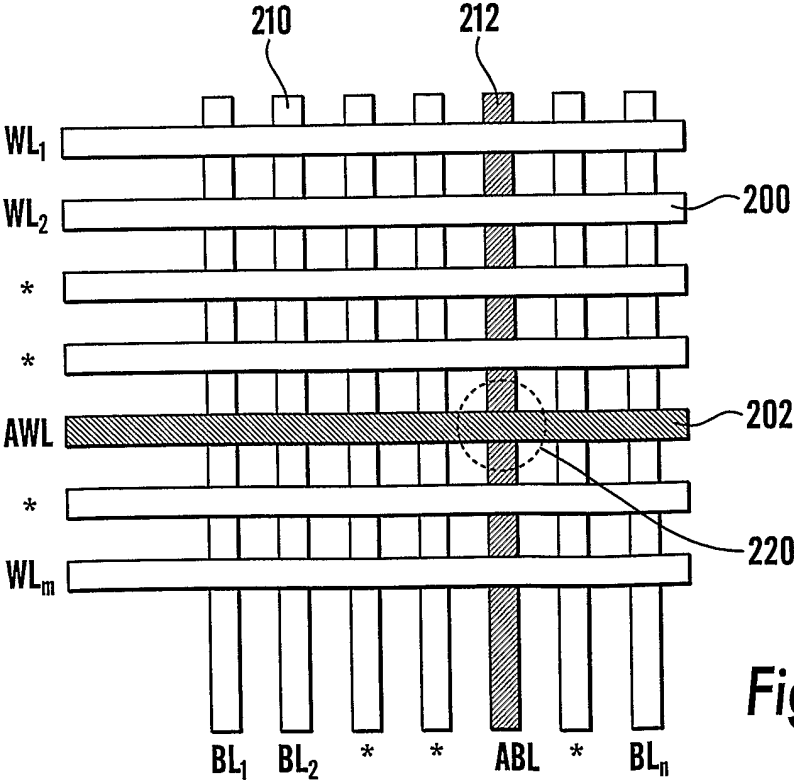
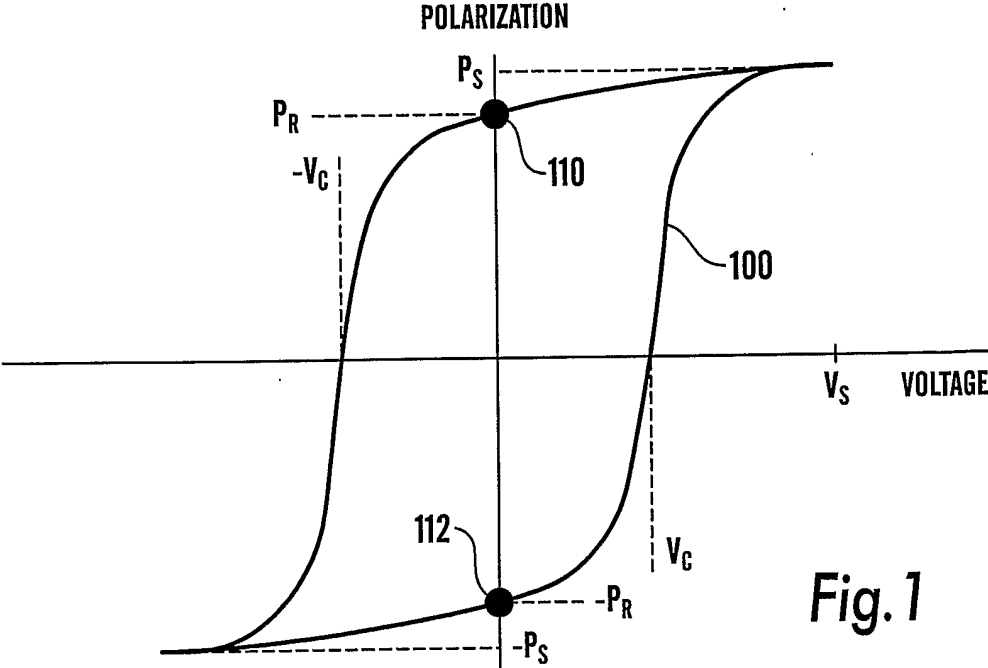
1. A method for making a ferroelectric memory cell, comprising steps for
(a) providing a substrate consisting of a silicon layer, and optionally a silicon
dioxide isolation layer;
5 (b) forming a first electrode comprising at least one metal layer and at least
one metal oxide layer, and providing said first electrode adjacent to said
substrate and in contact with said silicon layer or said optional silicon
dioxide isolation layer;
(c) forming a first ferroelectric layer consisting of a polymer ferroelectric
10 thin film, and providing said first ferroelectric layer adjacent to and in
contact with said first electrode; and
(d) forming a second electrode comprising at least one metal layer and at
least one metal oxide layer, and providing said second electrode adjacent to
and in contact with said first ferroelectric layer, the method being
15 characterized by step (d) further comprising
forming one of said at least one metal oxide layer by placing said substrate,
said first electrode and said first ferroelectric layer in a vacuum chamber,
providing a high-purity evaporation source in an effusion cell, said effusion
cell being provided in said vacuum chamber, evaporating thermally said
20 high-purity evaporation source from said effusion cell onto the surface of
said first ferroelectric layer while supplying a working gas at a first gas
pressure; and forming one of said at least one metal layer by evaporating
thermally said high-purity evaporation source from said effusion cell onto the
surface of said at least one metal oxide layer while maintaining a second gas
25 pressure.
2. A method according to claim 1, characterized by said high-purity
evaporation source being high-purity titanium.
3. A method according to claim 2, characterized by said at least one
metal layer of said second electrode being a layer of titanium and said at least
30 one metal oxide layer of said second electrode being a layer of titanium
oxide, titanium dioxide or a combination of titanium oxide and titanium
dioxide.
4. A method according to claim 3, characterized by said working gas
being oxygen gas.

5. A method according to claim 1, characterized by said working gas being a gas mixture of at least oxygen gas and nitrogen gas.
6. A method according to claim 5, characterized by the oxygen gas constituting less than 50% of said working gas by volume and the nitrogen gas constituting more than 50% of said working gas by volume.
7. A method according to claim 6, characterized by the oxygen gas constituting 15 to 25% of said working gas by volume.
8. A method according to claim 1, characterized by said first gas pressure in said vacuum chamber being between 10^{-3} and 10^{-6} Torr.
9. A method according to claim 2, characterized by said effusion cell comprising a crucible made from carbon in its graphite form.
10. A method according to claim 10, characterized by said crucible being heated to between 1600 and 1900 degrees centigrade during the thermal evaporation of said high-purity evaporation source.
11. A method according to claim 1, characterized by further comprising steps for
- (e) forming a second ferroelectric layer consisting of a polymer ferroelectric thin film, said second ferroelectric layer being provided adjacent to and in contact with said second electrode;
- (f) forming a third electrode comprising at least one metal layer and at least one metal oxide layer by thermal evaporation, said third electrode being provided adjacent to and in contact with said second ferroelectric layer;
- (g) forming a first dielectric interlayer consisting of a dielectric material, said first dielectric interlayer being provided adjacent to and in contact with said third electrode; and
- (h) repeating steps (a) through (g) at least once.
12. A method according to claim 12, characterized by step (h) being repeated three times, and further comprising a step for
- (i) forming a thirteenth electrode comprising at least one metal layer and at least one metal oxide layer, said thirteenth electrode being electrically connected to at least two of the other electrodes.
13. A ferroelectric memory device comprising ferroelectric memory cells capable of storing data in either one of at least two polarization states when

no electric field is applied to the memory cells, wherein the ferroelectric memory device comprises at least one ferroelectric layer (520) formed by a polymer ferroelectric thin film and at least a first set and a second set of respective parallel electrodes (510;530), wherein the electrodes (510) of the first set are provided in substantially orthogonal relationship to the electrodes (530) of said second set, said first set and second set of electrodes (510;530) contacting ferroelectric memory cells at opposite surfaces of said at least one polymer ferroelectric layer (520), and wherein at least the first set and second set of electrodes (510;530) are adapted to read, refresh or write ferroelectric memory cells by applying appropriate voltages thereto, characterized in that said first set of electrodes (510) comprises at least one metal layer (512) and at least one metal oxide layer (514), said first set of electrodes (510) being provided adjacent to a substrate (500) and in contact with a silicon layer (502), or optionally, a silicon dioxide isolation layer (504), that said second set of electrodes (530) comprises at least one metal layer (532) and at least one metal oxide layer (534), said second set of electrodes (530) being provided adjacent to and in contact with a ferroelectric layer (520), and that said second set of electrodes (530) is formed in a vacuum chamber (400) by thermally evaporating a high-purity evaporation source (430) from an effusion cell (410) onto the surface of said ferroelectric layer (520) while providing a working gas at respectively a first and a second gas pressure.

14. A ferroelectric memory device according to claim 13, characterized in comprising three or more sets of electrodes (510,530,602,...), and at least two ferroelectric layers (520,600,...), each set of electrodes (510,530,602,...) being provided adjacent to and in contact with at least one ferroelectric layer (520,600,...) and each ferroelectric layer (520,600,...) being provided between and in contact with two sets of electrodes (510,530;530,602;...).

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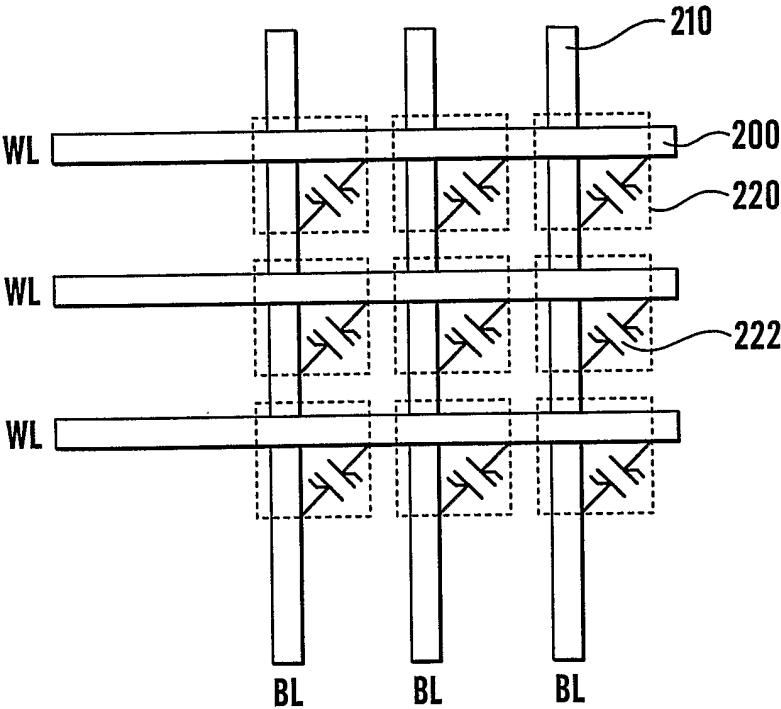


Fig.2b

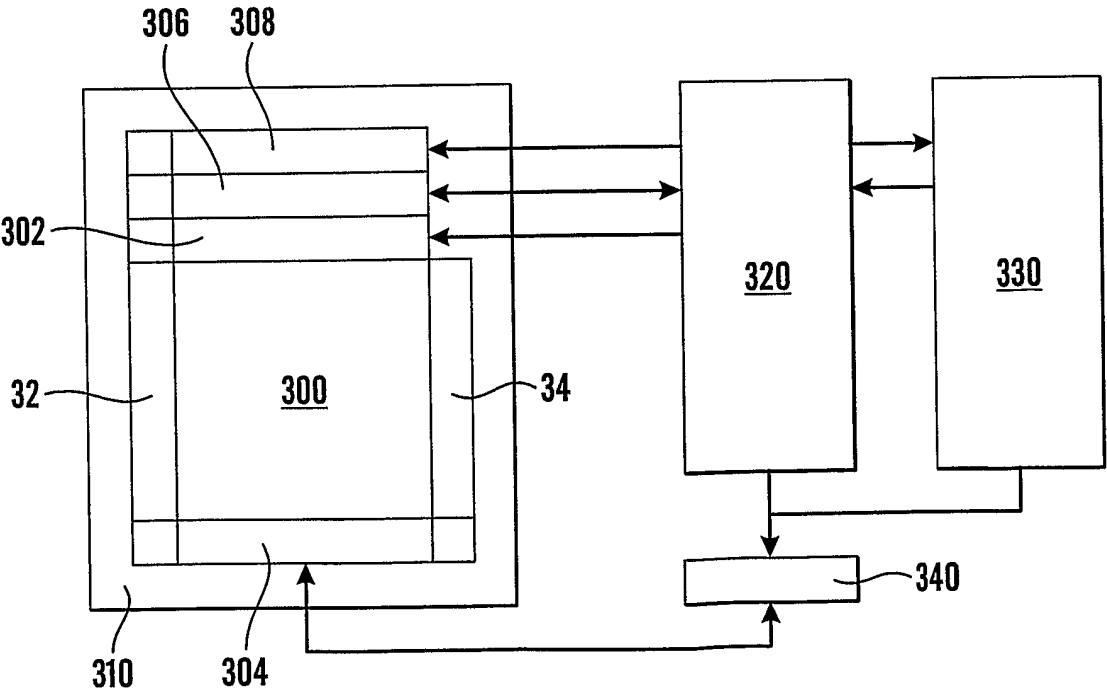


Fig.3

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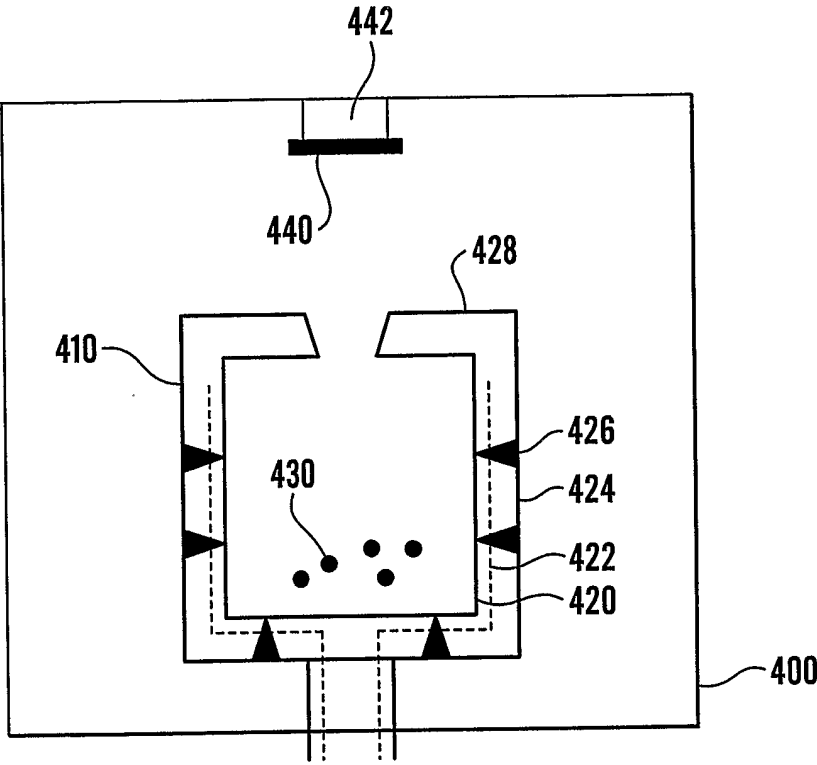


Fig.4

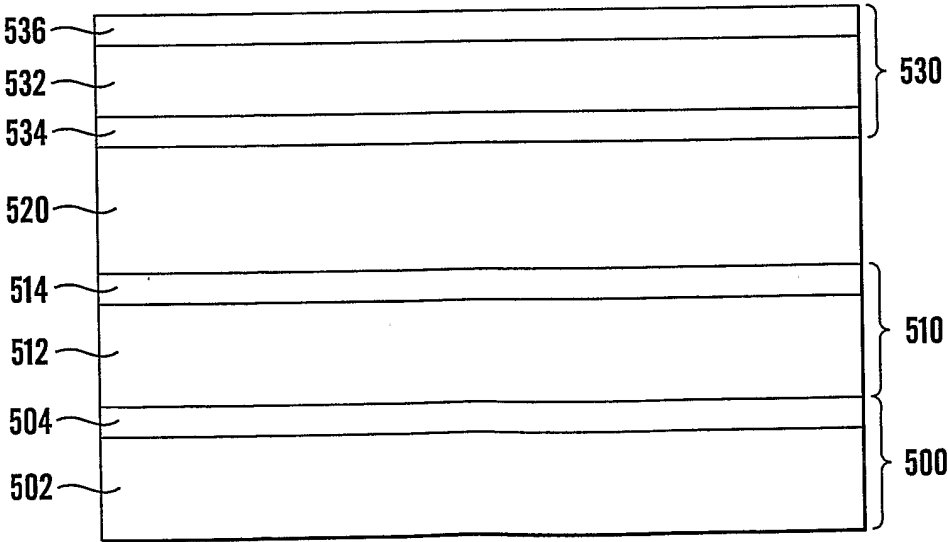


Fig.5

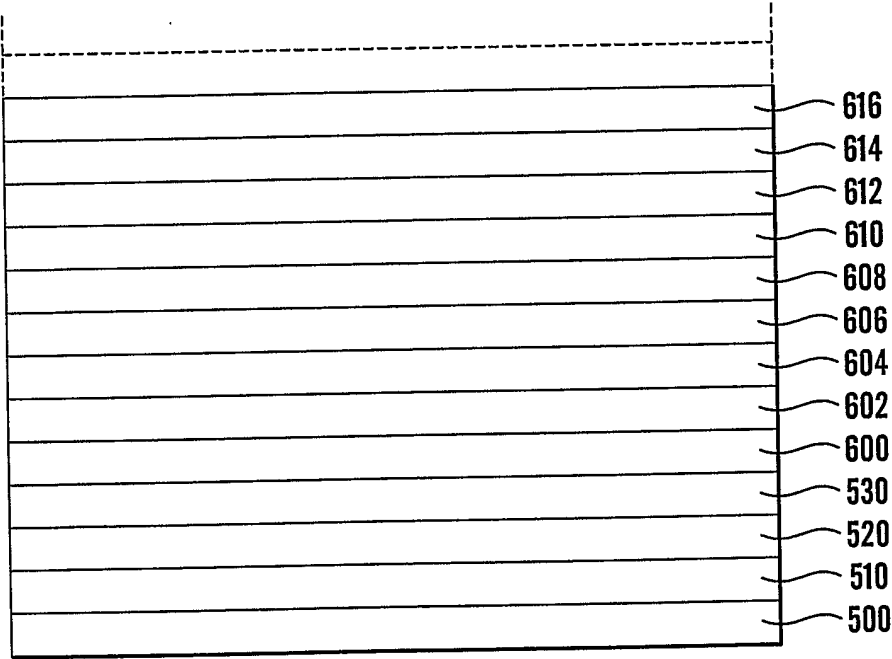


Fig.6

INTERNATIONAL SEARCH REPORT

International application No.

PCT/NO 03/00198

A. CLASSIFICATION OF SUBJECT MATTER

IPC7: G11C 11/22, C23C 14/24, H01L 21/285

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC7: G11C, C23C, H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WPI DATA, EPO-INTERNAL; PAJ, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	PATENT ABSTRACTS OF JAPAN Vol. 0186, no 31 30 November 1994 (1994-11-30) & JP 6243519 A (SHIGERU SAGAI) 2 September 1994 (1994-09-02) abstract --	1-14
A	WO 0001000 A1 (MATSUSHITA ELECTRONICS CORPORATION), 6 January 2000 (06.01.00), abstract --	1-14
A	US 6359289 B1 (STUART STEPHEN PAPWORTH PARKIN), 19 March 2002 (19.03.02), abstract -- -----	1-14

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

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Date of the actual completion of the international search

Date of mailing of the international search report

10 October 2003

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INTERNATIONAL SEARCH REPORT

Information on patent family members

06/09/03

International application No.

PCT/NO 03/00198

Patent document cited in search report			Publication date	Patent family member(s)		Publication date
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				EP	1099242 A	16/05/01
				JP	2002519864 T	02/07/02
				TW	449794 B	00/00/00
				US	6384946 B	07/05/02
				US	6541375 B	01/04/03

US	6359289	B1	19/03/02	NONE		
