Abstract: An integrated circuit die (10) comprises a stack of a substrate and multiple layers (31, 32, 33) extending in parallel to the substrate. A number of integrated electronic components is formed in the stack, and connected to form an electronic circuit. The electronic circuit comprises a first electric contact (11) coupled to one or more of the integrated electronic components, a second electric contact (12) coupled to one or more of the integrated electronic components, and a coupling which couples the electric strips electrically to each other. The coupling comprises a circuit via (21) which extends through at least two of the layers. The integrated circuit die further comprises an integrated current sensor for sensing a current flowing through at part of the electronic circuit, the current sensor comprises a coil arrangement provided in the stack. The coil arrangement is magnetically coupled to the circuit via (21) over at least a part of a length of the circuit via to sensing a magnetic flux generated by a current through the circuit via. A measurement unit (52) can measure a parameter of the coil arrangement representative of a current flowing through the circuit via.
Title: Integrated circuit with integrated current sensor

Description

Field of the invention

This invention relates to a multi-layered integrated circuit comprising a current sensor.

Background of the invention

Palmer, P.R.; Stark, B.H.; Joyce, J.C.; "Noninvasive measurement of chip currents in IGBT modules," Power Electronics Specialists Conference, 1997. PESC '97 Record., 28th Annual IEEE , vol.1, no., pp.166-1 7 1 discloses a method to measure currents in an IGBT (Insulated Gate Bipolar Transistor). The method uses an external miniature probe consisting of two coils of ten windings each, wound onto a plastic former. The miniature probe is positioned in an IGBT module with multiple IGBTs, with one probe per IGBT to measure the current into the respective IGBT.

However, a disadvantage of the known method is that the probe is not suitable to measure currents inside multi-layered integrated circuits.

Summary of the invention

The present invention provides a multi-layered integrated circuit as described in the accompanying claims. Specific embodiments of the invention are set forth in the dependent claims. These and other aspects of the invention will be apparent from and elucidated with reference to the embodiments described hereinafter.

Brief description of the drawings

Further details, aspects and embodiments of the invention will be described, by way of example only, with reference to the drawings. Elements in the FIG.s are illustrated for simplicity and clarity and have not been drawn to scale.

FIG. 1 schematically shows a partially sectional perspective view of part of an example of an integrated circuit with a current sensor.

FIG. 2 schematically shows a cross sectional view the example of FIG. 1, taken along the line II-II in FIG. 3.

FIG. 3 schematically shows a sectional view of the example of FIG. 1, taken along the line III-II I in fig. 2.

FIG. 4 schematically shows a sectional view of elements of the example of FIG. 1, taken along the line IV-IV in fig. 2.

FIG. 5 schematically shows the same view as FIG. 4, but with hidden elements indicated with dashed lines.

FIG. 6 shows exemplary signals obtained by the example of FIG. 1.
Detailed description of the preferred embodiments

Because the integrated circuit implementing the present invention is, for the most part, composed of electronic components and circuits known to those skilled in the art, circuit details will not be explained in any greater extent than that considered necessary for the understanding and appreciation of the underlying concepts of the present invention and in order not to obfuscate or distract from the teachings of the present invention.

FIG. 1 schematically shows a partially sectional perspective view of part of an integrated circuit 10 with a current sensor. The integrated circuit 10 may be provided as a bare die or as an packaged integrated circuit which comprises an integrated circuit package and one or more integrated circuit dies provided in the packaged and connectable to the outside of the package through suitable connects.

An integrated circuit 10 is a configuration of electronic components on a single die that forms an electronic circuit, such as a logic circuit and analog or mixed signal circuit. The integrated circuit 10 of FIG. 1 comprises comprises a stack of a substrate 30 and multiple layers 31, 32, 33 extending in parallel to the substrate. The layers 31, 32, 33 are made of semiconductor material, such as silicon and can comprise, e.g., doped regions, implanted ions, insulator elements and electric strips for being able to carry out the various functions an integrated circuit 10 may have. In this example, the integrated circuit 10 comprises three layers 31, 32, 33, but more layers of active electronic components may be integrated both vertically and horizontally into a single integrated circuit 10.

A number of integrated electronic components (not shown), such as transistors, resistors, capacitors, diodes or otherwise, can be formed in the stack and be connected to form an electronic circuit. As shown in FIG. 2, the electronic circuit can comprise a first electric contact 11 coupled to one or more of the integrated electronic components, and a second electric contact 12 coupled to one or more of the integrated electronic components. The electric strips can be coupled electrically to each other via a coupling which comprises a circuit via 21 which extends through two or more of the layers 31-33. It is to be noted that the circuit via 21 may cross more layers. The circuit via 21 may for example extent through a stack of component layers, of interconnect layers or of a mixture thereof (e.g. the stack comprising at the bottom closest to the substrate one or more component layers and one or more interconnect layers on top thereof, and the circuit via extending through at least one of the component layers and at least one of the interconnect layers)

The integrated circuit die 10 further comprises an integrated current sensor for sensing a current flowing through at least a part of the electronic circuit. The current sensor is provided for, e.g., detecting high dynamic (> 1 MHz) currents flowing into the integrated components or for detecting electrostatic discharge (ESD) or electromagnetic interference. With the current sensor integrated on the same die as the other electronic components of the integrated circuit, the currents to be detected can be measured with high accuracy.

The current sensor comprises a coil arrangement 13,14,22 provided in the stack, as explained below in more detail. The coil arrangement is magnetically coupled to the circuit via 21 over at least a part of a length of the circuit via 21 to sense a magnetic flux generated by a current
through the circuit via 21. The current sensor is arranged to detect currents 15 running through this
circuit via 21 inside the integrated circuit 10. When the electrical current 15 running through the
circuit via 21 generates or changes a magnetic field 51 inside the integrated circuit 10, this can be
sensed using this magnetic sensor. The galvanic isolation between the sensor (metal elements 13, 14 and sensor vias 22) and the current path (metal elements 11, 12 and circuit via 21) limit the
disturbance that other types of current sensors may encounter.

As shown in FIG.2 and 3, a measurement unit 52 can be connected to the coil arrangement
to measure a parameter of the coil arrangement, e.g. the voltage difference between two different
points or the current flowing through the coil arrangement, representative of a current flowing
through the circuit via. In the shown example, the voltage that is induced in the coil is proportional
to the rate of change (derivative) of current in the circuit via 21, and the measurement unit 52 is a
voltage meter suitably connected to measure the voltage difference between the beginning and the
end of the coil, as respectively indicated with points 43,44 in the FIGs..

It will be apparent that the parameter sensed by the integrated current sensor may be
treated before or after being received by the measurement unit 52. The integrated circuit die 10
may for example further comprise an integrator for integrating the voltage.

The coil arrangement can be any arrangement suitable for the specific implementation. In
the example of FIG. 1, the coil is a curved coil which operates as a Rogowski coil. The curved coil
extends along a path curved around the longitudinal axis of the circuit via 21 over at least a part of
the circumference of the circuit via 21. In this example, the path is in a plane perpendicular to the
longitudinal axis. The coil encloses the circuit via 21 in circumferential direction and forms a loop
around the circuit via 21.

The coil comprises several windings, and has a toroidal helix like shape. From FIG.3, it can
be seen how an electrically conductive path is present that runs through an electric strip 13 in the
first plane 41 to a sensor via 22, to a electric strip 14 in the second plane 42, to another sensor via
22, to a further electric strip 13 in the first plane 41 and so on, thus having several windings. At the
outer ends of the coil arrangements two metal pads 18 are coupled to electric strips 13, 14 in the
first and/or second plane 41, 42. The voltage measurement unit 52 is coupled to these metal pads
18. In this example, the metal pads 18 are placed in the same planes 41, 42 as the electric strips
13, 14 they are coupled to, however they may be placed in a different plane and e.g. be coupled
through further vias to the other electric strips 13, 14. The two metal pads 18 may be placed at
different depths inside the integrated circuit 10.

The coil arrangement comprises a first plurality of electric strips 13 distributed around the
circuit via 21 in a first plane 41, the first plane being non-parallel to a longitudinal axis of the circuit
via. The arrangement further has a second plurality of electric strips 14 distributed around the via
21 in a second plane 42, the second plane being non-parallel to the longitudinal axis of the circuit
via, the second plane 42 being in a longitudinal direction of the circuit via at a distance from the first
plane 41. A plurality of sensor vias 22 is present. Each sensor via 22 electrically couples an electric
contact 13 of the first plurality to a electric contact 14 of the second plurality in such a way that the
first plurality of electric strips 13, the second plurality of electric strips 14 and the sensor vias 22
together form a winding of the coil arrangement. Although the shown example has less than ten windings, more specifically eight, it has been found that this allows a simple yet sensitive sensor to be obtained.

In the shown example, the first and second planes 41,42 are separated by a single layer 32. However, the first plane 41 and the second plane 42 may be separated by more than one layer. It is also possible to use a third and fourth, or even more, planes with electric strips for constituting the coil arrangement

As can be seen in FIGs. 2 and 3, each winding comprises an electronically conducting, e.g. metal, first strip 13 in a first plane 31 which extends in radial direction of the coil (and of the circuit via), from an inner circumference of the coil to an outer circumference of the coil. The winding further comprises an electronically conducting, e.g. metal, second strip 14 in a second plane 33 above the first plane which extends in radial direction of the coil (and of the circuit via), from an inner circumference of the coil to an outer circumference of the coil.

The strips 13,14 may be provided in metallization layers. In such case, the layers 31-33 may comprise a sub-stack of dielectric layers in which two or more metallization layers are patterned, each of the metallization layers comprises one or more interconnects for integrated electronic components, and the coil arrangement comprises one or more first metal path extending in one of the metallization layers and a second metal path extending in another of the metallization layers, the metal paths being electrically isolated from the one or more interconnect.

As show, and particularly derivable from FIG. 3, the windings are spaced in tangential direction, and the windings are arranged in a radial pattern. The strips 13,14 of the arrangement are arranged in a star-like pattern, which zig-zags in a radial direction between a distal point and a proximal point (relative to a longitudinal axis of the circuit via 21).

The first strip 13 and the second strip 14 are connected to each other at a distal end (with respect to the circuit via 21), in this example through a sensor via 22 extending through the layers separating the first and second strip. The first strip 13 is further connected to a second strip of a preceding winding at a proximal end (with respect to the circuit via 21) in this example through a sensor via 22 extending through the layers between the first and second strip 13,14. The second strip 14 is further connected to a first strip 13 of a following winding at a proximal end (with respect to the circuit via 21), in this example through a sensor via 22 extending through the layers between the first and second strip 13,14.

As shown, the first strip 13 and the second strip 14 are positioned in circumferential direction (of the circuit via 21) adjacent to each other. In the FIGs, the strips have no overlap thereby reducing the capacitive effects. However, the drawings represent an idealized case, in an actual implementation some overlap may be present. The integrated circuit die 10 thus comprises a first radial pattern (of the first strips) and a second radial pattern (of the second strips) separated from the first radial pattern by one of more of the layers 31-33, i.e. positioned in the longitudinal direction of the circuit via at a distance from the first radial pattern. The strips of the first radial pattern are, in a circumferential direction of the circuit via, interdigitated between the strips of the second radial pattern.
The integrated circuit can be used in a method of manufacturing electronic circuits. The method may, for example, comprise manufacturing a multiple of integrated circuits using a set of wafers. Of one or more wafers one or more integrated circuit dice provided with an integrated current sensor comprising a coil arrangement may be manufactured. The integrated current sensor of the integrated circuit die may then be used to perform tests of one or more of: the electronic circuit of the integrated circuit die, the wafer provided with the integrated circuit die, other wafers of the set.

FIG. 6 shows exemplary signals 58, 59 obtained by the current sensor of FIGs. 1-5. The upper diagram shows an exemplary course of the signal 58 measured by voltage measurement unit 52. At t=t₁, a 100 ns TLP (Transmission Line Pulse) current 15 is injected into the integrated circuit. The magnetic fields 51 caused by this current 15 are detected by the integrated magnetic sensor. The voltage 58 shows a clear peak when the current suddenly increases (t=t₁) and a less clear peak when it decreases (t=t₂). In between t₁ and t₂, the constant current through the circuit via 21 does not change the magnetic field 51 and no sensor signal 58 does not show a significant amplitude. The exemplary sensor signal 58 in the upper diagram shows that the current sensor is indeed capable of detecting currents 15 running through the circuit via 21.

In the lower diagram, a signal 59 is shown which is obtained by integrating the signal from the voltage measurement unit 52 over time. The integration may be performed computationally, based on the signal values 58 from the upper diagram. Alternatively, the integration may be performed electronically using a voltage integrator.

In the foregoing specification, the invention has been described with reference to specific examples of embodiments of the invention. It will, however, be evident that various modifications and changes may be made therein without departing from the scope of the invention as set forth in the appended claims, and that the claims are not limited to the specific examples described hereinabove. For example, the connections may be of type of connection suitable to transfer signals from or to the respective nodes, units or devices, for example via intermediate devices. Accordingly, unless implied or stated otherwise the connections may for example be direct connections or indirect connections.

The semiconductor substrate described herein can be any semiconductor material or combinations of materials, such as gallium arsenide, silicon germanium, silicon-on-insulator (SOI), silicon, monocrystalline silicon, the like, and combinations of the above.

In the claims, any reference signs placed between parentheses shall not be construed as limiting the claim. The word 'comprising' does not exclude the presence of other elements or steps then those listed in a claim. Furthermore, the terms "a" or "an," as used herein, are defined as one or more than one. Also, the use of introductory phrases such as "at least one" and "one or more" in the claims should not be construed to imply that the introduction of another claim element by the indefinite articles "a" or "an" limits any particular claim containing such introduced claim element to inventions containing only one such element, even when the same claim includes the introductory phrases "one or more" or "at least one" and indefinite articles such as "a" or "an." The same holds true for the use of definite articles. Unless stated otherwise, terms such as "first" and "second" are
used to arbitrarily distinguish between the elements such terms describe. Thus, these terms are not necessarily intended to indicate temporal or other prioritization of such elements. The mere fact that certain measures are recited in mutually different claims does not indicate that a combination of these measures cannot be used to advantage.
Claims

1. An integrated circuit die (10), comprising:
   a stack of a substrate (30) and multiple layers (31, 32, 33) extending in parallel to the
   substrate;
   a number of integrated electronic components formed in the stack, and connected to form an
   electronic circuit;
   the electronic circuit comprising a first electric contact (11) coupled to at least one of said
   integrated electronic components, a second electric contact (12) coupled to at least one of said
   integrated electronic components, and a coupling which couples said electric strips electrically to
   each other, said coupling comprising a circuit via (21) which extends through at least two of said
   layers;
   the integrated circuit die further comprising an integrated current sensor for sensing a current
   flowing through at least a part of said electronic circuit, the current sensor comprising a coil
   arrangement provided in said stack, which coil arrangement is magnetically coupled to the circuit
   via (21) over at least a part of a length of the circuit via to sense a magnetic flux generated by a
   current through the circuit via, and a measurement unit (52) for measuring a parameter of said coil
   arrangement representative of a current flowing through said circuit via.

2. An integrated circuit die (10) as claimed in claim 1, wherein said coil is a curved coil, the curved
   coil extending along a path curved around a longitudinal axis of the circuit via (21) over at least a
   part of the circumference of the circuit via, and wherein the measurement unit is a voltage
   measurement unit (52) for measuring a voltage between a first point (43) and a second point (44) in
   the curved coil.

3. An integrated circuit die (10) as claimed in claim 2, wherein the coil arrangement comprises a
   toroidal helix.

4. An integrated circuit die (10) as claimed in any one of the preceding claims, further comprising
   an integrator for integrating the voltage.

5. An integrated circuit die (10) as claimed in any one of the preceding claims, wherein the coil
   arrangement zig-zags in a radial direction relative to a longitudinal axis of the circuit via.

6. An integrated circuit die (10) as claimed in any one of the preceding claims, wherein the coil
   arrangement comprises:
      a first plurality of electric strips (13) distributed around the circuit via (21) in a first plane (41),
      the first plane being non-parallel to a longitudinal axis of the circuit via;
a second plurality of electric strips (14) distributed around the via (21) in a second plane (42),
the second plane being non-parallel to the longitudinal axis of the circuit via, the second plane (42)
being in a longitudinal direction of said circuit via at a distance from the first plane (41);
a plurality of sensor vias (22), each sensor via (22) electrically coupling a electric contact (13)
of the first plurality to a electric contact (14) of the second plurality in such a way that the first
plurality of electric strips (13), the second plurality of electric strips (14) and the sensor vias (22)
together form the coil arrangement.

7. An integrated circuit die (10) as claimed in claim 6, wherein the coil arrangement further
comprises:

7. An integrated circuit die (10) as claimed in any one of the preceding claims, wherein the coil
arrangement comprises:

7. An integrated circuit die (10) as claimed in any one of the preceding claims, wherein the coil
arrangement comprises:

a number of longitudinal, electrically conducting, elements arranged in a radial pattern
around said circuit via.

8. An integrated circuit die (10) as claimed in claim 8, comprising a first radial pattern and a
second radial pattern positioned in the longitudinal direction of the circuit via at a distance from the
first radial pattern, and the elements of the first radial pattern being, in a circumferential direction of
said circuit via, interdigitated between the elements of the second radial pattern.

9. An integrated circuit die (10) as claimed in any one of the preceding claims, wherein the
layers comprise a sub-stack of dielectric layers in which at least two metallization layers are
patterned, each of said metallization layers comprising at least one interconnect for integrated
electronic components, and the coil arrangement comprises at least one first metal path extending
in one of said metallization layers and a second metal path extending in another of said
metallization layers, said metal paths being electrically isolated from the at least one interconnect.

11. An integrated circuit, comprising: an integrated circuit package and an integrated circuit die as
claimed in any one of the preceding claims provided in said package.

12. A method of manufacturing electronic circuits, comprising using a set of wafers, providing at
least one wafer of said set with an integrated circuit die as claimed in any one of claims 1-10 and
using the integrated current sensor of the integrated circuit die to perform tests of at least one of:
the electronic circuit of the integrated circuit die, the wafer provided with the integrated circuit die,
other wafers of the set.
FIG. 6
A. CLASSIFICATION OF SUBJECT MATTER

HOIL 23/48(2006.01)i, HOIL 25/065(2006.01)i, HOIL 21/66(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

HOIL 23/48; GOIR 33/00; HOIL 23/34; G01R 33/09; G01R 33/07; H03F 3/60; H01L 27/04; G01R 33/06; G01R 1/20; H01L 25/065; H01L 21/66

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: current sensor, IC, coil, magnetic, inside, measurement

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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<th>Category</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No.</th>
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<tr>
<td>A</td>
<td>US 2006-0027917 AI (FRANZ WACHTER) 09 February 2006 See abstract, paragraphs [0038]-[0064] and figures 1-5</td>
<td>1-4</td>
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<td>A</td>
<td>US 5041780 A (WALLY E. RIPPE) 20 August 1991 See abstract, column 7, line 61 - column 8, line 34, claim 1 and figure 8</td>
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<td>A</td>
<td>US 2006-0181264 AI (GIUSEPPE CATONA et al.) 17 August 2006 See abstract, paragraphs [0022]-[0025] and figures 2a-2c</td>
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<td>A</td>
<td>US 2009-0295368 AI (MICHAEL C. DOUGER et al.) 03 December 2009 See abstract, paragraphs [0032]-[0085] and figures 1-4A</td>
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<td>JP 11-266129 A (TOSHIBA CORP.) 28 September 1999 See abstract, paragraphs [0002]-[0011] and figures 1-2</td>
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Further documents are listed in the continuation of Box C. See patent family annex.

T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

& document member of the same patent family

Date of the actual completion of the international search
19 November 2013 (19.11.2013)

Date of mailing of the international search report
20 November 2013 (20.11.2013)

Name and mailing address of the ISA/KR
Korean Intellectual Property Office
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Facsimile No. +82-42-472-7140

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Form PCT/ISA/210 (second sheet) (July 2009)
**Box No. II  Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)**

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1.☐ Claims Nos.:
   because they relate to subject matter not required to be searched by this Authority, namely:

2.☒ Claims Nos.: 7, 9
   because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
   The claims 7, 9 are not clear, since these claims refer to multiple dependent claim which does not comply with the third sentence of PCT Rule 6.4(a).

3.☒ Claims Nos.: 5-6, 8, 10-12
   because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

**Box No. III  Observations where unity of invention is lacking (Continuation of item 3 of first sheet)**

This International Searching Authority found multiple inventions in this international application, as follows:

1.☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2.☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3.☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4.☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

**Remark on Protest**

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.
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