Title: SELF-ALIGNED FLASH MEMORY CELL AND METHOD OF MANUFACTURING THE SAME

Abstract: Provided a self-aligned flash memory cell and a method of manufacturing the same. The method of manufacturing the self-aligned flash memory cell includes: forming a spacer silicon nitride layer at a region where a tunnel oxide layer is to be formed; forming spacers by performing etching process on the spacer silicon nitride layer and forming one or more protrusions of a substrate in a direction of a width of a channel region of the flash memory cell by etching portions of the silicon substrate by using the spacers as masks; etching portions of an oxide layer filling trenches, sequentially forming the tunnel oxide layer and a first polysilicon layer, and performing a planarization process thereon; conformably forming a dielectric layer on the entire planarized first polysilicon layer; stacking a second polysilicon layer which is used to form a control gate on the dielectric layer formed on the substrate; and partially etching the second polysilicon layer, the dielectric layer, and the first polysilicon layer by performing a patterning process.
Description
SELF-ALIGNED FLASH MEMORY CELL AND METHOD OF MANUFACTURING THE SAME

Technical Field
[1] The present invention relates to a flash memory device and a method of forming the same, and more particularly, to a structure of a self-aligned flash memory cell and a method of forming the same.

Background Art
[2] A non-volatile memory is a memory that can retain stored information even when the power is turned off. As an example of the non-volatile memory, there is a flash memory. Since data stored therein can be electrically erased and reprogrammed, the flash memory is used in various devices. According to a cell array structure, the flash memory is classified into a NOR-type flash memory which offers high speed random access and an NAND-type flash memory which offers fast programming and erasing speed and can be integrated.

In general, a cell transistor of the flash memory has a structure further including a floating gate in addition to a conventional metal oxide semiconductor (MOS) transistor. In the cell transistor of the flash memory, a tunnel oxide layer is formed on a semiconductor substrate and a floating gate is formed on the tunnel oxide layer. A gate interlayer dielectric layer is formed on the floating gate and a control gate electrode is formed on the gate interlayer dielectric layer. For a writing operation of the non-volatile memory, a Fowler-Nordheim (FN) tunneling method and a hot electron injection method are used. In the FN tunneling method, electrons are injected from the semiconductor substrate into the floating gate by a high electric field applied to the tunnel oxide layer so as to perform the writing operation. In the hot electron injection method, hot electrons generated at a channel region in and around a drain are injected into the floating gate so as to perform the writing operation. For a deleting operation of the flash memory, electrons stored in the floating gate are extracted by FN tunneling in a direction of a source or of the semiconductor substrate.

In order to effectively inject or extract a carrier into or from the floating gate, 1) a method of applying a high voltage to the control gate and the substrate, 2) a method of allocating most of the control gate voltage to the floating gate, are used.

In the first method, there are problems in that, overhead of a device for generating the high voltage increases, and periphery circuits that can stand the high voltage have to be constructed. Therefore, the method does not follow the current trend that a driving voltage is lowered. In the second method, when a high voltage is applied to the
control gate, a coupling ratio representing that what ratio is used to allocate the voltage to the floating gate becomes an issue. The coupling ratio depends on an electrostatic capacity between the control gate and the floating gate and an electrostatic capacity between the channel portion of the substrate and the floating gate. For example, in order to effectively perform the electron injection, the coupling ratio is increased, so that much of the voltage applied to the control gate has to be allocated to the floating gate. Therefore, an electrostatic capacity of a capacitor constructed with the control gate and the floating gate has to be increased.

FIG. 1 is a view showing a conventional gate electrode structure of a memory cell transistor in an NAND-type flash memory cell. Referring to FIG. 1, a control gate 9, a floating gate 13, a dielectric layer 5, a gate insulating layer 11, a device separation layer 3, and a substrate 10 are shown. In this structure, in order to increase a coupling ratio between the control gate 9 and the floating gate 13, a method of increasing a channel width W and a method of increasing of height H of the floating gate are used. However, for the high integration, in order to increase a coupling ratio, the method of increasing a height of the floating gate has been more widely used than the method of increasing a channel width.

FIGS. 2 to 5 are views for explaining a self-aligned method of forming a gate structure of a conventional flash memory cell and show a data disclosed in IEDM 1994, p61 by TOSHIBA.

Referring to FIG. 2, a tunnel oxide layer 11 and a first polysilicon layer 13 are stacked on a silicon substrate 10, and a silicon nitride layer 7 that is to be used as a hard mask is stacked. Thereafter, trenches 19 are formed by performing a patterning process. In a conventional patterning process, a photoresist is stacked on the silicon oxide layer, exposed, and developed so as to form a photoresist pattern. The lower silicon nitride layer 7 is etched by using the photoresist pattern as an etching mask, and the photoresist pattern is removed. Thereafter, the first polysilicon layer 13, the tunnel oxide layer 11, and the substrate 10 are etched by using a silicon nitride pattern 7 as an etching mask.

Referring to FIG. 3, the trenches 19 formed in FIG. 2 are filled with an oxide layer 40 by performing a low pressure chemical vapor deposition (LPCVD) process.

Referring to FIG. 4, a planarization etching process using chemical mechanical planarization (CMP) is performed on the oxide layer 40 filling the trenches 19, so that portions of the oxide layer 40 on the first polysilicon layer 13 and the silicon nitride layer 7 used as the hard mask are removed. An etching process is performed again on the oxide layer 40 filling the trenches 19, so that portions of side walls of patterns constructed with the first polysilicon layer 13 are exposed. An oxide-nitride-oxide (ONO) dielectric layer 5 is then conformably formed on the entire substrate 10.
Referring to FIG. 5, a second polysilicon layer 9 that is used to form the control gate 9 is stacked on the dielectric layer 5 formed on the substrate 10. The polysilicon layer 9, the ONO dielectric layer 5, and the first polysilicon layer 13 are partially etched by performing a patterning process.

According to a United Patent Number 6,074,917, there is a conventional problem in that, in a process of patterning a gate line, it is difficult to etch vertical portions of the ONO layer that is the dielectric layer. When the vertical portions of the ONO layer are not properly etched by performing an anisotropic etching process, a portion of the first polysilicon layer at a bottom of the inclined vertical portions of the ONO layer is not sufficiently removed, so that a bridge may be formed between transistors of a flash memory string connected in series.

In order to prevent the aforementioned problem, spacers are formed at both side walls of the floating gate pattern so as to easily perform the anisotropic etching process on the ONO dielectric layer, or an over-etching process may be performed on the ONO dielectric layer. In a case where the ONO layer is sufficiently etched, the device separation layer of the trenches may be etched, so that the substrate under the first polysilicon layer pattern may be exposed. When the substrate is exposed, in a process for forming the floating gate by selectively etching the first polysilicon layer pattern after etching the ONO dielectric layer, a portion of the substrate may be etched, so that device characteristics may decrease and deterioration may occur. In addition, since a region where the control gate and the floating gate overlap is small, in order to increase the coupling ratio, the height of the floating gate has to be increased. However, as described above, when the height H of the floating gate increases, the vertical portions of the ONO dielectric layer increase, so that the vertical portions become a problem when etched.

In order to solve the problems, in another conventional method, a flash memory cell with a split gate structure manufactured by SST company (United Patent Number 5,029,130) is used. In a conventional self-aligned structure, when electrons are injected into or extracted from the floating gate using the FN tunneling method, an electro field of more than 10MV/cm is required. However, in the flash memory with the split gate structure of SST company, electrons can be injected or extracted by using an electric field of less than 6MV/cm that is much less than 10MV/cm which is a minimum required for the conventional self-aligned flash memory. A principle that the method can be implemented is that locally enhanced electric fields are formed between the floating gate and the control gate. The structure having the locally enhanced electric fields can be implemented by using band bending of a nonplanar insulating material which exists between the floating gate and the control gate. FIGS. 6 and 7 show a data disclosed in ED 1987, p.1681 by TOSHIBA.
However, since the flash memory structure with the split gate structure has complexity of processes and a difficulty in cell shrink, the flash memory structure with the split gate structure has a limitation to be used for a high integrated flash memory cell.

Disclosure of Invention

Technical Problem

The present invention provides a self-aligned flash memory cell in order to solve problems of a conventional self-aligned flash memory cell and a flash memory cell with a split gate structure and remove the complexity of forming processes and lack of a process margin.

The present invention also provides a method of manufacturing a self-aligned flash memory cell in which enhanced Fowler-Nordheim (FN) tunneling is possible.

The present invention also provides a method of manufacturing a self-aligned flash memory cell which is provided with a wide channel width, so that it is possible to increase a sensing margin caused from a decrease in unit cell current according to high integration of a memory.

Technical Solution

According to an aspect of the present invention, there is provided a flash memory cell including: a semiconductor substrate; a device separation layer formed on the semiconductor substrate; a gate insulating layer which is formed between the semiconductor substrate and the device separation layer and is to be a channel region of the flash memory; a floating gate which is formed on the gate insulating layer and is enclosed by the device separation layer; a dielectric layer formed on the floating gate; and a control gate formed on the dielectric layer, wherein the semiconductor substrate includes one or more protrusions in a direction of a width of the channel region of the flash memory cell.

According to exemplary embodiments, the substrate may include a dent in the direction of the width of the channel region of the flash memory cell. The protrusion of the substrate of the flash memory cell may have an apex with an interior angle less than 90°.

According to another aspect of the present invention, there is provided a method of manufacturing a self-aligned flash memory cell, the method including steps of: stacking a buffer oxide and a silicon nitride layer on a silicon substrate, forming trenches by performing a patterning process, and filling trenches with an oxide layer; performing a planarization etching process on the oxide layer filling the trenches down to the silicon nitride layer; removing the silicon nitride layer by performing an etching process and forming a spacer silicon nitride layer at a region where a tunnel oxide
layer is to be formed; forming spacers by performing etching process on the spacer silicon nitride layer and forming one or more protrusions of the substrate in a direction of a width of a channel region of the flash memory cell by etching portions of the silicon substrate by using the spacers as masks; etching portions of the oxide layer filling the trenches, sequentially forming the tunnel oxide layer and a first polysilicon layer, and performing a planarization process thereon; conformably forming a dielectric layer on the entire planarized first polysilicon layer; stacking a second polysilicon layer which is used to form a control gate on the dielectric layer formed on the substrate; and partially etching the second polysilicon layer, the dielectric layer, and the first polysilicon layer by performing a patterning process.

According to another aspect of the present invention, there is provided a method of manufacturing a self-aligned flash memory cell, the method including steps of: stacking a buffer oxide layer, a first silicon nitride layer, and a first silicon oxide layer on a silicon substrate and performing a patterning process thereon down to the first silicon nitride layer; forming a second silicon oxide layer on the patterned region of the first silicon nitride layer by performing an oxidation process, stacking a second silicon nitride layer, and performing a planarization process thereon; forming trenches in the substrate and filling the trenches with an oxidation layer; performing a planarization process on the oxidation layer filling the trenches down to the second silicon nitride layer; removing the second silicon nitride layer by performing an etching process, removing portions of the oxide layer filling the trenches and the second silicon oxide layer, sequentially forming a tunnel oxide layer and a first polysilicon layer, and performing a planarization process thereon; conformably forming a dielectric layer on the entire planarized first polysilicon layer; stacking a second polysilicon layer which is used to form a control gate on the dielectric layer formed on the substrate; and partially etching the second polysilicon layer, the dielectric layer, and the first polysilicon layer by performing a patterning process.

According to exemplary embodiments, the second silicon layer may be formed by performing an oxidation process in order to form an active region having an electric field concentration effect.

According to another aspect of the present invention, there is provided a method of manufacturing a self-aligned flash memory cell, the method including steps of: stacking a buffer oxide layer, a first silicon nitride layer, and a first silicon oxide layer on a silicon substrate and performing a patterning process thereon down to the first silicon nitride layer; forming a second silicon oxide layer on the patterned region of the first silicon nitride layer, stacking a second silicon nitride layer, and performing a planarization process thereon; forming trenches in the substrate and filling the trenches with an oxide layer; performing a planarization etching process on the oxide layer
filling the trenches down to the second silicon nitride layer; removing the second silicon nitride layer by performing an etching process, removing portions of the oxide layer filling the trenches and the second silicon oxide layer, sequentially forming a tunnel oxide layer and a first polysilicon layer, and performing a planarization process thereon; forming one or more protrusions of the substrate in a direction of a width of a channel region of the flash memory cell by forming recesses on the oxide layer filling the trenches and conformably forming a dielectric layer on the entire substrate; stacking a second polysilicon layer which is used to form a control gate on the dielectric layer formed on the substrate; and partiallyetching the second polysilicon layer, the dielectric layer, and the first polysilicon layer by performing a patterning process.

Accordingly, the self-aligned flash memory cell according to the present invention has enhanced FN tunneling and is provided with a wide channel width, so that it is possible to increase a sensing margin caused from a decrease in unit cell current.

The attached drawings for illustrating exemplary embodiments of the present invention are referred to in order to gain a sufficient understanding of the present invention, the merits thereof, and the objectives accomplished by the implementation of the present invention.

Brief Description of the Drawings

The above and other features and advantages of the present invention will become more apparent by describing in detail exemplary embodiments thereof with reference to the attached drawings in which:

FIG. 1 is a view showing a conventional gate electrode structure of a memory cell transistor in an NAND-type flash memory cell;

FIGS. 2 to 5 are views for explaining a self-aligned method of forming a gate structure in a conventional flash memory;

FIGS. 6 and 7 are views showing a data disclosed in ED 1987, p.1681 by TOSHIBA.

FIG. 8 is a view showing a self-aligned flash memory cell according to an embodiment of the present invention;

FIGS. 9 to 12 are views for explaining a first example of a manufacturing process for forming a self-aligned flash memory cell according to the present invention; and

FIGS. 13 to 17 are views for explaining a second example of a manufacturing process for forming a self-aligned flash memory cell according to the present invention.

Best Mode for Carrying Out the Invention

Hereinafter, exemplary embodiments of the present invention will be described in
detail with reference to the attached drawings. Like reference numerals in the drawings denote like elements.

[35] FIG. 8 is a view showing a self-aligned flash memory cell according to an embodiment of the present invention. Referring to FIG. 8, a cross-sectional view of the self-aligned flash memory cell in a direction of a width is shown. The flash memory cell includes a device separation layer 103 formed on a silicon substrate 110. In addition, the flash memory cell includes a gate insulating layer 111 which is to be a channel region of the flash memory cell and is formed on the substrate 110 in a device separation layer 103, a floating gate 113 which is formed on the gate insulating layer 111 and is enclosed by the device separation layer 103, an oxide-nitride-oxide (ONO) dielectric layer 105 formed on the floating gate 113, and a control gate 109 formed on the dielectric layer 105.

[36] Here, the substrate 110 of the flash memory cell has one or more protrusions in a direction of the width of the channel region, and the substrate 110 has a dent in the direction of the width of the channel region. The protrusion of the substrate has an apex with an interior angle less than 90°. Accordingly, the gate insulating layer 111 formed on the protrusion of the substrate 110 has locally enhanced electric fields (shown as circles), so that electron injection and extraction into and from the floating gate 113 can be performed in a low electric filed at the same as or a faster speed than that in a conventional method.

[37] A first example of a manufacturing process for forming the self-aligned flash memory cell 800 having the locally enhanced electric fields (shown as circles) at the gate insulating layer is shown in FIGS. 9 to 12.

[38] Referring to FIG. 9, a buffer oxide layer 102 and a silicon nitride layer 107 which will be used as a hard mask are stacked on the silicon substrate 110, and trenches 109 are formed by performing a patterning process. Thereafter, the trenches 109 are filled with an oxide layer 140 by performing a low pressure chemical vapor deposition (LPCVD) process.

[39] Referring to FIG. 10, a planarization etching process using chemical mechanical planarization (CMP) is performed on the oxide layer 140 filling the trenches 109 down to the silicon nitride layer 107 which is used as the hard mask. Thereafter, the silicon nitride layer 107 is removed by performing a predetermined etching process, and a spacer silicon nitride layer 108 that is used to locally generate high electric fields at a region where a tunnel oxide layer is to be formed is formed. Spacers are formed by performing a dry etching process on the spacer silicon nitride layer 108, and by using the spacers as masks, portions of the substrate are etched.

[40] Referring to FIG. 11, in order to increase an electrostatic capacity of a capacitor, an etching process is performed on the oxide layer 140 filling the trenches 109.
Thereafter, a tunnel oxide layer 111 and a first polysilicon layer 113 are sequentially formed, and a planarization process using CMP or the like is performed thereon. The ONO dielectric layer 105 is then conformably formed on the entire substrate 110.

Referring to FIG. 12, a second polysilicon layer 115 that is used to form the control gate is formed on the dielectric layer 105 formed on the substrate 110. By performing a patterning process, the second polysilicon layer 115, the ONO dielectric layer 105, and the first polysilicon layer 113 are partially etched.

Accordingly, the flash memory cell according to the current embodiment has an enhanced Fowler-Nordheim (FN) tunneling.

FIGS. 13 to 17 are views for explaining a second example of a manufacturing process for forming a self-aligned flash memory cell 800 having locally enhanced electric fields at a gate insulating layer.

Referring to FIG. 13, a buffer oxide layer 102, a silicon nitride layer 107, and a silicon oxide layer 115 which will be used as a hard mask are stacked on a silicon substrate 110. After a patterning process is performing thereon down to the silicon nitride layer 107, in order to form an active region having an electric field concentration effect, a silicon oxide layer 116 is formed by performing an oxidation process, and a silicon nitride layer 117 is stacked.

Referring to FIG. 14, the silicon nitride layer 117 is planarized by performing a planarization process. Thereafter, the silicon oxide layer 115 which is used as the hard mask and the silicon nitride layer 107 are etched to form trenches 109. The trenches 109 are filled with an oxide layer 140 by performing the LPCVD process.

Referring to FIG. 15, a planarization etching process using CMP is performed on the oxide layer 140 filling the trenches 109 down to the silicon nitride layer 117 that was used as the hard mask. Thereafter, the silicon nitride layer 117 is removed by performing a predetermined etching process, and in order to form the tunnel oxide layer, portions of the oxide layer 140 filling the trenches 109 and the oxide layer 116 formed by performing the oxidation process are removed. The tunnel oxidation layer 111 and the first polysilicon layer 113 are then sequentially formed.

Referring to FIG. 16, a planarization process using CMP or the like is performed on the first polysilicon layer 113. The ONO dielectric layer 105 is then conformably formed on the entire substrate 110. Thereafter, a second polysilicon layer 109 is stacked on the dielectric layer 105 formed on the substrate 110 in order to form the control gate.

The second polysilicon layer 109, the ONO dielectric layer 105, and the first polysilicon layer 113 are partially etched by performing a patterning process.

Referring to FIG. 17, unlike the aforementioned process shown in FIG. 16, after
the planarization process is performed on the first polysilicon 113, recesses are formed on the oxidation layer 140 in order to increase an electrostatic capacity between the control gate and the floating gate, and the ONO dielectric layer 105 is conformable formed on the entire substrate 110. Thereafter, the second polysilicon layer which is used to form the control gate 109 is formed on the dielectric layer 105 formed on the substrate. The second polysilicon layer, the ONO dielectric layer 105, and the first polysilicon layer 113 are partially etched by performing a patterning process.

Therefore, the flash memory cell according to the embodiment is provided with a wide channel width, so that it is possible to increase a sensing margin caused from a decrease in unit cell current.

While the present invention has been particularly shown and described with reference to exemplary embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the present invention as defined by the appended claims.

Industrial Applicability

The self-aligned flash memory cell according to the present invention has an enhanced Fowler-Nordheim (FN) tunneling and is provided with a wide channel width, so that it is possible to increase a sensing margin caused from a decrease in unit cell current.
Claims

[1] A flash memory cell comprising:
a silicon substrate;
a device separation layer formed on the silicon substrate;
a gate insulating layer which is formed between the substrate and the device
separation layer and is to be a channel region of the flash memory;
a floating gate which is formed on the gate insulating layer and is enclosed by the
device separation layer;
a dielectric layer formed on the floating gate; and
a control gate formed on the dielectric layer,
wherein the substrate comprises one or more protrusions in a direction of a width
of the channel region of the flash memory cell.

[2] The flash memory cell according to claim 1, wherein the substrate comprises a
dent in the direction of the width of the channel region of the flash memory cell.

[3] The flash memory cell according to claim 1, wherein the dielectric layer is an
oxide-nitride-oxide (ONO) layer.

[4] The flash memory cell according to claim 1, wherein the device separation layer
is made of an oxide layer filling trenches formed in the substrate.

[5] The flash memory cell according to claim 1 or 2, wherein the protrusion of the
substrate of the flash memory cell has an apex with an interior angle less than
90°

comprising steps of:
stacking a buffer oxide and a silicon nitride layer on a silicon substrate, forming
trenches by performing a patterning process, and filling trenches with an oxide
layer;
performing a planarization etching process on the oxide layer filling the trenches
down to the silicon nitride layer;
removing the silicon nitride layer and forming a spacer silicon nitride layer at a
region where a tunnel oxide layer is to be formed;
forming spacers on the spacer silicon nitride layer and forming one or more
protrusions of the substrate in a direction of a width of a channel region of the
flash memory cell by etching portions of the silicon substrate by using the
spacers as masks;
etching portions of the oxide layer filling the trenches, sequentially forming the
tunnel oxide layer and a first polysilicon layer, and performing a planarization
process thereon;
conformably forming a dielectric layer on the entire planarized first polysilicon layer;
stacking a second polysilicon layer which is used to form a control gate on the dielectric layer formed on the substrate; and
partially etching the second polysilicon layer, the dielectric layer, and the first polysilicon layer by performing a patterning process.

[7] The method according to claim 6, wherein the trenches are filled with the oxide layer by using a low pressure chemical vapor deposition (LPCVD) method.

[8] The method according to claim 6, wherein the dielectric layer is an ONO layer.

[9] The method according to claim 6, wherein the protrusion of the substrate used in the method of manufacturing the self-aligned flash memory cell has an apex with an interior angle less than 90°.

[10] A method of manufacturing a self-aligned flash memory cell, the method comprising steps of:
stacking a buffer oxide layer, a first silicon nitride layer, and a first silicon oxide layer on a silicon substrate and performing a patterning and etching process thereon down to the first silicon nitride layer;
forming a second silicon oxide layer on the patterned region of the first silicon nitride layer by performing an oxidation process, stacking a second silicon nitride layer, and performing a planarization process thereon;
forming trenches in the substrate and filling the trenches with an oxidation layer; performing a planarization process on the oxidation layer filling the trenches down to the second silicon nitride layer;
removing the second silicon nitride layer, portions of the oxide layer filling the trenches and the second silicon oxide layer, sequentially forming a tunnel oxide layer and a first polysilicon layer, and performing a planarization process thereon;
conformably forming a dielectric layer on the entire planarized first polysilicon layer;
stacking a second polysilicon layer which is used to form a control gate on the dielectric layer formed on the substrate; and
partially etching the second polysilicon layer, the dielectric layer, and the first polysilicon layer by performing a patterning process.

[11] The method according to claim 10, wherein the second silicon layer is formed by performing an oxidation process in order to form an active region having an electric field concentration effect.

[12] The method according to claim 10, wherein the dielectric layer is an ONO layer.

comprising steps of:
stacking a buffer oxide layer, a first silicon nitride layer, and a first silicon oxide layer on a silicon substrate and performing a patterning process thereon down to the first silicon nitride layer;
forming a second silicon oxide layer on the patterned region of the first silicon nitride layer, stacking a second silicon nitride layer, and performing a planarization process thereon;
forming trenches in the substrate and filling the trenches with an oxide layer;
performing a planarization etching process on the oxide layer filling the trenches down to the second silicon nitride layer;
removing the second silicon nitride layer, portions of the oxide layer filling the trenches and the second silicon oxide layer, sequentially forming a tunnel oxide layer and a first polysilicon layer, and performing a planarization process thereon;
forming one or more protrusions of the substrate in a direction of a width of a channel region of the flash memory cell by forming recesses on the oxide layer filling the trenches and conformably forming a dielectric layer on the entire substrate;
stacking a second polysilicon layer which is used to form a control gate on the dielectric layer formed on the substrate; and
partially etching the second polysilicon layer, the dielectric layer, and the first polysilicon layer by performing a patterning process.

[14] The method according to claim 13, wherein the second silicon oxide layer is formed by performing an oxidation process in order to form an active region having an electric field concentration effect.

[15] The method according to claim 13, wherein the dielectric layer is an ONO layer.

[16] The method according to claim 13, wherein the protrusion of the substrate used in the method of manufacturing the self-aligned flash memory cell has an apex with an interior angle less than 90°.
A. CLASSIFICATION OF SUBJECT MATTER

H01L 27/115(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC8 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean Utility models and applications for Utility models since 1975

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
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<td>US06087223(LG Semicon Co) 11 07 2000 see the abstract, Figure 3, column3,hne10 - column4, hne20</td>
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See patent family annex

* Special categories of cited documents

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

Date of the actual completion of the international search 22 MAY 2007 (22 05 2007)

Date of mailing of the international search report 22 MAY 2007 (22.05.2007)

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Authorized officer

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